AUGUST 11, 1983

LINE-OF-LIGHT COMMUNICATIONS LURES THRIFTY COMPANIES/91

Direct-memory-access controller chip unburdens CPU/121

Silicon-gate C-MOS avoids SCR latchup/136

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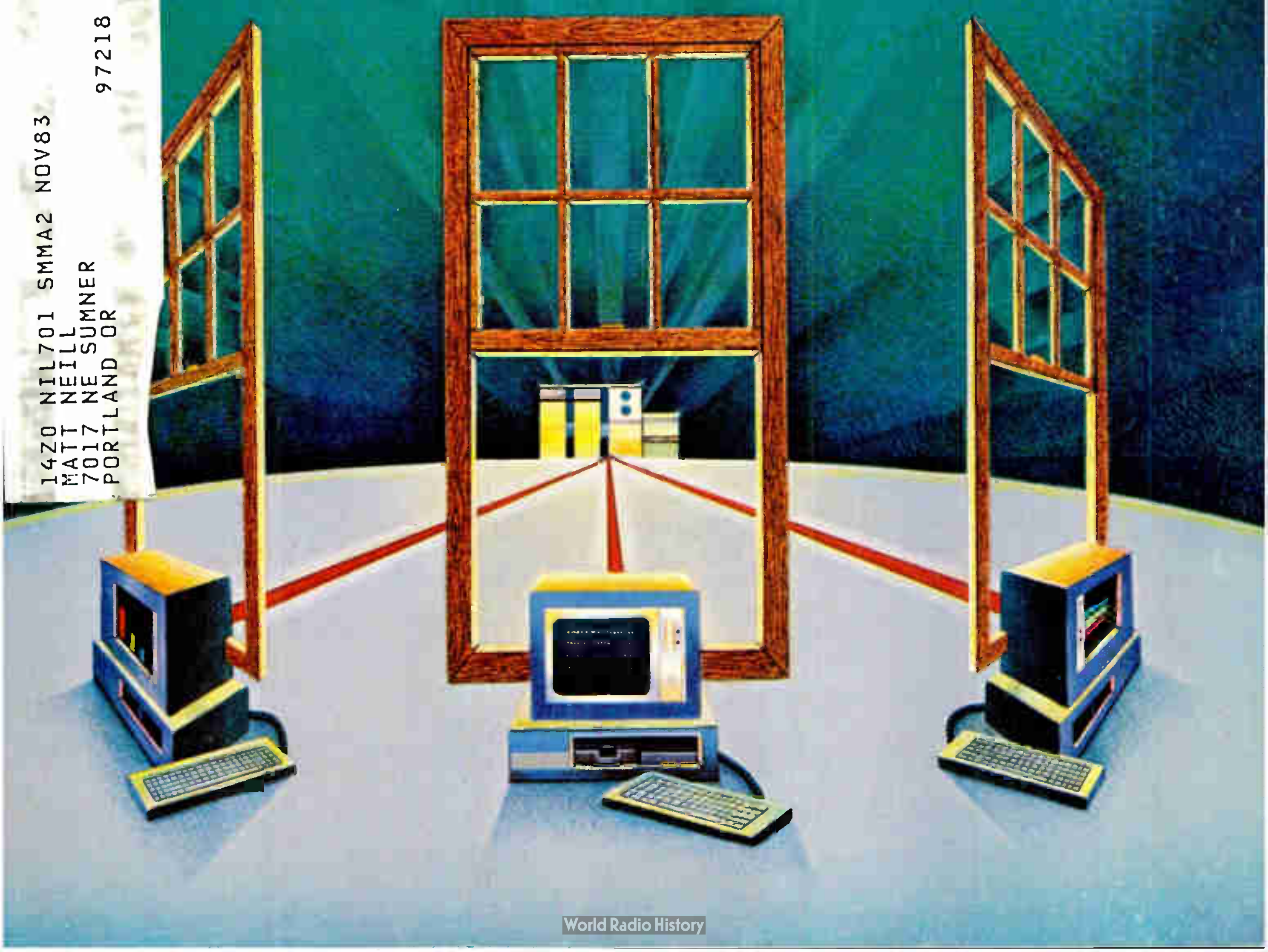
SPECIAL REPORT

Opening the micro-to-mainframe window



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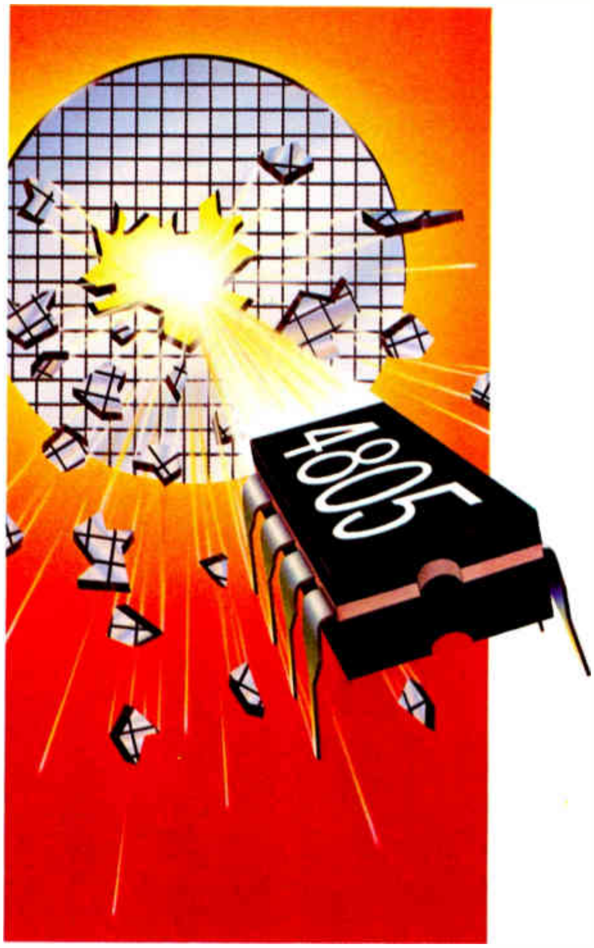

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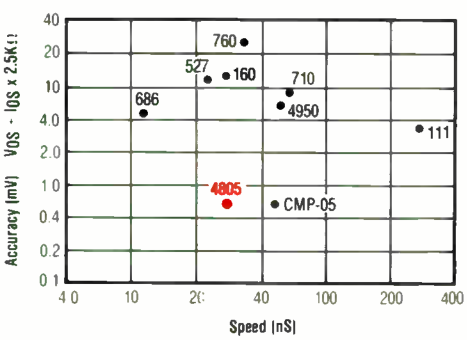

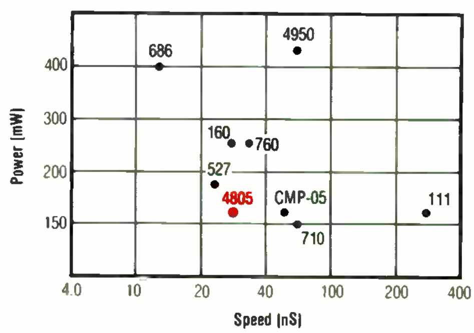

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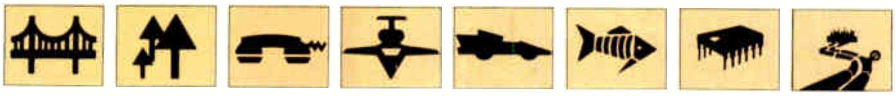

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Cover illustrated by Andy Levine.

The Cover Story

Major New Developments

NEWSLETTERS

DEPARTMENTS

SERVICES

Vol. 56, No. 16 • August 11, 1983

Highlights

Cover: Linking microcomputers to mainframes: a special report, 105

To widen access to the corporate data base, a rash of companies has devised various ways of linking personal computers and mainframes. This special report surveys the scene, then presents six specific solutions.

- In one approach, the mainframe software specialist develops a personal-computer package, plus the interface between the machines, **108**
- Work-station makers can do their part by designing machines that emulate terminals, thereby smoothing the way for linkups to mainframes, **110**
- A carefully wrought interface lets a user extract data as needed from mainframes and manipulate it on his or her desktop machine, **112**
- Another interface approach is a software protocol, intended as an industry standard, that lets the user perform sophisticated file transfers, **114**
- Open-architecture hardware and software can do their part by taking the multivendor environment into account in their interfaces, **116**
- Yet another way of defeating the incompatibility of personal computers and mainframes is a compiler written to run on both types, **118**

Optical communications take to the air, 91

Optical communications need not rely on glass-fiber cables, for the signal will zip through the air just as well. Such free-space optical systems may be at the point of takeoff as technological advances and market analysis combine to provide the needed boost.

Speedy DMA controller adds functions for increased flexibility, 121

Able to transfer 8 megabytes a second, a multichannel direct-memory-access controller also integrates circuitry that adds to its capabilities. For one thing, it has a pipelined architecture that overlaps microinstructions; for another it can perform command chaining and two types of data chaining.

Data manager opens new path for Unix operating system, 127

A relational–data-base–management system for Unix provides fast response and economical use of system memory through such features as a modular architecture, a menu handler, high-level query interfaces, and multiple on-line and programming access methods.

Design twists bring latchup immunity to silicon-gate C-MOS parts, 136

Process and layout upgrades combine to defeat the problem of latchup due to parasitic silicon controlled rectifiers. These improvements foil both external triggering and self-triggering and will work on future denser chips as well.

Coming up . . .

A new approach to automated design of custom chips . . . . a dense n-channel MOS technology for personal mainframes . . . . how to meet the requirements for controlling electromagnetic interference.

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Publisher's letter

Cross-fertilization isn't limited to the pure sciences, so our editors, in their interviews with people working at the outer edges of technology, constantly probe for pairings-up that will sire new markets for electronics.

Early in his travels this year, senior editor Harvey J. Hindin, our specialist in system integration, learned that many technology matchmakers had worked out schemes to tie personal computers or work stations to corporate mainframes. Such marriages, Harvey is convinced, will become a major endeavor in the next year or so for the computer industry.

"It's almost impossible—even for people in the field—to keep up with the announcements of new products to link the micro and the mainframe," Harvey reports. So, he decided it was high time that we do an anthology of short technical articles, along with an overview to provide perspective, to help our readers select the best way for them to tap corporate data bases (see p. 105).

The articles, Harvey points out, cover most of the different methods that have been proposed so far to make all this data available to managers at their desks—without having to burrow through layers of corporate bureaucracy with requests for specific services from their firm's data-processing or management-information-systems departments. In some cases, the methods proposed even allow the manager, if authorized, to change the data base.

Readers should be aware that the field is burgeoning and suppliers are still working at a feverish pace to better their products and expand their product lines, Harvey points out. Once a manager opts for a particular method, Harvey urges, he or she should contact its purveyor to find out what is the latest thinking about the particular application in mind. "Even with the quick turnaround of these short articles, the field is just too new for the last word to have been said," he notes.

The reason for all the interest in tapping corporate data bases is simple. Managers have always wanted to use the latest, most valid data in their calculations. But, Harvey observes, they have been inhibited heretofore by the logistics problems involved in getting the data from other departments in their firm.

Today, in contrast, with millions of personal computers on office desks nationwide, these managers can get the information they need, in what amounts to real time, by tying into a mainframe. Realizing this, vendors of software for mainframes and personal computers, and system houses as well, have rushed to fill the need. So much is coming onto the market so fast that Harvey expects to follow up with another anthology in short order.

Incremental advances in technology often go practically unnoticed. But their cumulative effect sometimes has blockbusting effects.

Such is the case of free-space communications, reports Roger Godin, our communications and microwave editor. "There has been no real state-of-the-art breakthrough here," he maintains. "But the development of cost-effective optical sources and emitters has made free-space links a viable system element in modern communications" (see p. 91).

Such systems are like standing on one rooftop signaling with a flashlight to someone on another rooftop, but the sender would be switching that flashlight several million times a second, Roger explains. What makes them particularly attractive, he goes on, is that many people who need communications links are finding out that stringing cable, wire, or fiber is often more expensive and time-consuming than they can afford.

Thus, there is a strong future for wireless systems, and "line of light" systems will share it with microwave and millimeter-wave digital radio links. The market potential is also exceptional, he says, in developing nations where populations are spread out and no cable network exists.

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Readers' comments

A patent problem

To the Editor: We read with great interest your piece on the proposal that Semiconductor Research Corp., Research Triangle Park, N. C., develop giant random-access memories ("Megabucks for megabits," July 14, p. 68). It seems likely that these products are related to, or based on, our 3-d integrated-circuit research report, which was imported into the U. S. in April—with confidentiality restrictions. If so, I would like to point out that we are pursuing patents vigorously and will be seeking court injunctions to prevent commercial exploitation by any American company that has not requested and been granted a license agreement from us.

Despite appearances, neither the current negativity of so much of British industry and government nor the official word from the U. S. that such products have "no practical applications" has discouraged us from taking the patents through to the international stage.

Thank you for your continuing high-quality coverage.

J. W. Harris
Wave Pyramid Systems
Dyfed, Carmarthen
Great Britain

Corrections

A recent Washington Newsletter item ("Trade opening to China is a boon to Honeywell, National, and CDC," June 30, p. 67) should have reported that Honeywell Information Systems has an order for 14 DPS-8 large-scale computers rather than for PDP-8 minicomputers.

"IC houses are fruitful in multipliers" (July 14, p. 155) should have said that the parts from Advanced Micro Devices Inc., of Sunnyvale, Calif., have internal emitter-coupled logic with an interface that makes them compatible with external TTL circuitry. Dissipation of Am29516/7 16-by-16 multipliers was halved to 1.2 watts in the new low-power versions, rated at 90 nanoseconds. For the 50-ns versions, the part was speeded up by a factor of two, without increasing dissipation.

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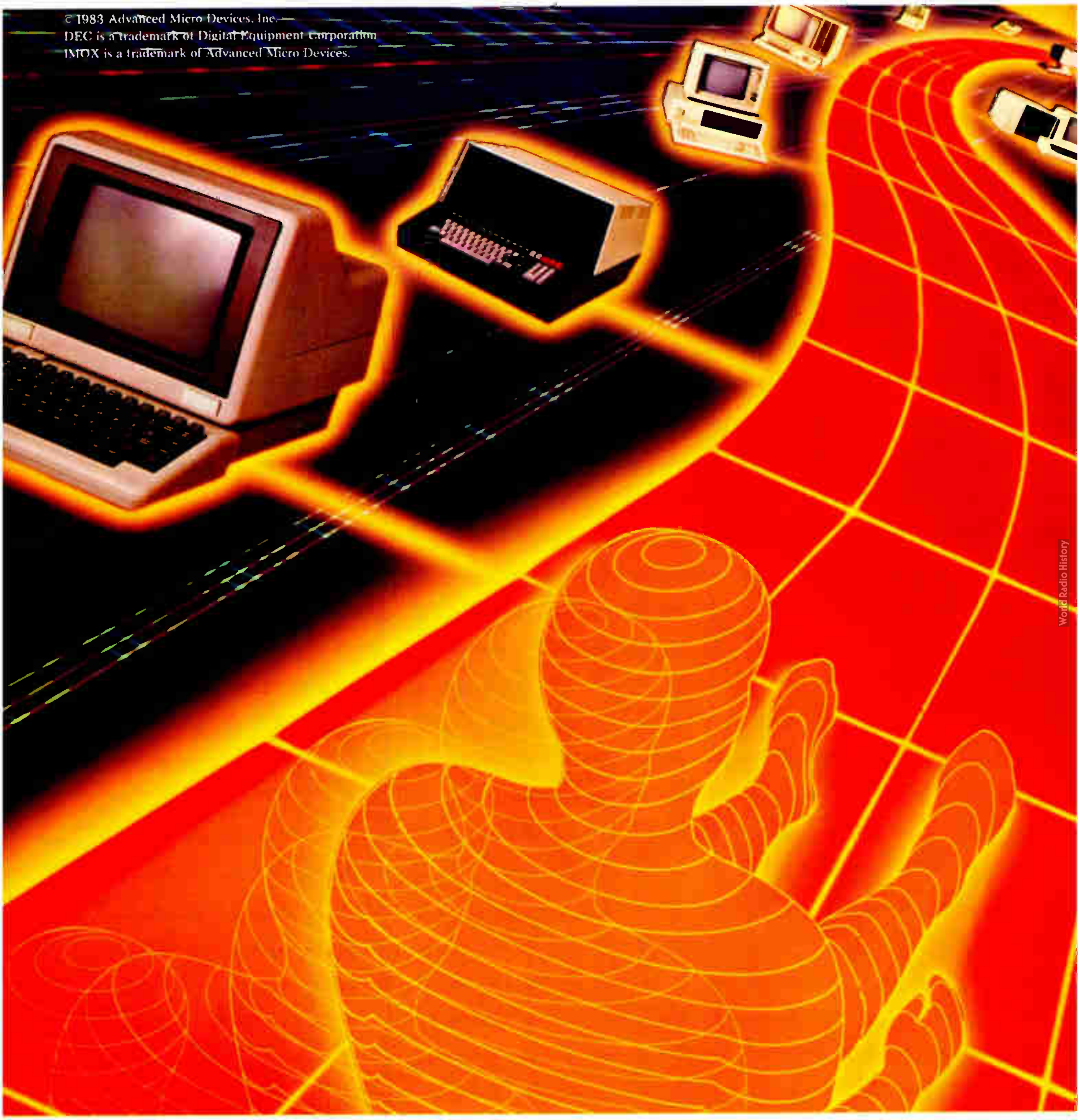

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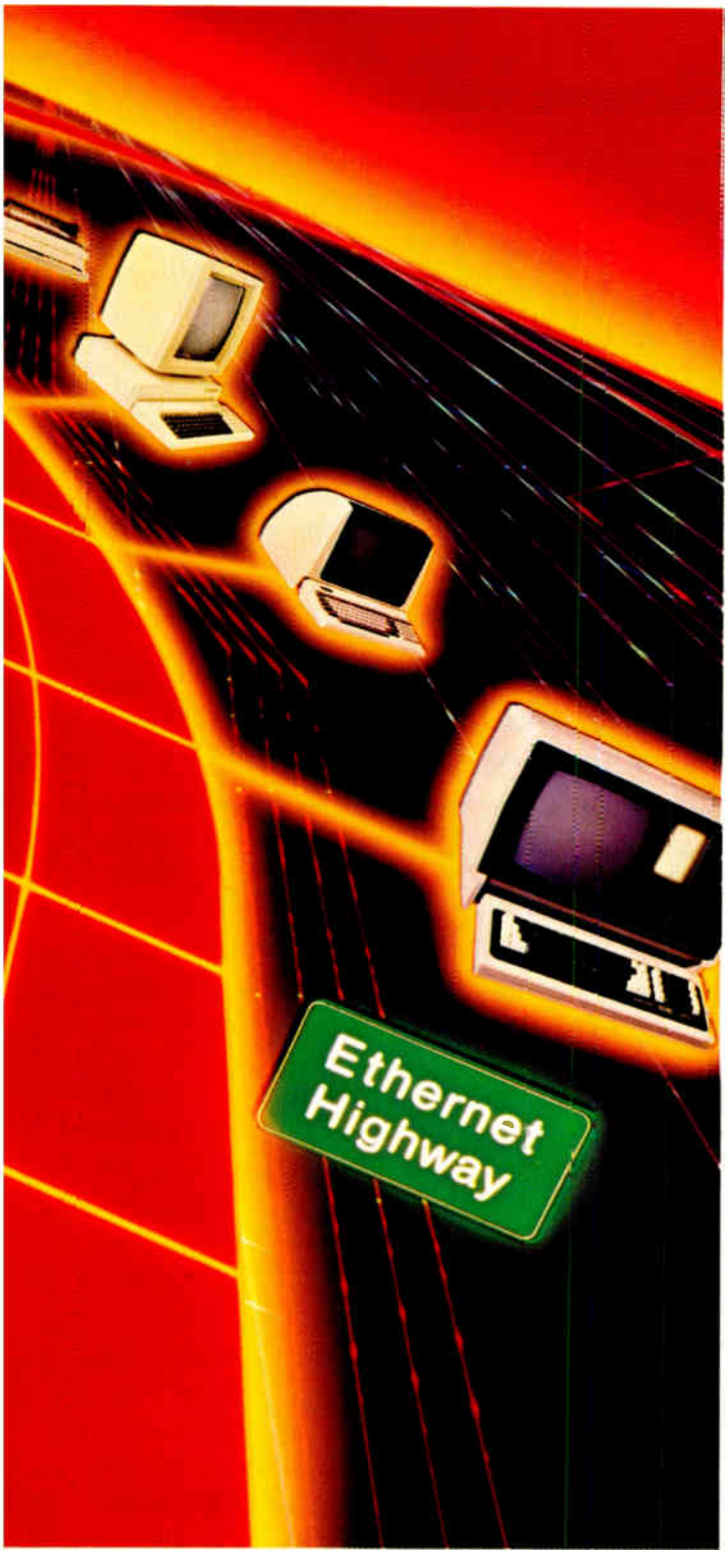

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Editorial

Congress must deal with the copyright problem

As technology gallops off into the future, it usually generates great excitement, energy, satisfaction, and prosperity. Advances in such areas as electronics can make life easier and better in two important ways: by permitting individuals to accomplish more in less time and by engendering new products and industries.

Then comes the hard part: reconciling established laws and customs with the new methods and products. The advanced information technologies have now arrived at this very stage. In fact, these technologies are turning Federal copyright law—overhauled just seven years ago—into an anachronism.

Despite the 1976 Copyright Revision Act—which then seemed to be capable of dealing with modern technologies like the ubiquitous photocopying machine for the foreseeable future—Congress must again grapple with the prickly fruits of innovation. The future, it would seem, has arrived very much ahead of schedule.

In fact, this country's legislators are now beginning to worry about what one witness at a recent House subcommittee hearing called a real swamp, where "things grow off each other and one change creates many changes." The witness darkly warned the subcommittee members that "anything you do has to be very flexible and very general, or you'll be back here every three or four years."

The issue's importance can be seen in at least one battle awaiting settlement by the U. S. Supreme Court: the bitter dispute between motion-picture makers and the electronics industry—particularly its home-entertainment sector—about whether or not the videotape recording of movies off home TV screens violates the 1976 law. Of course, seven years ago there was no need for the law even to mention VCRs.

The scale of the task comes through in a plea from Rep. Romano L. Mazzoli (D., Ky.). "Somehow," he declares, "we have to navigate that swamp without being swallowed up by it." What he wants are "certain pole stars, certain immutable truths that we can incorporate into the law, so that we do not discourage inventors and, at the same time, [do] protect the creative community from being picked to death by schools of piranhas."

One possible solution, at least as certain members of Congress see it, would be to throw out the whole apparatus of legal regulation and leave everything to the judgment and self-interest of those directly involved in the question. As an impatient Rep. Harold S. Sawyer (R., Mich.) said at the subcommittee hearing, "Why should we not just get rid of the whole machinery and let the people with the problems work out their own solutions?"

Why not? Because in the long run, that seductively simple solution is no solution at all. The truth is that innovations must be sheltered from the piranhas and that nothing in this society except the Federal government has enough might, majesty, and muscle to do the job.

The members of Congress responsible for securing that protection should get on with the work. Whatever they may think at first, they really can write a good, equitable law to protect the people who are advancing our technological frontier. And if they must rewrite the law every 5 or 6 or 10 years, so be it. For where is it writ that human law is eternal?

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People

Pebereau to lead CIT-Alcatel into U. S. telecommunications

A year into the presidency of France's CIT-Alcatel, Georges Pebereau is engineering the Paris-based telecommunications maker's invasion of world markets, especially the U. S. Fourth in the world in the number of telephone lines installed in 1982, CIT-Alcatel is pushing to be equally powerful in the U. S. by the end of 1986.

New world. Georges Pebereau has big plans for his company: its exports to the U. S. went up 75% last year.

"We want to be a permanent presence in the U. S.," says the 52-year-old Pebereau, also a director of the Compagnie Générale d'Electricité, CIT-Alcatel's diversified parent company and among the 50 largest corporations in the world. The tall, distinguished former civil engineer rose through government ranks before joining CGE in 1968.

CIT-Alcatel has spent $100 million over the last four years to develop a U. S. version of its E10 time-division digital switching system, says Pebereau. A pillar of his strategy is to sell to the Bell operating companies.

In fact, says Pebereau, CIT-Alcatel expects to be approved as a supplier by all the independent phone companies. It already sells digital switches to one, MCI Communications Corp.

The company's first U. S. beachhead, now two years old, is in Reston, Va., where it employs some 130 technicians and support staff in offices, laboratories, and an assembly plant. Its 1,800-line Class 5 E10 switches, sold this year to Indiana's Clay County Rural Telephone Cooperative, were 60% built in Reston, with the rest imported from France. The first switch was operational by the end of March; the second was set to start at the end of last month.

Pebereau admits the dollar's current strength against the franc is a windfall he intends to take advantage of. In 1982, CIT-Alcatel, half of whose sales are abroad, increased its exports to the U. S. by 75%. "We will look to new applications like teletext and videotex" to deepen the U. S. thrust, Pebereau says.

Elsewhere, CIT-Alcatel is marketing its switching equipment with equal vigor. In 1982, 4.5 million of its lines were in operation in 33 countries, with 5.5 million more on order.

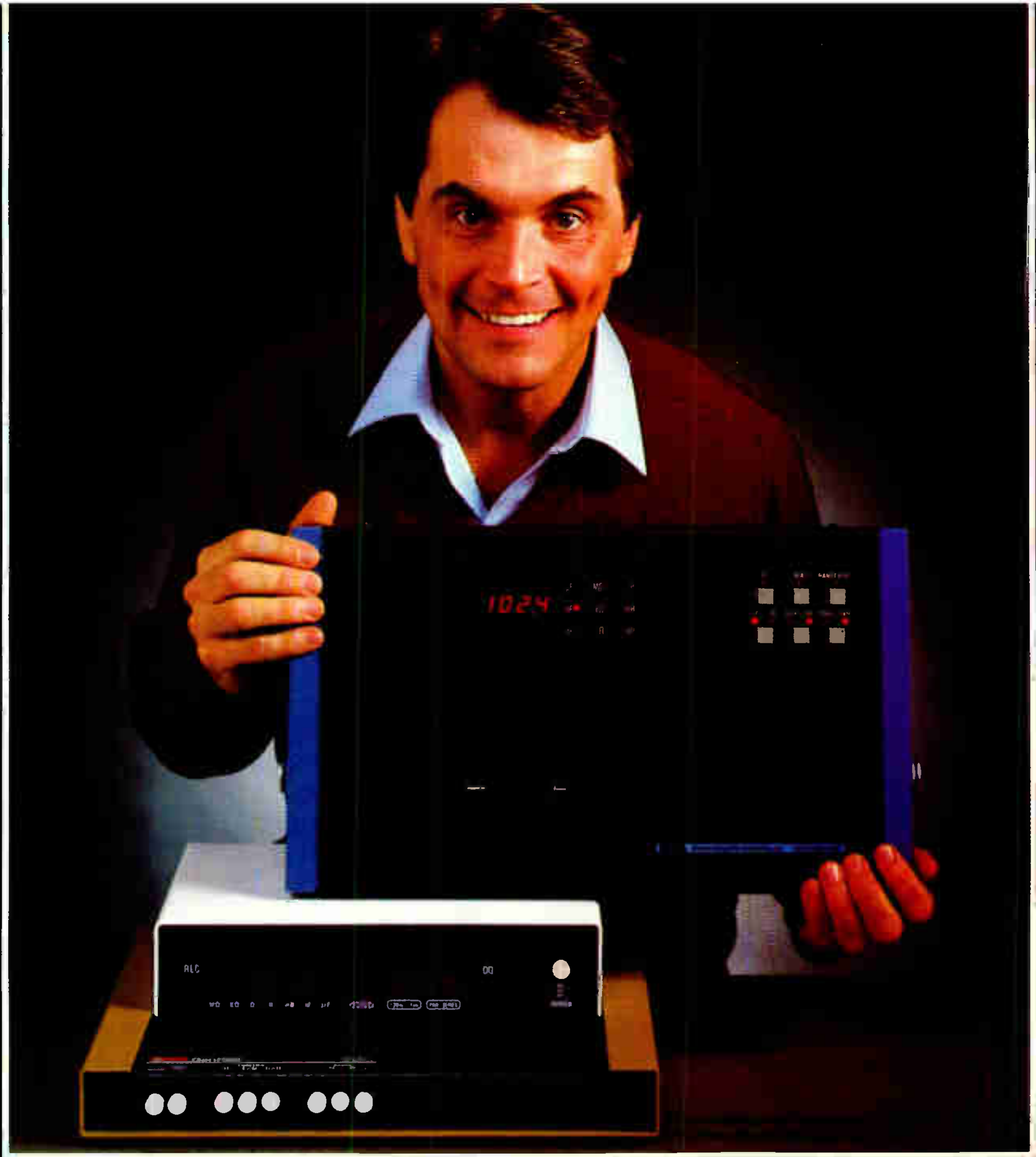
Moreover, last month it won a contract to put 46,000-line E10 switches into Morocco; it is also considering setting up a new subsidiary in Japan, and it is bidding on a major installation in India. The company says this year's sales will rise 13% to 14% over 1982's $1.7 billion, with profits up more than 20% over last year's $15 million.

Spectravideo's Fox applauds home-computer standards

When a group of 14 Japanese manufacturers announced that they planned to adopt the MSX software and hardware standard for home computers from Microsoft Corp., Bellevue, Wash. [*Electronics*, June 30, p. 48], Spectravideo Inc.'s president Harry Fox could not have been happier. He believes that standards are what will keep the market going and wants his company in the forefront of firms embracing them.

Fox's company, soon moving from Manhattan to Plainview on Long Island, is the only U. S. firm adopting the MSX standard. In fact, the chip set in Spectravideo's SV-318 computer has been licensed by Microsoft for MSX use.

Fox says his participation in the



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So what makes the new ESI Model 2400 the better bridge? First, it's fully automatic. Turn the power on and the bridge sets itself for the most used test conditions.

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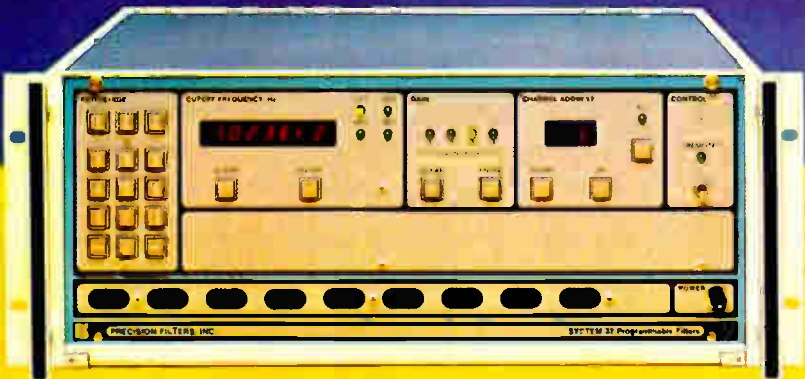

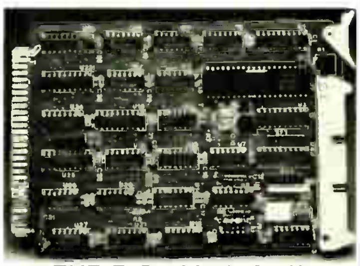

People

Long view. Spectravision's Harry Fox believes home computers need standards.

development of the standard came up by chance last October, during an inspection tour of his Hong Kong manufacturing plant with Kazuhiko Nishi, who is head of ASCII Corp., Microsoft's Japanese agent (Spectravideo uses Microsoft Basic).

He recalls that he and Nishi were excited about the prospect of a software standard and the use of Spectravideo's chip set as its hardware basis. MSX itself uses a variation of Microsoft Basic and a standard chip set. Nishi started recruiting companies, he adds, and since then Fox has been making his machines so that they may be updated easily as the standards technology improves.

Watch it. But it was only recently that Fox started publicly waving the standards banner. In fact, before he formed Spectravideo in 1982, he had been doing time in the electronic watch business. After leaving New York University in 1974 just shy of a bachelor of science degree in business and then working at various firms, he formed Personal Electronics Inc. in 1979 to develop watches that talked and played games.

Believing that the future was in personal computers, he sold his business in 1981 and formed Spectravideo. He took his new company public last May and raised $6.25 million, to be used for sales and marketing.

Fox blames the current incompatibility in the home-computer market on competitors that are more concerned with what is happening today than tomorrow. His push for standards comes from the fact that "I'm a CEO at 30, and I plan to be in business in 10 years." □

STD BUS SYSTEMS

Here's how they stack up.

When you compare STD BUS systems, the DS22/S from Micro/sys comes out on top. It's the most cost-effective disk-based STD BUS system available. Just look at the comparison chart below. It proves that on a feature-for-feature basis, the DS22/S is your best choice. And at a price that can't be beat.

The DS22/S and DS22/H are the latest members of our popular, field-proven DS22 line. They continue the Micro/sys tradition of being at the forefront of STD BUS systems. We were first to deliver completely integrated STD BUS systems, and we've been on top ever since.

The reasons? Our superior performance. Recognized quality. Fast delivery. Proven reliability. The broadest range of options. And most importantly, unequalled customer support.

And our commitment to these qualities doesn't stop with our systems. It's why we stack up best against the others across our entire broad line of STD BUS products-cards, systems, software, and accessories.

When you need STD BUS products, do what knowledgeable STD BUS OEM's, system integrators, and end users have done since the beginning of STD BUS . . . call Micro/sys.

For another $2000, the DS22/H includes an integral 5MB hard disk.

Compare these STD BUS systems.

	DS22/S	ABL-1	MATRIX 200	3020
CPU	Z80/8085	Z80/8085	Z80	Z80/8085
MEMORY	64K	64K	64K	64K
STD SLOTS	26	13	10	16
RS232 PORTS	2	2	1	2
PARALLEL PORTS	0	0	1	3
DISKS	Dual 8"	Dual 8"	Dual 8"	Dual 8"
DISK DENSITY	Double	Single	Double	Double
DISK SIDES	Double	Double	Double	Double
O/S SOFTWARE	CP/M	---	M/OS-80 MOSGEN	CP/M-80
PRICE	$5250	$6295	$5495	$5500
OPTIONS				
8088 CPU	YES	NO	NO	NO
CP/M-86	YES	NO	NO	NO
HARD DISK	YES	NO	NO	NO
PROM PROG	YES	NO	YES	YES
CENTRONICS PORT	YES	NO	STD	STD
LANGUAGES	YES	NO	YES	YES

Per manufacturers' published data, 5/83. CP/M trademark of Digital Research

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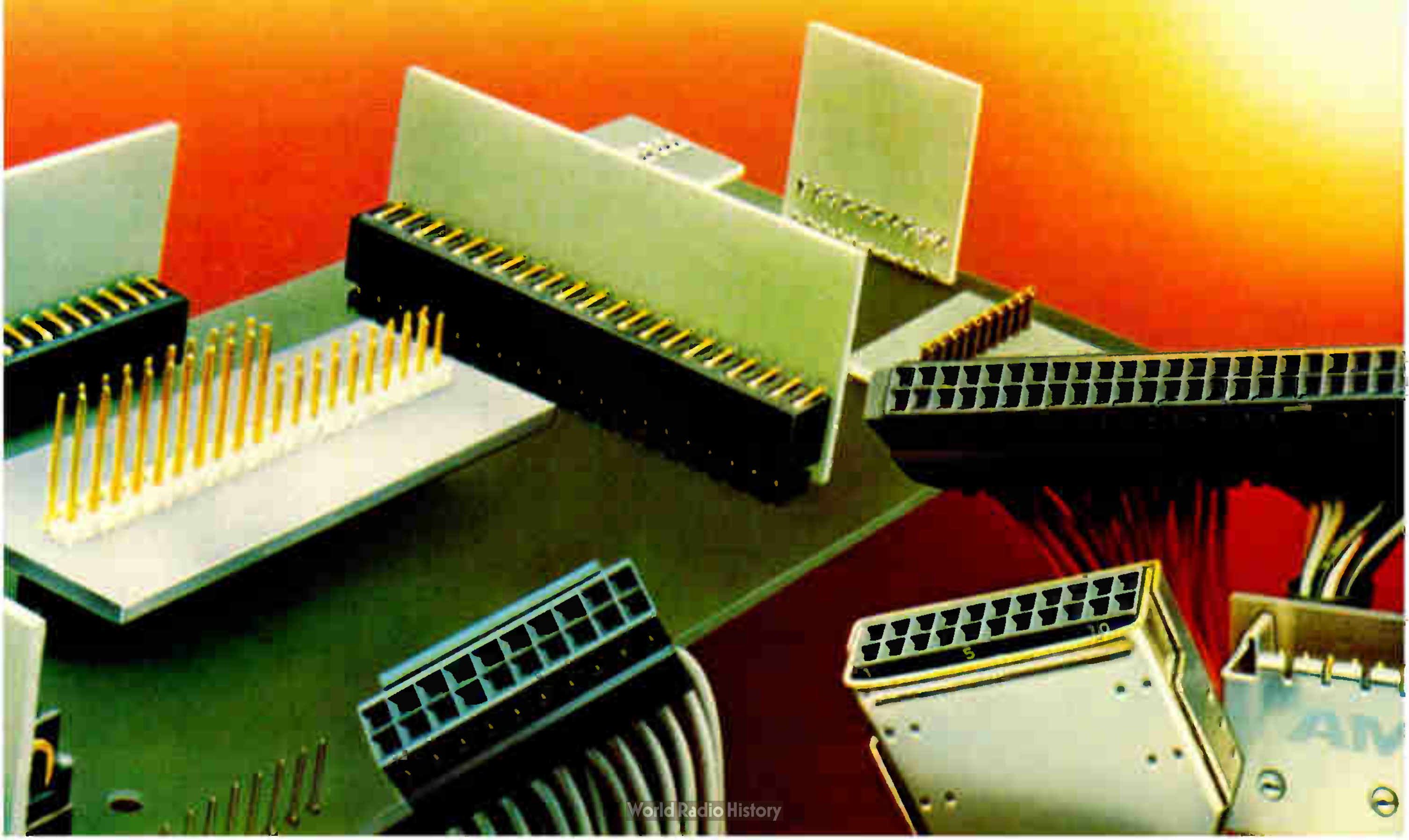
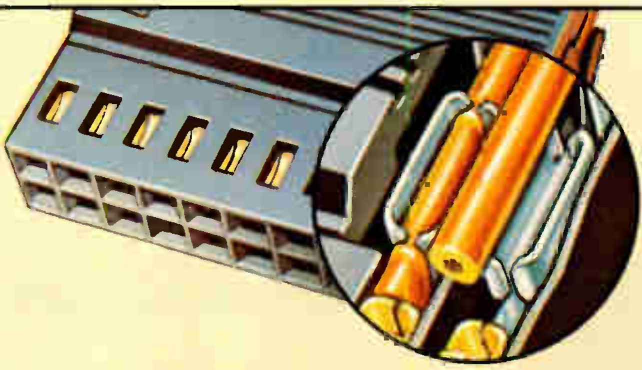
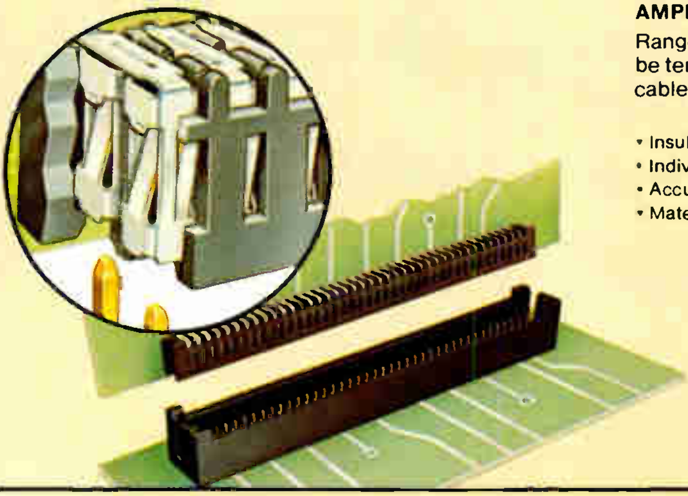


AMP Facts

AMPMODU 2-piece connectors:
High density interconnection, with up to 300 positions per connector

- Two-piece design eliminates gold pc edge fingers
- Proven receptacle design
- Solderless compliant pin insertion in motherboard
- Molded-in polarization and daughter card guides





AMPMODU MT Connectors:
Range from 6 through 72 positions and can be terminated to discrete wire, jacketed cable, twisted pair cable, and ribbon cable.

- Insulation displacing contacts
- Individual wire strain reliefs
- Accu-plate precision plating
- Mates with quick-eject headers

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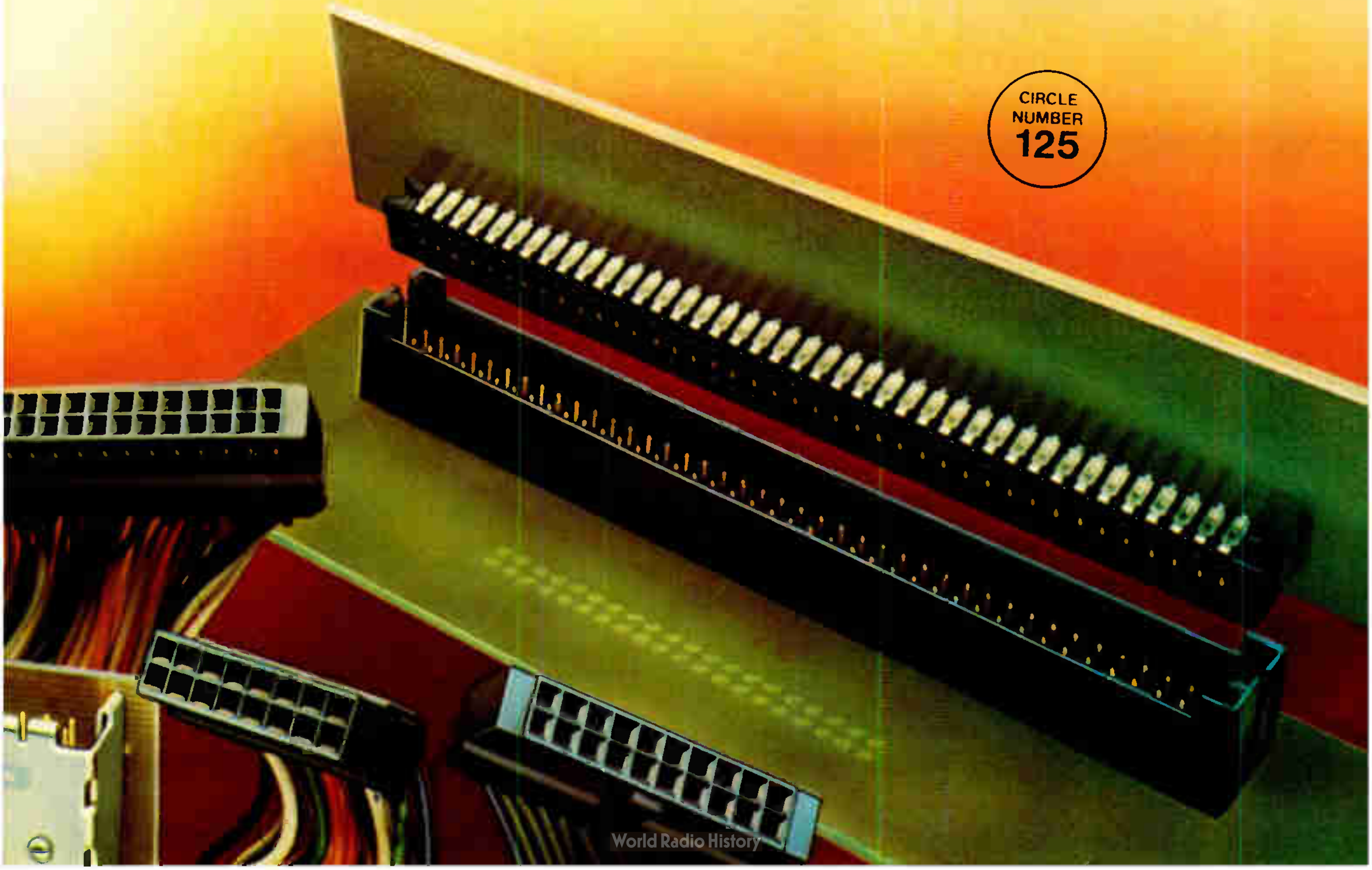
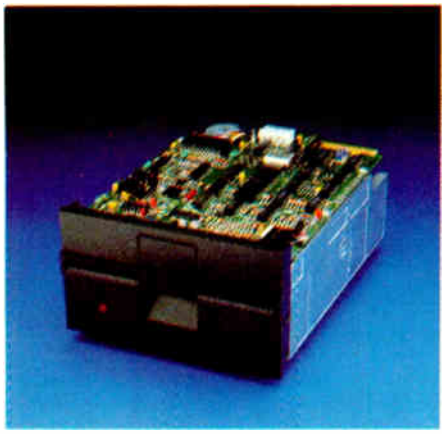
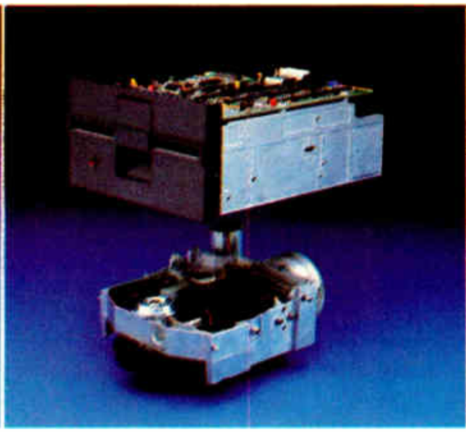
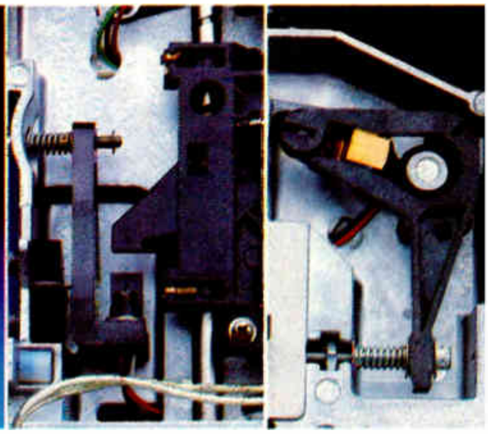


CIRCLE NUMBER 125







When we designed our new 1100 Series 5¼," 96 TPI floppy with up to 2Mbytes of storage, we set our standards high. High in reliability and high in performance. Naturally, we made it fully compatible with the industry—the same size, power, interface and bezel. It's even priced to compete with floppies that can't begin to match its performance. But that's where the similarities stop.

To begin with, we developed the 1100 with a unique chassis-within-a-chassis design to provide unequaled alignment stability—assuring that the positioning mechanics are isolated from mounting and system handling stresses. At the same time, it provides unmatched electrical shielding and acoustic noise reduction.

And in order to make alignment simple, the 1100 has only three mechanical adjustments—all featuring stable, micrometer-quality precision. All easily accessible while operating the drive with the PCBA in place.

Then, we included our temperature compensating positioner-to-spindle referencing and precision diskette clamping techniques for pre-

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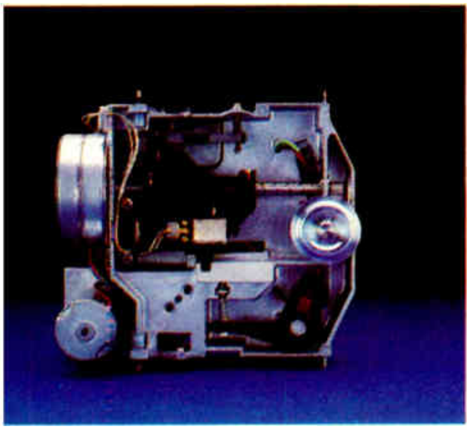
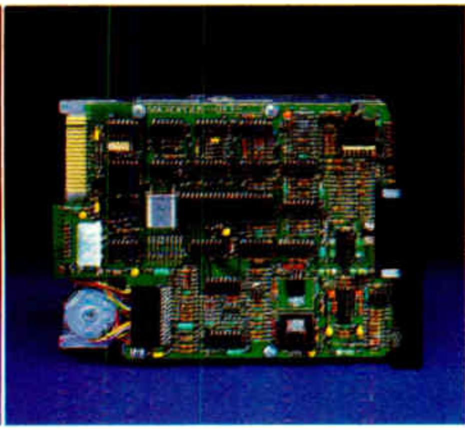
5¼" floppy





cise track positioning—every time. With our 1100 series, diskette interchangeability is guaranteed.

And if that weren't enough, we designed out all electrical adjustments—making board replacement a breeze. The microprocessor electronics precisely control the spindle motor at the spindle, eliminating speed drifts and wear factors typically handled by pot settings. Nobody else can compete with that.

And because we've been building high performance floppies since 1977, nobody can mass produce them like we can. Nobody.

So if you want a high performance floppy for the same price you're now paying for low performance, give us a call.

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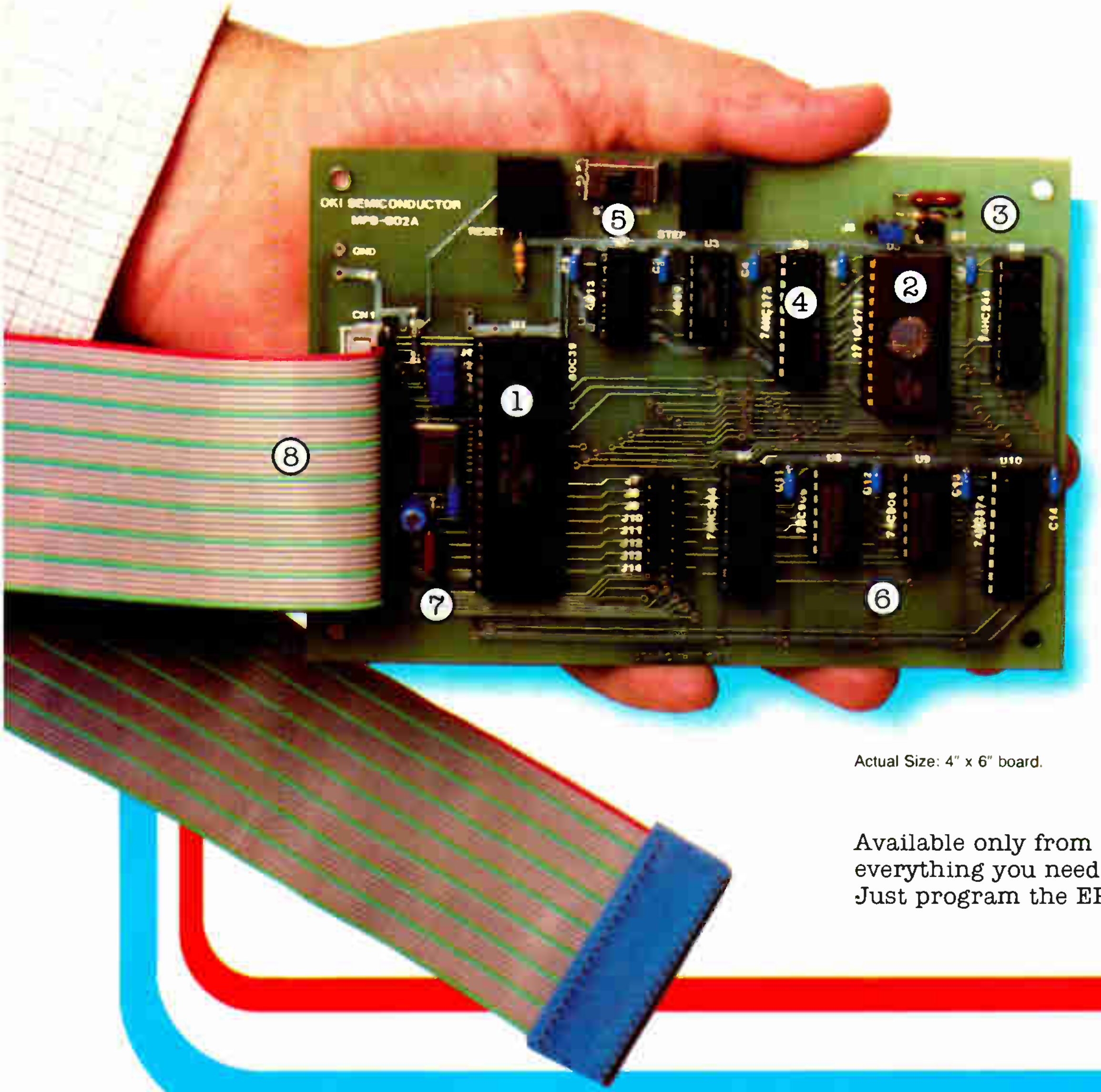


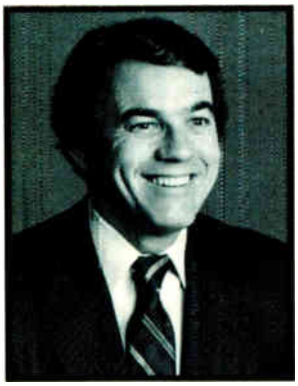
Actual Size: 4" x 6" board.

1. **80C49 MCU development chip** – the OKI 8-bit ROMless 80C39 in CMOS.
2. **EPROM socket** – OKI Breadboard includes a 2716 memory, ready for programming.
3. **EPROM power-strobing devices** – transistor, resistor, capacitor.
4. **Octal address latch**
5. **Switches** – single step, step/run mode selector, reset.
6. **"Bus" port restoration logic**
7. **6 megahertz crystal**
8. **MCU interconnect** – cable with 40-pin plugs for exact match of production MCU socket.

Available only from OKI Semiconductor: everything you need to get started. Just program the EPROM . . . and go!

The recession has changed the landscape

by James C. Morgan
president and chief executive officer, Applied Materials Inc., Santa Clara, Calif.



The recession may be over, but things are not "back to normal" in the semiconductor industry, and in my opinion, they never will be. No one survives a crisis situation unchanged, and certainly the past three years have brought about some permanent alterations in the way the industry—and its equipment suppliers as well—do business.

Those of us on the equipment side lost much of our complacency over the world marketplace. When we went into the recession, we knew the Japanese were challenging our U. S. semiconductor customers, but for the most part they were doing it with our equipment. As we come out of the recession, the Japanese have had three years of steady development on the equipment and processes with which semiconductors are made, so we know we can never take our world leadership for granted again. Only those equipment companies—and I'm glad to say Applied Materials is among them—who have formal Japanese-managed subsidiaries are likely to share in that country's market in the future.

R&D transformed. The recession has changed our view of research and development, as well. Equipment makers' approach to research and development has been dramatically transformed by the recession. We will continue to spend a large percentage of sales on R&D, but you can expect to see it more focused on systems where the likelihood of success is already well-demonstrated. Companies that in the past have started from scratch on an idea will take greater advantage of basic research already done at universities or by other companies.

The new Semiconductor Research Corp., the cooperative R&D funding program started by the Semiconductor Industry Association, is now fully supported by the Semiconductor Equipment and Materials Institute. I expect that all of us will learn to take advantage of such jointly funded R&D on new generations of semiconductor processes, focusing our own R&D dollars on the proprietary design work we believe will give us the competitive edge. Continued high development costs in semiconductor equipment will also encourage a greater number of private R&D partnerships to be formed.

Speaking of partnerships, I believe the recession taught us all the advantages of long-term commitments with major customers. I don't mean just sales contracts, but preferred-vendor agreements as well. For example, Applied Materials enjoys preferred-vendor status with GTE Microcircuits, in Tempe, Ariz., which makes us its primary source of plasma etching and epitaxial systems. That relationship means our process engineers are there, working with their engineers to develop the etching and epitaxial processes they need for specific products. Arrangements such as this tend to be more recession-proof than do individual sales and so will be sought after by all equipment vendors in the future.

Shakeout coming. There are other changes that come about—or will occur—because of the recession. Despite the recent flurry of start-up companies, I believe the recession left some smaller companies very vulnerable financially. When we look back a few years from now, I think we'll see that this recession triggered the long-awaited shakeout in the equipment industry and caused a number of mergers and acquisitions that might not have happened had the downturn not taken place or at least had not been so severe.

Finally, I think the recession will have made us all more cautious about our hiring and use of engineering talent. Before the recession, we were adding engineers as fast as we could find them and then turning up a slot for them in the organization. Now I think you'll see the organizational need more firmly identified before the engineer is hired. In some cases, particularly our growing need for software engineers, I suspect many will be hired only on a contract basis for a specific time.

Does all that add up to the post-recession blues? I don't think so. None of us liked the recession, but I do think it has made us wiser and more competitive as an industry.

Electronics *will periodically invite the expression of outside views on this page concerning issues of importance to the electronics industries.*

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The Series 5000 is easy to integrate into existing systems and a must for future designs. Call now for delivery, pricing, and facts on Wangtek's new Peripheral Integration Program.

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Meetings

Automan '83, British Robot Association (IFS Conferences Ltd., 35–39 High St., Kempston, Bedford MK42 7BT, England), National Exhibition Centre, Birmingham, Sept. 5–8.

13th European Microwave Conference, German Engineers Association, *et al.* (Prof. Groll, Technical University, Arcisstrasse 21, D-8000 Munich, West Germany), Fairgrounds, Nuremberg, Sept. 5–8.

6th European Conference on Circuit Theory and Design, IEEE *et al.* (Dr. Gleissner, AEG-Telefunken, ABT K1, P. O. Box 1120, D-7150 Backnang, West Germany), Stuttgart University, Stuttgart, Sept. 5–9.

Ineltec '83—Industrial Electronics Exhibition, Swiss Industrial Fair (Ineltec Secretariat, Postfach, CH-4021 Basel, Switzerland), Foire des Echantillons, Basel, Sept. 6–10.

International Conference on Computer-Aided Design, IEEE (445 Hoes Lane, Piscataway, N. J. 08854), Marriott Hotel, Santa Clara, Calif., Sept. 12–15.

2nd European Signal Processing Conference, European Association for Signal Processing (U. Arnold, Lehrstuhl für Nachrichtentechnik, Cauerstrasse 7, D-8520 Erlangen-Nuremberg, West Germany), University of Erlangen, Erlangen, Sept. 12–16.

Autofact Europe, Society of Manufacturing Engineers (1 SME Dr., P. O. Box 930, Dearborn, Mich. 48128), Palexpo Conference Center, Geneva, Switzerland, Sept. 13–15.

Midcon/83, Electronic Conventions Inc. (8100 Airport Blvd., Los Angeles, Calif. 90045), O'Hare Exposition Center, Rosemont, Ill., Sept. 13–15.

Symposium on VLSI Technology, The Japan Society of Applied Physics (2-4-16 Yayoi, Bunkyo-ku, Tokyo 113, Japan), Surf Hotel, Maui, Hawaii, Sept. 13–15.

13th European Solid State Device Research Conference, IEEE *et al.* (Clive Jones, The Institute of Physics, 47 Belgrave Sq., London SWIX 8QX, UK), University of Kent, Canterbury, UK, Sept. 13–16.

Euromicro '83—9th Symposium on Microprocessing and Microprogramming, Euromicro Association (T. H. Twente, Department INF, P. O. 217, NL-7500 AE Encshede, The Netherlands), Madrid, Spain, Sept. 14–16.

1983 Dry Process Symposium, Institute of Electrical Engineers of Japan (2-2-1 Katahira, Sendai 980), Tokyo, Sept. 19–20.

16th Electronics and Aerospace Conference, IEEE (Dr. John M. Walker, Westinghouse Electric Corp., Mail Stop 3200, P. O. Box 1521, Baltimore, Md. 21203), Shoreham Dunfey Hotel, Washington, D. C., Sept. 19–21.

6th Conference on Digital Satellite Communications, IEEE *et al.* (Howard Briley, Comsat Corp., 950 L'Enfant Plaza, Washington, D. C. 20024), Hyatt Regency Hotel, Phoenix, Ariz., Sept. 19–23.

9th World Computer Congress, International Federation for Information Processing *et al.* (Philip H. Dorn, Dorn Computer Consultants Inc., 25 East 86th St., New York, N. Y. 10028), Palais des Congrès, Paris, Sept. 19–23.

Semicon/East '83, Semiconductor Equipment and Materials Institute (Mary Beth Kern, Semi, 625 Ellis St., Suite 212, Mountain View Calif., 94043), Hynes Auditorium, Boston, Mass., Sept. 20–22.

9th European Solid-State Circuits Conference, Swiss Federal Institute of Technology (V. Valencic, EPFL-33 av. de Cour, CH-1007 Lausanne, Switzerland), Lausanne, Sept. 20–23.

33rd Broadcast Symposium, IEEE (Robert A. O'Connor, CBS TV Network, 51 West 52nd St., New York, N. Y. 10019), Hotel Washington, Washington, D. C., Sept. 21–23.

If you have a Personal Computer and want to talk to IBM, PCI speaks your language.

The PCI 1076 protocol converter supports your Personal Computer - Apple, Cannon, DEC, Hewlett Packard, IBM-PC, Kaypro, NEC, Osborne, Sanyo, Sony, Tandy/Radio Shack, MOD, Xerox, etc, etc, etc – in IBM's SNA/SDLC world.

Simply, conveniently, economically, the PCI 1076 makes IBM SNA hosts talk to your Personal Computer in its own language, with absolutely no change in host application programs. It converts the Personal Computer's ASCII code to appear as the SNA/SDLC protocol used by IBM hosts, and vice versa. When you use your Personal Computer's display and keyboard, they appear and function as 3278s IBM's CRTs.

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PCI has written a free book, including glossary and complete explanation of how to support Personal Computers in IBM's world. But if you'd like to hear more now, let PCI's 1076 speak for itself. Call PCI for a demonstration unit today.

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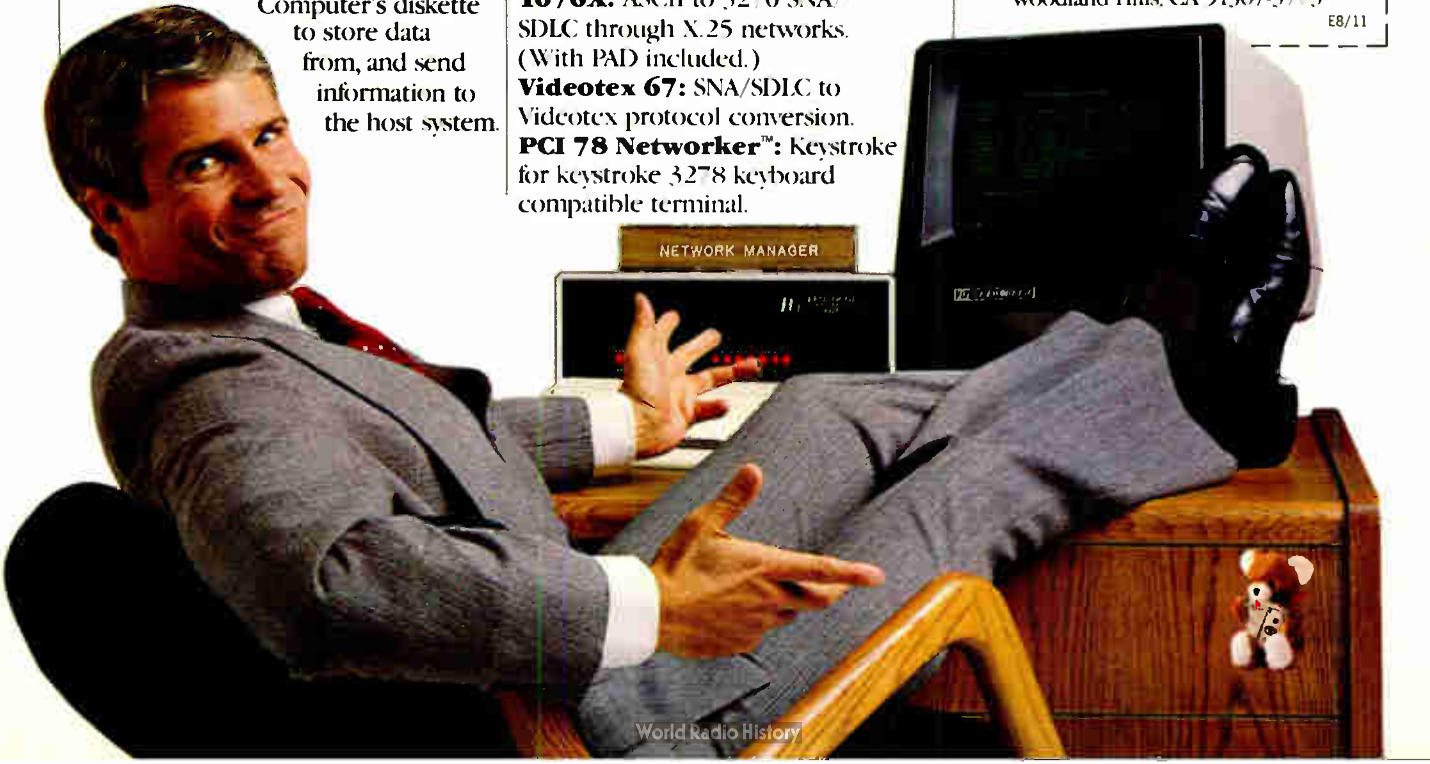


Others say they solve your computer power problems.

We say that's a lot of noise.

Electrical noise. It's part of *all* utility electric power. And what noise can do to your computers is a crime.

Many companies say their power conditioners eliminate noise. But none eliminate *all* types of destructive transients. As important, when they try to reduce one type of noise, they actually create others.

There are no such trade-offs with Oneac. Because only Oneac power conditioners eliminate *all* forms of dangerous noise that chips away at processor performance . . . without generating new problems.

Power that performs.
Other power conditioners, in an attempt to eliminate noise disturbances and provide voltage regulation, introduce high impedance into the power path. This can actually create noise. And in the process, compromise power transfer to the computer.

So in trying to improve noise attenuation and voltage regulation, they actually compound your system's problems.

Oneac, on the other hand, provides complete noise attenuation without using high impedance. We re-establish a perfect electrical environment at the output, independent of ground quality. Thus, noise is eliminated...without compromising power transfer.

At issue, too, is voltage regulation. It's been the prescribed cure for many power-related ills. But consider the switch-mode power supplies you now use. Most spec between 90V and 135V. That's far beyond the variation allowed by the electric utility.

Obviously, voltage regulation isn't the problem. But current is.

Your computer systems need both high peak *and* high inrush current to operate reliably.

The only way most power conditioners can provide this current is to be greatly oversized. There's a serious downside here: oversizing can create instability and overshoots that can confuse or damage your system.

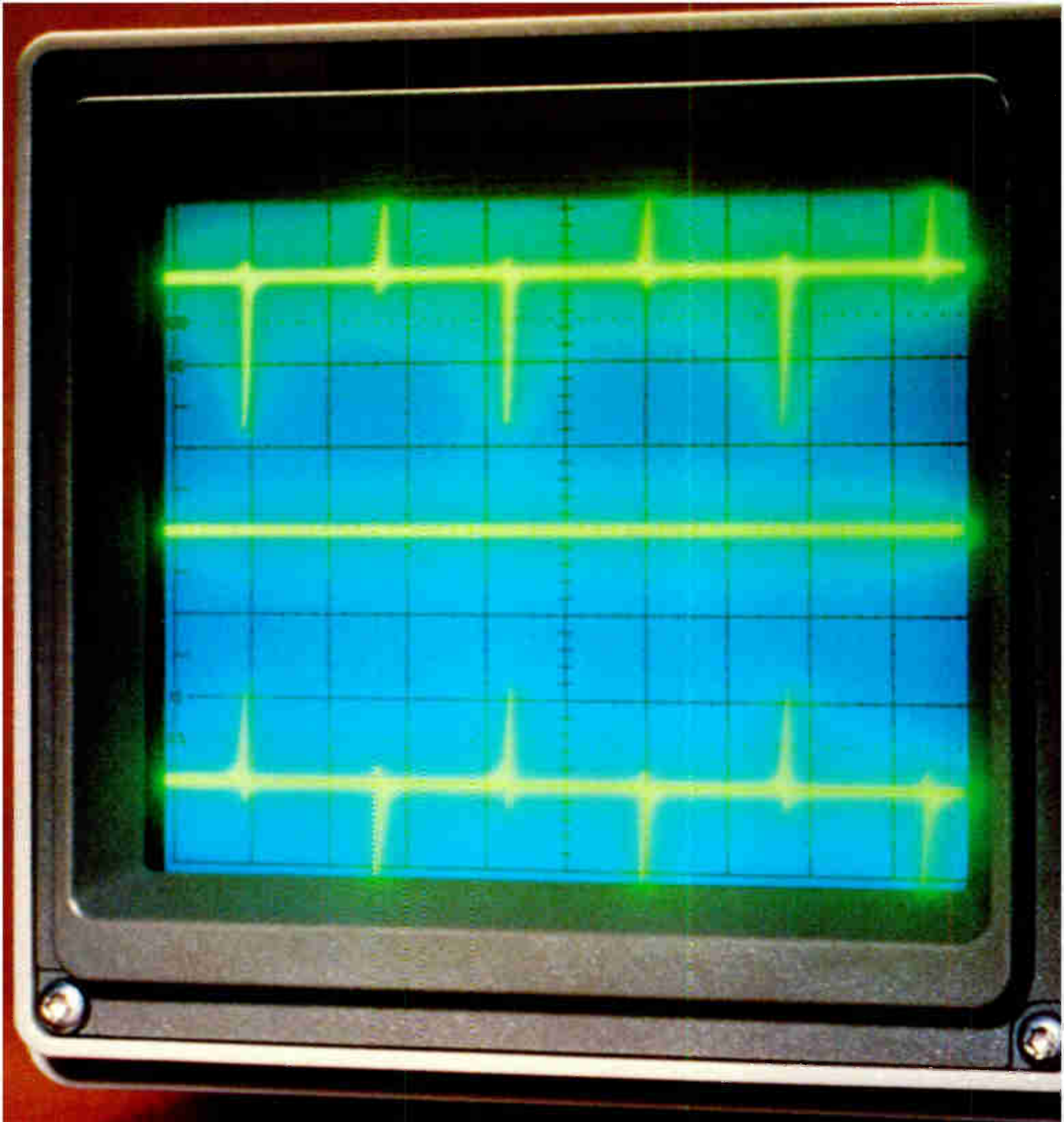
Oneac power conditioners do not regulate line voltage. There's no need to. Instead, they provide peak current with high crest factors and inrush current up to 20 times their rating...with complete noise protection. All to meet the needs of modern systems.

Take our lead as others have.
Already, many leading makers of microprocessor systems—from business computers to PBX's—have selected Oneac to solve their power problems. So it makes sense to check into Oneac for your systems, too.

Ask other power conditioning companies about their specs. Their noise control. Their power transfer capability. And the trade-offs they want you to make between the two.

Then, ask Oneac. We'll prove to you why everything the others say is just a lot of noise.

Oneac: Power that performs.



Noise generated at the output of a 1 KVA high isolation transformer (top), 1 KVA Oneac Condition One® (center) and 1 KVA ferroresonant transformer (bottom) driving a 750 Watt power supply, measured through a high pass filter (bandwidth of 5 KHz to 2 Mhz). Scale: 50 V/vertical div., 5 mS/horizontal div.

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CIRCLE 29 FOR SALESMAN'S VISIT

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Circle 30 for Literature

Circle 31 for Demonstration

News update

■ For the second time in a decade, Philips Test & Measurement Inc.—the American instrumentation arm of Netherlands-based NV Philips Gloeilampenfabrieken—has quit making oscilloscopes in the U. S.

Robert Joseph, vice president and general manager of the Mahwah, N. J., subsidiary, announced last month the January 1984 close of the company's low-end-scope facility, which opened four years ago [*Electronics*, June 7, 1979, p. 35]. Low market acceptance had once before made Philips abandon its U. S. scope-making operation back in the early 1970s.

The company will still sell scopes in the U. S., Joseph explains, but will consolidate their manufacture at its highly automated Enschede, Netherlands, facility, so it can use "economy of scale and vertical-integration manufacturing procedures to combat pricing pressures of the offshore [Far] Eastern countries." The cost of duplicating the Enschede facility in the U. S. would now be prohibitive, he says, adding that the consolidation "is motivated by our desire to become more aggressive in the marketplace."

Dwindling share. In the last year or so, Philips has been giving up market share to Kikasui, Hitachi Ltd., and, to a lesser extent, Hewlett-Packard Co., says industry analyst Adam Cuhney, of Salomon Brothers Inc., in New York. "Its 10% to 15% share of the market is slipping," he points out, claiming that Philips "should have been able to take advantage of the stronger U. S. dollar but has not."

During the last four years, Japanese scope makers Kikasui and Hitachi entered the 100-MHz-and-under U. S. scope market, which (according to the *Electronics* annual survey) hit $250 million in 1982. Each company has won about 4% of that market, which is now highly competitive.

Cuhney also points out that Philips "has not been a name" in the military market, with its strong demand for the very class of scopes the Dutch firm manufactured in Mahwah. —**Richard Comerford**

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Data I/O's new 22A PROM programmer is all you'll need for programming more than 400 PROMs and 40-pin microcomputers, including 256K devices. It's priced so competitively that every engineer can have one at his workstation. And it's the ideal programmer for field service applications.

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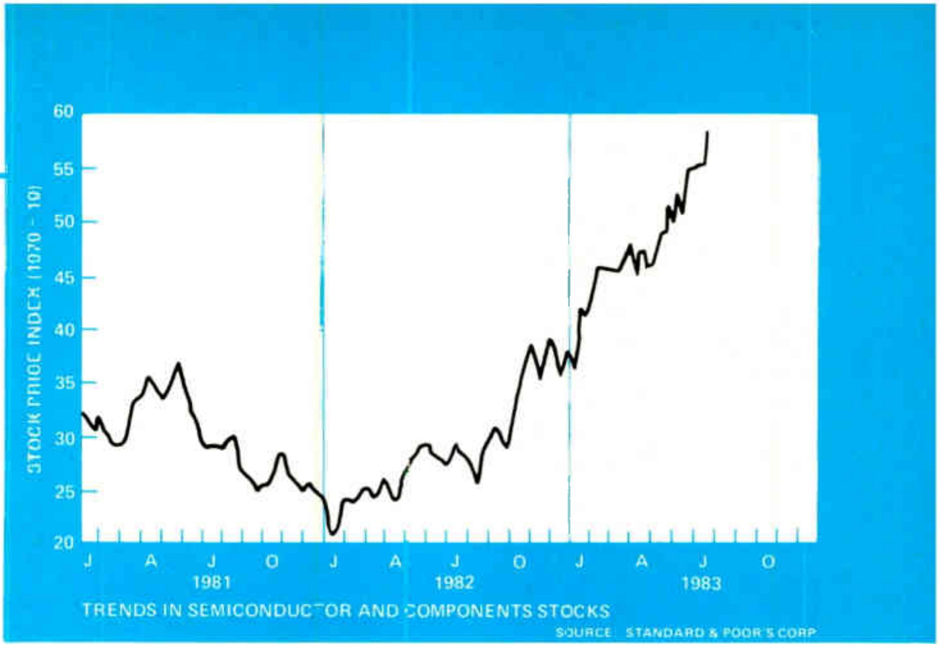
BUILDING BETTER COMMUNICATIONS

Circle 34 on reader service card

Business activity

"Trends in semiconductor and components stocks" records the stock market activities of a selected group of publicly owned semiconductor and components manufacturers. The index weights the companies by size and therefore reflects their relative performance.



The economy is picking up for the electronics industry, but the gains may take some time to trickle down to employees. A new study says merit pay raises for workers at electrical and electronics equipment manufacturers will be smaller this year than last. The survey, by New York–based management consultants Towers, Perrin, Forster & Crosby, covers producers of radio and TV transmitting and receiving equipment, electronic components (such as integrated circuits, printed-circuit boards, and tubes), and electronic instruments, as well as of electric motors and generators. Its findings: the average merit raise in 1983 for exempt employees (salaried professional and managerial workers who do not get overtime pay) is 7%, down from 10% in 1982. For nonexempt workers (hourly-wage earners in production, service, and clerical positions who are paid overtime), the average merit raise is 6.7%, also down from last year's 10%. In comparison, exempt and nonexempt workers in all industry classifications received an average merit pay raise of about 6% in 1983, down from 9% in 1982.

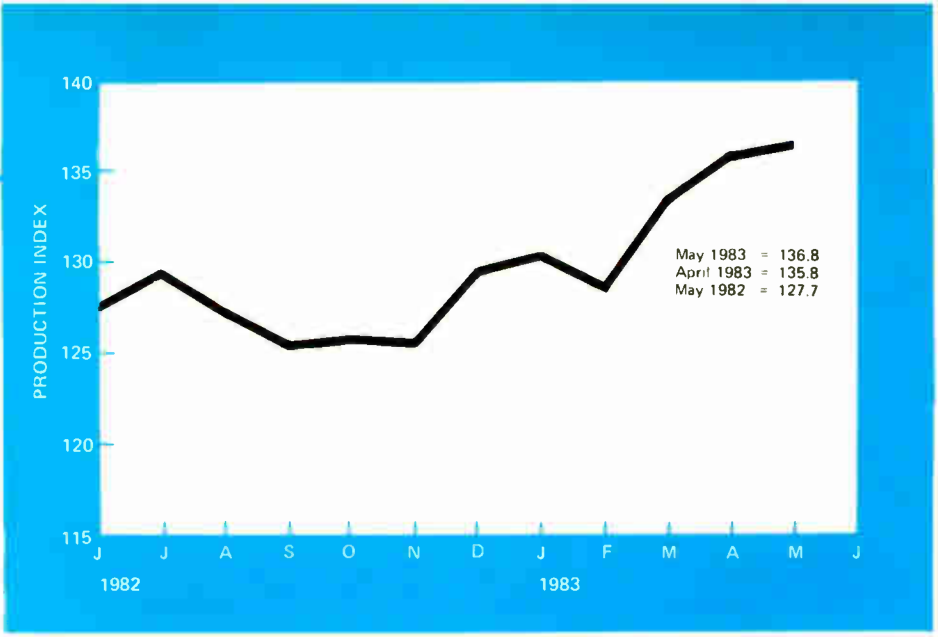
To help U. S. high-technology firms compete with their overseas counterparts, the U. S. Department of Commerce has started a newsletter on technological developments abroad. The "Foreign Technology Abstract Newsletter" groups summaries of technical information from over 50 countries into 10 subject areas. The abstract costs $90 a year from the Department of Commerce, NTIS, 5285 Port Royal Rd., Springfield, Va. 22161. Also, the deparment's new "Export Statistics Profile" provides detailed statistics on exports of electronic components for the last five years, including the 75 top foreign markets, major foreign competitors, and the 10 best market prospects. The report is $20 from the Department of Commerce, ITA/OTIS, Room 1320, Washington, D. C. 20230.

Financings . . . Pyramid Technology Corp., of Mountain View, Calif., which makes a supermini-computer based on Bell Laboratories' Unix operating system, received $15 million in a second round of financing. The firm has raised $21 million since its formation in December 1981. . . . Winchester-disk–drive maker DMA Systems Corp., based in Goleta, Calif., raised $6 million in a third round of financing, bringing total investments to $18.6 million.

–Robert J. Kozma

Business activity

The *Electronics* production index is a seasonally adjusted measure of the level of production activity among U. S. manufacturers of office and data-processing equipment, communications and radio-television equipment, instruments, and components. As a reference point, the 1977 yearly average = 100.

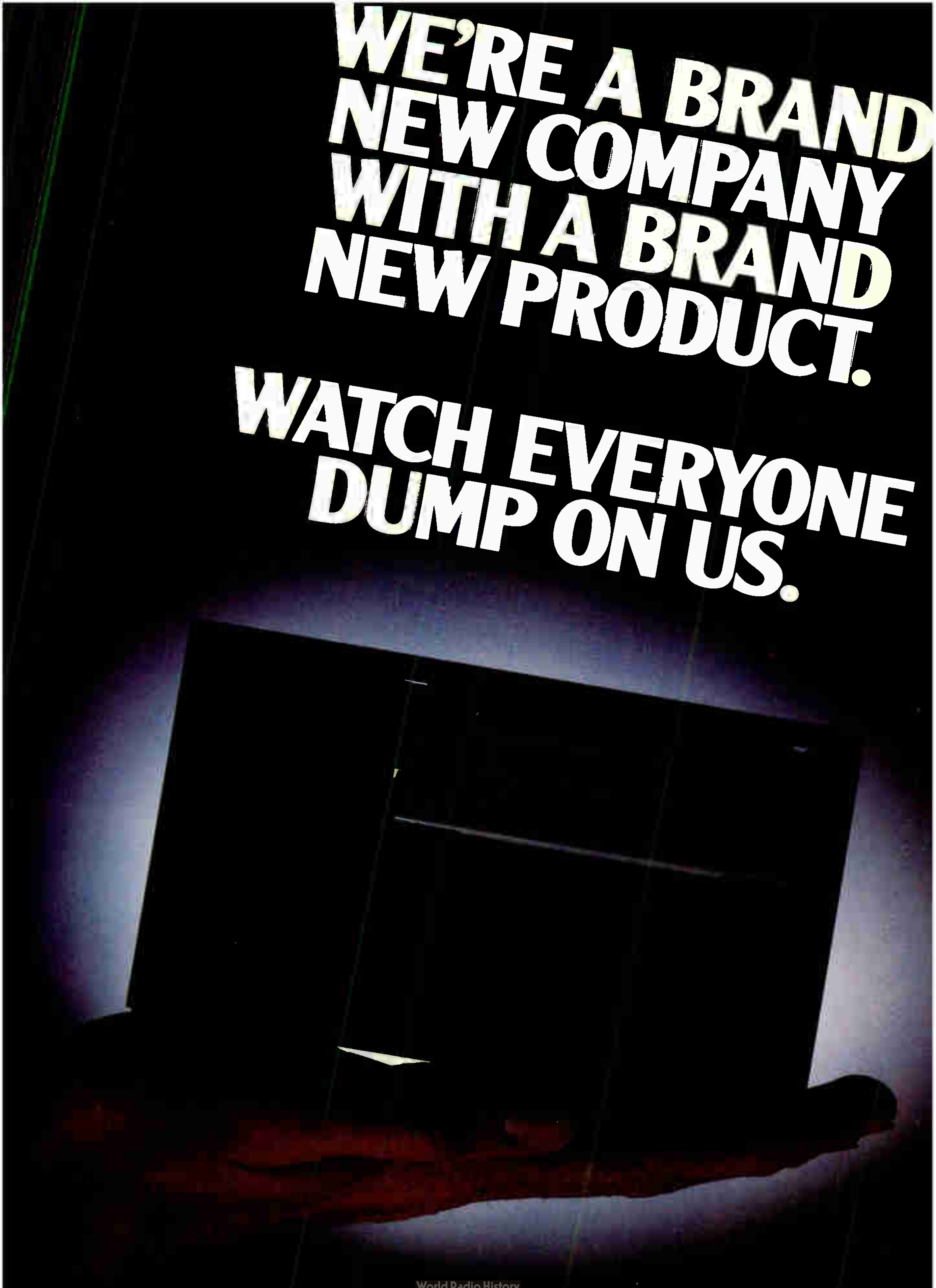


U S INDUSTRIAL PRODUCTION INDEX[1]	May 1983	April 1983	May 1982
Office and data-processing equipment	262.3	260.6	241.6
Communications equipment	176.7	177.8	167.8
Radio and TV equipment	80.6	80.6	78.5
Electronic and electrical instruments	156.7 (June '83)	157.0 (May '83)	164.8 (June '82)
Components	343.2	339.2	317.5

U S ELECTRONICS ECONOMIC INDICATORS			
Production workers[2] (thousands)	May 1983	April 1983	May 1982
Office and computing machines	190.2	190.2	190.8
Communications equipment	261.4	260.8	268.1
Radio and TV receiving equipment	60.3	59.7	63.5
Components	335.7	335.7	322.9
Shipments[3] ($ billions)	May 1983	April 1983	May 1982
Communications equipment	3.934	3.994	3.696
Radio and TV receiving equipment	0.729	0.759	0.711
Electronic and electrical instruments	3.938	3.971	4.158
Components	2.845	2.688	2.698

U S GENERAL ECONOMIC INDICATORS	May 1983	April 1983	May 1982
Index of leading economic indicators[4]	154.5	152.6	136.2
Budgeted outlays of the Federal government[5] ($ billions)	63.040	69.542	55.683
Budgeted outlays of the Department of Defense[5] ($ billions)	17.309	17.524	15.204
Operating rate of all industries[6] (% capacity)	74.1 (June '83)	73.5 (May '83)	70.7 (June '82)
Industrial-production index[1]	745.9 (June '83)	144.3 (May '83)	139.2 (June '82)
Total housing starts[3] (annual rate in thousands)	1,747 (June '83)	1,799 (May '83)	1,028 (June '82)

Sources:
[1] Federal Reserve Board (1967 = 100) [2] Bureau of Labor Statistics [3] Bureau of the Census [4] Department of Commerce (1967 = 100)
[5] Department of the Treasury [6] McGraw-Hill Publications Co., Department of Economics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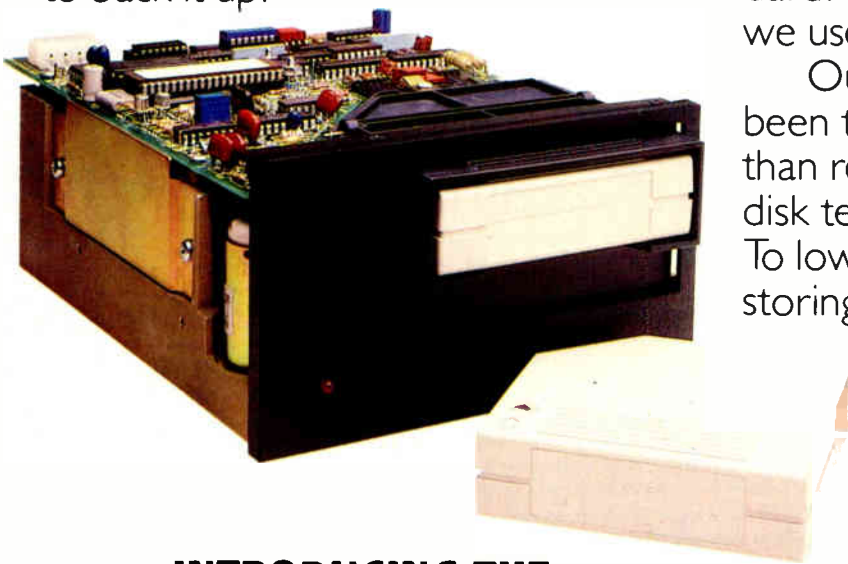
We're the newest of Tandon's advanced micro peripherals companies. Like all Tandon companies, we concentrate all our energies on a single related product line. And like them, we're dedicated to becoming the world's leading producer of what we make best.

That's a pretty brash goal for a company that just built its very first tape drive. But we have the product to back it up.



INTRODUCING THE TANDON TM951 TAPE DRIVE.

What's the world's biggest producer of micro peripheral disk drives doing in the tape drive business?

Building a half-inch tape drive with a capacity of 50 megabytes and an OEM price that's pure Tandon.

Everything about our streaming tape drive is pure Tandon. That's because we have the highest degree of vertical integration of any manufacturer in the business. Which means we can better control our costs and quality.

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Tandon got its start as a head manufacturer. Our floppy heads quickly became the industry standard. Those are the very same heads we use on our new tape drive.

Our philosophy throughout has been to use evolutionary, rather than revolutionary, tape and floppy disk technology in our new drive. To lower costs and minimize risk for storing your back-up data.

That approach has paid off not only in a low price but also in high data reliability and performance. With a soft error rate of 1×10^9 and an MTBF of 8000 power-on hours.

FEATURES EVERYONE WILL WANT TO DUMP ON.

Our low cost and high reliability will help us become number one in disk back-up.

So will our drive's great features.

The TM951 is the same size as a standard 5¼" floppy drive. It records on half-inch tape on twenty tracks, arranged in a serpentine pattern, using standard MFM format. And dual heads allow instant data verification while writing.

We not only make the drives, we also make the cartridges. From a unique Tandon design, using a video-style, self-threading, single reel for high performance and reliability.

DISK BACK-UP THAT KEEPS COSTS DOWN.

Providing the most advanced technology at the lowest possible price has made all Tandon companies leaders in their fields.

That's exactly how we intend to succeed in ours.

Five years ago our floppy company was a newcomer in a highly competitive market. Today it's the world's leading supplier of 5¼" drives.

That success story gives us a lot to live up to. Which is just what we've set out to do.

For full information on the newest tape drive from the newest tape drive company, call us. It's your chance to dump on us before everyone else does.

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The biggest advance in recording in 45 years.

The new Gould 2000W

Everything you need for trend, waveform and transient recording. Not since the oscillograph was invented in 1937 has there been anything like this. The new Gould 2000W Series merges proven digital storage technology with a superb direct writing oscillograph to deliver a compact, versatile, high frequency analog recording system.

For the first time, tremendous measurement flexibility in a single instrument. Now, you can make permanent hard copy of trend, waveform and transient data from dc all the way to 50 kHz.

Capability that leaves all other recorders behind. The 2000W is faster. Uses low-cost paper. Provides the best trace quality. Is easy to use.

Key Features
- dc to 50 kHz response
- 10 μs transient response
- Chart speeds from 0.002 to 13,000 ips
- Accurate triggering
- Pre-trigger viewing
- RS 232C digital output
- Low-cost hard copy
- Up to 8 channels

It lets you capture and record random and one-shot transients—even while unattended. Record pre-trigger information to show cause as well as effect. You can even transmit stored waveform data with RS232C output for subsequent analysis. And replot or retransmit the same stored data repeatedly.

In short, the Gould 2000W stands alone as the only single instrument that gives you the power of digital storage plus accurate, clean hard copy of analog signals.

Get the full story on its unprecedented break-away performance. Write: Gould Inc., Recording Systems Division, 3631 Perkins Avenue, Cleveland, Ohio 44114. Or call (216) 361-3315.

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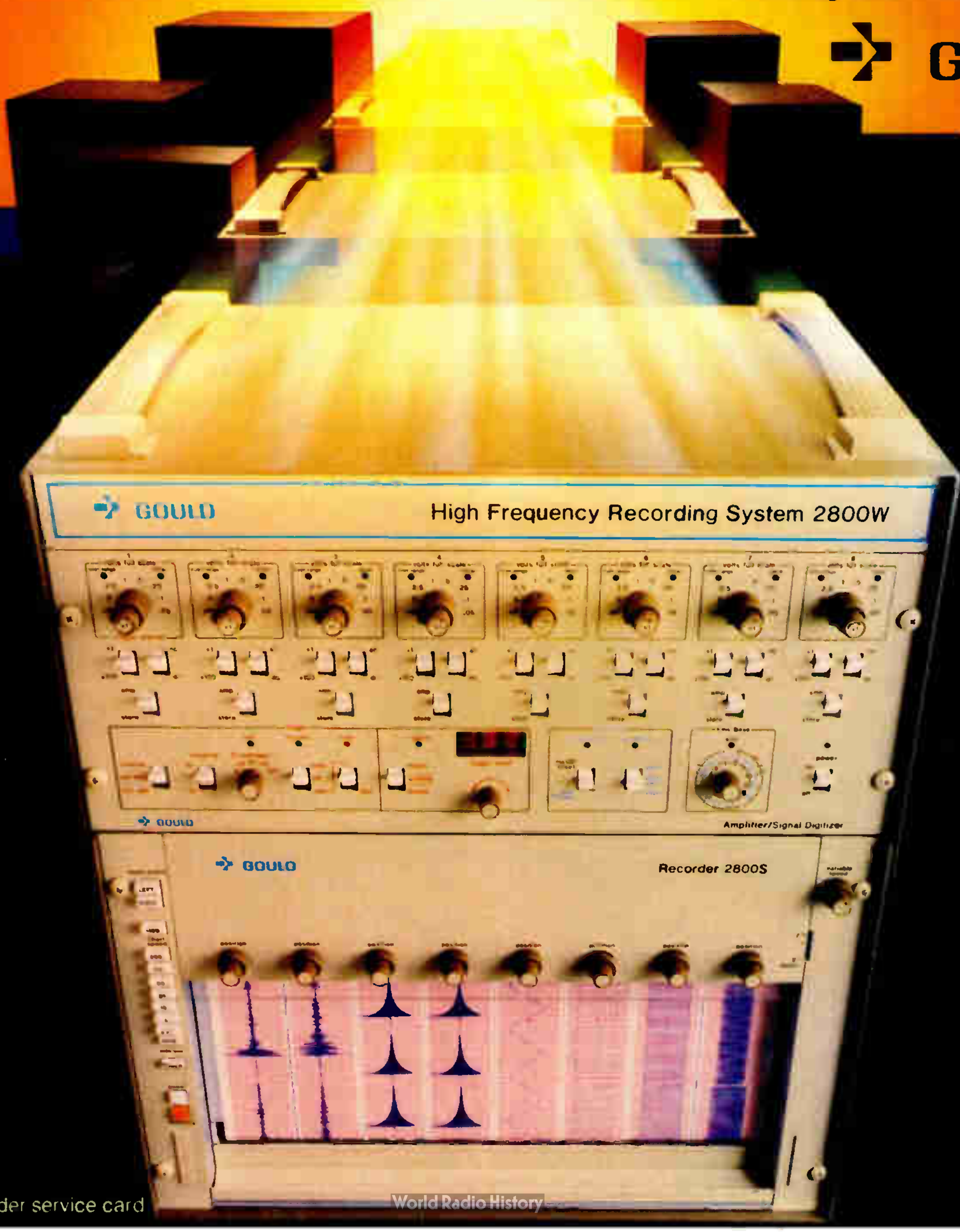


Circle 40 on reader service card

Electronics newsletter

Software links diverse systems to Ethernet . . .

Interlan Inc. has stolen a march on its fellow vendors of equipment that connects devices to Ethernet. Working with Polygon Associates, of Maryland Hills, Mo., the Westwood, Mass., firm has come up with a system that links, not the usual one device at a time, but a multitude of products. **Interlan is offering file-transfer or terminal-emulation software that hooks up such peripherals** as modems, terminals, and printers; 12 makes of personal computers, including those from IBM, Apple, Digital Equipment, Xerox, Osborne, and Televideo; three microcomputer development systems from Intel and Motorola; and four minicomputers from Digital Equipment. By attaching these devices to Interlan's new hardware—the NTS10 terminal server, which is connected, in turn, to an Ethernet—network users can link personal computers to other personal computers, to host computers, to peripherals, and to development systems.

. . . though hardware makes actual connection

Interlan's network software transmits and receives error-free ASCII text files and binary files. It will facilitate access of data from remote mainframes or minicomputers, since the NTS10 interfaces any RS-232-C serial input/output device (including mainframes) to an Ethernet or to any collision-detection–based network satisfying the 802.3 specification of the Institute of Electrical and Electronics Engineers' Local Network Standards Committee. But the four- or eight-port NTS10 is more than a simple interface. **It also allows port switching, so that different computers on the network can be accessed,** and it searches for an open port on a called computer if the requested port is busy. It also handles privileged users, permanent connections, symbolic port naming, passwords, and diagnostics. To simplify software upgrades, the NTS10's software is resident in random-access memory and boot-loaded from an NTS10 boot server. The $3,200 eight-port version, part of the new Net/Plus line, can be daisy-chained to 32 ports. Shipments start next month.

Seagate sets high-speed Winchester interface

With small manufacturers of high-performance 5¼-in. Winchester disk drives and controllers scrambling to establish a new standard high-speed interface, Seagate Technology will release its own late next month. The Scotts Valley, Calif., company gives no details except to say that the interface will be tied to a new product but **will not be compatible with existing controllers because it will have a higher transfer rate** than its commonly accepted 5-Mb/s ST412 controller. The new interface will, however, be as consistent as possible with the ST412, Seagate says.

Research teams report bipolar SOI transistors

Silicon-on-insulator technology, established as one of the most promising vehicles for high-speed, high-density MOS circuits, could begin extending its benefits to bipolar devices as well. In achieving what they say are the first bipolar transistors built on SOI wafers, researchers in Cambridge, Mass., at the Massachusetts Institute of Technology and in Lexington at MIT's Lincoln Laboratory say they have achieved the first bipolar transistors built on SOI wafers. They are using a heating and recrystallization process developed at Lincoln Lab [*Electronics*, Oct. 6, 1981, p. 44], which they report **eliminates the large-crystal dislocations that have made SOI thin films off limits for bipolar parts.** The higher-quality silicon and silicon dioxide films also increase the nanosecond-

Army chooses radio for the millimeter range

by Marilyn A. Harris, Staff reporter

Gallium arsenide oscillator yields electronic tunability across a 2.5-gigahertz range, the widest yet available

After a decade's wait for sturdy equipment that could transmit and receive signals in the millimeter-wave band, the Army finally has its hands on a radio it likes—the first that is electronically tunable over a 7% band (at 38 gigahertz). The radio should be in pilot production by mid-1985, and commercial versions, exploiting its ability to carry high-speed data, will likely be spun off shortly thereafter.

Millimeter-wave radio—both lightweight and difficult to intercept—has long played a part in the Pentagon's scenario of sleek, fast, high-tech combat units. In June, United Technologies Corp.'s Norden Systems division, Norwalk, Conn., delivered eight multichannel command-post radios to the Center for Communications Systems at Fort Monmouth, N. J. They have passed almost all the military-qualification tests posed to them over the –50°-to-+160°F temperature range. Only fungus and salt-spray tests remain.

GaAs. The radio's range is 8 kilometers or so, with enough gain margin to ensure 99.9% availability in all weather. Based on a gallium arsenide Gunn diode, its transmitter-oscillator unit puts out 20 dBm at 100 milliwatts of power over the full 7% tunable range from 36 to 38.5 GHz.

That combination sets a record, says John W. Strozyk, chief of Fort Monmouth's millimeter-wave–radio team. "Other GaAs diodes may put out more power, but with nowhere near the tuning range—say, 200-mW output with only a 500-megahertz or 1-GHz range. Or they may tune a full 3-GHz range but only put out 20 to 30 mW."

Within that 2.5-GHz range, Norden has managed to fit five full-duplex rf channels, each of which can carry up to 20 megabits of data per second, analog color TV with voice, and digital TV from 100 kilobits a second to 20 Mb/s. The radio, which Strozyk calls a "universal workhorse," can interface with most present Army communications gear.

More reliable. Electronic tuning was a must, Strozyk says. The usual tuning method is to fix a cavity resonator mechanically at the factory for a particular carrier frequency. Electronic tuning, which Norden handles with a varactor that has a voltage change of under 20 volts, is more flexible and reliable and needs less maintenance than mechanical tuning.

At first, the Army could not find suppliers of the high-performance GaAs diode. "Manufacturers considered it too risky to shoot for a 7% tuning range with that power output," notes Strozyk. Norden, once it won the contract in 1980, went for the part to Central Microwave Corp., in St. Louis.

The challenge, says Norden's Sal Amoroso, manager of the receiver group, was to couple the varactor and the Gunn diode and lower the equivalent Q factor, while maintaining frequency stability. The radio's channels are burned into two programmable read-only memories, one

On the air. A member of the Army's millimeter-wave and superhigh-frequency team operates a multichannel command-post radio over a 13-km test link at Fort Monmouth, N. J. The 27-lb advanced development model includes a 10-in. Fresnel lens, as well as GaAs components.

each for the local and the transmit oscillator.

The Army has more than battlefield applications in mind, says J. Robert Christian, chief of the multichannel transmission division. For one, Fort Monmouth is already installing a 13-km test link that could upgrade its voice phone links for data transmission. Since each radio system can carry 20 Mb/s of data, one replaces about a dozen Bell System T1 1.5-Mb/s carriers.

"Most domestic Army bases are over 25 years old," Strozyk notes. "The cabling is old and patched—it can't take data without an unacceptable level of error." One way to avoid expensive phone bills, he suggests, is to install fixed-frequency versions of the line-of-sight radios.

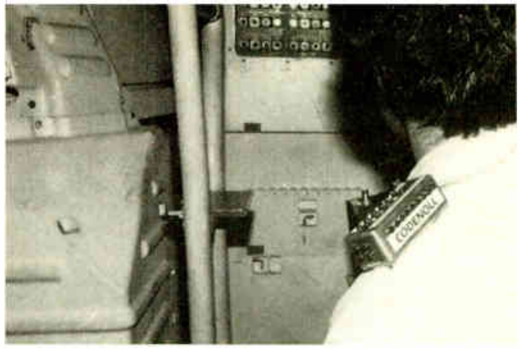
Under $2,000. That is where the system's commercial possibilities emerge. M/A-Com Inc.'s Millimeter Products Co., Burlington, Mass., may just have a leg up on the competition. Late last month, its $800,000 bid won a two-year Army contract to set up a pilot production line for fully integrated front ends, including the receiver and transmitter portions. The goal, says Wesley Matthei, manager of government operations for M/A-Com's Components Group, is to get the unit price below $2,000.

After M/A-Com satisfies its defense obligations, it can shoot for commercial versions—which may be microprocessor-tuned—by making a simple frequency adjustment, says Matthei. In fact, he notes, the company bid low on the Army contract to gain just that opportunity. "We're an aggressive company," he says, "and we'll be starting to study commercialization in about a year—as soon as we get out the first Army breadboards."

Communications

Astronauts to talk via infrared headsets

As the space-shuttle program nears full operation, the National Aeronautics and Space Administration's Johnson Space Center has started upgrading some spacecraft subsystems to accommodate larger flight crews and more complex missions. The prime target for improvement is the rf communications equipment, for besides being too large and heavy, it must meet the Department of Defense's so-called Tempest standards for electromagnetic radiation induction and leakage in order to fulfill future secret DOD missions.



Infrared epaulet. Prototype infrared p-i-n diode receiver built for NASA by Codenoll Technology is worn like an epaulet during a test inside the shuttle simulator.

Tempest satisfied. According to Harry Erwin, head of the microwave and laser section at the Houston, Texas, center, optical communications systems relying on radiated infrared carriers are the solution. Such free-space optical systems, as they are called, make unnecessary the costly process of proving to Tempest specifications that fields induced by rf communication links do not reradiate from the spacecraft structure and wiring. IR induces no electromagnetic fields, so satisfying Tempest standards presents no problem.

A prototype IR system has been built for NASA by Codenoll Technology Corp., a Yonkers, N. Y., firm specializing in fabricating III-V compound semiconductors and fiber-optic communications systems. It employs a digital time-division–multiplexed scheme that digitizes voice signals at a 32-kilobit-per-second rate using continuously variable-slope delta modulation. This is then multiplexed onto an intensity-modulated light-emitting diode. The scheme is planned for about the twentieth shuttle mission; in June, the seventh was successfully completed.

A digital, rather than an analog, approach was picked because it supports multiple channels in a straightforward way while leaving room for pure data-transmission applications, such as reading data from remote instruments. Furthermore, analog systems suffer from intermodulation products caused by having one subcarrier frequency for each channel.

The TDM system employs synchronous time slots to eliminate the possibility of collisions. Manipulating 16-bit frames and transmitting 32,000 frames per second, the system has an aggregate data rate of 512 kb/s, fast enough for six astronauts to communicate simultaneously with mission control on the ground, even with the synchronization overhead.

P-i-n epaulets. In Codenoll's system, each astronaut will wear p-i-n–diode arrays mounted on a pair of epaulets. These arrays connect to a headset by wire. LED transmitters on the headset send data to transceivers mounted at key places inside the crew areas of the shuttle. The transceivers are linked to the rest of the shuttle communications system and, therefore, to earth.

Lithium-battery packs in the epaulets will last about 8 to 12 hours per charge. Since the IR radiation fills the entire spacecraft, communication can proceed without interruption as the free-floating crew moves around.

For Codenoll, the project has grand implications. By making slight modifications, the firm has the chance to commercialize not just a voice communications system but a full-duplex free-space data network.

In particular, Michael Coden, Codenoll's cofounder and chief executive, is eyeing the electronic office. His system could greatly simplify the wiring of work stations, for as many as 32 terminals, corresponding to the system's 32 addresses, could be interconnected with IR links instead of with wires. The only hard wiring would be the ac power cords, so moving work stations around would be an easy matter. An office system similar in concept, in fact, is being developed by Japan's Fujitsu Ltd., which described it at the National Computer Conference in May.

Codenoll's multiplexing scheme may offer advantages over Fujitsu's. It reduces access-protocol overhead and permits full-duplex operation. Full-duplex networks with speeds of around 1 megabit/s could be built on a single fiber, instead of with the dual transmit-and-receive fibers now required, Coden says. The installed cost could be below that of copper twisted-pair wire, hastening fiber's entry into such applications, he concludes. –Roger J. Godin

Local networks

IEEE-488 bus to get a local-net route

The IEEE-488 bus has cropped up in a multitude of systems since its adoption eight years ago by the Institute of Electrical and Electronics Engineers. Its most popular niche—in test and laboratory markets as a byte-wide digital interface between a master computer (or controller) and instruments slaved to it—is about to be carved even wider by National Instruments Corp. The Austin, Texas, firm is preparing software that converts the bus for a local-networking scheme that allows control to pass from one host to another.

Just as in the office-automation market, a multihost network in the laboratory would provide a common data path for sharing such expensive peripherals as test, measurement, and plotting gear among work stations and computers. Such networks could also handle computer-to-computer file transfers, providing, for example, an easy data path for one engineering operation to pass its work and measurements on to another. What's more, control of an experiment or test could be handed off to another computer if the host was needed for a higher-priority task.

Next year. National Instruments will introduce the software to turn the IEEE's General-Purpose Interface Bus into a full-fledged token-passing network early next year. It is be added to the company's NET488, a hardware and software interface that lets general-purpose computers transfer files over the standard IEEE-488 bus (or GPIB).

NET488 had its origins early last year in a scheme for transferring files among a variety of Digital Equipment Corp. computers. Expanding the concept to other computers, National Instruments introduced IEEE-488 interface boards for S-100 and Multibus-based based units [*Electronics*, Aug. 25, 1982, p. 154, and April 7, p. 178]. In May, it began expanding its file-transferring software to these units as well as to IBM Corp.'s Personal Computer. STD- and VME-bus systems are due to be available by the fall.

In engineering, test, and laboratory facilities, a byte-wide, token-passing NET488 will in the long run have a great advantage over highly publicized bit-serial approaches such as Ethernet, asserts Donald Nadon, strategic marketing engineer at National Instruments. The reason is familiarity: the organization and protocols of the IEEE-488 bus are better understood by more potential users than any other networking package, he says.

Plug-in. Well over 2,000 types of equipment from more than 180 manufacturers are made with IEEE-488 ports, permitting their direct attachment to the bus. Networking usually requires extra interface hardware, but with its upcoming token-passing capabilities, the NET488 system will fit onto a single plug-in interface board. Relying on the IEEE-488 bus also ensures a source of low-cost, debugged interface chips, Nadon notes. Large-scale integrated circuits for other networks, just now coming to

Static-RAM access drops to 35 nanoseconds

Hoping to give "fast" yet another meaning in the static-random-access-memory arena, Motorola Inc., Austin, Texas, is now ramping up to produce a 16-K-by-1-bit MOS RAM chip clocking in with a 35-nanosecond access time. Thus, the MCM2167H beats its nearest MOS competitors by a full 10 ns, which should encourage makers of high-speed supercomputers. Hot on Motorola's heels is Advanced Micro Devices Inc., Sunnyvale, Calif., which is showing samples of a 35-ns version of its AM2167 part to select customers.

The 10-ns advantage could help eliminate processing bottlenecks in supercomputer main storage and high-speed cache memory, notes Peter Gregory, vice president of planning and corporate development at Cray Research Inc., Minneapolis. As MOS-memory speed increases, the more expensive bipolar RAMs, with their generally lower bit densities, can be replaced. "It's worth noting for all future systems that memory has not kept up with the kinds of speed improvements we are seeing in logic," says Gregory. "Therefore, it becomes the bottleneck, and any improvements in memory become proportionately more attractive."

Cost is also an advantage. For example, the price of a Cray 1 supercomputer with 8 megabytes of memory was slashed less than a year ago from \$7.2 million to \$4 million by switching from 4-K-by-1-bit bipolar chips to denser, if slower, MOS parts, says Gregory. A smaller cooling system and the need for less board space helped, too. The switch incurred only a 5% speed penalty.

Housed in a ceramic dual in-line package, the n-channel MOS memory sells for \$40.18 each in 100-piece lots. A 45-ns version is \$21.36. The 20-pin chip is fabricated from Motorola's H-MOS II Plus technology with 2.5-micrometer line widths and a metal pitch of 7 μm. The by-1-bit RAM is similar to an older Motorola 2-K-by-8-bit part, the 2016H, whose byte-wide 45-ns access speed is targeted at microprocessor-based systems [*Electronics*, Jan. 13, p. 48]. Maximum dissipation of the new 2167H is 128 milliamperes while active, compared with 90 mA for the byte-wide part.

Other chip makers, like Integrated Device Technology, Inmos, Toshiba, and Sharp, have mentioned 35-ns parts for "the near future." Meanwhile, "We see the fast static-RAM 16-K market—70 ns and below—just starting, and peaking in 1986 at \$135 million," says Richard R. Phlegar, a Motorola strategic marketing engineer. About half will be 35-ns parts. **–J. Robert Lineback** market, are more expensive.

Though other networks may tout higher data rates—for example, Ethernet runs at 10 megabits per second—National Instruments believes NET488's 4 Mb/s is adequate for most uses. Still, it acknowledges that bit-serial schemes will continue to dominate in office markets that are unfamiliar with the IEEE standard. But because NET488 is "on the fringes of the office-automation market," according to Nadon, the company is also prototyping a NET488 gateway to Ethernet, hoping to slice off a piece of that action, too.

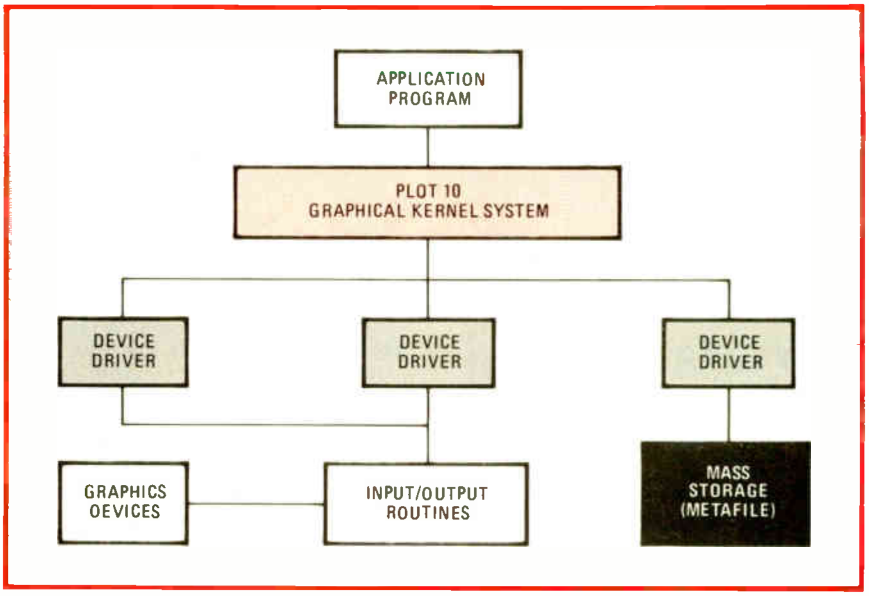
Tailored. He says that because NET488 employs a parallel bus architecture for both data transfer and network management, its software is more easily tailored than other networking schemes to a range of characteristics, such as token passing and even the Ethernet-like carrier-sense multiple access with collision detection. This amenability would enable equipment integrators to create hybrid transmission schemes, with networking modifications made through the NET488 source code.

The IEEE-488 bus's eight parallel control lines—three handshake and five bus-management lines—and its byte-wide data bus make for its exceptional flexibility. These lines provide many control combinations without the extra software overhead required by bit-serial networks. With standard IEEE-488 cable, links between devices can stretch 300 meters per extender box at $1,000 to $2,000 a node, including software. The token-passing enhancement is expected to add little, if at all, to system costs. –J. Robert Lineback

Computer graphics

Graphics standard gets boost in U. S.

Though formal acceptance may not be stamped on it until next year, the proposed Graphical Kernel System standard for graphics software gained a major backer last month. Tektronix Inc., the giant instrumentation manufacturer, said it was offering a software package, PLOT 10 GKS, that follows the graphics programming syntax being developed by the American National Standards Institute and the International Standards Organization.



Standard. Graphics application programs work with a standard set of functions with Tektronix' PLOT 10 Graphical Kernel System. The output goes to operating-system device drivers, which could be replaced by another proposed standard, one for a so-called virtual-device interface. The metafile is a proposed standard for storing graphics information.

Tektronix announced its offering late last month in Detroit at a meeting of the Special Interest Group for Graphics (Siggraph) of the Association for Computing Machinery. With its set of Fortran routines, it will be the first such package to be widely available, although other companies are reportedly developing versions.

Usually, graphics software is written from libraries of subroutines that may differ widely from one computer installation to the next and must be rewritten extensively in order to be transported. Programs using GKS-compatible packages may be transported as is.

Fortran 77. PLOT 10 GKS, from Tektronix' Information Display division in Wilsonville, Ore., is a set of Fortran 77 subroutines that can be called from application programs. In turn, output from PLOT 10 GKS passes through operating-system device-driver subroutines (shaded in the figure) either to create graphical output directly or to be stored in a file on a mass-storage device as data to be plotted later.

An earlier standards proposal by Siggraph, called Core, has also earned a measure of acceptance in the U. S., and Core packages are likely to coexist in the marketplace with the new standard [*Electronics*, May 19, p. 32]. Tektronix, for example, offers a plotting package, called PLOT 10 IGL, based on Core.

However, GKS, originally developed in West Germany, is considered simpler than Core and easier to implement. The original GKS was modified by ANSI's X3H3 committee, which was charged with developing a graphics standard, as well as by the ISO. The two organizations agree on fundamentals, though ANSI has included some supplemental sections.

For one thing, it allows for a subset of the full GKS specification. Called minimal GKS, this subset is intended for hardware with more limited graphics resources, such as personal computers. Also, ANSI allows a looser interpretation of conformance to GKS. There is, of course, a minimal set of functional specifications, but, after that, vendors may supply additional procedures, though at the risk of losing transportability. ISO, on the other hand, requires

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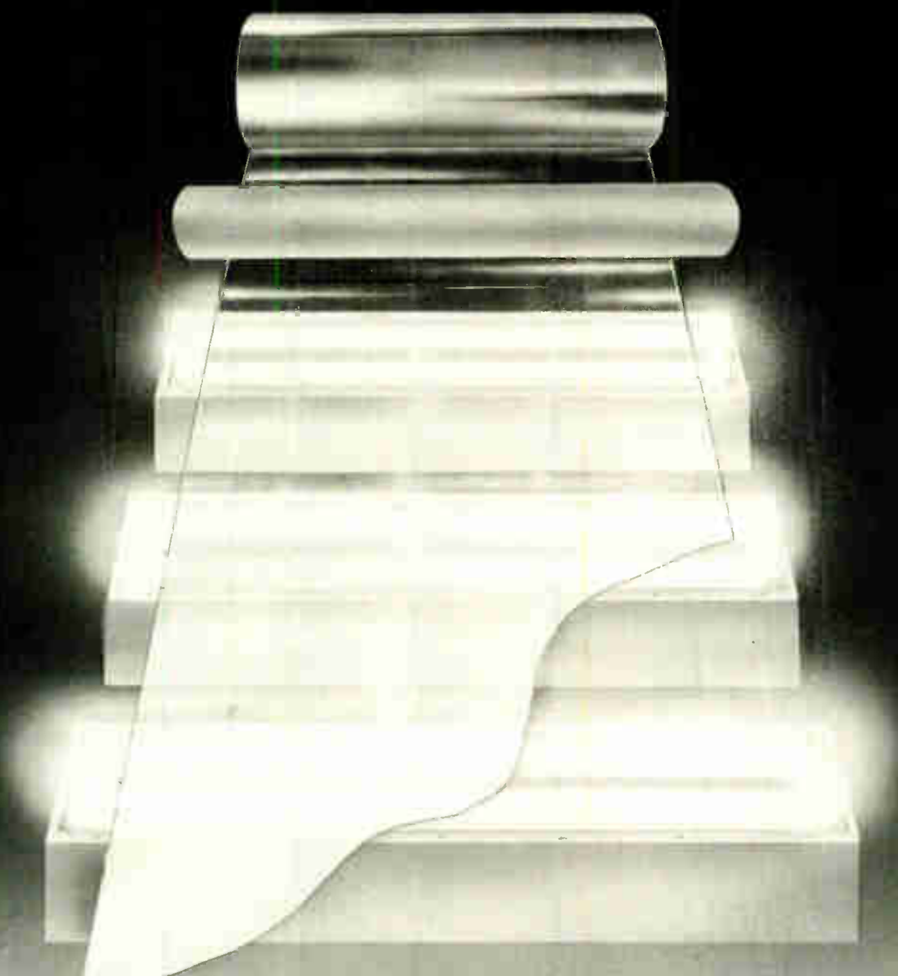

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Moving somewhat faster than ISO, ANSI is including descriptions of interfaces with specific programming languages, called bindings. One of the first language bindings will be Fortran; however, Basic, the U. S. Department of Defense's Ada, C, and Pascal are expected to follow.

More. GKS is, though, only part of the picture. Other graphics standards are in development [*Electronics*, Feb. 24, p. 124]. Included is an ANSI specification for a virtual-device interface to make all graphics hardware devices, such as cathode-ray tubes and plotters, appear similar.

Thus, in effect, one standard software package would replace the various device drivers currently needed. Another specification, called the virtual-device metafile, is for a standard method of storing graphical information. Further, three-dimensional graphics are being considered separately by European and U. S. software designers. **–Stephen Evanczuk**

News Briefs

Consortium awards contract for 1-micrometer device technology
Semiconductor Research Corp., the industry consortium in Research Triangle Park, N. C., has awarded $551,000 to the Microelectronics Center of North Carolina to research materials and low-temperature manufacturing processes leading to the production of 1-micrometer complementary-MOS devices. The award covers five major tasks: device modeling; shallow-junction fabrication techniques; methods for removing impurities; the use of plasma processing to grow and deposit films at relatively low temperatures; and the development of new instruments to detect particulates in the 10-to-100-angstrom range. Though the contract will span only nine months, it marks the beginning of a funding relationship likely to last five years—about the time planned for transferring to industry the technology for 1-μm C-MOS field-effect–transistor logic and memory devices, says SRC executive director Larry Sumney. The Microelectronics Center is a privately funded research and teaching institution affiliated with five universities in the Research Triangle Park area.

Fast-food marketing comes to computers
Coin-operated computers for the traveling businessperson may turn out to be just as ubiquitous and accessible as the familiar golden arches that span U. S. highways. Data & Research Technology Corp., Pittsburgh, has designed a desktop computer terminal and printer combination that takes $1 and $5 bills and gives 3 minutes of computer time for a buck. Called the Answers Machine, the first will be installed next month for a trial in a Sheraton Hotel in Pittsburgh. Plans are for installation in hotel lobbies and other public places in 50 U. S. cities by 1984. "We believe this is like a soda machine or pay phone," says company president Ken McNulty. Businesspeople on the move will be targeted first, he adds, but the firm says it ultimately wants to popularize the convenience for "John Q. Public" and become "the McDonald's of information."

Solarex will nurture amorphous silicon
RCA Corp. has licensed its effort to develop photovoltaic solar cells made of amorphous silicon to Solarex Inc., a supplier of solar-cell arrays in Gaithersburg, Md., and will cease further development on its own. Next month, Solarex starts work in a new 15-person facility near RCA's David Sarnoff Laboratories, in Princeton, N. J., whence the technology comes. Cells made of 1-micrometer-thick films of amorphous silicon deposited on glass promise to be much cheaper than standard silicon-crystal designs, which are 300 times thicker. The difficulty has been in boosting the amorphous cell's efficiency from its disappointing 4%-to-5% range. Commercial panels are not expected until 1990, says Solarex vice president John Goldsmith, who hopes to make cells to match the 14%-to-15% efficiency possible with Solarex's Split semicrystalline process [*Electronics*, March 24, p. 52]. RCA declined comment on its action.

Industrial

Capacitance sensor makes robots safer

As robots move into light assembly operations, human interaction with the machines is likely to grow, increasing the chances of injury due to human carelessness or robot malfunction. At General Motors Corp., a system that makes for a safer robot is set to move from prototype to field testing this fall.

Stopper. Known as Roboguard, the system is under development at the GM Technical Center. It relies on a capacitive sensing system tied to a dedicated computer that halts a robot arm in mid-motion if a person comes too close.

The system may eventually serve as an alternative to current safety methods that erect fences or other barriers to limit access to robot work areas, explains Lee O. Reid, an associate engineer in robotics on the Warren, Mich., center's advanced product and manufacturing engineering staff. A multiple-branched antenna is mounted rigidly on the robot's arm, and a weak electromagnetic field is projected around the antenna in about a 12-inch envelope.

Attached to the antenna is a GM-developed sensor for detecting the capacitance changes that occur when any conductive or dielectric object, including a person, intrudes within the envelope. The sensor output is an analog voltage, varying between roughly 2 and 14 volts, that is converted into a digital signal and fed to the computer.

Signatures. As the robot goes through a work routine and moves its arm about, the sensor output varies with changes in the distance of the arm from metal workpieces or other conductive or dielectric objects. Monitoring these variations leads to development of a signature for each


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work routine, which is stored in computer memory. Any change in that signature caused by the intrusion of an unexpected object, such as a person's hand or body, can thus be detected, and the system programmed to stop the robot if the intruder moves too close to its arm.

Prototype. The center so far has put Roboguard through about six months of testing in a prototype that works with a Puma robot from Unimation Inc. and a Digital Equipment Corp. PDP-11/23 minicomputer. Through changes in the system software, GM researchers have already overcome problems with electrical interference, which caused the system to shut down the robot arm at improper times, says Reid. A second system now being built will begin tests in a GM division plant this fall.

Among other factors to be studied in the next nine months or a year, says Reid, are the system's ease of use, maintenance costs, repeatability, and reliability. If the results are favorable, the next step would be to develop a microprocessor-based version that could fit in a small box at a robot's base.

Applications within GM could eventually be vast. A pioneer in robot use, the automobile maker has a significant commitment to the technology, with plans to employ 14,000 robots or more by 1990. Some 2,500 of the machines are already performing primarily heavier jobs, such as spot welding and spray painting.

Like other manufacturers, though, GM expects to make greater use of smaller assembly robots in the future—with robots in some instances working side by side with people. "Assembly robots are typically small . . . and it's easy to forget that you can still get hurt by them," Reid observes. The system is being considered for all sizes of robots, however.

Safety features. Robots today come equipped with a variety of safety features, including emergency stop buttons and motor overload systems that stop an arm when contact is made with an object, notes Reid. He claims, though, that GM's scheme is the most sophisticated available.

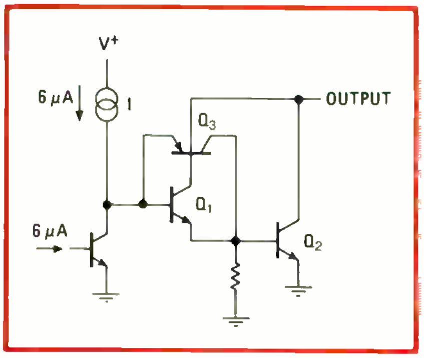
GM is also one of several companies supporting robot safety research being conducted at the Rensselaer Polytechnic Institute, Troy, N. Y. The RPI effort has been directed at various types of safety systems, employing technologies including microwave, ultrasound, and infrared sensors, as well as capacitive sensor techniques. –Wesley R. Iversen

Circuit design

Merged transistor yields low-power IC

Although the advent of complementary-MOS microprocessors and memories has generated increasingly portable low-power systems, plus their accompanying low-power components, low power can be achieved without C-MOS, especially in the analog world. One example is a technique developed by engineers at National Semiconductor Corp. to create a C-MOS–compatible quad comparator.

The Santa Clara, Calif., chip maker introduced its first quad comparator about 10 years ago. The LM339 packed four independent comparators in a 14-pin dual-in-line package selling in 100-unit quantities for 46¢ apiece. Other unique features included 36-volt operation and the ability to pull the outputs to within 0.3 V of ground (which meant that it could sink higher currents without dissipating excessive power). What's more, for a device not especially low in power, it had reasonable specifications: a supply current of 800 microamperes, a bias current of 25 nanoamperes, and outputs that could each sink 16 milliamperes.



Merged. With switching transistor Q_3 sitting across transistor Q_1 of the Darlington pair and sharing its collector and its base, Q_3's switching point occurs at just the proper voltage to provide a glitch-free output.

Trick. To improve that device, says Dennis Monticelli, the trick was "to come up with a new part with significantly decreased supply and bias currents without sacrificing output drive current or the ability to pull very close to ground." Monticelli is group leader for National's industrial linear–integrated-circuit design department.

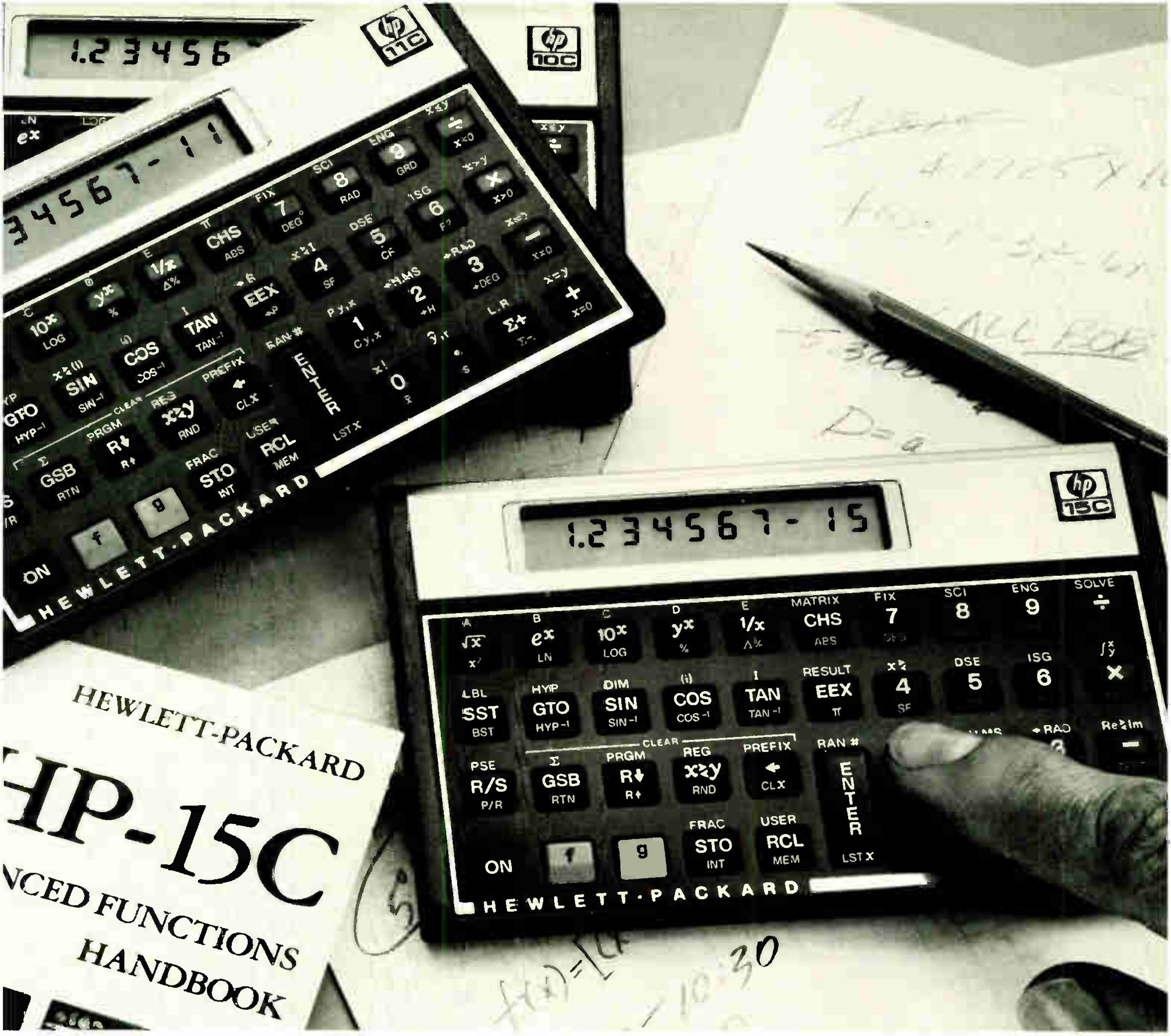
The obvious solution was to replace the LM339's single-transistor output stage with a Darlington transistor pair, which would require much less bias and supply current. "The problem with a Darlington, however," says Monticelli, "is that it won't pull closer than about 1 V to ground, which was not acceptable."

To get around this, Monticelli designed an output stage with an extra transistor merged into the base region of a Darlington pair (see diagram). The Darlington functions as the output starts to pull down. Then, because the third transistor essentially short-circuits the first drive transistor in the Darlington, the output switches over to one output transistor, enabling the output to pull to within 0.3 V of ground.

The key to the new technique, which National expects to patent, was to design a merged, three-transistor output, so that the switchover occurs without a glitch. That is, the transition between the Darlington configuration and the single output transistor must be smooth.

Built-in switch. To accomplish this, the switching transistor, Q_3, is built as part of the Darlington pair. That transistor sits across the collector and base of the initial drive device, Q_1. As the output voltage goes down, pulling closer to ground, Q_1 saturates first. At that point, its collector-base junction is forward-biased, causing Q_3 to turn on, bypassing Q_1 and feeding the drive current directly to the second transistor in the Darlington pair, Q_2.

"It's a Darlington when you need it for high gain, and it supplies high



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current when you start to pull the output down," Monticelli points out. "It switches to a simple, single-transistor output when you get about 0.8 V from ground, allowing the output to pull to within 0.3 V of ground."

Nesting. To smooth the switching, Q_3 is actually part of Q_1 and Q_2—the merged-transistor structure. Q_1 is nested within the base region of Q_3; Q_3's emitter-base junction is Q_1's collector-base junction; and Q_3 and Q_2 share a collector-base junction

"There is no problem as to when Q_3 turns on," says Monticelli, "because the junction of Q_1 that defines its saturation point [its collector-base junction] is the same junction [the emitter-base junction] that defines when Q_3 turns on. Q_3 can't turn on too soon because its turn-on is determined by Q_2—its base drive can't be shut off too soon." What's more, the merged-transistor structure takes up no additional die area.

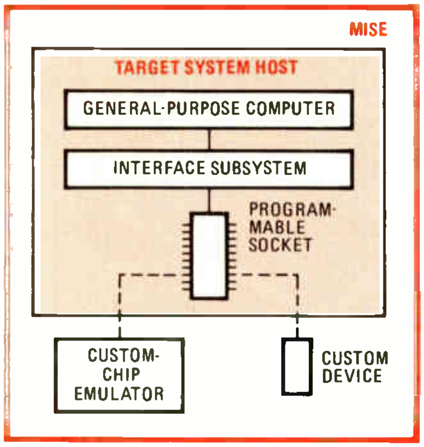
The result is the upcoming LP339, with its supply current of 60 μA, in contrast with 800 μA for the older LM339; input bias current of 3 nA, instead of 25 nA; and an output-sink capability of 30 mA, as opposed to 16 mA. The only performance sacrifice is that the new device's response time has been slowed to 8 μs, compared with 1.3 μs for the old one.

Samples of the new quad comparator will be available in September, to sell for 72¢ each in 100-unit quantities. Automotive-temperature-range parts and a dual part in an eight-pin DIP are also in the works, all C-MOS–compatible. –**Stephen W. Fields**

Systems integration

Chips and systems get togetherness test

What could be the cat's meow of custom VLSI chip testers is now on the drawing board at Carnegie-Mellon University, in Pittsburgh. The tester will not only evaluate chip designs by simulating them in software but simulate the design's reaction to a target system, as well. Actual chips too can be tested.



Real data. MISE, the machine for in-system evaluation, will test a custom VLSI chip—either emulated or in silicon—while it interacts with a simulated target system.

Until now, simulators have been used for devices only. Chip and system interaction could be evaluated either by laborious modeling with custom software or by hand-done calculations. Once designers thought a design might work, the next step involved breadboarding a target system and building a custom emulator for the chip. Engineers would figure out how to test an actual chip by estimating how it would interact with the still-unbuilt target system.

All in one. When Carnegie-Mellon's MISE (machine for in-system evaluation) is finished, it will unite these processes in a single machine. MISE, asserts Prof. H. T. Kung, head of Carnegie-Mellon's computer science department, "will provide system integrators with a way to avoid deluding themselves about the usefulness of their chips."

Kung and his colleague, Prof. Roberto Bisani, the MISE project manager, used funding from the Office of Naval Research, the Defense Advanced Research Projects Agency, and the National Science Foundation to build the first hardware and software parts of MISE, which now simulates one VLSI chip at a time. Multichip architectures and chip emulators will be accommodated later.

Host. MISE's architecture (see figure) includes a target-system host for either a custom-chip emulator or the chip itself. The host includes a general-purpose minicomputer, an interface subsystem to a programmable socket that holds the chip, and the software to develop several target-system simulations and control the interface to the custom chip.

For instance, to evaluate a VLSI chip for controlling the joints on a robot arm, the host simulates both chip and arm movement. The computer monitors the simulated interaction of the chip and the target system. Once built, the chip replaces its simulator and the chip–target-system interaction is simulated again. At any point *en route*, the designer can see the results, presented on a graphics terminal through simulation data captured on the system's disk drives.

The interface subsystem has memory, buffers, input/output channels for real-time data acquisition from the chip and the target system, and a chip controller to manage data transfer from chip to central computer.

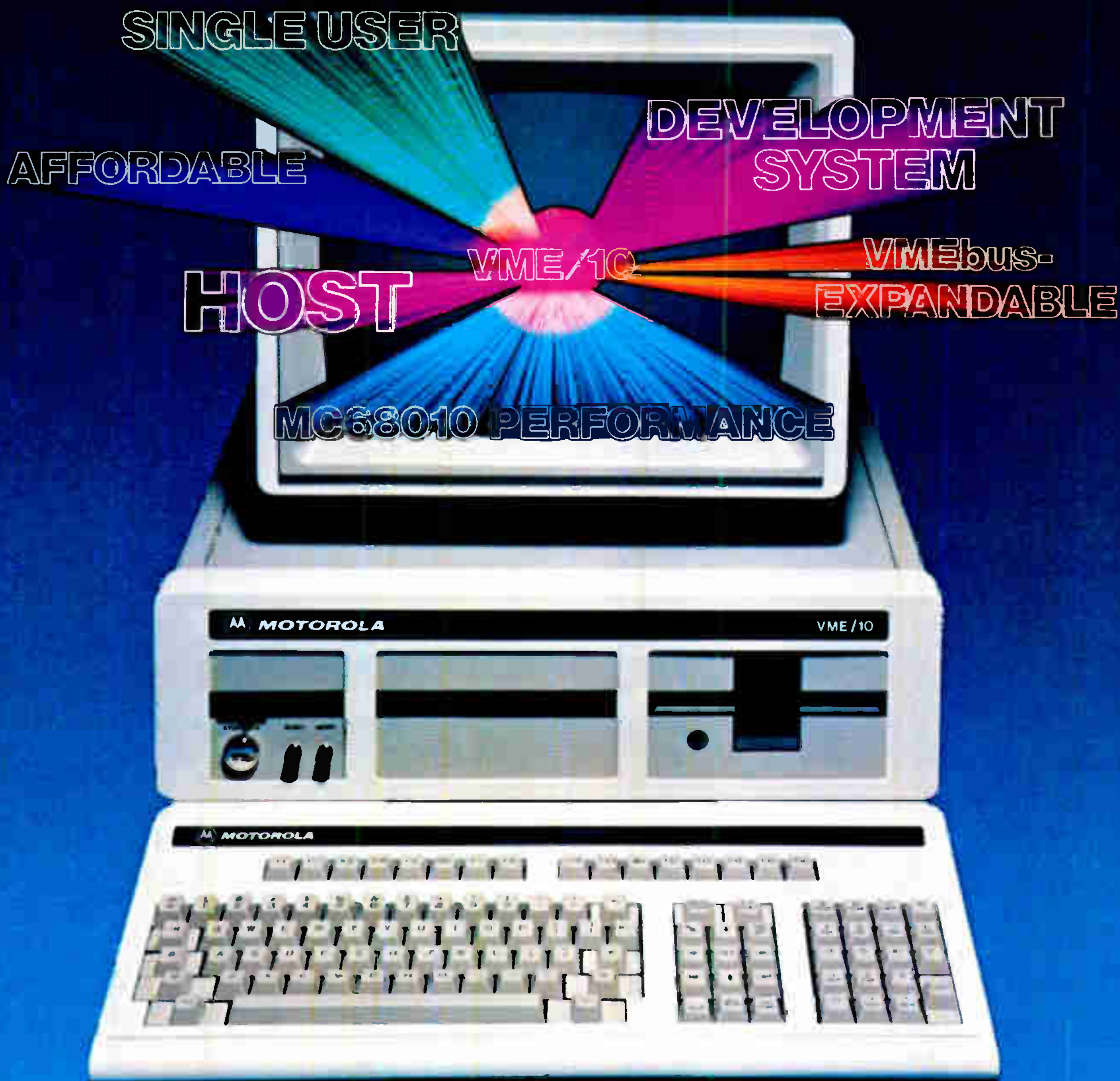
Commercial chip testers—with their fast test-pattern generators—fall short because they cannot be plugged into a target system. So they do not help users integrate the chip with the target system's software, a chore that MISE will mostly handle itself. What's more, the commercial machines cannot be programmed for as many custom chips as MISE can, and in-circuit emulators for microprocessor-based systems cannot handle custom chips at all.

Bisani says that a prototype of MISE will be finished by the end of the year. Several problems remain to be solved, including exactly how to specify the custom chips' interface behavior. Hardware-description languages could help with this chore, so Ada is being considered, says Bisani, along with more traditional languages, like Carnegie-Mellon's Slide. MISE's man-machine interface is another lingering difficulty.

Solving these problems could yield big payoffs. One current Darpa project supports 300 fast-turnaround, custom chip designs a year, with more than 1,000 expected soon. "Even if MISE supports in-system evaluation of, say, a quarter of the Darpa designs, the savings in time and money will be enormous," say the researchers. **–Harvey J. Hindin**

Motorola Reports

AUGUST 1983 ISSUE



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Stripped of development software, VME/10 becomes a powerful, state-of-the-art microcomputer with unique applications potential. It can be all or a major part of the same system it helped design.

Where other micros are optimized for one specific end use, VME/10 is configurable to **your** function—for within its attractive desktop enclosure are slots for up to nine additional modules for tailoring to many applications.

VME/10 draws on the substantial selection of VMEmodules,™ memory and I/Omodules™ offered as building blocks for instant, functional, system implementation—ensured virtual obsolescence-proof stature through IEEE standardization activities and growing industry vendor support.

A bus for performance and growth

VMEbus™ architecture, thoroughly documented and widely adopted as an international 8- to 32-bit standard, is further enhanced by the I/O Channel which increases the speed of multiprocessor systems by relieving VMEbus from servicing local peripherals...significantly valuable in I/O-intensive systems.

Mainframe memory and management

The new and powerful MC68010 virtual-memory MPU, latest in the M68000 Family, and the MC68541 Memory Management Unit provide enough capability to permit several development tasks with full protection for each and for security of programs and data in multitasking OEM systems.

Plus, VME/10 provides 384K bytes DRAM, multi-mode graphics—color and monochrome—built-in 655Kbyte floppy disk, 5 or 15 Mbyte Winchester, a full ASCII keyboard, 16 user programmable keys, numeric keypad and all the ergonomic features.

Support. Support. Support.

It's total in software and customer commitment.

From initial technical orientation and seminars to our toll-free service hotline, VME/10 answers and support are here. Always.

Because Motorola is consistently a frontrunner in technology and support, our natural—indeed mandatory—commitment to things like regular software updating programs, field application assistance, on-site installation and repair, third-party support and comprehensive documentation is a "given."

Our field-proven, warranty-backed quality and reliability is renowned.

And, in an industry full of high-priced competition, you can acquire the VME/10 **with development software for under $10,000.**

Send for a new brochure. Or call (602) 829-3501.

VME/10. Everything you want in your system. And more.

Check ☐ A for information.

Save a bundle on a bunch of TO-218 power packages.

You can save 10% - 20% - 30% and more on your power device components by designing in the industry's newest standard plastic package — the TO-218 — from the industry's standard discrete source...Motorola.

And we have a lot of them: general purpose discrete and Darlington devices, Switchmode™ units, deflection transistors, power MOSFETs, Schottky, Ultrafast and fast recovery rectifiers.

Extremely cost-effective and easy to mount, the TO-218 package is capable of 150 W P_D with lead spacing wide enough to meet most industry requirements. Its basic design lends itself famously to automated, stripline assembly techniques yielding uniform, high-volume economy and performance.

TIPoff to economy

Nowhere is TO-218 cost-effectiveness as pronounced as in our TIP-series, low-voltage, general purpose discretes and Darlingtons. The TIP33B, 10 A, 80 V NPN costs $1.15 in TO-3, just 77¢ in TO-218. The PNP TIP34B complement has a $1.35 vs. 84¢ comparison. And, the rest of the family, as well as units in higher voltages, offer similar savings.

You can save 20 to 30% with the TIP140-145, 60 V to 100 V Darlington complements and 10% or more with the MJE4340/4350 120 to 150 V discretes — just by changing to a TO-218 mentality.

And realize a more-work-for-less-pay advantage.

Plus, Motorola-originated Switchmode high-voltage devices provide optimized performance/value selection: the MJH16002-8 series of 450 V, 5 A to 8 A devices offer 0.25 μs to 0.35 μs maximum fall times with price tags as low as $2.20 in TO-218 — over a dollar less than a TO-3 costs.

A similar saving is yours in Switchmode II where the MJH13090 15 A TO-18 costs $4.10 vs. $5.15 in TO-3.

Thrifty TO-218 TMOS™ power MOSFETs

If you're into high-performance TO-3 power MOSFETs and don't like the pricing, try a Motorola TO-218 in the MEH6N/7N/8N family. They offer 350 V to 600 V, 6 A to 8 A power-handling capability with r_{DS} (on) specs as low as 0.55 Ω. The 400 V, 150 W unit is priced at $9.50...a 35% saving over equivalent TO-3s. The 500 V type has a $9.50 tag...50% less than a comparable TO-3.

Upcoming TMOS TO-218 power MOSFET intros will include performance characteristics to 25 A with significantly more efficient switching while maintaining traditional Motorola cost-effectiveness. In fact, prices may even be lower than the above series.

First source for fast TO-218 dc

Motorola is the only domestic supplier of Schottky, Ultrafast and fast recovery rectifiers to offer all three technologies in the economical TO-218.

The dual-chip, 15 A MBR3035PT/45PT Schottkys offer a 30% saving in TO-218; their 100-ups are $3.35 and $3.75 vs. $4.80 and $5.35 in TO-3. Built-in guard rings rule out dv/dt stress and they're 100%-tested for reverse trace anomalies and avalanche capability.

High-efficiency Ultrafasts for higher-voltage outputs are capable of 15 A/leg at 150°C with 35 ns recovery and price out at $3.00 to $3.80, 100-up.

The R710/11/12/14XPT fast-recovery types offer similar performance up to 400 V with 100 ns maximum recovery and have a $2.00 to $2.95 range.

Broad selection...exceptional capability...high technology...low cost. Motorola TO-218.

Check ☐ B for information.

Fast, bipolar power fits high-frequency like I - II - III.

Eighty percent of power switching applications remain within the realm of bipolar power — under 100 KHz.

Motorola-originated Switchmode™ now offers the fastest devices around — typically 50 ns — with second-to-none ruggedness — at prices only the world's leading discrete source could offer.

The 2N6833-37 Switchmode III series incorporates RBSOA capability that runs out to 460 V at 10 A and 850 V at 2 A with reverse bias of 5 V.

That's state-of-the-art.

This combination of high speed and large RBSOA derives from a proprietary process that uses narrow emitter strips, high emitter periphery-to-area ratio and hollow emitter structuring.

The geometry reduces stored charge and current density under the emitter fingers minimizing hot spots during turn off which results in large RBSOA.

Better efficiency and reliability result. And switching inductive loads at high frequency results in low switching losses — which translate to lower operating temperatures and, of course, longer, more reliable operating life of the circuit.

Prices for the 450 V series (850 V_{CEV}) compare favorably with units of lesser performance and specing. Switchmode I, II and III families are 100° C characterized on Designers™ data sheets for real-world performance and no dark corners.

Check ☐ C for information.

Device	Typ @ 100°C IC (A)	Typ @ 100°C t_f (ns)	Package*	100-999 Price
2N6833	5.0	100	TO-220	$2.10
2N6834	5.0	100	TO-204AA	2.20
2N6835	8.0	80	TO-204AA	3.65
2N6836	15	50	TO-204AA	6.30
2N6837	20	50	TO-204AE	8.50

*Note: TO-204 package was formerly TO-3.

Unbeatable & available

New MECL10KH™ parts, same old advantages.

Like 1 nanosecond propagation delay.
Two times improvement in speed-power product.
Lower ASP and cost per gate.
Less board space for equivalent functionality.
Higher reliability and one third less system cost.

You probably knew all that, but, in case you didn't, we'll send you documented proof MECL10KH offers huge cost and space savings over any other comparable in the industry.

Including these state-of-the-art additions to the most efficient, highest-performance logic line around:

Fastest industry DRAM

The 64-bit MC10H145 offers an address access time of 3 ns typical and 6 ns max., substantially boosting performances of your SSI/MSI functions. It's organized as a 16 x 4 memory array and has rise and fall times of 0.7 ns (min.) and 2.5 ns (max.) for both address and chip-select signals to the output.

Applications include a scratch pad for ECL processors, cache memory between ECL processors and slower memory and, naturally, any storage system requiring high-speed access time.

$10.65, 100-up ceramic, $9.25 plastic.

25 Ω bus transceivers

Primarily intended for bus interfacing, the MC10H330/332 units drive 25 Ω lines and provide useful logic functions.

The MC10H330 is a quad bus driver/receiver with 2-to-1 output multiplexers. The '332 is a quad bus driver/receiver with 4-to-1 output mux and the '334 is a dual bus driver/receiver with transmit and receiver latches.

The receivers furnish 200 mV of hysterisis on their bus inputs to ensure proper operation on noisy buses. When low, the outputs appear as high impedance to the bus and thus eliminate discontinuties in characteristic bus impedance. They also provide small capacitances to minimize bus loading.

100-ups range from $6.79, plastic, to $13.02, ceramic.

Single power supply translater

You use only the +5 V or the −5.2 V power supply in ECL-to-TTL level translation with the MC10H350.

You can cut your power use in half plus save board layout and space with this quad device.

In ceramic, 100-999, the price is $10.65, plastic $9.25.

All 10KH devices are compatible with 10K logic and memories, the MC10800 bit-slice family, the MC10900 LSI group and MACROCELL™ arrays.

Since 10KH operates in forced-air environments, its uncompensated, 0-75° C range better matches constraints of these well-established lines than compensated 100K. And, it's less noisy because of reduced edge speeds and provides 20 mV better noise margin than 100K.

Delivery? Short and sweet.

Check ☐ D for information.

Powertap™ Schottky replaces four DO-5s.

Quick, convenient and easy, one new Power Tap Schottky replaces four expensive, DO-5 devices in high-frequency, high-temperature switching.

The centertapped, dual-diode structure equals two 60 A diodes per leg and is capable of a 240 A rating at 125°C case with 175°C maximum junction temperatures. Reverse voltages are 35 and 45 V for the MBR20035CT/45CT units.

You can use the center mounting hole to assure excellent heat-sink interface and nut drivers for mounting and terminal attachment to avoid the variability in solder operations.

The transfer molded epoxy is interlocked to the copper base and virtually impervious to moisture.

The die are sandwiched between molybdenum discs for θ_{JC} matching which shrugs off rapid temperature cycling without degradation. Results are documented on samples undergoing 5,500 cycles of power cycling with maximum DC repeatedly passing through each device for 1 to 2 minutes... at T_J of 100°C.

Motorola's Schottky guardring eliminates dv/dt problems and affords zener-like protection against transients. All Motorola Schottkys are 100% tested for reverse energy capability and reverse-trace-tested for anomalies.

You can parallel PowerTaps for higher output and still not pay any more than you would for discrete units. The MBR20035CT is $18.70, 100-up and the −45CT $22.

Soon-to-be-available are 120 and 300 A versions plus a 120 A, 50 to 200 V Ultrafast type.

Check ☐ E for information.

The cost-effective pair for streamlined 8-bit development: EXORset™ 110 and HDS-200.

Now there's a new EXORset™ development system to host the HDS-200 Microprocessor Hardware/Software Development Station. It's the most cost-effective approach to complete hardware and software development for Motorola's extensive M6804, M6805, and M146805 families of CMOS and HMOS single-chip microcomputers.

The new EXORset 110 has all the familiar features that have made earlier EXORset models the ideal low-cost desktop development system and host/terminal for the HDS-200. It also has a larger, easier-to-read 12-inch CRT.

EXORset 110 is based on the high-performance MC6809 microprocessor, so it's powerful enough to support major development projects, yet its operation is simple enough for use even by novice system designers. It serves as an integration center for hardware/software development.

The HDS-200 does more than simply provide debugging tools. It helps you analyze microcomputer system performance.

The HDS-200 emulates your system in real time, providing a chip's-eye view of the action and assisting the integration of software into prototype system hardware. It keeps you in control at all times.

By plugging the HDS-200 into the MCU socket on the prototype hardware, it serves as a functional substitute for the processor chip, allowing efficient hardware testing in addition to software debugging. Monitoring the target system via its MCU during emulation allows you to see exactly what the MCU sees. You can halt activity and make program changes on the spot, at exactly the point where behavioral abnormalities occur.

The HDS-200 system consists of the control station and RS-232 interface to the EXORset 110, plus an emulator module for the specific MCU being used in the target system. There's an emulator module for each M6804, M6805 and M146805 MCU. Reconfiguring for another project is as simple as unplugging one emulator

module and connecting a different one.

Although EXORset is the least expensive host for the HDS-200, the EXORciser,® EXORmacs,® and the new VME/10™ development systems are equally effective hosts.

And remember, you have the capability with the HDS-200 Development Station to immediately halt, restart or redirect target system operation at will as the need arises. You are always in total control. Your system will be bug free and ready for market faster.

EXORset, EXORciser, VME/10 and EXORmacs are trademarks of Motorola, Inc.

Check ☐ F for information.

Fast ECL RAM Hits 15 ns, max.

Motorola's MCM10415 and 10415A are recently introduced 1024 x 1-bit RAMs for high-speed scratch-pad, cache, control and buffer memory applications. The 15 ns max. access time of the A version and 20 ns speed of the standard version make them excellent upgrades from the MCM10146, as well as for application in new designs.

Their speed is achieved by use of Motorola's advanced MOSAIC technology, which features oxide isolation, 2-layer metal, and implanted transistors. Alpha particle protection is provided by a combination of cell design and package materials.

Data is stored or selected by means of a 10-bit address which is decoded on the chip. The chip is designed with a separate data-in line, a non-inverting output and an active-low chip select. The MCM10415 and MCM10415A are surprisingly low priced for their performance level, making them terrific values. Ceramic dual-in-line units are $10.35 in 100-999 quantities for the 15 ns MCM10415A, and the 20 ns MCM10415 is just $5.35.

Check ☐ G for information.

Control AC easily with optically-isolated Triac drivers.

You can interface sensitive logic or MPU with Triac-controlled 110 V or 220 V AC directly, easily. Just hook up with one of our 18 different optically isolated Triac drivers...most complete line in the industry.

Both zero- and non-zero-crossing types are available.

And, if you're designing from very low input levels, our MOC3000 series contains devices offering maximum trigger current levels down to 5 mA—sensitive to the low-power needs of many of today's CMOS circuits.

Just 5 to 30 mA to the LEDs in these units latches on the detector. And, when off, they block 250 or 400 V in either direction, depending on type. When on, they conduct up to 100 mA continuous with less than 3 V drop—more than enough to trigger almost any power Triac.

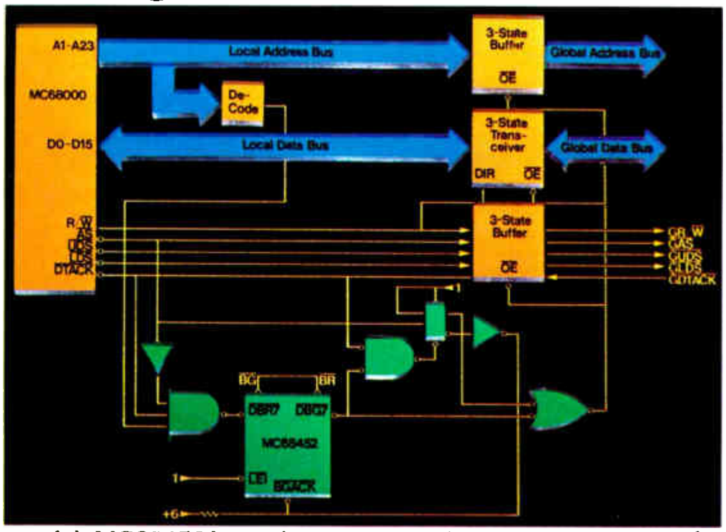
All 18 provide 7,500 V isolation of drive circuitry from noisy power lines—a standard. All are UL-recognized. And all 400 V devices are available with German VDE approval for use in a wide variety of European applications.

Zero-crossing functions as an active snubber network typically increasing dv/dt immunity to 100 V/μs.

Low price, high-volume and the assurance that top quality and the latest technology are built into each one make these Motorola optocouplers the easiest choice for coupling into any AC design. And the most obvious because they're from the leader.

Check ☐ H for information.

Multiplex multiple MPU buses onto a common global bus, fast and effectively.



Motorola's MC68452 bus arbitration module is a bipolar asynchronous bus controller that allows the fastest and best possible interface in multiplexing local microprocessor buses onto a common global bus.

It allows the local buses to share memory and I/O devices, and to communicate easily and efficiently with each other. The bus arbitration module (BAM) performs arbitration for as many as eight users of a global bus, and can be cascaded indefinitely to any number of required users. This allows implementation of systems requiring more than one bus master using only one chip per bus, where previous circuits required one chip per bus master.

Designers using Motorola's VERSAbus™ or VME systems in particular should find the MC68452 a good building block for generation of more computing power per board.

The BAM supports cycle-by-cycle or block-mode arbitration equally, and implements fixed physical priority. Arbitration time is less than 52 ns max. for eight users of a 68000 bus.

The MC68452 is available in both ceramic and plastic dual in-line 28-pin packages. Pricing for 100-499 units is $25.00 in ceramic.

Check ☐ L for information.

Have computer/game, will oscillate.

Just when everyone's doing PCs and games, along comes a low-cost, low-power voltage- (or crystal-) controlled master oscillator that's just right for those kind of applications.

The SN74LS724.

Now you can replace those overpriced and overboard-sized 16-pin dual oscillators with one single, 8-pin unit. And generate sound IF, a colorburst reference and/or an MPU clock in the bargain. Plus, the edge rates are slow compared to standard LS so EMI interference is cut dramatically.

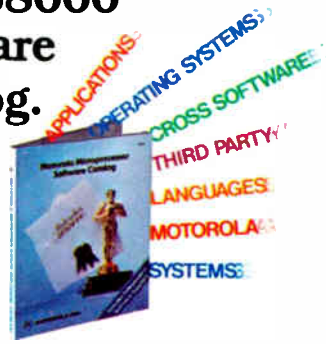
With an external capacitor across pins 1 and 8, the output frequency can be varied over a 3.5 to 1 range by adjusting the control voltage input (V_{in}) from 1 to 4.5 V.

And it uses just 45 mW maximum — bringing home the most basic reason to use state-of-the-art LS in new designs and further proof we're leading in the commitment to save you energy for them through technology.

74LS724 — right-part, right-time, right-price.

Check ☐ N for information.

New 68000 software catalog.



Although the Spring issue of Motorola's 1983 microprocessor software catalog contains software for the earlier 8-bit MPUs, the bulk of its 300-plus pages are devoted to the mass of software developed by Motorola and Independent Software Vendors (ISVs) for the M68000 Family processors.

As the popularity of the MC68000 spread, software houses and users joined in. Now there's Cross Software, Applications Software, Systems Software, Languages and Operating Systems — including UNIX™ derivatives and look-alikes.

Motorola was one of the first microprocessor manufactures selected to jointly develop a UNIX™ System V product with Western Electric. And, the scheduled August availability of our System V/68, derived from UNIX System V, M68000 version, should make it the first System V product delivered by a microprocessor house.

Although the catalog had to go to press before System V/68 could be included, future editions will include it. As it stands, the catalog is still an excellent guide to the variety of M68000 software that increases almost daily.

One other point should be considered about software for the MC68000. The nature of the 8/16/32-bit compatibility of the M68000 Family means that software you buy or write for the MC68000 today, migrates with virtually no modification to all the other processors of the family.

The Microprocessor Software Catalog costs $1.75, which may be the best money you'll ever spend on software information. Send your check or money order to Motorola Inc., Literature Distribution Center, P.O. Box 20912, Phoenix, AZ 85036 and ask for it.

UNIX™ is a trademark of Bell Laboratories.

Orchestrated memory support harmonizes with DRAMs, MPUs.

You can buy low-performance memory support parts that play together...or high-performance ones that don't.

In either case, you probably lack the flexibility, control and economy inherent in Motorola's state-of-the-art product.

This Bipolar chip set, consisting of the memory controller (MC74F2968), two timing controllers (MC74F2969/2970), the EDAC unit (MC74F2960) and the EDAC bus buffers (MC74F2961/62), can be used with any DRAM up to 256K x 2. They directly drive large memory arrays containing up to 88 DRAMs—anyone's DRAMs—without additional buffers.

They are the complete, precise solution to memory control.

By selecting the devices required for your application and possibly adding a minimum amount of logic glue, you realize:

- EDAC (Error Detection And Correction)
- Error scrubbing (sniffing) during refresh
- MC68010 bus retry support
- Byte operation support
- Synchronous or asynchronous arbitration
- Burst or distributed refresh with hidden refresh performed when the processor accesses other devices
- Adaptability to support nibble, page, ripple or static column access

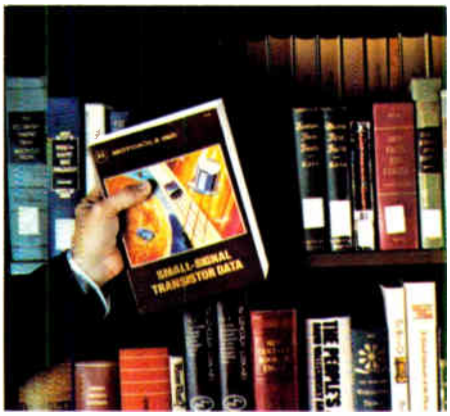
The unique architecture, generic processor interface and derivation of system timing from up to 10 timing tap inputs give this set the capability to operate with most available MPUs, too. And, of course, all of today's high-performance dynamic memory.

The DMC and MTC are fabricated using the Motorola-originated oxide-isolated MOSAIC technology with TTL-compatible I/O levels.

All units are jointly being developed with AMD with sample quantities on the 2968, 2969 and 2970 expected in 4Q and production in early 1984. 2960 samples are expected in 3Q of this year.

Check ☐ J for information.

If you have room for only one small signal transistor data book, this is it.



It has room for everything.

Without a doubt the most comprehensive publication of its kind, it presents technical data on all you need to know about small signal devices...from the industry's number one source.

It includes bipolars and FETs available in metal can, plastic and microminiature packages, plus complete device specs and typical performance curves given on more than 1,750 individual data sheets grouped by family.

The plastic TO-92 section encompasses hundreds of devices running the gamut from general-purpose amplifiers and switches with a wide variety of characteristics to dedicated special-purpose devices for the most demanding applications.

Microminiature products (SOT-23 and SOT-89) include diverse components from Motorola's repertoire of reliability-proven semiconductor processes and geometries: bipolar, FET, switching, zener and varactor diode technologies. Standard and low-profile.

In metal can, GP switching, high-voltage, chopper, Darlington low-noise and RF amplifier units are detailed. The section includes the industry's largest selection of MIL-S-19500-processed units too, all the way from JAN to JANS.

And Motorola's multiple transistors have been implemented with discrete chips, proven most popular for all-around performance at low cost. Package options include plastic, ceramic DIPs, ceramic flat-pak and various metal can outlines.

FETs include DC to UHF switching and amplifying applications including new small signal TMOS™ devices. All in plastic and metal.

RF transistors and hybrid modules are characterized as low-noise amplifiers, oscillators, high-speed switches, Class A linear amps and Class C types. Packaging embraces plastic/ceramic stripline and various metal cans.

A quick comparison is presented in easy-to-use selector guides with separate sections on package dimensions and the mysteries of hi-rel processing and testing.

$6.25, plus 15% postage.

Check ☐ M

MC6804: VLE MCU=VLC

Translated, that means the new 8-bit MC6804P2 single-chip microcomputer is at the Very Low End of our broad MCU offerings and gives you a Very Low Cost. Put another way, its small die size permits a small price: an 8-bit MCU at 4-bit prices.

And, though we call it low end, in addition to the CPU it offers

32 bytes of RAM, memory-mapped I/O, 1024 bytes of user ROM plus 72 more for look-up tables, self-check, master reset and an on-chip clock generator. The 20 TTL and CMOS compatible bi-directional I/O lines include eight that are LED compatible as well.

It also has a software programmable timer prescaler, and this low-cost 8-bit MCU is pin compatible with the venerable MC6805P2, the MC68705 EPROM version and the forthcoming MC68HC04P2 high-speed CMOS MCU. It's the industry's first Very Low End MCU that is upward compatible with a cohesive 8-bit family.

Software features also are impressive. It's derived from the M6800 Family and resembles the M6805 HMOS Family. It has a byte-efficient instruction set, programs easily and has true bit manipulation. And more. Bit test and branch instruction, separate flags for interrupt and normal processing, conditional branches, versatile indirect registers and interrupt handling, and single instruction memory examine/change.

It offers nine powerful addressing modes, and numerous user-selectable optional functions are available. Full system development hardware and software support is in place. The MC6804P2 is the right answer for the user who wants an economical MCU that packs the proven capabilities of an M6800-based instruction set.

If you are a high-volume user, please contact your local sales office or distributor for information on the low prices. Minimum order on this one is 10,000 pieces.

Check ☐ P for information.

High-performance MC6801 single-chip microcomputer gets enhanced capabilities.

Motorola is introducing two new variations on the long-established high-performance MC6801 single chip microcomputer.

The MC6801U4 doubles the amount of ROM from 2K bytes to 4K, and also doubles the functions of the 16-bit timer from three to six. The MC6803U4 is a ROMless version of the MC6801U4.

The expandability feature of the MC6801 is retained, so that the MCUs can function alone and self contained or can be expanded to a 64K byte addressable multi-chip system. In fact, all the features that have made the MC6801 one of the very high end 8-bit MCUs are retained as is unless they are enhanced.

To refresh your memory, the powerful CPU and ROM (or no ROM as the case may be) are joined on the chip by 29 I/O lines, 192 bytes of RAM of which 32 are

retainable during power down, clock, 16-bit timer and a serial communications interface that supports both NRZ and bi-phase serial data formats.

These enhanced MCUs are object code and source code compatible with the MC6800 and the MC6801, and have the same flexibility the MC6801 derives from its tremendously wide range of seven different operating modes.

There is no minimum order for the MC6803U4. Minimum quantity for the MC6801U4 is 1,000 units.

Check ☐ Q for information.

Coupon missing? Get information on any of the advertised products and systems by contacting your Motorola sales office or authorized Motorola distributor, or by writing Literature Distribution, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

To: Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036

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☐ D – MECL 10KH
☐ E – Power Tap Schottky
☐ F – Streamlined 8-Bit Development
☐ G – Fast ECL RAM
☐ H – Opto Triac Drivers
☐ J – Memory Support
☐ L – Bus Arbitration Module
☐ M – Remit $6.25 Per Copy Plus 15% Postage. No P.O. Under $50. Please
☐ N – Master Oscillator
☐ P – Very Low Cost MCU
☐ Q – Enhanced MC6801 MCU

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Washington newsletter

NOAA computer network combines weather data

The National Oceanographic and Atmospheric Administration is testing what it describes as a new computer system that could be the architectural prototype for the next generation of meteorological forecasting equipment used by the National Weather Service. NOAA scientists say that custom-designed interfaces connecting a network of Digital Equipment Corp. 11/780 and 11/750 computers and Ramtek 9400 displays helped to create **the first system that allows forecasters to retrieve, combine, and analyze weather data from all existing sources on a single screen.** Another big help is a new set of NOAA-built instruments that make routine short-range forecasts more dependable by giving almost continuous information on winds and humidity. The weather service may make the system the basis for its new equipment, which will be in place nationwide by 1988.

MCI starts massive facilities expansion

With $1 billion just raised on the capital market, MCI Communications Corp. is launching a major expansion campaign to spearhead its new drive into the telecommunications market, which it expects to double within five years, from $75 billion a year now to $150 billion. Major projects to augment the Washington, D. C., company's 20,000-mile microwave network call for the installation of 4,000 miles of 450-Mb/s fiber-optic cable, for the purchase of two 12-transponder satellites with a total capacity of 48,000 circuits, and for complete digitization of switching exchanges. **MCI is also test-marketing a digital pager, made by Japan's NEC Corp., that can receive and store up to four messages.** The company awaits Federal Communications Commission approval to introduce cellular mobile-phone service in 51 cities.

Telecom industry sees no threat to PO

Technological change will not displace conventional post office services, said telecommunications-industry representatives at hearings held in late July by the House subcommittee on postal service personnel and modernization. **New technology for managing information will continue to raise the productivity of mail operations** and strengthen the Postal Service's price and quality position *vis-à-vis* private competitors, spokesmen from American Telephone & Telegraph Co. and MCI Communications Corp. agreed. Nevertheless, the subcommittee is concerned that new services like electronic mail and videotex will make some post office functions obsolete. It plans to hear from academics and from representatives of the Postal Service and its employees before deciding whether legislative action is needed.

FCC seeks wider input on Integrated Services Digital Network

Concerned that a broad cross-section of U. S. interests is lacking representation in forums to develop global standards for the Integrated Services Digital Network, the Federal Communications Commission has issued a notice of inquiry urging all the relevant private players to speak up, lest ISDN become a *fait accompli* [*Electronics,* July 28, p. 49]. At issue is the fact that **virtually all U. S. contributions have thus far come from American Telephone & Telegraph Co.,** says Tony Rotkowski of the FCC's Office of Science and Technology Policy. The commission's objective is to induce industry to formulate positions that strike a balance among the interests of computer and telecommunications service providers, equipment manufacturers, and users as well as to maintain consistency between its own policies and those of ISDN, notes Rotkowski. The network would provide a common mode of interconnection for nearly all computer and telecommunications systems.

U. S. says Japan will promote imports of ICs . . .

During President Reagan's November visit to Japan, his hosts will unveil an import-promotion package designed to boost U. S. sales of semiconductors there, according to testimony by U. S. Trade Representative William Block before the Joint Economic Committee of Congress. Brock did not disclose details of the Japanese plan, though he did say that **an information-exchange agreement will permit the U. S. to monitor it.** Under the agreement, data on semiconductor trade between the two countries will be collected starting this September. American negotiators who worked on the package emphasize that the import-promotion measures will focus on removing the "psychological and cultural barriers to trade," such as the popular Japanese notion that imports are unpatriotic. One U. S. proposal calls for Japan's Ministry of International Trade and Industry to use its long-term development plans for targeted industries to specify the import levels it desires.

. . . as Galvin seeks stiffer dumping penalty

Robert W. Galvin, Motorola Inc.'s outspoken chairman, wants Washington to concentrate on actions to combat dumping in the U. S. Representing a group of technology manufacturers united in the Coalition for Trade Equity, Galvin urged the Joint Economic Committee to reform antidumping laws by "imposing import duties . . . **sufficient to eliminate injuries and neutralize the effect of foreign-government targeting."** Although the Schaumburg, Ill., company just got the Federal Trade Commission to slap current antidumping duties on U. S. importers of Japanese tone pagers, Galvin claims that the costs of filing a case greatly outweigh any possible relief.

Deregulate phones, World Bank urges the Third World

A new World Bank report asserts that the major stumbling block to expanded telecommunications in Third World countries—which have an average of 2.8 telephones per 100 persons compared with 83.7 per 100 in the West—is not money but **poor management and staffing by national telephone monopolies**. Citing the benefits of growing telecommunications competition in the U. S., the bank says that in many developing countries, deregulating the industry would generate more capital and introduce the dynamism, innovation, cost-consciousness, and management efficiency that are now lacking.

Modernization urged for U. S. C^3 systems

The U. S. military's command, control, and communications systems will lack survivability, timeliness, and reliability—the most important C^3 requirements—unless they are modernized extensively, says Brig. Gen. J. T. Stihl, the Strategic Air Command's deputy chief of staff for communications and electronics. Particularly troublesome, Stihl asserted in an address to C^3 experts early this month, is the way **the technology that jams and disrupts information systems has raced ahead of the technology that provides them.**

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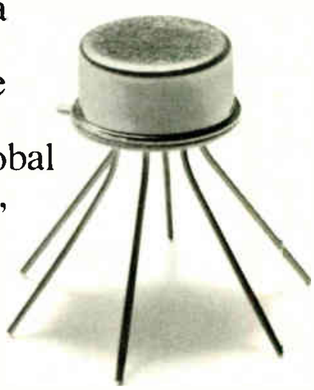

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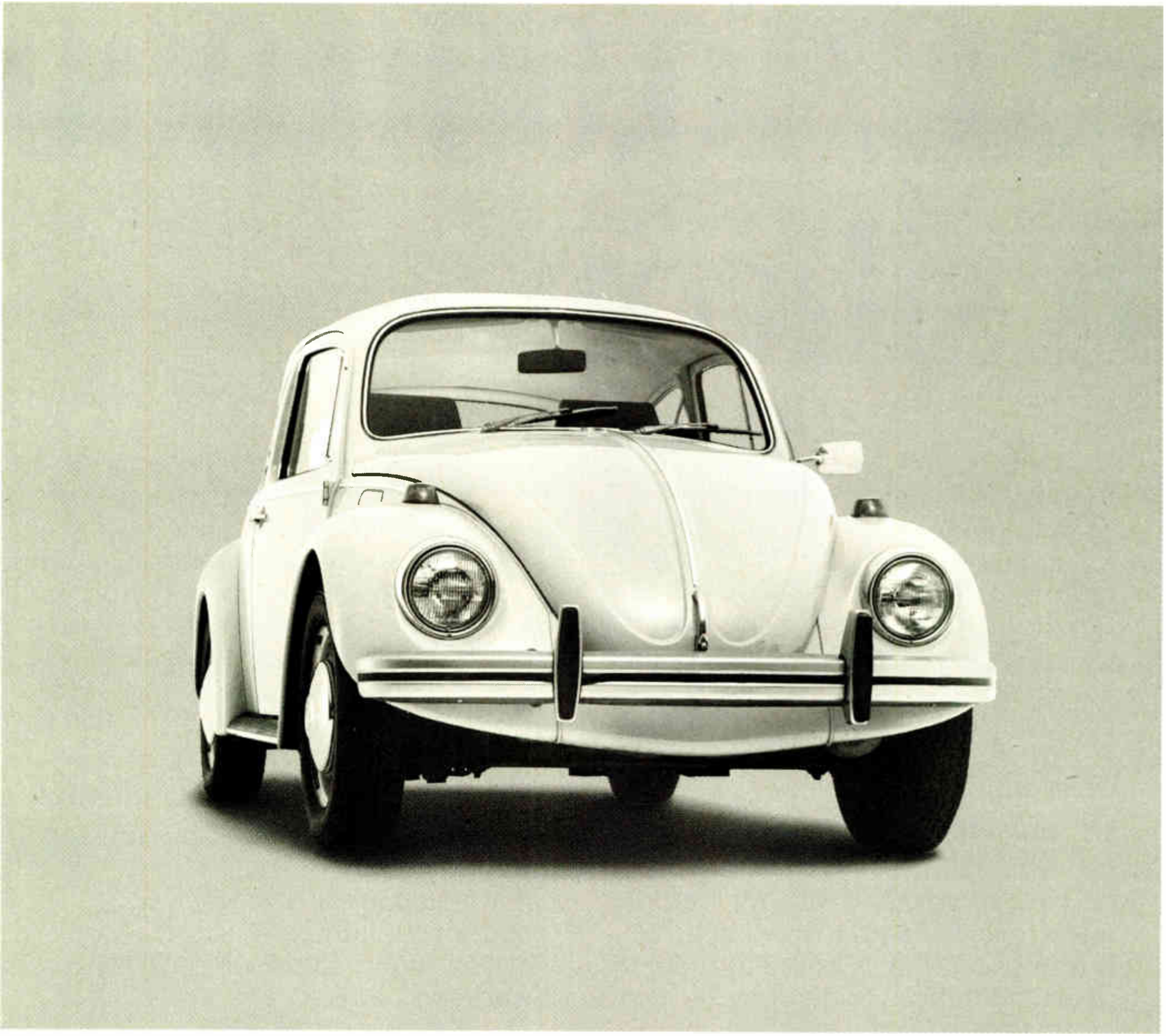

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Single-crystal epitaxy grows 3-d ICs

A method of building three-dimensional ICs by deposition of successive layers of single-crystal epitaxial material is being developed at the Research Center of Sanyo Electric Co., Hirakata, under the auspices of the Japanese government's project on future electron devices. **Insulation between the layers of silicon in which devices are fabricated is primarily two layers of single-crystal spinel,** a magnesium aluminum oxide, while source and drain contacts and gates are single-crystal silicon. On each device level, source and drain regions are diffused before a thin layer of spinel is deposited by vapor-phase epitaxy. Oxygen is diffused through the spinel to form an oxide layer underneath, and then silicon source and drain contacts are grown through windows in the insulation by ionized-cluster beam deposition. The gates are formed above the spinel at the same time. A thick layer of spinel caps the level and is followed by a layer of silicon that forms the substrate of the next level.

Sanyo claims to have working samples but will not divulge their characteristics. Most other firms are attempting to make 3-d ICs by depositing amorphous silicon on amorphous silicon dioxide and the recrystalizing the silicon.

Systolic arrays to double complexity

The complexity of bit-level systolic arrays—first developed at Britain's Royal Signals and Radar Research Establishment—could readily be doubled by the incorporation of fault-tolerant circuitry on chip, according to the research group in Malvern. These arrays attain extremely high performance by a parallel processing architecture in which hundreds of bit-serial processors are hardwired into a regular array. **RSRE's idea is to bypass faulty rows by associating simple transfer gates with each cell and switching them in by way of an on-chip multiplexer.** The technique could be employed to increase yield as in memory manufacture or, more likely, the greater potential yield could be traded for increased complexity by designing bigger systolic arrays. One likely candidate for this technique is a multibit convolver jointly developed by RSRE and General Electric Co. Ltd.'s Hirst Research Centre, Wembley. The chip, to be described at the VLSI '83 conference in Trondheim, Norway, later this month, operates on 8-bit serial data and words. The 16-stage cascadable circuit can be clocked at more than 20 MHz, giving a throughput in excess of 1 megaword/s.

IC promises to slash videotex decoder prices

Britain's Mullard Ltd. and West Germany's Valvo GmbH, both subsidiaries of the Netherlands' NV Philips Gloeilampenfabrieken, are collaborating on the development of a new large-scale integrated-circuit videotex decoder. The chip will support the new standard to be adopted by the West German Bundespost when it launches its videotex service in 1984. In trials, the Bundespost used British Prestel standards based on the level 1 standard of CEPT (the European conference for postal and telecommunications administrations). **For the full service, however, the Germans are moving to level 3, which has a greater color range and improved graphics.** A level 3 decoder based on standard ICs would cost an impractical $750, so the two Philips subsidiaries are now readying a 40-pin, n-MOS circuit to be available as samples in the spring of 1984, with volume production during the second half. Called Eurom (for European read-only memory), the IC will contain all the video controls for a TV set or video monitor and work with other Philips videotex chips.

Rubidium oscillators steady digital networks

Looking ahead to the time when international telecommunications will be standardized to the 2.048-Mb/s norm of the International Consultative Committee for Telegraphy and Telephony, engineers at the Centre National d'Etudes des Télécommunications in Lannion, Brittany, have developed **a highly stable 2.048-MHz reference frequency source to facilitate the synchronization of digital networks.** Based on two rubidium atomic oscillators that serve as phase and frequency slaves to a master cesium atomic oscillator, the source can perform for up to several years in constant operation. In addition, the system uses three independent power sources to guard against blackouts.

Preprocessing scheme forces separation of TV luminance, chrominance

In an attempt to improve the picture quality of French TV, the Société Française de la Télévision is developing a field-store–based Secam scheme that uses preprocessing at the studio end to permit precision decoding by viewers' equipment. In conventional Secam coding, the subcarriers of adjacent lines belonging to two consecutive fields of a frame carry the same information with opposite phase. Halving the sum of the composite signals of these two lines cancels the subcarriers and yields a full-bandwidth luminance, while halving the difference gives the chrominance signal. The snag is that a difference in these two lines modifies the phase relationship between subcarriers, and the luminance-chrominance separation becomes incorrect for the rest of the line, causing cross-color, cross-luminance, and excessive noise. **The scheme adjusts the information to correct values in both fields of a frame, resulting in a perfect separation of luminance and chrominance.** Though a field-store decoder is necessary to reap the benefits at the viewer's end, the system is compatible with existing equipment.

Addenda

The first wholly Australian-made optical-fiber cable used by the government-run telecommunications authority, Telecoms Australia, has been ordered from Amalgamated Wireless (Australasia) Ltd. for radio communications within Sydney. Amalgamated Wireless says it is able to manufacture optical cable—previously imported from Japan—**of equal quality to that made abroad, following its 11 years of research.** . . . Israel's Communications Ministry has called on Tadiran Electronics Industries Ltd., Givat Shmuel, and AEL Israel Ltd., Bnei Brak, to purchase technology from partners abroad for the construction of digital telephone exchanges worth $200 million. **The move is an attempt to speed up the modernization of the Israeli telephone system** following the collapse of a deal between Siemens Albis of Switzerland and AEL. . . . The 10 Japanese companies in the Video Home System video-cassette-recorder group have **formally announced adoption of the hi-fi VHS system for recording high-fidelity stereo sound** [*Electronics*, June 16, p. 82]. Matsushita, the developer of the system, already has a product on sale, while the other companies expect to have products in time for year-end sales. Meanwhile, in the Beta VCR group, Sony, NEC, Sanyo, and Toshiba have already started selling machines using the hi-fi system developed by Sony. . . . Britain's Sinclair Research Ltd. has come up with an inexpensive bulk data store 30 to 40 times faster than home cassette-recorder setups. **The $76 cassette-cartridge microdrive can load a 48-K-byte program in under 10 seconds.**

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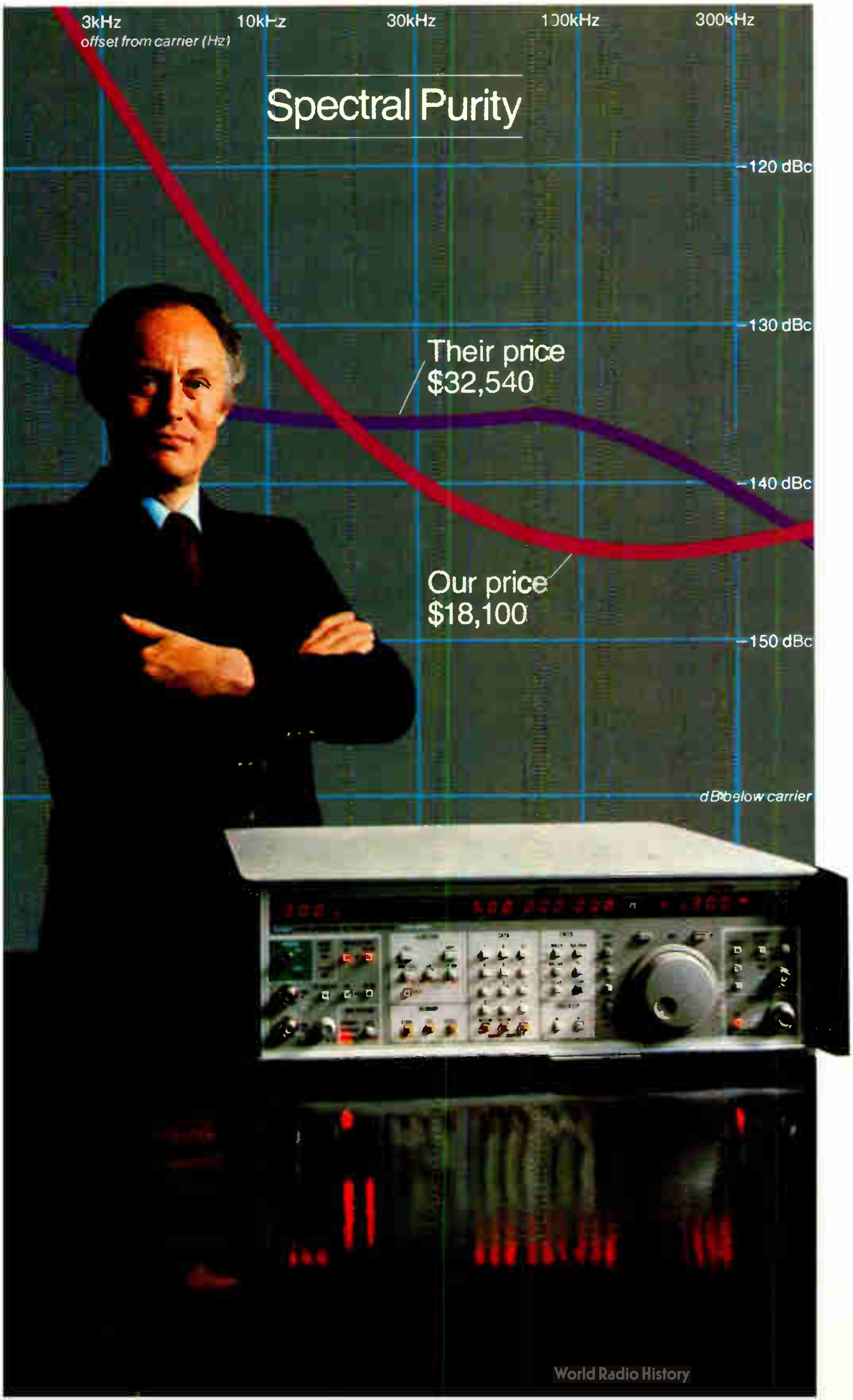

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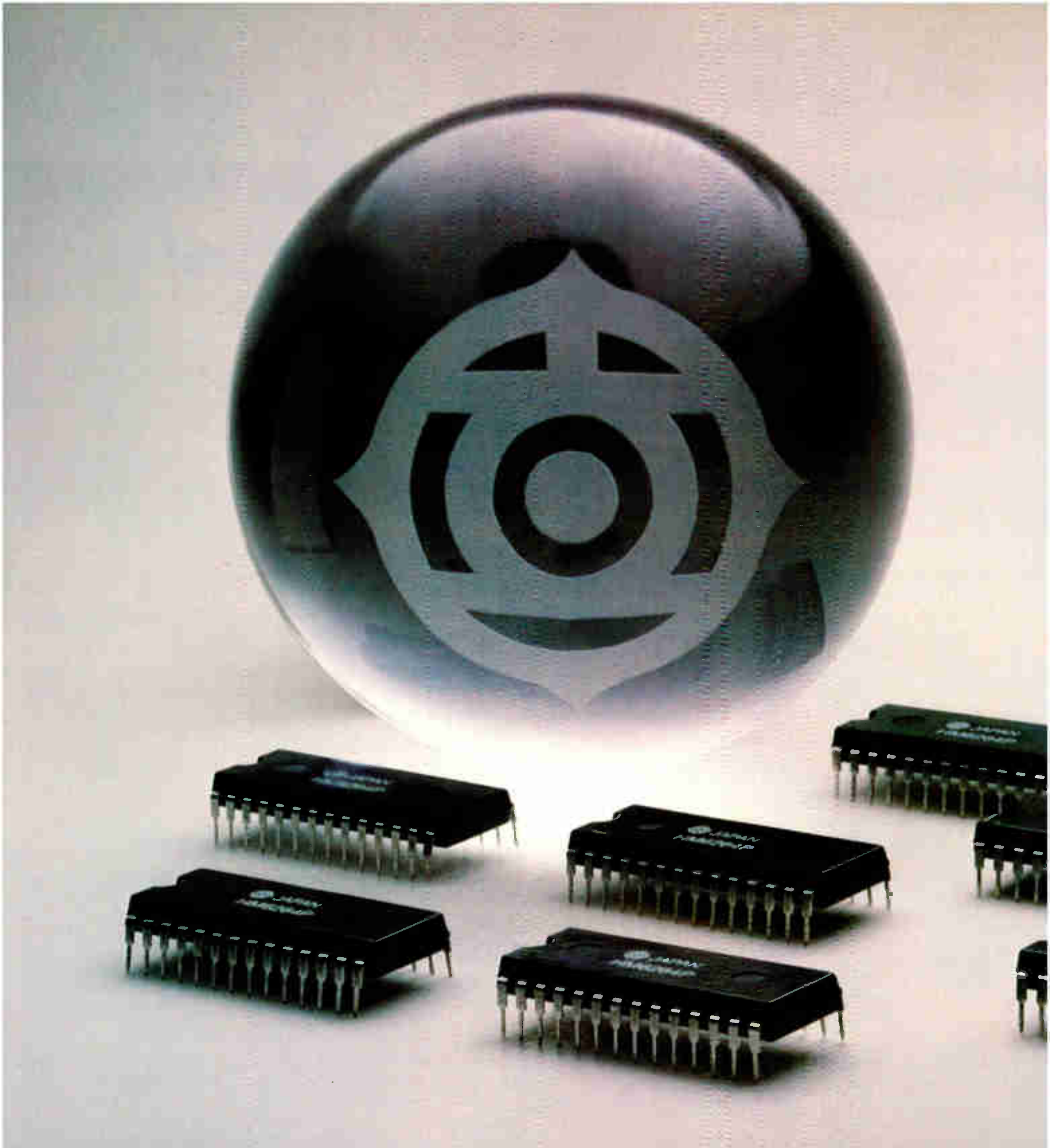

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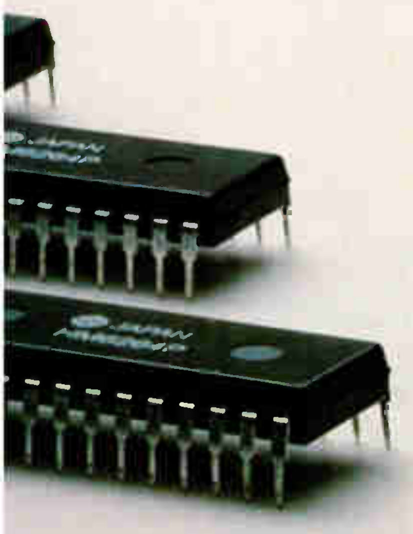

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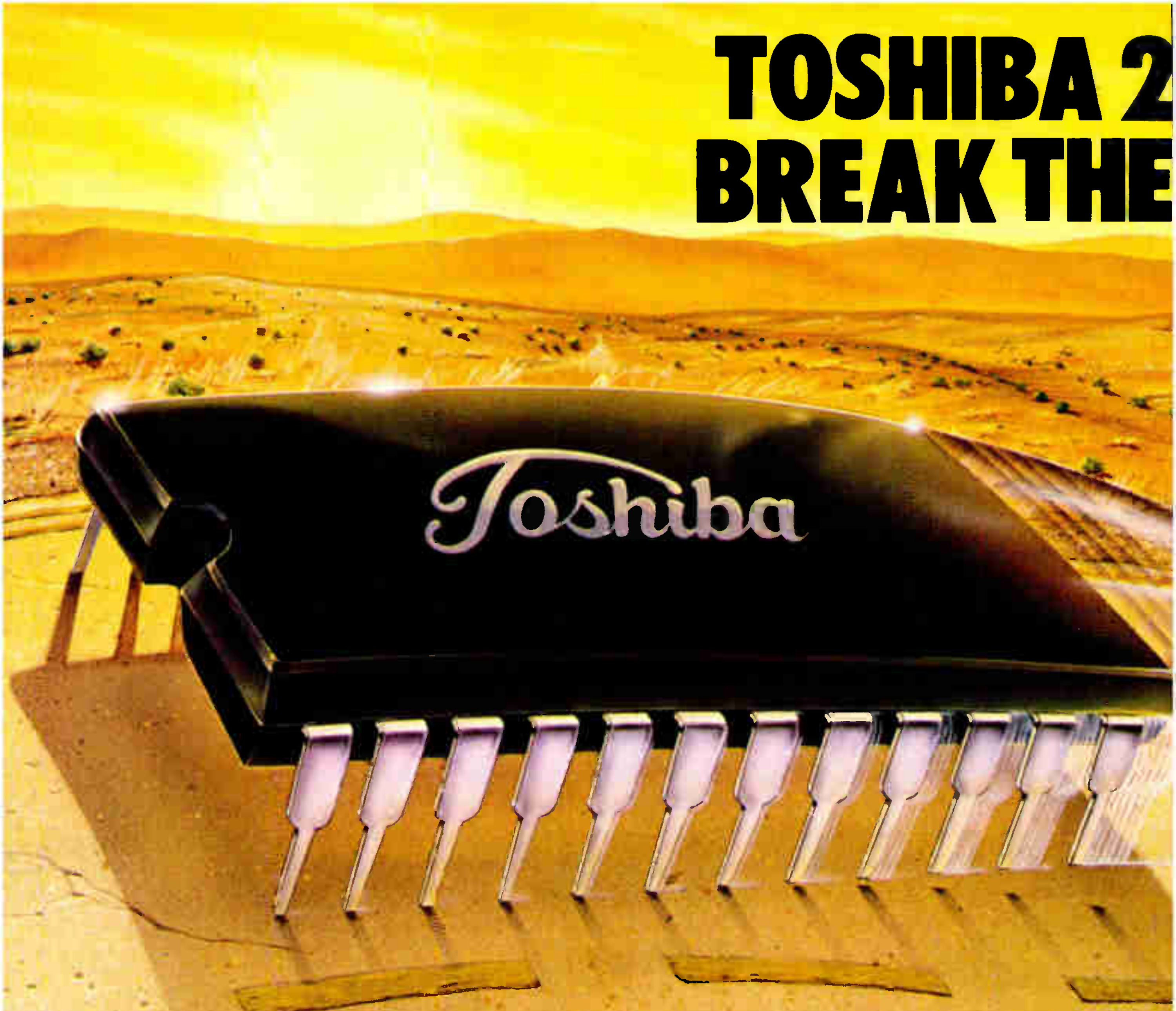

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*2016AP-12	NMOS	120ns	65mA	7mA
*2016AP-15	NMOS	150ns	65mA	7mA
**2018D-45	NMOS	45ns	120mA	20mA
**2018D-55	NMOS	55ns	120mA	20mA
5516P	CMOS	250ns	55mA	30μA
5516P-2	CMOS	200ns	55mA	30μA
5516PL	CMOS	250ns	55mA	1μA
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Circle 79 on reader service card

Image processor handles 256 pixels simultaneously

by Kevin Smith, Senior Editor

Using 2-μm C-MOS process, chip packs up to 140,000 transistors into an area just 6 millimeters square

Though it will be many decades before image-processing researchers can begin to match the massively parallel processing power of the human eye, very large-scale integrated-circuit technology is at least bringing nearer the more modest goal of practical and inexpensive industrial vision systems.

One such image-processing chip is now being developed at Brunel University, Uxbridge, near London, using 2-micrometer complementary-MOS technology to crowd as many as 140,000 transistors onto a single silicon chip 6 millimeters square. With a highly regular structure, reminiscent of a random-access memory, it is capable of processing 256 picture elements simultaneously in real time.

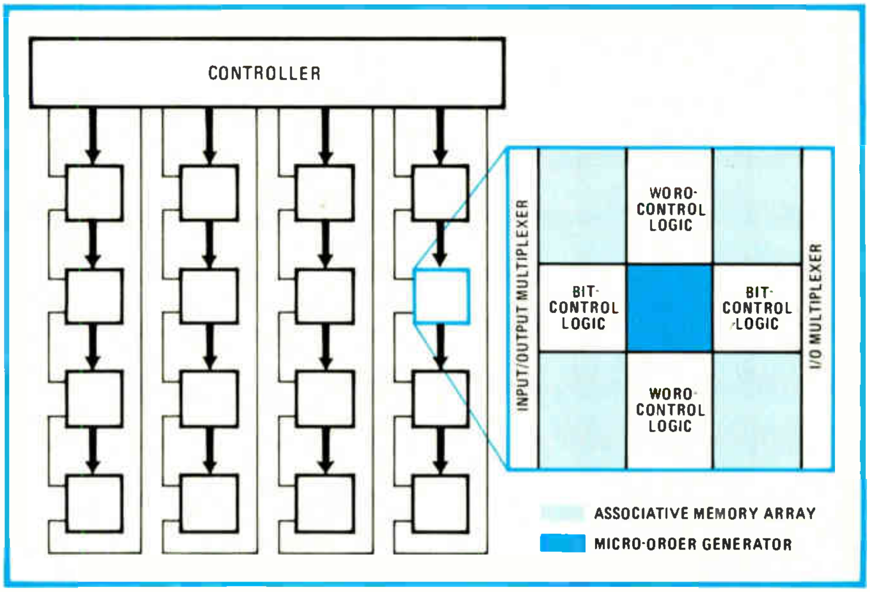
The chip is one of the most complex yet developed for image-processing tasks. Earlier designs, like the CLIP-4 developed at University College [*Electronics*, July 14, p. 75] or the Goodyear Massively Parallel Processor (MPP), pack eight pixel processors to a chip and have a 3,000- to 8,000-transistor complexity. General Electric Co. Ltd., at its Hirst Research Centre, Wembley, is completing development of a chip with 64 pixel processors of 50,000-transistor complexity, while Japan's Nippon Telegraph & Telephone Public Corp. has a 64-processor system of 81,000 transistors in the works.

Called Scape—for single-chip array-processing element—the Brunel image processor has been developed by Mike R. Lea, who will describe his work at the VLSI '83 conference to be held in Trondheim, Norway, later this month.

The idea behind Scape, says Lea, was to produce a highly integrated general-purpose chip capable of making image processing a practical proposition in many industrial applications. Lea uses a serial architecture so that the 24 pins of an inexpensive package can handle all communications. Also, Scape chips can be easily strung together to any length to obtain any desired performance—64 of them can easily be packed onto a single printed-circuit board to process an array of 128 by 128 pixels, some 16,000 pixels in total. Scape is also flexible enough to handle linear signal processing.

Inside the chip. Development of the Scape chip grew out of Lea's earlier work on intelligent memories. At first, his interest was in content-addressable memories; then he gradually began to combine these on a single chip with special-purpose microprocessor hardware. The result is a class of devices that he calls Micro-Apps (for associative parallel processors).

Aside from the chip, Lea's group is developing needed image-processing software and a control microcomputer using bit-slice technology. In the final setup, selected picture segments, called patches, can be loaded from a frame store, under control of a dedicated microcomput-



Mapping it out. Floor plan of the Scape image-processing array, which is capable of handling 256 pixels, reveals a highly regular structure reminiscent of static random-access memories. As a result, 120,000 to 140,000 transistors should fit on a 6-millimeter-square chip. Using serial architecture, the complementary-MOS chip will fit in an inexpensive 24-pin package.

er, into the Scape array.

Array chips are chained together and communicate serially with each other. However, the chain can be broken into smaller strings during loading.

The Scape chip itself includes an associative memory of 256 words, each 32 bits long, together with special-purpose logic for bit (column) and word (row) control. At the center of the chip is what is called the micro-order generator, which receives broadcast instructions from the microcomputer controlling the array and forwards them to the chip's row-control and column-control logic.

The Scape chip is thus a bit-serial example of single-instruction control of a multiple-data-stream computer system, like ICL's distributed array processor, the University College CLIP-4, and the GEC grid chips. Completing the Scape floor plan is the input/output multiplexer used to stream data on and off chip.

Most image-processing tasks, such as finding an edge, involve interactions between neighboring pixels. In the Scape chip, each pixel, variable up to 8 bits, is stored in a single memory location, while extra memory space can be allocated for storing intermediate results.

In operation, pixels selected by the associative-memory logic are acted on by the word-control logic. This bit-serial logic can execute microinstructions on the contents of its memory or can communicate with distant pixels over a data highway in the word-control logic block.

Communication with distant pixels is thus superior to that in other image-processing arrays, as these are usually hardwired to communicate with their eight nearest neighbors.

The layout of the chip is highly regular, says Lea, and hence is extremely efficient, comparing well with static RAMs. For example, the Scape chip usually works with pixels than can vary in length up to 8 bits, but to store intermediate results, more than one memory location can be allocated per pixel. This ability to program the array structure is what suits the Scape chip to linear signal-processing tasks.

France

Silicon assembler generates VLSI masks by using ultimate function as input

A team of French engineers has taken a significant step toward the realization of the ultimate computer-aided design tool for integrated circuits. The goal is a silicon compiler capable of generating masks for very large-scale ICs by using the circuit's desired ultimate function as input.

What the engineers at the Computer Architecture Research Group at the Laboratoire d'Informatique et de Mathématiques Appliquées de Grenoble have achieved is an assembler made of silicon that permits hierarchical design of functional IC cells according to basic interconnection structures. It has already been used to generate a 6,000-plus-transistor data-path computer circuit.

The name chosen for the assembler is Lubrick, for LUcie BRICK, Lucie being a French acronym for "university language for integrated circuits and teaching"—a geometric and graphic manipulation language similar to the American CIF language. "Brick" is an English analogue to the French word for cell.

The data-path circuit is intended for use in IMAG's familiar-instruction-set computer, which is parallel to the RISC reduced-instruction-set computer [*Electronics,* Nov. 17, 1982, p. 101, and p. 149 in this issue]. Realizing the FISC is one of the applications of the compiler project.

Designing circuits with Lubrick begins with a bottom-up approach where basic cells are designed first in order to solve topological and electrical problems at the most basic elementary level. After this, functional cells can be generated with more flexible topology and functionality.

A top-down approach, however, is also possible so that a designer compiling a high-level description need provide only functional characteristics, with a functional cell-generation program implementing the silicon. The overall method is based on the principle of solving topological problems first—good solutions must be achieved first at the level of basic cells, then at the level of functional cells, which must have flexible shapes.

Many features planned. When complete, the compiler will feature (in addition to Lubrick) tools like a floor-plan evaluation aid and a register-transfer language design for one-to-one correspondence with hardware components. There will also be an extractor that derives the structure of the data path and the control section from the behavior specification, a data-path generator, and a control-section generator.

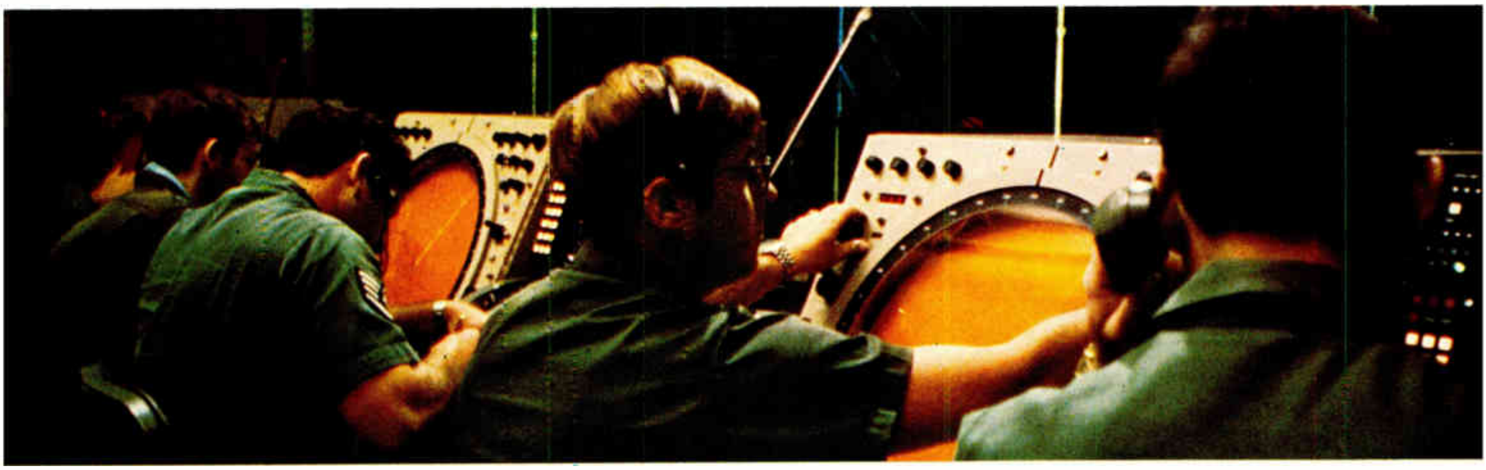
Jean-Pierre Schoellkopf, the IMAG engineer who will give a paper on the assembler at VLSI '83 in Trondheim, Norway, later this month, says that Lubrick revolves around the definition of chip hierarchy by a block-structured program, written in Pascal. In this program, the nesting of procedures reflects the chip hierarchy, and the content of the procedures describes how the internal cells are built until leaf cells are reached at the bottom of the tree. A leaf cell is any cell whose content or shape and input/output pins is known.

Beginning with these leaf cells, Lubrick generates cell positions and connectors, as well as building more complex cells by following the chip hierarchy. In designing the data-path chip for FISC, Schoellkopf and his colleagues chose a bit-slice structure based on Mead-Conway design rules.

The resulting data path for the 16-bit computer is exercised from data pads (connecting points) by way of two shift registers used to hold 105 commands and 17 flags. The mode pad allows the choice of either execution or test mode.

Other characteristics of the chip include seven address registers imple-

The strategic connection.



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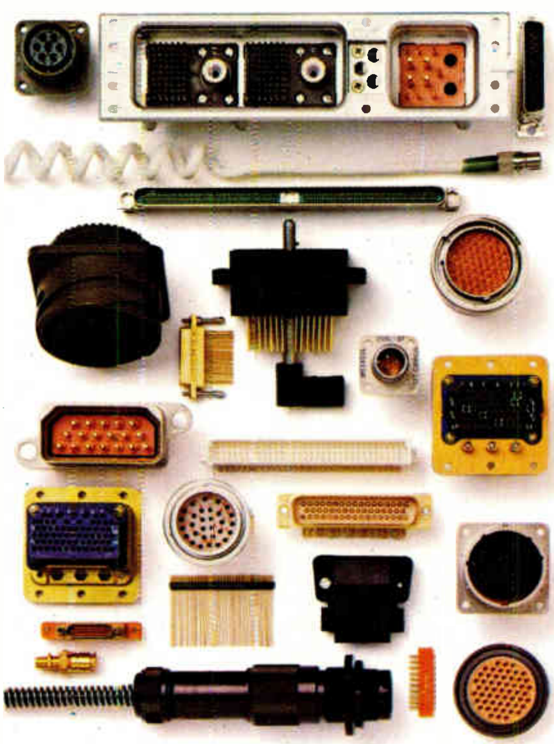

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mented in a double-port random-access memory with a 17-bit adder performing address calculations. Bidirectional communications are available between both address and data ports, which can work in real parallelism, except when a transfer is performed.

Standard organization. The data-computation module is organized in standard manner around two buses with a six-register dual-port RAM and a general-purpose arithmetic and logic unit connected to a shifter for serial multiplication and division. The ALU features two input latches and one output latch to permit accumulation.

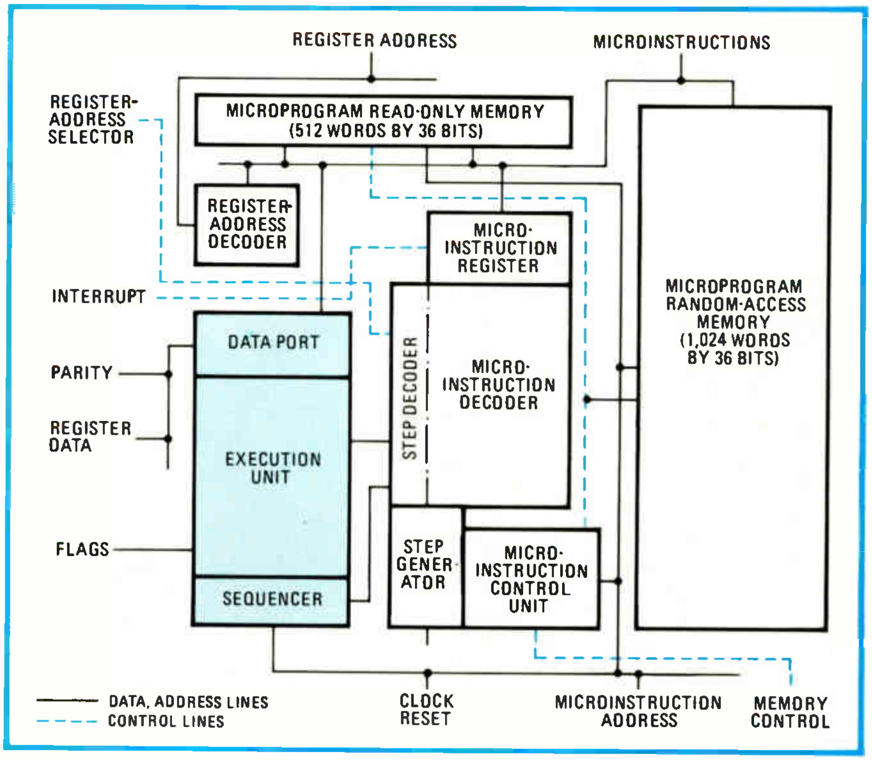
The 6,036-transistor data-path chip design took two engineers only four months, including the hand drawing of 23 basic leaf cells and their electrical simulation. The entire data path was generated by Lubrick programs hierarachically organized in the same way as the chip. IMAG is now designing a controller part for the chip, and future Lubrick applications related to FISC will include read-only-memory modules and first-in, first-out and last-in, first-out controllers. –**Robert T. Gallagher**

West Germany

Stack design speeds 16-bit tryout chip

An experimental 16-bit microprocessor from Siemens AG uses a novel register-stack structure to obtain fast execution times. The chip, which packs nearly a third of a million transistors on a 10.2-by-10.4-millimeter area, is the latest step in the West German company's very large-scale integrated-circuit research project aimed at developing new processor architectures, regularly structured designs, and improved computer-aided–design tools.

To obtain fast execution times, the Siemens designers hit upon a register-stack structure in which the stack consists of a static double pointer and of dual-port register cells. The double pointer simultaneously addresses two neighboring cells, one for reading and the other for writing.



Fast experiment. Siemens' 16-bit microprocessor uses a novel stack-register structure to obtain fast execution. It consists of a static double pointer and dual-port register cells, which simultaneously address two neighboring cells, one for reading and the other for writing.

This setup provides for fast internal access times—from 10 to 15 nanoseconds—because there is no shift operation prior to the read and write operations. That also results in low power consumption. The register stack uses only 75 milliwatts, or about a third that of a conventional stack of comparable 8-bit-deep, 16-bit-wide complexity.

Using 2-micrometer n-channel MOS technology with polycide gates and two metalization layers, the microprocessor operates at a clock frequency of 25 megahertz. Its instruction cycle time, typically 200 ns, can be varied between 120 and 360 ns. It is designed to control peripheral mass-storage devices, such as disk and tape memories, in data-processing equipment.

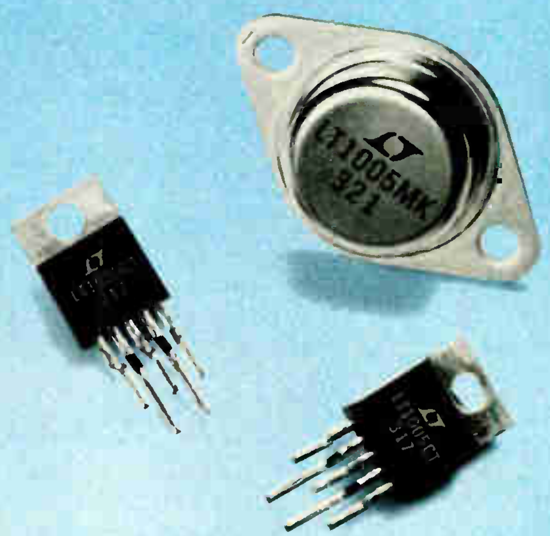
"Although an important objective, a high integration level was not our prime goal," says Michael Pomper, head of the design team at the firm's Munich-based research laboratories. Indeed, putting more than 300,000 transistors on a chip as large as 105 square mm is not really a feat, compared with what some U. S. companies have done.

Rather than a superchip, "we wanted to develop a test vehicle for trying out new design methods and layouts," Pomper says. In this effort, his team has perfected a device using not only a faster and less power-hungry register stack, but also a control circuit whose unusually high degree of regularity supports the use of automated design methods.

Three main parts. The processor, to be described at the Sept. 21–23 Ninth European Solid-State Circuits Conference in Lausanne, Switzerland, consists of three main parts (see figure): the data unit with its data port, execution circuitry, and sequencer; the control unit with the microinstruction register, instruction decoder, and step generator; and the memory unit, which contains a 1,024-by-36-bit random-access memory and a 512-by-36-bit microprogram read-only memory.

Also in the data block are a barrel

Carl Nelson's Answer



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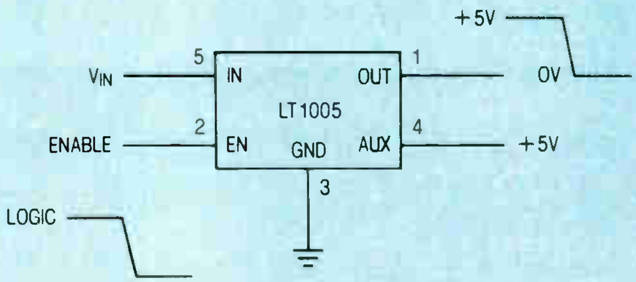
Functional Diagram



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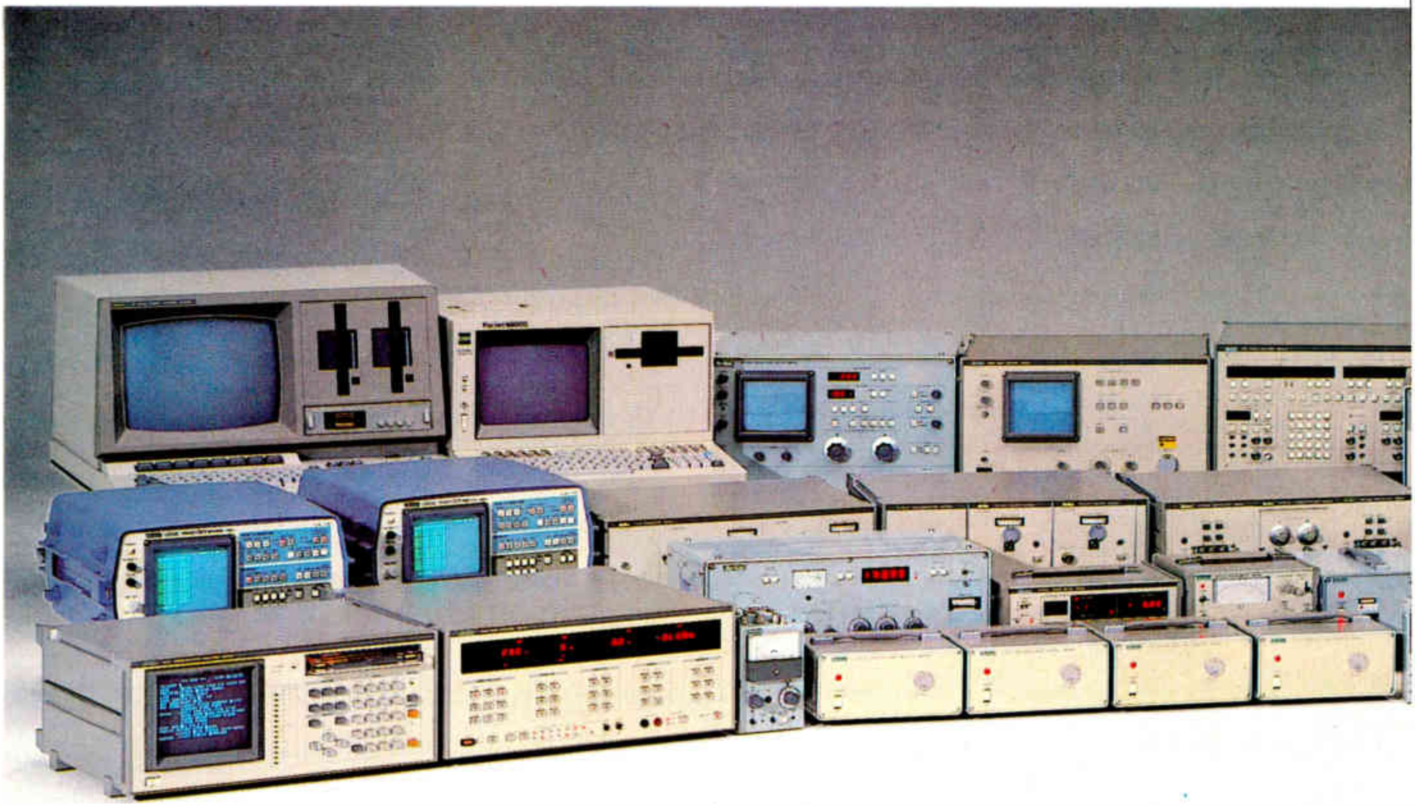

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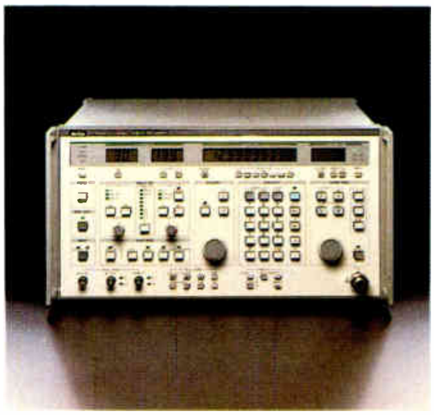

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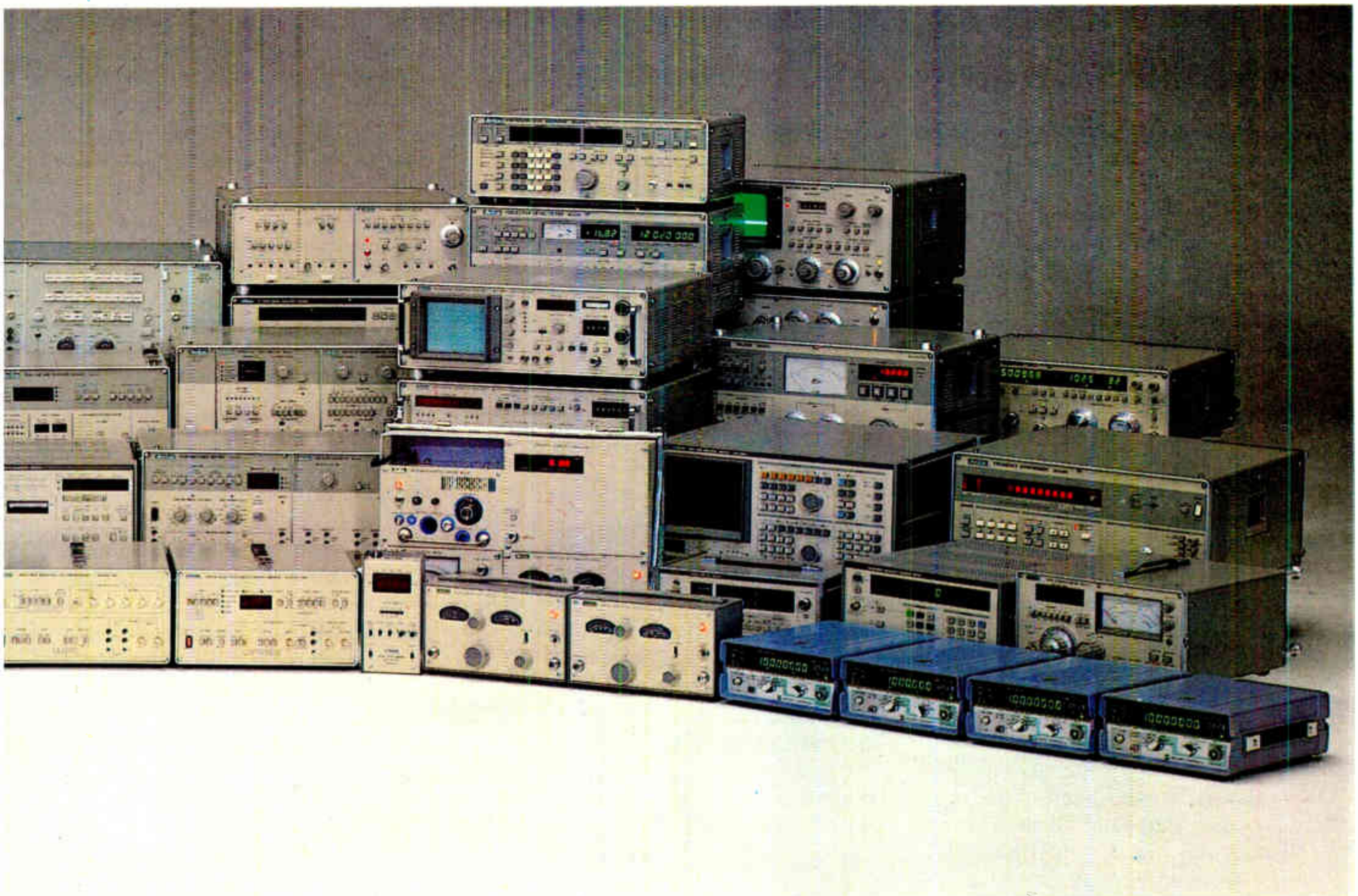

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shifter and a status block. The barrel shifter performs shift- and bit-manipulation instructions, and the status block generates and stores status and condition bits for jumps and subroutine calls.

Sequencer integrated. Characteristic of the control unit, the circuit's second major part, is its high degree of regularity. The first step toward achieving this was removing the sequencer from the controller and integrating it into the data unit. Second, the function of the literal supply for the data unit was shifted to the data port.

The remaining control circuitry is then implemented by extensive use of programmable logic arrays. For both the microinstruction- and step-decoder stages, PLAS with OR lines rather than OR planes are employed. This results in decoder slices that are each associated with just one function slice in the data unit—a layout scheme that makes for no control-line crossings and provides topographical benefits.

The advantage of this control-unit design concept comes to the fore during layout generation. All that is needed are a few hand-designed basic cells. Well-known programs for PLA generation, standard-cell placement, and routing can then be used.

Inside the controller. The controller's microinstruction decoder is based on a single PLA. To reduce the RC delay of the 5.5-mm-long input lines, the aluminum conductors are connected in parallel with the polycide gates. The step decoder, based on three PLAS, supplies the time-dependent control-line signals.

The step generator, which also consists of three PLAs, produces 17 internal time steps. To enhance processor performance, the timing has been made variable. Depending on the instruction type (for example, fetch instruction or fetch and store) and the location of the source and destination (on or off chip), the instruction cycle time can vary from three internal steps (120 ns) to nine steps (360 ns).

In the memory unit, a large RAM—with 1,024 by 36 bits, it occupies about 41 mm^2 of the chip area—has been chosen to store most of the characteristic data of the mass-storage device under control.

Often-used microprogram routines can also be stored in the RAM. In this case, the cycle time for a fetch and store instruction can be reduced from 200 ns (in the case of external memory access) to 160 ns (in the case of internal access). –**John Gosch**

Japan

Personal computers head for Europe

Four of Japan's leading personal-computer makers—Sord Computer Systems Inc., NEC Corp., Fujitsu Ltd., and Hitachi Ltd.—have revealed plans for what amounts to a selling blitz in Europe. They seem undeterred by the fact that their well-known weakness in providing software documentation makes the multilingual European market harder for them than the U. S.

"The language problem makes it difficult for Japanese firms to penetrate foreign personal-computer markets," says Sord spokesman Yoshiya Kitamura, "but we have built up a good distribution network in Europe, where the smaller market allows us to have better contact between dealer and customer. This closer communication allows up to overcome many of our documentation problems."

Sord has been producing personal computers at its own plant in Ireland since 1981, with annual sales of about $42 million. The company says it will start selling a new model, the M68, in both Europe and the U. S. this fall.

It predicts that the M68, which has software that will allow it to run either 8-bit or 16-bit application programs, will achieve worldwide sales of 100,000 units this year. It exports about 25% of its personal computers, and of those sales, about half will be in Europe. The M68 will be priced at about $3,000.

NEC, which estimates that 60,000 personal computers will be sold in Britain this year, projects a market growth of between 25% to 30% for 1984. The company is looking to get a good-sized hunk of this market by aggressive marketing and pricing.

It has contracted 40 dealers in the UK to sell its 16-bit, 128-K-byte APC series and expects to expand its dealerships to 100 by next March. The APC has been a great success in the U. S., selling over 6,500 units in the first eight months after its introduction last July, the firm says.

The computer, which goes for $3,300 in the U. S., will be priced at $3,023 in Britain. The Japanese firm says it plans to sell 1,600 units in Britain this year and 5,000 more by the end of next year.

Secondary market. Fujitsu, which began selling its 16-bit, 128-K Micro 165 in the U. S. earlier this year, will market the unit in both Britain and West Germany starting in October or November. The price will be about $4,000. "Our main market continues to be Japan," says a Fujitsu spokesman, noting that 1983 domestic personal-computer sales are expected to reach 1 million units.

Hitachi, which began shipping its personal-computer models to the U. S. last year, says that it will market its 16-bit, 256-K MB-16000 in Britain this fall. The price will be announced later this summer, but is expected to be about $3,000.

As well as the four newcomers to the continent, Sharp Corp., which has been selling its 8-bit, 64-K MZ-700 series and MZ-80B models in Europe for two years, says it will introduce a 16-bit, 128-K model, the PC-5000, in Japan this October, and will begin shipments by 1984 to the U. S. and Europe. The price in Japan will be $1,792, including a printer. The U. S. and European price is expected to be in the $2,000 to $3,000 range.

None of the Japanese companies has plans for production in Europe, except Sord, which has an Irish operation to which it is planning to add a research and development laboratory. A NEC spokesman, for example, says European production will not be economically feasible until the company's sales reach at least 10,000 units annually. –**Michael Berger**

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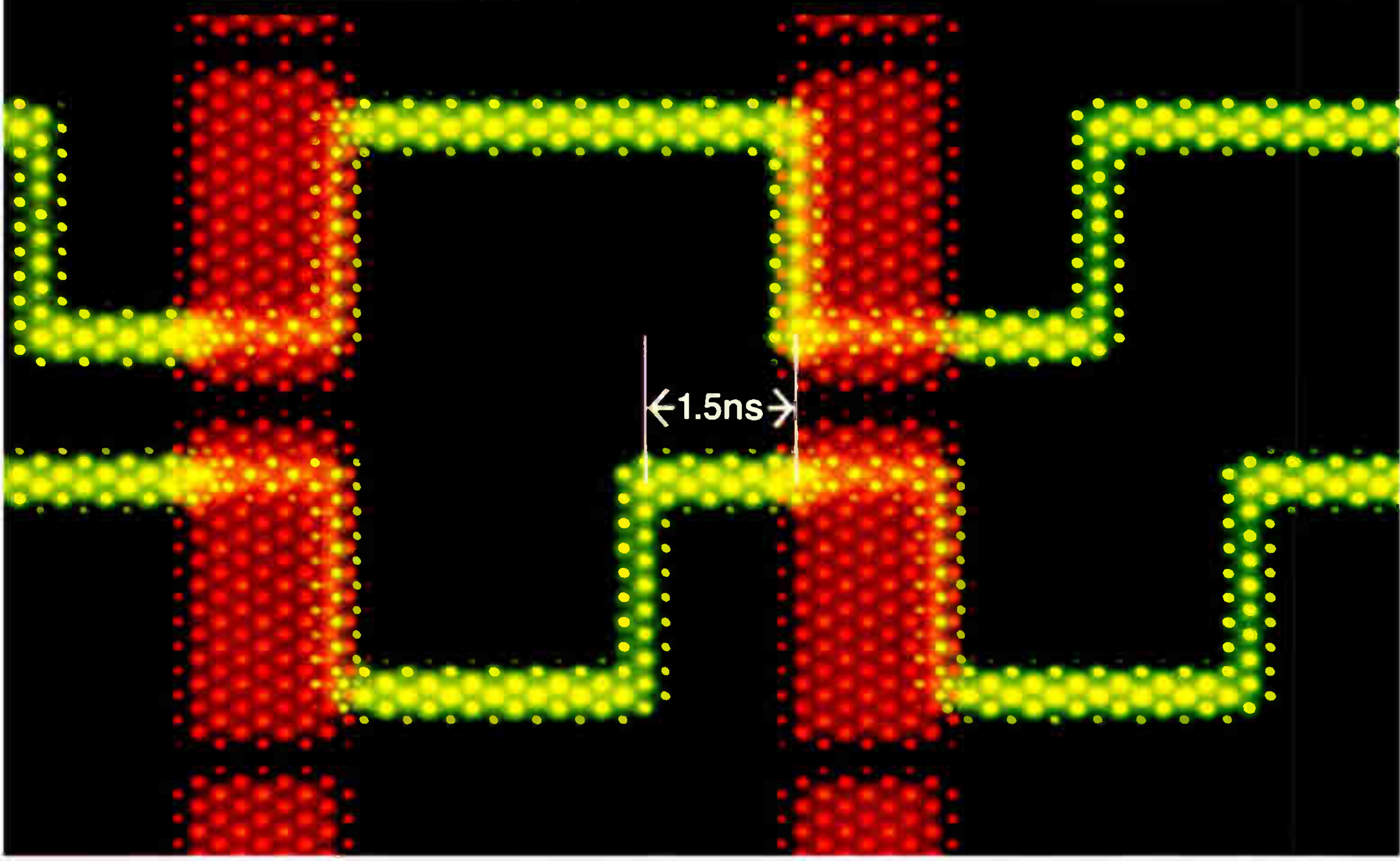

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Line-of-light links start to shine

Free-space optical communications needs no cable or Federal licensing and is cheap for links up to 10 kilometers long

by Roger J. Godin, Communications & Microwave Editor

Back in 1880, Alexander Graham Bell experimented with transmission of information through the air in the form of light. Now excitement is growing over what is known as free-space, or atmospheric, optical systems, though it has taken 100 years of technological advances to reach the point of takeoff.

Additional impetus comes from corporations wary of the rising prices of equipment charges, even as they fear imminent substantial rate increases in telephone line charges—especially for the ubiquitous 1.544-megabit-per-second DSX-1 and T1 carrier services. As a result, free-space optical transmission is viewed increasingly favorably.

The medium has several advantages to recommend it. Free-space systems need no fibers because light modulated with information propagates freely through the atmosphere on line-of-sight beams up to several kilometers long. What makes the systems practical now are advances in the technology of light sources and detectors, in turn stimulated largely by research on optical-fiber gear.

As fiber systems have grown, infrared light-emitting- and laser-diode transmitters and p-i-n and avalanche photodiode receivers have come rapidly down the learning curve. Using those elements, free-space systems are now even more cost-effective than fiber for short hops, such as between buildings.

Free-space technology is also being planned as a backup to fiber links in the new Teleport project in New York City [*Electronics*, July 14, p. 52]. There, optical transceivers on the World Trade Center in Manhattan will maintain communications with satellite earth stations on Staten Island in the event of a disruption in regular fiber channels.

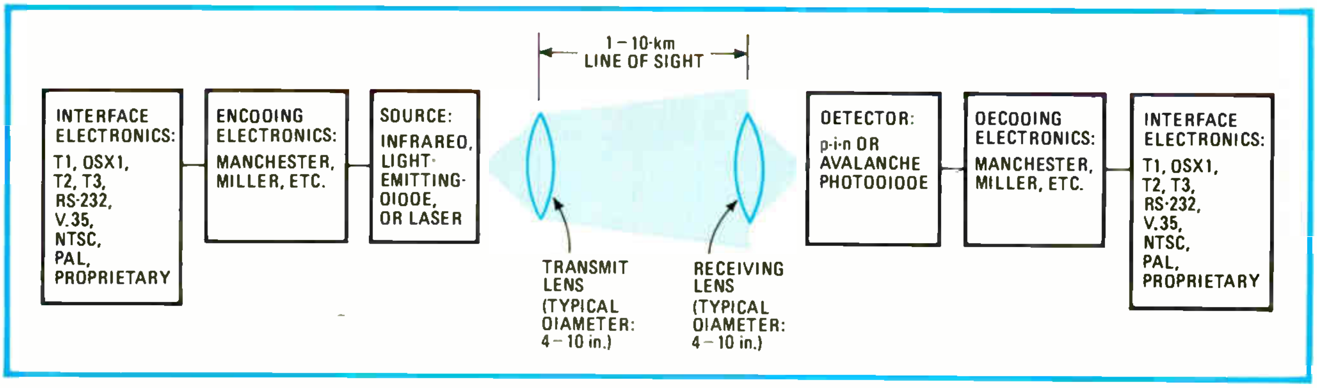
Weatherproof. By operating at near-infrared wavelengths, free-space links of about 1 mile are immune to most foul weather, such as snow and rain. The only possible interfering weather condition is extremely dense fog. However, according to surveys of climate records for all major regions in the U. S., independently conducted by Codenoll Technology Corp., Yonkers, N. Y., and Datapoint Corp., San Antonio, Texas, free-space atmospheric systems can meet the requirement of at least 99% availability anywhere in the country.

Still, the overriding attraction of free-space communications is the lack of wires. In large metropolitan areas where the frequency spectrum is saturated or in older manufacturing plants where existing wiring space is full, new wiring duct capacity, even high-capacity optical fiber, is expensive. Therefore, connecting buildings or departments with only light can save a great deal of money while also cutting installation time substantially.

Congestion may not be a problem in such places as between buildings in suburban office parks or satellites in orbit (see "Getting free-space systems into space," p. 92). Even there, the line-of-sight capability of free-space systems can save significant amounts of weight, mass, and power over alternative technologies such as microwave radio.

No license. Furthermore, free-space technology does not require Federal licensing, as do microwave radios. This consideration is impor-

Turning on the light. Typical free-space links need two simplex channels to maintain full-duplex communication. Telescope sights are used to align the system.



tant for users where the frequency spectrum is highly allocated.

In addition, multipath reflections off buildings or other obstructions that can cause distortions and reduce channel security are a consideration in the microwave region. In contrast, optical systems are unaffected by multipath reflections, says Joseph Svacek, manager of the electro-optic department at General Optronics Inc., an Edison, N. J., maker of laser-based free-space systems.

The market for free-space optical links is substantial. James McNabb, president of Light Communications Corp. of Norwalk, Conn., a supplier of turnkey communications systems that also makes free-space equipment, conservatively estimates that if 25% of the users of leased T1 lines buy the free-space alternative, the market in 1983 would be approximately $1 billion.

Besides use in data applications, replacement of phone lines represents a big business opportunity, and the office is one area free-space equipment makers hope to cash in on. They can provide the linking needed for a local network that joins work stations, word processors, and personal computers, where one of the biggest difficulties is in designing a flexible wiring plan.

Nearly all the companies offering free-space equipment have or plan systems that will interface directly with 1.544-Mb/s DSX-1 or T1 standards used to carry 24 channels of voice digitized at 64 kilobits/s, as well as data. Many also include a 2.048-Mb/s option for the European T1 standard.

Given voice capability, users that have private-branch exchanges with these standard interfaces can link several small exchanges in satellite buildings to a master exchange. They will be employing free-space links to create a completely private voice- and data-communications network.

Currently, most of the available free-space systems are using infrared LED sources that operate at 880- or 904-nanometer wavelengths and are matched with p-i-n diodes for receivers. Such a layout keeps the cost in the $10,000 range. Besides Light Communications, LED Systems Inc. of Boulder, Colo., has LED-based free-space equipment capable of handling various interfaces, including T1 and multiplexed RS-232-C lines.

Also, Fibronics International Inc. of Hyannis, Mass., a maker of turnkey data-communications systems, builds a proprietary 14-Mb/s LED-based free-space link to connect IBM 3274-type cluster controllers at one location to as many as 32 of the 3278-type terminals at another.

In addition to LED technology, there are also laser-diode-based systems, including a 10-mile 9,600-bit/s simplex link built by American Laser Systems Inc. of Goleta, Calif. That company also has an analog television free-space link based on LED sources aimed at temporary applications such as live-event coverage.

Using lasers. General Optronics also specializes in laser-based systems utilizing components from its other line of business, semiconductor lasers. General Optronics equipment can support 10 to 12 T1 channels, and can multiplex different information on different light wavelengths so that several data links can move on one light beam.

Also important from a maintenance perspective, says Svacek of General Optronics, is the fact that the system uses a fiber-optic cable from the laser to the transmit optics. This allows all the electronics to be rack-mounted in a closet anywhere in a building, rather than on a roof or in a window where the link optics must be placed. The drawback is that such laser-based systems are typically about four times as expensive as LED-based equipment.

Codenoll Technology takes the top-speed prize with a 150-Mb/s laser system called the Codebeam. It also takes advantage of its strengths in sources, detectors, and fiber-optic products by using a Manchester encoding scheme designed for very high-speed fiber data links. Further, it offers its transmitter and receiver units as components, as well as full free-space systems.

Japanese players. In Japan, NEC Corp., a leader in fiber-optic systems and therefore in a good position to use its sources and detectors in free-space systems, markets a single-channel video link similar to American Laser's. Likewise, Hitachi Ltd. is developing a free-space system for possible commercialization. A 1.2-km link connects computers in Hitachi's Central Research Laboratory to those at an engineering division at the Musashi Works.

A third Japanese company actively pursuing free-space technology is Fujitsu Ltd.'s Kawasaki Works, site of most of that company's fiber-optic research. At May's National Computer Conference, Fujitsu engineers described a free-space office communications system that can support multiple 19.2-kb/s terminals. □

Getting free-space systems into space

Scientists and engineers are conducting advanced experiments in two applications of free-space optical communications in conjunction with the National Aeronautics & Space Administration. One, aimed at improving crew communications, is designed for use in the space shuttle (see p. 48) and eventually in the space station. The other is for possible links connecting tracking and data-relay satellites with the space station—in space, line of sight can extend thousands of kilometers and there is no atmosphere to create a problem.

McDonnell Douglas Corp.'s Astronautics division in St. Louis, Communications Satellite Corp. in Washington, D. C., and the Massachusetts Institute of Technology's Lincoln Laboratory in Lexington, Mass., have done research on the use of heterodyne laser communications for such links. Recent advances in semiconductor lasers that have extended their lifetimes to approximately 10^8 hours mean that free-space optical links will probably replace the millimeter-wave (30- and 60-gigahertz) systems that were used to verify the concept. The main advantages of optical links over existing millimeter and microwave technologies are that receiver apertures and antennas can be almost an order of magnitude smaller; electronics can be lighter; and narrower free-space optical beams are harder to intercept. **–Roger J. Godin**

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Data communications

Low-cost modems will change the rules

The advent of an integrated 212A version will accelerate the trend to making communication links standard on personal computers

by Clifford Barney, San Francisco regional bureau

Dial-up low-speed modems, which can interconnect computers over the telephone system, are shrinking in size and price to the point where they soon will be standard offerings with most small-business systems, personal computers, and portable machines.

Integrated 300-baud full-duplex modems have already appeared in several desktop machines and in briefcase computers like the Gavilan and the Radio Shack model 100. But it will be the emergence of the integrated Bell 212A modem, functioning at either 300 or 1,200 baud, full duplex, that will open this segment of the communications market—and it also may change the way people use personal computers.

"We believe that the major growth market over the next five years will be in the Bell 212 area," says Mark Tyson, strategic marketing manager for Fairchild Camera & Instrument Corp.'s linear division, in Mountain View, Calif. "High-speed modems [9,600 baud and faster] are really for dedicated-line applications; the 300-baud modem is ideal from the reliability point of view, but poor because of its [low] speed.

"The 212A seems to be the perfect compromise. Having dual 300-baud and 1,200-baud capability makes it the ideal product to communicate with the largest number of systems." (See "Modem scorecard," right).

How many systems will there be? Kim Maxwell, vice president for business development of modem maker Racal-Vadic Inc., of Sunnyvale, Calif., figures that by 1986 half of the then installed base of some 10 million personal computers will have modem capability, about 80% being integrated units. At present, he says, low-speed modems account for only about 350,000 units a year, most of them standalone units.

The driving force behind the upsurge in integrated-modem sales will be more sophisticated communications software, Maxwell says. "Someone will figure out how to do electronic mail, which is the primary application," he adds.

Software is crucial. Present mail systems generally require a central controller, which entails a heavy outlay for hardware and software. A mail system that used an automatic-dial and -answer capability, with software that filed incoming messages, would be able to bypass central mainframes and offer communication by electronic mail on the same level as present voice telephones.

It is the smaller size and lower price of the modem hardware that makes integration practical for the original-equipment manufacturer and system integrator. Cermetek Microelectronics Inc., for example, makes a complete intelligent 212A modem, with automatic-dial and -answer and self-diagnostic capability, that fits on an 8-square-inch board and uses only half of an expansion slot.

The module, containing a standard 8-bit microprocessor and some propietary modem circuits, is probably the smallest and least expensive completely functional 212A modem available. It is being built into the Grid Systems Corp.'s Compass portable, the Altos Computer Systems model 586 business computer, and the Texas Instruments Professional Computer. Volume prices now are in the mid-$200 range, according to the Sunnyvale, Calif., firm's marketing

Modem scorecard

Asynchronous modems of the type described in the accompanying article are primarily used for interactive communications in host computers, cathode-ray-tube terminals, word processors, and business and home computers. They can be employed over conventional phone lines but require that start and stop bits surround the data, with the result that only 80% of their capacity is used for data. Higher-speed synchronous modems require conditioned or private telephone lines, achieve synchronization by encoding a clock with the data, and are 100% efficient. The table compares modems of different speeds.

Baud rate	U.S. standard	European standard	Mode	Format
300	103	V.21	full-duplex	asynchronous
1,200	202	V.23	half-duplex	asynchronous
300/1,200	212A	V.22	full-duplex	asynchronous/synchronous
2,400	201	V.26	half-duplex	synchronous
2,400	none	V.22 bis	full-duplex	synchronous
4,800	208	V.27	half-duplex	synchronous
9,600	209	V.29	half-duplex	synchronous

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director, Stephen J. Durham. By 1984, the OEM price of a complete 212A modem will be $100, he says.

The shrinkage of the modem hardware is taking place in stages. Only a few years ago, users who wanted Bell 212A modems were leasing them from the phone company at $40 a month as bulky standalone units that cost $120 to install and required a special jack at an extra $60. By 1982, outside suppliers were chipping away at this market, and Novation Inc., of Chatsworth, Calif., introduced an auto-dial 212A modem that cost the buyer $695.

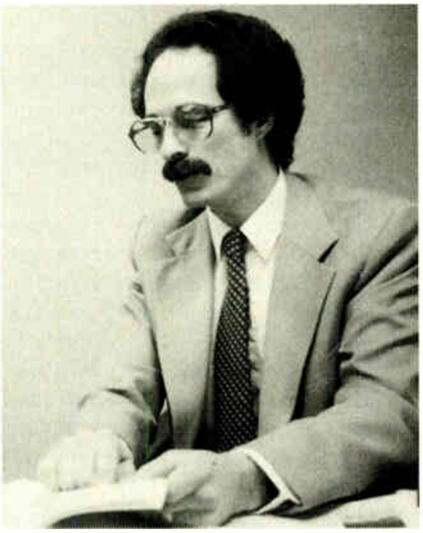
Dropping the cost. Novation thus became the first company to break the traditional price formula of "a dollar a baud" with its Autocat, an intelligent Bell 212A (1,200-baud, full-duplex) modem with auto-dial and -answer and self-testing. Since then, similar products in the same price range have been marketed by several other manufacturers, including Racal-Vadic, Chicago's U. S. Robotics Inc., and Hayes Microcomputer Products Inc. (a Norcross, Ga., firm that had been the first to offer a smart 300-baud modem). Hayes, Novation, and most other makers of standalone modems also offer board-level products that fit into a computer expansion-board slot.

However, the real breakthrough in modem technology has been in the development of chip-level modems, which can be integrated more fully into the processor [*Electronics*, Nov. 3, 1982, p. 111]. "An integrated modem becomes an address off the bus like any other peripheral," says Fairchild's Tyson. "It's just another place to squeeze data through."

Putting the modem inside not only saves on hardware, it also gives the system responsibility for the telephone interface. The system integrator can then build in sophisticated diagnostics and a variety of dial and answer modes. (It also makes life easier for the user, who does not have to worry about making the external connections and configuring the unit into the system.)

The Cermetek module, for instance, not only provides the traditional conversions between analog and digital and auto-dial and -answer capability, it also allows the host complete control over communications modes and testing. It has five dialing procedures and eight diagnostic test modes, and it monitors the call progress electronically.

There are as yet no single-chip Bell 212A modems on the market, or even in the sampling stage, but several makers are developing chip sets. One such company in Sunnyvale, Calif.—Exar Integrated Systems Inc.—offers a modem kit: three chips with 212A capability mounted on a printed-circuit board with all of the other components needed to provide modem functionality.



Price coming down. Cermetek's marketing director, Stephen J. Durham, believes that the OEM price of a 212A modem, now in the mid-$200 range, will be $100 by next year.

Key to the Exar set is a 1,200-baud chip volume-priced at $21.99. The difference in complexity between the 1,200-baud chip, which requires phase-shift keying, and the accompanying frequency-shift–keyed 300-baud chip can be seen in the relative prices: the latter costs only $2.81. A switched-capacitor filter at $18.43 completes the three-chip set; however, additional components bring the price of the kit up to $53.09.

Exar, a custom-chip maker, does not intend to get into the modem business *per se,* according to marketing manager John Sundell. Rather, it wants to provide a solution using very large-scale integrated circuitry with which systems houses can integrate the modem.

The board is intended as a product that the systems house can use while designing a system with a built-in modem. Within six months, Exar expects to integrate all of the functions on its board into a single three-chip set that will sell for less than $40.

More complex. The one-chip 212A modem is another matter. "Surviving the on-line environment is a significant challenge," Cermetek's Durham says. A single-chip modem, he adds, is really a microprocessor with a modem front end; the modem appears to the central processing unit as another controller that drives telephone lines instead of a conventional peripheral device.

"There are no standard protocols, and that alone will slow development," Durham says. Nevertheless, he expects to see a 212A modem on a chip, with a telephone interface, by 1985. "Anyone who plans to be a serious player in the rest of the decade will work on it," he maintains.

One of those players will be Motorola Inc.'s Semiconductor Products division, which is already a volume supplier to the 600-baud-and-below market. The Austin, Texas, division is now offering samples of a two-chip 212A set (a modem chip and a transmit-receive filter) and will market the product by next year.

Some doubt. Other chip sets are forthcoming from Texas Instruments, Racal-Vadic, Advanced Micro Devices, and American Microsystems. Each company is taking a different approach to integration and functionality—and Motorola, at least, is skeptical about the immediate size of the 212A market. "The 300-baud market is the one to go after right now," observes telecommunications marketing manager Al Mouton. "212A won't be a factor until 1985."

But even faster asynchronous modems, to 2,400 and 4,800 baud, are already being designed. For example, Tymnet, which operates a packet-switched network for Tymshare Corp., of Cupertino, Calif., will use one of these faster modems to support 2,400-baud asynchronous dial-up service beginning next month. Marketed by Concord Data Systems, of Lexington, Mass., the Tymnet modem conforms to the European V.22 standard. □

Companies

TI consumer units struggle to regroup

With a price war sending its computer operation stumbling to a $183 million loss in the second quarter, the company shuffles executives as it seeks to right itself

by J. Robert Lineback, Dallas bureau

Dallas-based Texas Instruments Inc., saddled with its first quarterly loss in three decades, nonetheless hopes to ride out the rough times facing its home-computer business. TI's overly aggressive computer operation has piled up a stunning second-quarter deficit of $183 million, which leaves the company as a whole $119.2 million in the red. (TI held back a $70 million tax benefit that would have cut the loss to $49 million.)

TI now warns that it could end the year with a significant loss if sagging consumer sales do not leap upward in this fall's Christmas buying season. The home-computer debacle has clearly been the most serious challenge of all TI's 10 years in the consumer business.

TI first entered the retail fray in 1972 with its Datamath calculator, priced at $142. The company's Consumer Group, which is based in Lubbock, Texas, has its roots in TI's effort to create the first hand-held electronic calculator during the late 1960s, as well as a tradition of firsts in chip technologies. The small-calculator division not only built its products with TI's semiconductor technology but also borrowed the celebrated learning-curve approach, driving prices lower as production volumes rose. The retail market for electronic goods has never been the same again—and neither, say critics, has TI.

For the sometimes hot, sometimes cold Consumer Group—which now, by outside estimates, accounts for some 15.5% of TI's total revenues—has not always been able to link price cuts to technology: touted in the mid-1970s as the digital-watch champion, TI was slow to adopt such emerging technologies as liquid-crystal displays and power-saving semiconductors. But marketing errors are most often blamed for TI's 1981 decision to quit the watch business. Now the Consumer Group has reached another critical crossroad, with the home computer.

At stake, top TI officials maintain, is the company's ability to participate in the huge future market for high-performance systems priced below $1,000. Without a home computer, they argue, TI would likely forfeit mass-distribution channels won by its now-ailing 99/4A home unit. "These broader considerations underlie our decision to continue participation in computers for the home market," explain chairman Mark Shepherd Jr. and president J. Fred Bucy. Both believe that new computing products, and others, too, will move

Change and failure. The Speak & Learn, for children 2 to 6, was the Speaking Reader when it was aimed at 4-to-8-year-olds, before TI found home computers were chewing up the learning-aid market. At right, TI's consumer operations were not helped by the TI-88 calculator, which fell victim to the pocket computer, or by the ill-fated 99/2 computer.

through those distribution channels.

TI's dilemma has touched off a fresh round in a longstanding industry debate. Can chip makers successfully compete in retail markets? Doubters cite the second-quarter loss as yet another argument against vertical integration of semiconductor firms. Others claim that TI relies too heavily on price-cutting in nearly all its consumer markets.

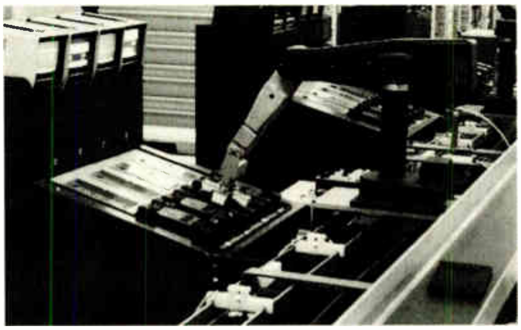
True grit. Still, TI is determined to turn its home-computer operation around, and that determination leaves a growing number of investors, market analysts, and employees uneasy. "The prime fear within TI is that the home computer is diverting attention and resources from other key businesses, which are finally showing some signs of life after years of little demand," complains a Semiconductor Group manager in TI's Dallas headquarters who declines to be identified.

TI's woes first became apparent in early June, after sales of its 99/4A console, peripherals, and software cartridges took a sudden nosedive. Immediately, TI jettisoned its bright 1983 forecast, presented before April's annual meeting, and slashed production schedules to lower inventories [*Electronics*, June 30, p. 50]. Assembly-line workers in Lubbock and in Abilene, Texas, went on mandatory vacations in July. More than 1,000 workers have been furloughed.

The corporate fathers have also shuffled upper management in hopes of quickly stamping out the losses in TI's Consumer Group and in its Austin, Texas–based Data Systems Group (which makes business computers). Consumer Group president William Turner—the architect of the ill-fated home-computer strategy—resigned in July. President Bucy has stepped in to watch over the troubled consumer and business-computing operations directly, for the moment turning over many of his corporate operating duties to chairman Shepherd, who now oversees such activities as semiconductors and military equipment. Executive vice president Jerry R. Junkins, responsible for both the Consumer Group and the Data Systems Group, is now assigned full-time to Lubbock.

Stewart Carrell, executive vice president for corporate development and marketing, resigned late last month, leaving what many analysts regard as a serious void in the corporate financial leadership. He had recently taken on extra duties in the sputtering Data Systems Group.

Value hunt. "In TI's case, the incentive for getting into the consumer computer business is an attempt to garner some of the added value that is perceived by taking a chip and turning it into a finished product," notes A. A. LaFountain III, vice president of research and electronics analysis for Shearson/American Express in New York. "But what happens, of course, is that when you are a semiconductor manufacturer you are selling to other businesses. When you are making consumer products you are dealing with a retail network, and that's a whole different situation."



Making money. TI-designed robot places calculators on automatic tester. TI has reduced calculator production costs with this and other automated systems.

LaFountain believes that "the problem, by and large, is a total inability to market." He claims that "the sum total of TI's marketing expertise seems to be in cutting prices, which is fine if you are beyond question the low-cost producer. But the simple fact of the matter—whether it was up against Oriental suppliers in calculators and digital watches or now, competing with Commodore in computers—is that TI has not been the low-cost producer."

Production costs are now widely recognized as one of the 99/4A's weak points. And the older 99/4 had more components and was less suitable for low-cost assembly techniques than its competitor: the more powerful model 64, introduced last year by archrival Commodore International Inc., of Norristown, Pa. This fall, TI hopes to introduce the higher-performance 99/8, which will take fuller advantage of large-scale chip integration.

The Consumer Group has trouble in other product areas, too. Hand-held learning aids—which TI's solid-state synthetic-speech technology helped pioneer in the late 1970s—continued to weaken in the second quarter. Some officials blame the drop on home computers, which now serve children in the 6-to-12 age bracket. Even so, such products and the low-cost speech technology behind them illustrate technology's power to create new consumer markets, says Kenneth G. Bosomworth, president of International Resource Development Inc., a Norwalk, Conn., market research firm.

"I think this learning-aid category—and the overall success of something like Speak & Spell—tends to suggest to us that there is a market [as yet unidentified] out there, perhaps in the $700-million-to-$800-million range, for just the right, bright ideas," estimates Bosomworth. He places the learning-aid segment at $80 million to $90 million.

Within the Consumer Group, only calculators—the oldest of TI's consumer activities—now show a steady profit, according to the quarterly report. The company, which currently offers about 25 different hand-held and desktop models, claims at least one third of the total market, as well as one of the world's broadest lines of calculators, priced from $7.95 to $150. Most of its low-end units are currently being assembled in Japan by subcontractors.

But the more powerful calculators are manufactured in Abilene on highly automated production lines that employ TI-made pick-and-place robots. Since the end of the 1970s, very little at the Abilene plant has been done by hand.

"The calculator business—and this is not just applicable to TI—has reached a stage of maturity. If you don't know how to make money in the business by now, you are probably out," notes Bill Meserve, consumer electronics analyst at Arthur D. Little Inc., of Cambridge, Mass.□

Consumer electronics

Home management systems speak up

Using microprocessors, speech synthesizers, and personal computers, a new species of electronic watchdog is guarding and controlling the home

by Erik L. Keller, Industrial & Consumer Editor

Everyone knows someone who has had to turn back from a vacation because the stove or the iron has been left on. But the new generation of microprocessor-controlled home-management systems has made turning electrical appliances off (or on) as easy as calling home. Better yet, these smart systems can do their own calling up—they can automatically phone, say, a neighbor or the police and describe certain conditions, like temperature, and whether someone or something has entered the house.

These systems can be installed easily by consumers and are more flexible than expensive hardwired alternatives. In case of power failure, they have battery backup, so they can continue to monitor. But their single most useful feature is their phone link with the outside world.

In fact, although back in 1979 BSR Ltd., of Blauvelt, N. Y., was the only player in the game with its X-10 system, over half a dozen companies now have products that exploit microprocessor intelligence. In addition, such manufacturing giants as General Electric, Sanyo, IBM, and Atari are positioning themselves to enter the market, and the recently announced MSX hardware and software standard from Microsoft [*Electronics*, June 30, p. 48] should help electronics manufacturers incorporate an inexpensive standard interface within entertainment units and appliances (see "What's in store for home management systems").

The X-10, which works through a home's power lines, has recently added Mattel Inc.'s Aquarius computer to its system. When the Aquarius machine is linked up to the house through its Microbot interface module, it creates a graphic representation of each room. This representation shows the location of all the appliances that are connected through X-10 wall-plug, -switch, or -receptacle modules and enables a person unfamiliar with computers to go through each room and program appliances and lights. After programming, the interface distributes and controls these commands throughout the dwelling. Peter Lesser, vice president of the X-10 division, adds that other computers will soon be able to connect with the X-10, which will soon have the ability to make phone

What's in store for home management systems

The current crop of home management systems is only an indication of where such controllers are headed, says Howard Anderson, managing director of the Yankee Group, a consulting firm in Boston. Besides home management, these systems will control home-entertainment systems and be linked with the telephone system, so that external monitoring will be possible. Some of the competitors that will introduce versions of this idea are Atari Inc., through its AtariTel division, and General Electric Co., through its Homenet network. IBM Corp. also has plans to utilize its Peanut home computer, which is slated to be introduced in October.

President Peter Wensberg says that AtariTel will offer a group of smart microprocessor-based telephones that will be used for communications, appliance, and home-environment control. In addition, the first products, which will be sold in early 1984 by the Sunnyvale, Calif., firm, will be followed by two other generations of products, which will integrate more sophisticated electronics and features, he says.

GE, from its Portsmouth, Va., operation, has a network configuration called Homenet, which it hopes will be the standard interface between a controller and appliances. Up to 256 stations may be linked using a carrier-sense multiple-access protocol. Jack Francis, a systems engineer for the video division, says that GE will start using the interface this fall at a factory cost of less than $2 a unit. (Other interfaces cost the consumer more than $30 and work only for particular systems.) Besides the interface, GE will also incorporate the brains of home-management systems in its television sets, which will be able to give instructions to appliances and monitor their status. GE has submitted Homenet to the IEEE for evaluation as a possible standard.

But GE may not be alone. Microsoft Inc., Bellevue, Wash., has introduced a hardware and software standard, MSX, for home computers that was adopted by 14 Japanese manufacturers, many of which make appliances and entertainment systems. Matsushita, whose lines include Panasonic, Technics, and Quasar, "has definite plans" to incorporate the needed interfaces in its products within a few years, says spokesman Ken Shimba. Sanyo, another company supporting the standard, has shown off a prototype of a home-management control center but does not plan to market it soon. **–E. L. K.**

calls when something goes wrong.

Though the X-10 can control appliances remotely and turn burglar alarms and other devices off and on, the system's ability to interact with users is limited. One technology easing this situation is speech synthesis. In fact, a recent study by Venture Development Corp., a consulting firm in Wellesley, Mass., indicates that over 80% of all consumers want speech capabilities incorporated into products.

With this in mind, Gulf & Western Industries Inc.'s Advanced Development and Engineering Center, in Swarthmore, Pa., has introduced Sensaphone [*Electronics*, June 16, p. 140], which incorporates National Semiconductor's Digitalker chip, an Intel 8050 microprocessor, and 32-K bytes of RAM. The unit can monitor three environmental conditions along with electricity, temperature, and sounds. Sensaphone works through either hardwire—coaxial cable or twisted pair—or wireless transmission, which has a range of 100 feet.

The unit's speech synthesizer has a vocabulary of 150 words and is preprogrammed. For instance, if the temperature should go too low, the machine would dial four telephone numbers until it finally got someone to listen to it say, "The temperature is too low," and give the telephone number of the home. If the person called should then ask what the temperature was, the unit would respond with the correct temperature, says Art Silverman, sales director of consumer products. The unit would then allow the recipient of the call to listen in on what was happening at the house.

Anova Electronics, a San Mateo, Calif., subsidiary of Dart & Kraft Co., offers a similar, albeit modular setup. The Anova master system consists of three modules: telephone, lighting-appliance control, and personal-property security. The configuration, which is controlled by Texas Instruments' TMS7040 microcomputer chip, can run up to 16 devices and answer the telephone.

The master system can give the status of all the controls for any time. It cannot be used to check the condition of the house from phone lines or to turn lights and appliances on and off, as can the BSR system. According to Ford Kanzler, a spokesman for Anova, these capabilities should soon be added to the system.

Baby Bell involved. With such a dependence on the telephone, it is no wonder that American Bell Consumer Products, a subsidiary of American Telephone & Telegraph Co., has entered the arena with its Emergency Call System. The system, using wireless transmitters, warns of a fire with an alarm and a speech-synthesized message of "fire, fire, fire." If not turned off within 30 seconds, the system calls either of two prerecorded numbers to say there is a fire at a certain address and phone number.

The unit's speech-synthesizer chip is programmed by the consumer, who simply punches his or her phone number and address into the call unit. As the information is entered, the device speaks the numbers or letters that have been punched.

According to spokesman Mike Tarpey, this system is the first of a line of products "designed to save people time and money." A similar product for medical emergencies will be introduced soon, he adds, along with other products that use the telephone to monitor or control appliances and other devices.

American Bell is not alone. Technicom International Inc., Darien, Conn., offers sophisticated phones that control appliances from telephone lines and call programmed numbers when emergencies occur.

The Smartcare phone dials four groups of four telephones when either police, firemen, doctors, or other help should be requested. The phone's speech-synthesizer chip tells the caller that help is requested and gives location by phone number. Through either wireless rf transmission, in the case of medical emergencies, or a hardwired sensor, for fire or burglar warnings, the set detects trouble and dials the appropriate group until someone answers.

Another Technicom device, Homefone, can also turn on or off appliances from the telephone. It is attached to an interface box that monitors appliances or lights through BSR-type modules. With the system, a person can phone home and, by using a security code, turn on or off electrical devices. □

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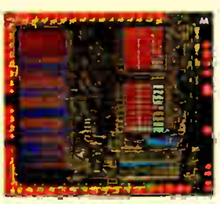

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LL5000	880-6000	3 micron double layer	2.5	YES	YES
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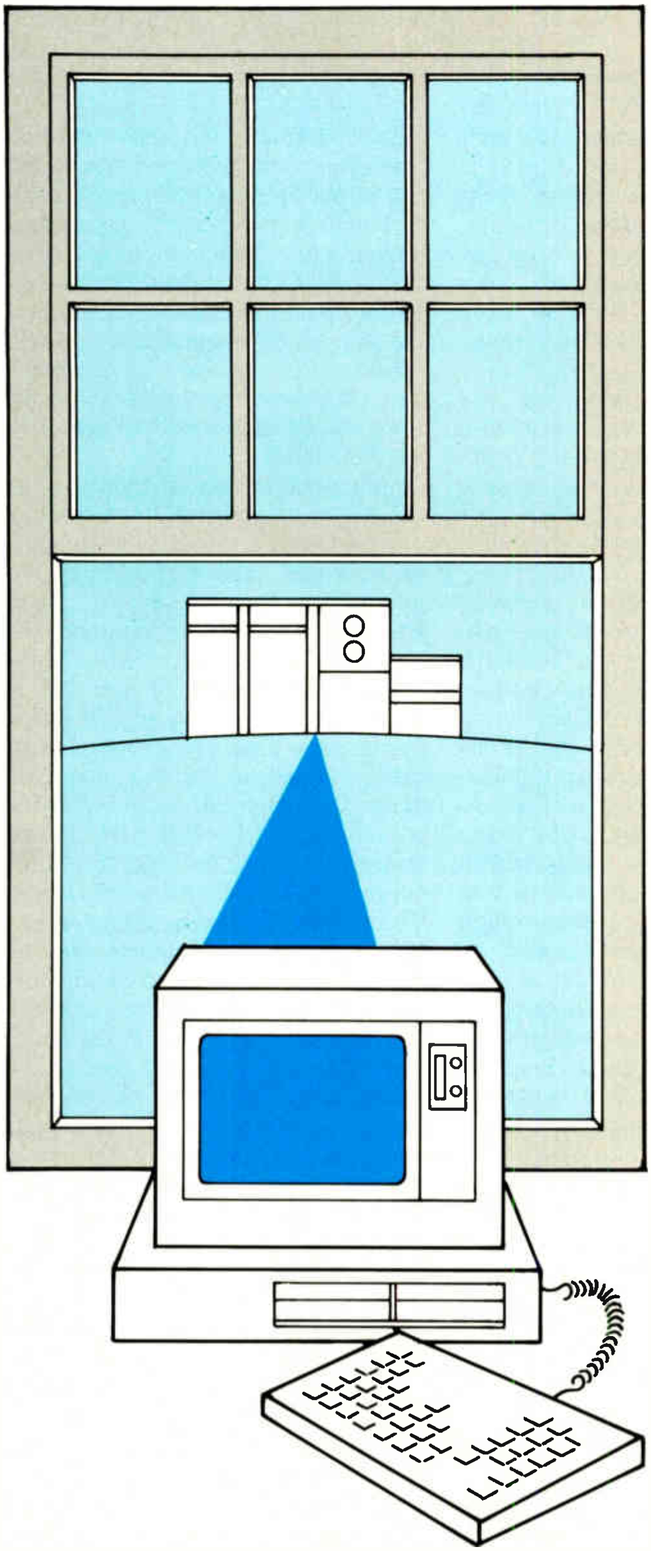
SPECIAL REPORT

Microcomputer and mainframe ally to bring offices new power



Communication between corporate personal computers and mainframes gives managers immediate access to data bases for decision making

by Harvey J. Hindin
Systems Integration Editor

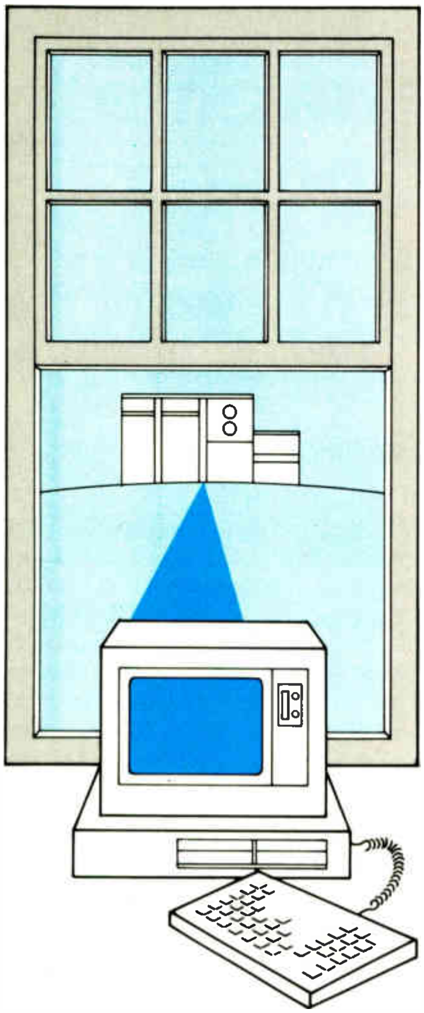
History records that the first message Alexander Graham Bell sent on the telephone, in 1876, was a call directing his assistant to come into the master's laboratory. The message was insignificant, yet the call itself marked the beginning of the electronic office. Today, events of similar import are taking place—but between machines, not people. What Mr. Bell was to Mr. Watson, the mainframe computer is to the personal computer. They too are now communicating, and in a quicker and more sophisticated way.

"Quick" and "sophisticated" are the watchwords of the dozen or so firms that in the last six months have introduced software to link personal computers and mainframes. In the next six months a dozen more plan to do the same. What spurs all of them on is a common recognition that access to the corporate data base is just as important to managers as is access to desk telephones.

The physical creation of two-way links between communicating machines is no trivial matter, but the required hardware is well within the state of the art. As for the software, however, it is not even clear what functions it should have. Indeed, software design is what distinguishes one new product from another.

These differences reflect the uncertainty of the would-be market leaders, none of whom knows what most customers really need or want. Each vendor therefore addresses the market it knows best, and a wide variety of products is available. On one end of the scale are terminal emulators that allow managers to look at information from the corporate data base but to do absolutely nothing else with it. On the other end are products that download data from mainframes to personal computers, manipulate and change it at the managers' desks, and uploaded it back to the mainframes, where it is incorporated into the corporate data base.

Several products lie between the extremes of "don't touch" and "do as you please." Some let application programs be developed with the same software on personal computers and mainframes. Others download mainframe data to personal computers and let it be used in integrated application programs where managers perform "what if?" experiments. Still others take the



"There is no 'best' method to link micros with mainframes, and products are evolving as vendors introduce them."

best personal-computer application programs and redesign them so they can run on mainframes. Even within the same product classes, the variation is endless. Certain personal-computer application programs that use mainframe data even sport English-like query languages.

Much information about the new products is vague. Many of them—even among those already introduced—are still in flux. In fact, even the articles in this report present the latest, not the final, views of their authors.

The new technology has spawned problems of corporate politics, and they make the technical problems even harder to solve. One of these political problems is the matter of control over the proliferating multitudes of corporate personal computers. The traditional caretaker of corporate mainframes and data bases has always been the management-information-systems department or the data-processing department. Some of these departments claim that if outside managers can access and—far worse—change data bases without restriction, their integrity will be subverted. Most vendors uphold this view by arming the new products with access control, file locks, passwords, and the like.

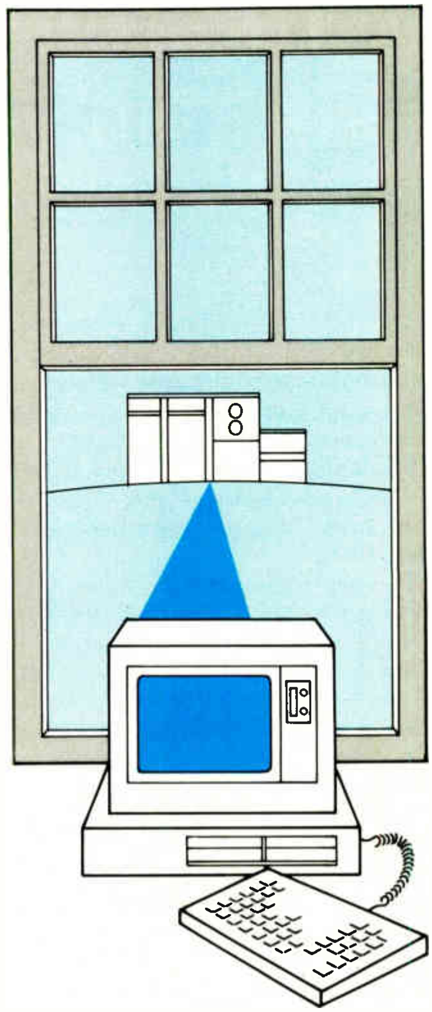
Another political problem is the responsibility for buying corporate personal computers. A firm can easily spend a fortune on personal machines that need expensive but redundant software to talk to one another or to mainframes. Of course, they can deal with this problem by compiling lists of approved hardware and software.

The problems of security and purchasing are not rooted only in the conflict between the data-processing department and the individual managers. The problems also grow out of the fundamental incompatibility between personal computers and mainframes—an incompatibility that stems from their fundamentally different operating systems, query languages, communications interfaces, memories, and powers of computation. Only clever and expensive software is capable of resolving this incompatibility.

One popular way of trying to resolve it is to combine the expertise of mainframe and personal-computer software houses. For example, Informatics General, in Woodland Hills, Calif., has gotten together with VisiCorp, of San Jose, Calif., and as a result, Informatics' Answer/DB, a program for accessing an IBM mainframe data base, will interact with Visi's VisiAnswer for the IBM Personal Computer. Applied Data Research Inc., of Princeton, N. J., has made a similar deal with VisiCorp. University Computing Co., of Dallas, Texas, has agreed to let its mainframe application programs provide inputs to the MBA personal-computer program designed by Context Management Systems, of Torrance, Calif. Context's products—which include such functions as spreadsheet, graphics, word processing, and communications—do not use a query language, and communications can be downloaded only.

Another way of dealing with the problem of incompatibility calls for mainframe specialists to devise their own personal-computer software. Cullinet Software is taking this tack in its effort to link its new relational–data-base–management system for IBM mainframes to the IBM PC. The Westwood, Mass., firm is also getting interface information from Apple Computer Inc., of Cupertino, Calif.,

"Integration products include everything from emulation packages to full-blown systems for up- and down-loading."



in order to develop software for Apple's Lisa personal computer.

Other contenders abound. Intel Corp., of Santa Clara, Calif., has a multiuser hardware and software link that connects the company's mainframe data-base–management system to its personal-computer application software. McCormack & Dodge, of Needham, Mass., has linked its financial–data-base–management system to personal-computer software from Lotus Development Corp., of Cambridge, Mass. And Ryan-McFarland, of Rolling Hills Estates, Calif., has designed a Cobol-based software-development system that allows identical applications to be worked up and run both on mainframes and personal computers. Traditional office-automation vendors are getting into the integration market, too: for example, Harris Corp., of Melbourne, Fla., is giving its office-automation computers data-base access to several different mainframes.

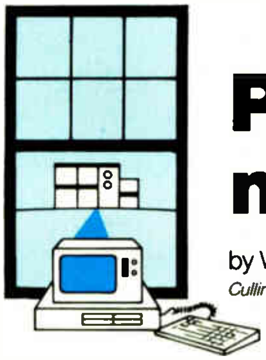
Of the various technologies for connecting the personal computer to the mainframe, terminal emulation is the oldest. It has been available for years but fails to create true integration, since all that users can do with the information they get is stare at it. But this limitation is rapidly disappearing. Software is being written, for example, to take data from emulated terminals and use it as input to integrated application-software packages that run on personal computers. The integration can go further still, in fact. Management Science America Inc., of Atlanta, Ga., has even built a data-base query language into its personal-computer programs.

The products described in this report typify what is now available for making the personal-computer-to-mainframe connection. The best technique for any particular application depends on the application itself. Everyone in the industry agrees that sophisticated vendors do not offer a single solution to all the problems, nor do sophisticated users seek one.

The six articles that follow on pages 108 through 119 do not represent the last word: many current vendors are not represented, and new ones rapidly enter the market. Cullinet's article, the first in alphabetical order, describes the firm's products for IBM mainframes and the IBM PC. Harris Corp., which believes that the best decisions are based on more than one data base, explains how its office-automation computers give managers access to IBM, Control Data, Sperry Univac, and other mainframes, as well as to external data bases.

Intel's article deals with its mainframe data-base–management system, whose "open" hardware—designed to accept industry-standard protocols, operating systems, and so on—can interface with personal computers linked in a network that runs an integrated applications-software package. Microcom Corp., of Norwood, Mass., outlines its proposed industry-standard protocol for file transfer between any personal computer and other personal computers and mainframes.

Microsoft Corp. of Bellevue, Wash., describes its commitment to an open-architecture design that can serve the multivendor environment. Finally, Ryan-McFarland describes its effort to deal with the basic incompatibility between the personal computer and the mainframe by designing a Cobol compiler that can develop identical application programs on both.



Partitioned software joins mainframes to personal units

by William G. Nisen
Cullinet Software, Westwood, Mass.

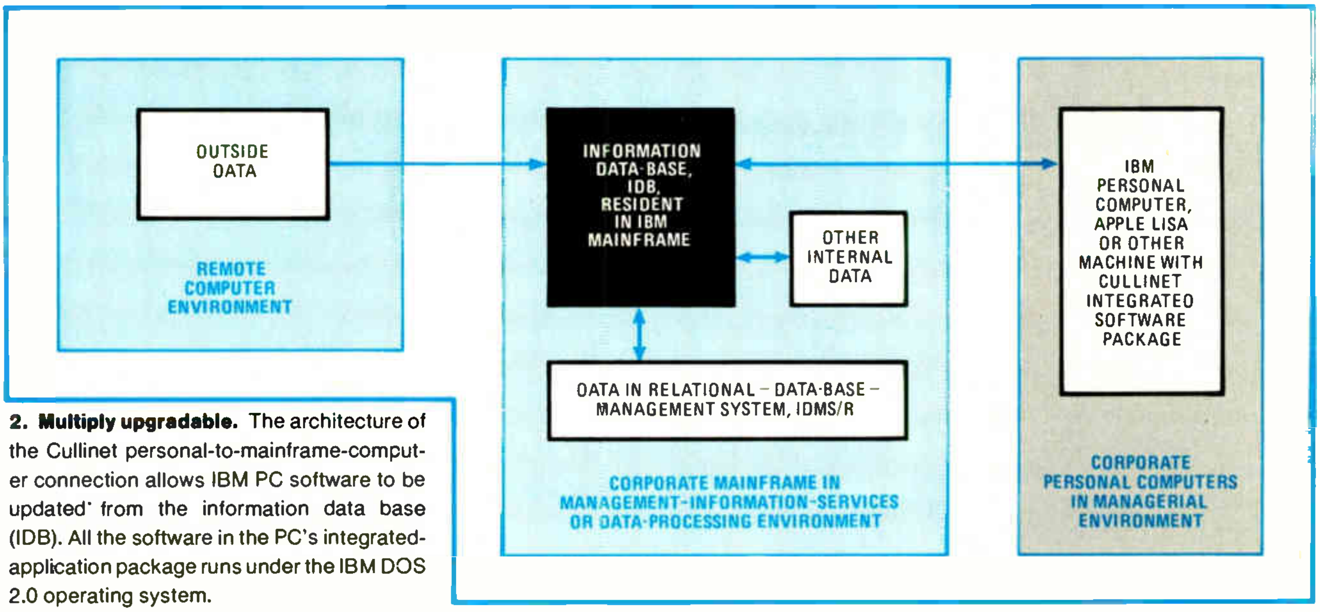
☐ To be truly useful, a corporate personal computer must be fortified by a two-way link to a mainframe data base and by an integrated software package that can use the data. Cullinet has developed software not only for the personal-computer and mainframe ends of the link but also for the interface between them.

Three products combine to do the job: an information data base (IDB), a relational–data-base–management system (IDMS/R), and an integrated package of personal-computer application programs (Fig. 1). The data-processing (or the management-information–systems) department's production and transaction data are handled by the relational–data-base–management system (Fig. 2). It is the IDB software that links the manager at the personal-computer end with a production- or transaction-oriented data base at the mainframe end.

This IDB is a cache of management-oriented information summaries that are derived from the production and transaction data bases and from data bases outside the company—Dow Jones, for example. IDB's relational architecture lets managers use it with nonprocedural—English-like—languages, and it is accessed though a personal computer, which runs an application-software package comprising spreadsheet and query, a relational–data-base–management system, business graphics, document processing, electronic mail, and mainframe communications.

Users can choose among three communications options: a coaxial-cable connection (both local and remote), IBM 3270 terminal emulation (through a protocol converter), and asynchronous communication (through teletypewriter emulation). Just as important, IDMS/R and IDR support a variety of IBM mainframe-software environments, including the various Operating System/Virtual Storage (OS/VS) and Disk Operating System/Virtual Storage Extended (DOS/VSE) operating systems; the Basic Direct, Basic Telecommunication, and Virtual Storage Access Methods (BDAM, BTAM, and VSAM); all major Teleprocessing (TP) monitors; and the Basic, Virtual, and Telecommunications Access Methods (BTAM, VTAM, and TCAM). Cullinet decided that the mainframe software—the IDB—and the management-information–systems department should control access to and manage the corporate data resources. The IDB therefore has all the follow-

1. First things first. Cullinet's IBM PC code is written in C with some 8086 assembler code. About 256-K bytes of RAM and one double-density drive will do the job for most managers. Requirements for Apple's Lisa are just a 3270 communications option with LisaTerminal.



2. Multiply upgradable. The architecture of the Cullinet personal-to-mainframe-computer connection allows IBM PC software to be updated from the information data base (IDB). All the software in the PC's integrated-application package runs under the IBM DOS 2.0 operating system.

ing: an integrated-data and catalog area, security and access controls for end-user information, data-query support, a user-oriented view of data, on-line access for personal computers, and a 3270 terminal interface.

The IDB must also provide an easy interface with the production and transaction data bases. As a relational data base, it can create, edit, add to, read, and erase data tables; maintain a catalog of data entities; and provide data security and access control. Finally, the IDB interfaces with a family of Cullinet mainframe software products, such as the Application Development System.

Two data structures

The new data-base–management system, IDMS/R, which works with the IDB and with the package of integrated applications, combines network (tree-type) and relational data structures—an approach that has several virtues. One system, for instance, can meet the needs both of production and end-user applications, so it is no longer necessary to compromise or to purchase two systems. Moreover, IDMS/R incorporates both kinds of data structures and therefore eliminates the need to duplicate information, use different data-base technologies, or apply different methods of implementation.

Wherever the data may have been first defined, it can be accessed directly and used either in production or by end-users. And IDMS/R is fully compatible with older, nonrelational versions of IDMS, so existing data-base applications run without modification. IDMS/R makes all this possible because instead of providing a simplistic relational view of network data, it directly supports the storage and maintenance of relational tables that apply the full range of relational operators.

The IDB not only gets information from the IDMS/R but also stores files created in personal computers. These files—documents, messages, or graphs—can later be retrieved and mailed to other users. Moreover, Cullinet will make it possible to create files in personal computers and to update the IDMS/R—under the data-processing department's control.

When all the parts are ready, the IDB will be the center of a personal-computer support system, which will allow complete two-way communication between the personal computer and the mainframe. Already, the IDB can act as a central information source and unite a multitude of personal computers into a network by accessing data from data bases and outside sources, summarizing it, and sending it to personal computers.

Giving host mainframes control over personal-computer networks might have generated many problems—for instance, the proliferation of data bases or portions of them. Proliferation tends to make data redundant and perishable, to undermine its integrity, and to complicate efforts to transmit it without errors. Access to data and data security can both become more difficult.

The IDB deals with data proliferation because it was written as an application program that runs under IDMS/R: it stores each piece of data (on the mainframe) independently of every other piece, so all the data can be combined in any way. Therefore it is unnecessary to keep two similar but not identical data bases.

Data redundancy is not itself the problem—data integrity is. The IDB maintains it by letting data-base administrators construct procedures that access the data bases and massage and store the data in the IDB, which also provides file checks to ensure that data is current and correct. Data transfer is easy and routine: error-detection and -correction, data-flow–control, and transmission-control software see to it that data moves reliably between the mainframe and the personal computers.

Finally, the centralization of corporate personal computers promotes control of data access and security. Passkeys that distinguish among "eyes only" read, copy, append, modify, erase, and view provide for access control. Data security is provided for by well-established ownership rules and passwords for signing on, by restricting the times and places of access to the data base, by establishing sensitivity thresholds to track unsuccessful attempts to log on or break in, by encoding data, and by establishing activity logs that track access to data.

Net helps work station talk to diverse computers

by James S. Lutz
Harris Corp., Melbourne, Fla.

☐ Harris Corp. had three fundamental aims for its executive work station. It had to provide integrated access to mainframes and thus to electronic-information sources, both through local and wide-area communications. It had to be capable of using data from these sources in application programs. Finally, it had to incorporate easy-to-use word processing. These requirements shaped the development of Harris' 9000 series of distributed, multifunctional, and clustered work stations (Fig. 1).

The 9000 provides several kinds of access to all of a company's mainframes. The simplest method permits the work station to emulate the industry-standard IBM 3270 terminal and use its Systems-Network-Architecture–based Synchronous Data Link Control (SNA/SDLC) protocols to create interactive access to a data-processing host (Fig. 2). Data received from host computers can be converted automatically into text and included in reports and memos.

Companies whose host computers cannnot support a 3270 terminal, as well as companies that have two or more mainframes, can form a gateway access to as many as four host computers by linking the Harris MIND series of distributed data-processors to a token-passing local network. The processor supports communications protocols for mainframes produced by IBM Corp., Burroughs Corp., Sperry Univac, Honeywell Inc., and Control Data Corp. thus giving work stations access to most possible corporate data bases.

The 9000 helps executives analyze such data by accommodating personal-computing software application programs written for Digital Research's CP/M-86 operating system—spreadsheets, for example. Finally, its easy-to-use word processor (with a menu-driven interface) can incorporate the data into documents. Throughout document processing, it has at least two levels of help messages.

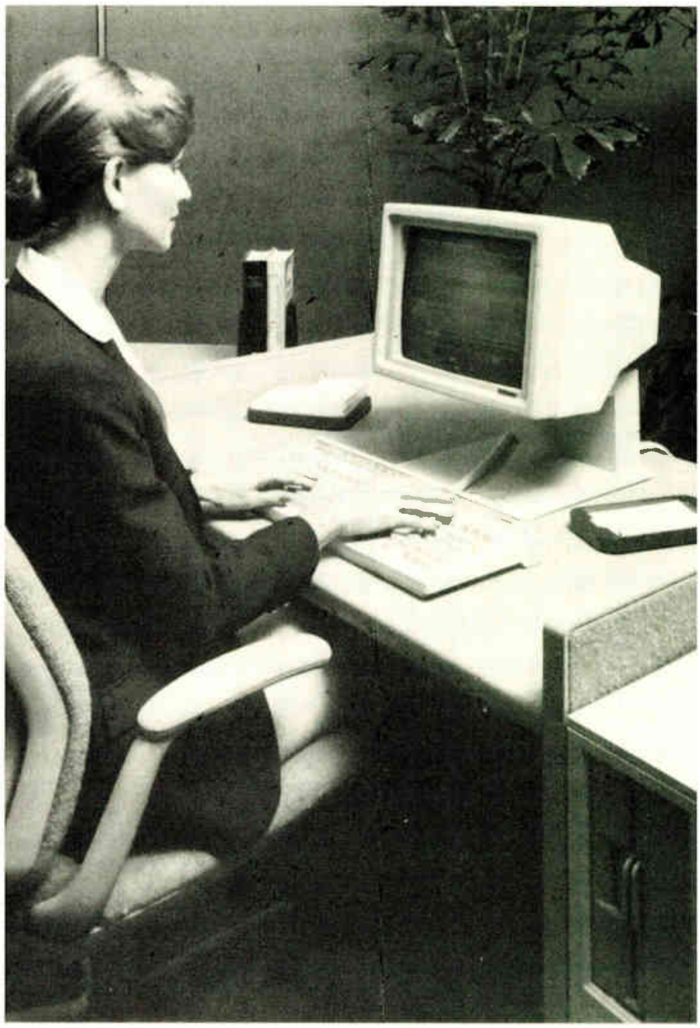
Cost-effective

Harris knew that most companies already had word-processing equipment but needed a cost-effective way of giving work stations access to it. The 9000 can therefore transfer documents to and from various Wang and IBM word processors through appropriate Binary Synchronous Communications protocols, which permit documents to be accessed from local and remote word processors. With little or no loss of text structure, transferred documents are automatically translated to and from the Harris document format. Other wide-area communications protocols are planned such as interactive teletypewriter, to provide access to such outside information sources as the Dow Jones News Service.

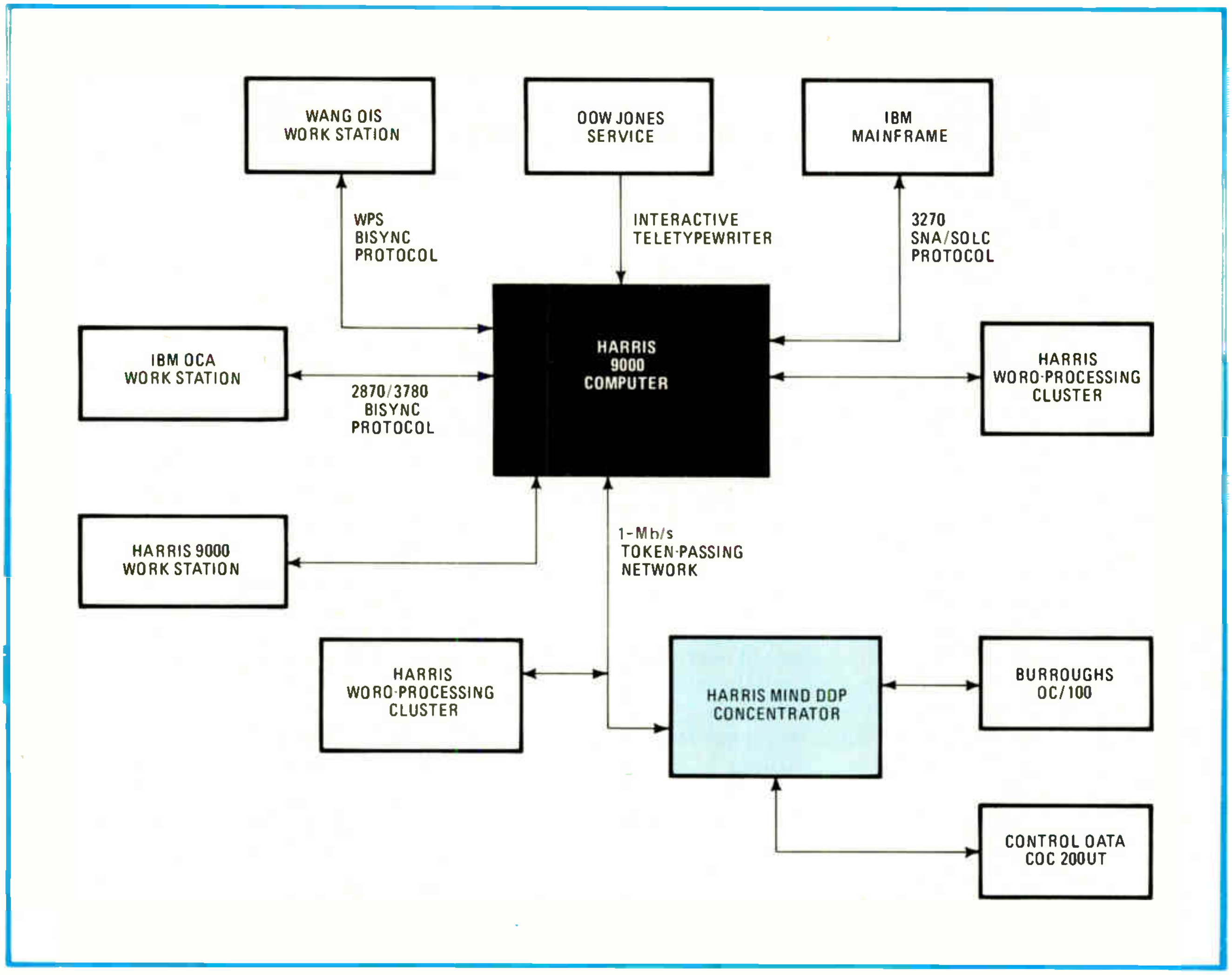
Timely service

An executive work station must be responsive if it is going to help executives analyze more data in less time. Therefore, for the 9000's main processor, Harris decided to use the Intel 80186, a 16-bit microprocessor that integrates functions formerly performed by peripheral chips.

The 80186 microprocessor permits the 9000 to use system and application software written in a proprietary, high-level language similar to Pascal, and this propri-



1. Easy to use. Work stations that Harris uses for connection to mainframes may be grouped in clusters or, as shown here, standing alone. Features include 15-inch-diagonal screens with 33 lines and a 108-key typewriter keyboard with 14 programmable keys.



2. Flexible. Local and wide-area communications in the Harris micro-to-mainframe link give users access to electronic-based information. The 9000 provides decision makers with the benefits of access to data bases, much as the production process has already benefited from them.

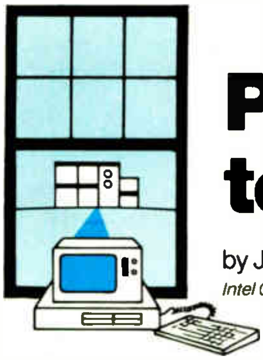
etary language makes possible a modular software design that promotes the efficient addition of software as needs evolve. Yet the 80186's processing power also helps the 9000 operate quickly enough to be a clerical work station and a nonclerical one, as well.

Intelligent peripheral-controller cards—which make it unnecessary for the main processor to handle input/output for communications, disk drives, and printers—also contribute to the present and anticipated performance of the work station, with its 1 megabyte of random-access memory. As many as 12 work stations may be attached to a cluster that shares the disk storage handled by the peripheral-controller card. Sharing allows documents to be accessed by any user in a cluster and still provides security on a document and part-of-document basis. Each cluster also has floppy-disk storage for documents and personal applications.

The entry-level product of the 9000 series is the 9010 standalone word processor, which also serves as a multifunctional work station integrating word processing, communications, and computing functions. It can handle 1 megabyte of RAM and 16 megabytes of floppy- and rigid-disk storage as well as its own letter-quality printer.

Different clusters may need to share documents, too—a fact that helped shape Harris's design for the 9000's communications scheme. Analysis showed that a 1-megabit-per-second, baseband, local network could connect up to 32 clusters. This proprietary network uses the token-passing logical-ring–physical-bus protocol developed by the IEEE's 802 Local Network Standards committee. A large-scale–integrated token-passing controller chip supports the token-passing access protocol and reduces both the software load on the devices attached to the network and the cost of the connection.

Harris chose token passing, a deterministic protocol not dependent upon propagation delay times, rather than Ethernet or one of the other collision-detection–based networks, because it lends itself to later migration to a broadband local network that may extend further than a baseband link. In fact, either the present baseband link or a later broadband one may be used as a bridge link, to permit hierarchical interconnections among department or "work group" networks. Executives will then have access to many document-storage areas spread throughout the network. Thus, they will be able to work with increased efficiency.



Pipeline links data bases to personal computers

by Jim Rutledge
Intel Corp., Austin, Texas

☐ Personal computers proliferate throughout large companies, most commonly for use with spreadsheets and other kinds of data-analysis software. Data can now be reviewed in hours or minutes instead of weeks.

In one way or other, users must themselves enter the data to be analyzed. This fact, obvious in itself, points to the major weakness of corporate personal computers. For data is usually as personal as the personal computer itself, and the spreadsheet, however powerful in theory, is worthless if its data is not correct.

Intel decided to create a hardware and software product—a data pipeline—that would move valid data from central data bases into networks of personal computers and work stations. Once the data got there, it was to be shared by several users involved in creating spreadsheets and other kinds of application software (Fig. 1).

Intel then had to design the actual pipeline. It first considered, but turned down, several existing technical alternatives that could not ensure the security of the data or permit it to be shared among several users and software application packages.

One is best

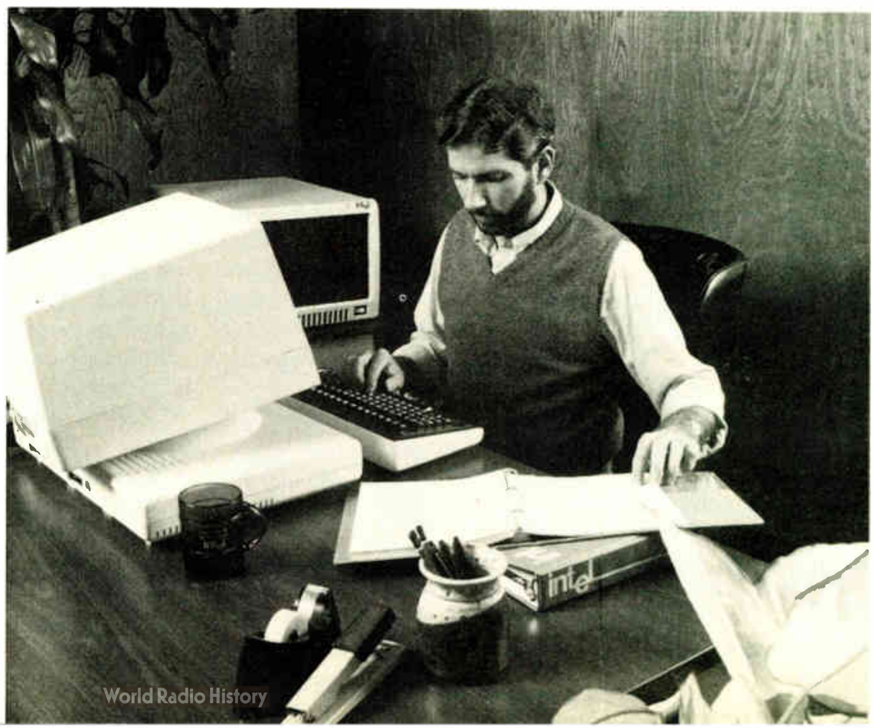
Four ways of getting data from a central computer to a personal-computer or work-station network have so far been devised. The most fundamental is just to copy (or dump) the data into a storage medium compatible with both systems. Among the most commonly used media are tape, floppy disks, and removable hard-disk devices. After the storage medium is copied at the host computer, it is carried and loaded—by hand—onto the distributed system—an unwieldy procedure subject to a myriad of security problems.

Because this kind of data sharing depends on human intervention, it has been called a "tennis-shoe" network. Time delays, the lack of true data sharing, and possible security failures made it unacceptable for Intel's pipeline.

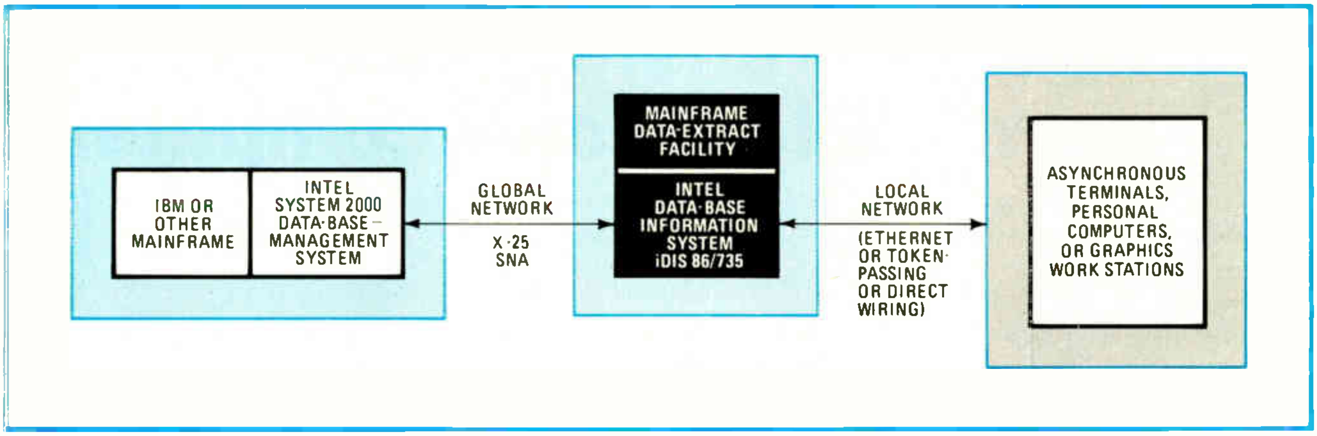
File-controller–type application programs are another technique often used with personal computers, frequently in conjunction with tennis-shoe networks. The data goes onto a central storage device controlled by a fairly simple software package that serves user requests for files. When it receives such a request, it downloads entire files into the personal computer's local storage. In many cases, however, users do not need an entire file, so the process is inefficient and costly. Besides, the data cannot be shared by the users. .

The third method of distribution is embodied in the design of the standard packages that permit personal computers to emulate an IBM 3270. Such packages have inspired announcements of others, which will allow users to access mainframe data-base–management systems directly from personal computers and thus share data. But the approach adds to the cost and burden of corporate mainframe and communications networks. And the unique computing powers of the mainframe and the personal computer go unused.

Intel eventually chose a method of distribution that lets users extract data as they need it from a mainframe data-base–management system. The extract software downloads bulk data into multiuser systems (Fig. 2) where it is manipulated by application packages and



1. Extras. Intel's personal-computer-to-mainframe connection, shown in a typical installation, offers more than mere data-base access. Users can implement spreadsheets, menus or forms, word processing, graphics, and project-management tools.



2. Pipeline layers. The 2000's data-base–management software acts as a gateway to IBM mainframe data. Once Intel's data-extracting software selects nonrelational data, it is sent over a global network. The downloaded, now relational, files are shared among two or more users.

accessed by an SQL-type (English-like) query language.

The data pipeline comprises four layers, with the top layer at the mainframe and the bottom one at the local network. The layer below the mainframe is the network-communication capability, which provides for bulk downloading of data and for on-line access to the mainframe.

The next layer down, the extract capability, allows users to construct requests for subsets of mainframe data. To do so, they need only follow a set of menu-driven prompts. The lowest layer in the mainframe–to–work-station connection is the local network. Here, local communications facilitate the sharing both of computing power and of data.

All users of Intel's Database Information System, the iDIS 86/735, can share the data. To aid in the sharing, the iDIS hardware includes a 35-megabyte Winchester disk, 765 kilobytes of random-access memory, support for five terminals, two lines for communicating with the host, and a printer. At both access and record levels, security is provided by the SQL-like relational language.

Data can be shared because it is automatically converted during extraction from the mainframe's hierarchical data-base–management system into the relational structures that the SQL-like language requires. As the data structures are modified, the data files are converted (enabling sharing of data by multiple work stations and personal computers) into the file format of Microsoft Xenix, which is derived from Bell Laboratories' Unix operating system.

These conversions and the pipeline's design free users from worry about file conversions. The most recent corporate data for their integrated packages of software applications—spreadsheets, word processing, electronic mail or agenda, forms or menus, and others—will always be available and entered, and they can forget about data structures. IBM, Control Data, and Sperry Univac machines with different operating systems can interface with Intel's iDIS 86/735, most of whose system software is written in C.

How Intel opens up its spreadsheet

Only if software packages from separate vendors have well-defined interfaces can they become building blocks in more powerful systems. Or, as Microsoft Corp.'s Mark Orsino (p. 116) puts it, such packages must be "open" to be integrated into a single system.

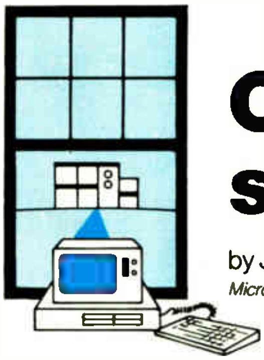
Consider, for example, the way Intel's iDIS data-base information system embeds data-base commands in a spreadsheet. When managers prepare these documents, they may need data kept in a remote data base. Each time they prepare the spreadsheets, they must retrieve the latest data automatically. Intel's spreadsheet (Microsoft's Multiplan) does so with a novel file format. The manager starts by creating a spreadsheet model with static data and data-base directives, including a data-base name, a command to retrieve data, and details about the locations that will receive it. The directives go into one of the spreadsheet cells as "alpha" text.

The spreadsheet is saved as a "model" file, and a software utility program processes it. Microsoft describes this formatting as a SYLK, for SYmbolic LinK file format. In the SYLK format, records of text written in the American Standard Code for Information Interchange define the spreadsheet's entire contents. The utility program locates all the SYLK file's directives and retrieves data from the mainframe data base.

The result is a spreadsheet file that contains both the newly acquired data and the spreadsheet's original contents. Once the model has been saved, the utility creates an up-to-the-minute spreadsheet whenever the manager calls for one, and it can be viewed or printed with the Multiplan application program.

The open iDIS system and defined software interfaces come with a bonus, too: a iDIS terminal can be accessed by an IBM Personal Computer through a terminal-emulation program and can also retrieve data from a mainframe through iDIS data-extract software, can prepare a spreadsheet model and a final spreadsheet, and can transfer it to the PC.

—**Jack Dorman,** *Intel Corp., Austin, Texas*



One file-transfer protocol serves all personal computers

by James Dow
Microcom Inc., Norwood, Mass.

☐ So many different personal computers and work stations have surfaced that their protocols for communicating with mainframes urgently need standardizing. The only such hand-shaking software available so far has been geared to specific situations or specific personal computers. Also, many of the protocols fail to treat the machines as anything more than dumb terminals. In contrast, the Microcom Networking Protocol (MNP) is suitable for file transfer by most personal computers to most mainframes, and it utilizes the personal computer's intelligence.

MNP has the support of Apple Computer, GTE Telenet, VisiCorp, and Victor Technologies, among others in the industry. Perhaps even more important, from the standards point of view, MNP is an expandable, layered protocol that conforms to both the International Standards Organization's Open Systems Interconnect model for computer communications and the National Bureau of Standards' specifications for message formatting. The MNP protocol is available for a one-time license fee.

Everyone benefits

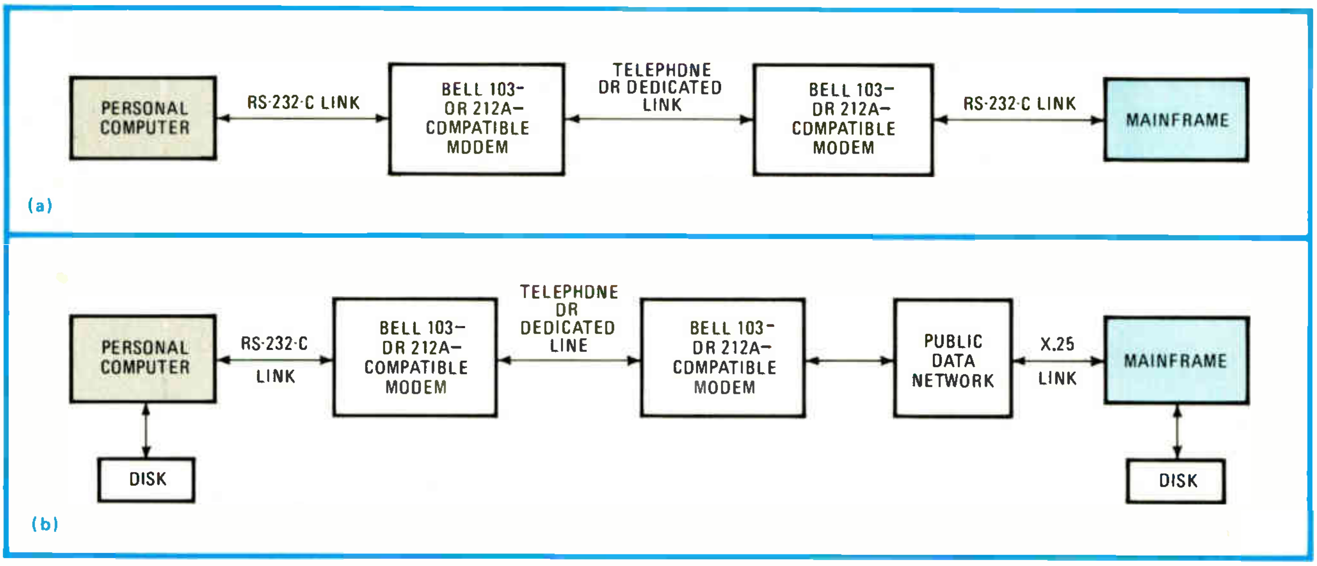
An industry-standard file-transfer protocol is much more than just a convenience for the users of a personal computer. Manufacturers of hardware products will no longer have to research and develop their own protocol techniques. Also, they will find the marketability of their products heightened by numerous new uses that should open up for them in conjunction with other computers—mainframe, mini-, or personal. Likewise, software producers will save on protocol development. Even vendors of networks and data-base services stand to profit from the resulting increase in network traffic in graphics information, spreadsheet templates, and software updates, as well as electronic mail.

Far away

Nonetheless, it is the personal-computer users who have the most to gain from file-transfer standardization; for by enhancing communications with mainframes it will guarantee these professionals the timely data that is essential to rapid decision making.

The largest single segment of the personal-computer-to-mainframe communications market (see "Who connects?" p. 115) is made up of people who are at least several miles away from the mainframe they wish to access, access it only on occasion, and require no more than moderate amounts of data. Establishing a connection through a local network is impractical because of the distance. Polled, leased-line networks, IBM 3270 terminal emulations, and protocol conversions are uneconomic because of the high cost of the communication lines, line drops, and interface equipment.

The majority of users in this category currently gain access to a mainframe by having their personal computers emulate dumb terminals and by using either the public switched telephone network (for direct connection to the host) or a public data network (without direct



Fits right in. The Microcom file-transfer protocol handles either a direct link between communicating computers (a) or a packet-switching link (b). The protocol software can be resident in the computers or the modems and has been proposed as a standard.

connection to the host), such as GTE Telenet, Tymnet, or Compuserve's network. Either way, communication generally occurs at rates of 300 or 1,200 baud (see figure).

Because the personal computer is forced to act as an unintelligent terminal and not as a computer in a network, it is usually limited to transmitting only 7-bit ASCII data or text files. No provision is made for error control, data transparency, or end-to-end file transfer—all of which are needed in the sort of reliable communications network described by the ISO seven-layer model.

These limitations have been the catalyst for the development of numerous custom asynchronous protocols that do exploit the machines' intelligence in order to provide some of the required services. Unfortunately, most of these asynchronous protocols have been developed for a single application. Therefore, the protocol developed by vendor A for file transfer will rarely, if ever, be compatible with the protocol developed by vendor B, whose machines also must transfer files to the same host mainframe. Clearly, too, a mainframe cannot be expected to support even a small percentage of the many protocols that are available.

Inside the protocol

The Microcom networking protocol makes short work of this confusion by providing reliable flow-controlled, transparent data transfer on point-to-point connections both as a stream of bytes and as files. Equally important, it defines a minimal virtual file that is essential to the transfer of data between dissimilar computer and operating-system architectures.

As the ISO model requires, the first and bottom layer of the protocol is the physical layer—the actual hardware connection to the transmission medium. For this layer the R-232-C standard was chosen because of its widespread use on every size of computer.

Also, as the ISO model requires, the second (or link) layer of MNP provides data transparency, flow control, and error control. Data transparency is provided by software through which this layer and those above it can detect the beginning and end of what are known as protocol data units. MNP accomplishes this chore by framing, or marking, the beginning and end of each protocol data unit sent.

On byte-oriented machine architectures, a byte-stuffing technique is used. Where more powerful bit-synchronous hardware interfaces and synchronous modems are provided, the MNP switches to the more efficient Synchronous Data Link Control (SDLC) framing known as start-and-stop-flag, zero-bit insertion.

Reliable data transfer is achieved through the use of positive acknowledgment, error correction via a 16-bit cyclic redundancy check, and retransmission where necessary. The flow of data is controlled by a credit allocation (assigning a fixed quantity of memory per data transmission) or by a sliding window scheme (allocating as much memory space as needed).

Skip one

The ISO session layer (the ISO network layer is not used) creates a full-duplex connection between communicating devices. At the session level a message is exchanged identifying the communicating-device type, the file operating-system type, the application program, the source address, and the destination address.

In the event that the two device types and operating systems are identical, the session is a "native" one. But in the case of personal-computer-to-mainframe communications, where the devices and operating systems are dissimilar, the session is virtual and files are transferred in a virtual-file format.

The top, or application layer (equivalent to ISO layer 7), provides file-manipulation and -transfer services. At this layer the communication initiator gives his or her password and identifies the file's action type (its purpose), transfer mode, and name. He or she also handles the file's type, record length, source, and destination.

Now the two computers can start to communicate. What has happened is that the implementation of the physical, link, session, and application layers has resulted in an orderly creation of transparent data-transfer connections between the two highest-level users—the application programs on the personal computer and those on the mainframe.

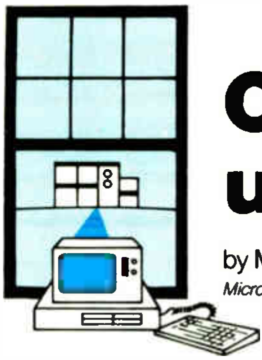
Who connects?

How often, for how much data, and from how far away—the answers to those questions define the best way of linking a personal computer to a mainframe from which it needs to access data. Ideally, if the two machines exchange data frequently and in volume and are less than several thousand feet apart, they should be linked by a local network, such as Ethernet, Omninet, or some form of the IEEE 802 standard. But in the real world, few mainframes have local-network interfaces, so instead they use dedicated terminals and communications links.

If the personal computer is more than several thousand feet away from the mainframe but the other factors are unchanged—large amounts of data are frequently accessed—the most practical access method is often through the IBM 3270 terminal (or terminal emulation) using the Binary Synchronous protocol of IBM's Systems Network Architecture (SNA). This is usually done with a polled, leased-line network and with synchronous modems.

Such emulation-based communications, if properly implemented, will be invisible to the IBM mainframe. For most users of personal computers, on the other hand, the leased-line drops, the high-speed modems, and the specialized software needed for their use are expensive, and many minicomputer and other vendor application programs were not written to support the 3270 terminal.

The largest class of personal-computer or work-station user—many miles from the mainframe, with a low to moderate frequency of use, for moderate amounts of data—is best served by a telephone-line link to the mainframe and a standard protocol.



Open-architecture design unites diverse systems

by Mark S. Ursino
Microsoft Corp., Bellevue, Wash.

☐ By tradition, most computers are designed to be "open," capable of addressing many different needs. That flexibility confers great freedom of choice on the end user, of course, but it also forces system integrators to unify a wilderness of machines, networks, protocols, and operating systems. Usually, this system integrator must confront architectures with varying degrees of openness, embodied in a jumble of components—including communications logistics (like physical connections and protocols), data sources (such as data-base–management systems and files), and data applications (like accounting and productivity tools).

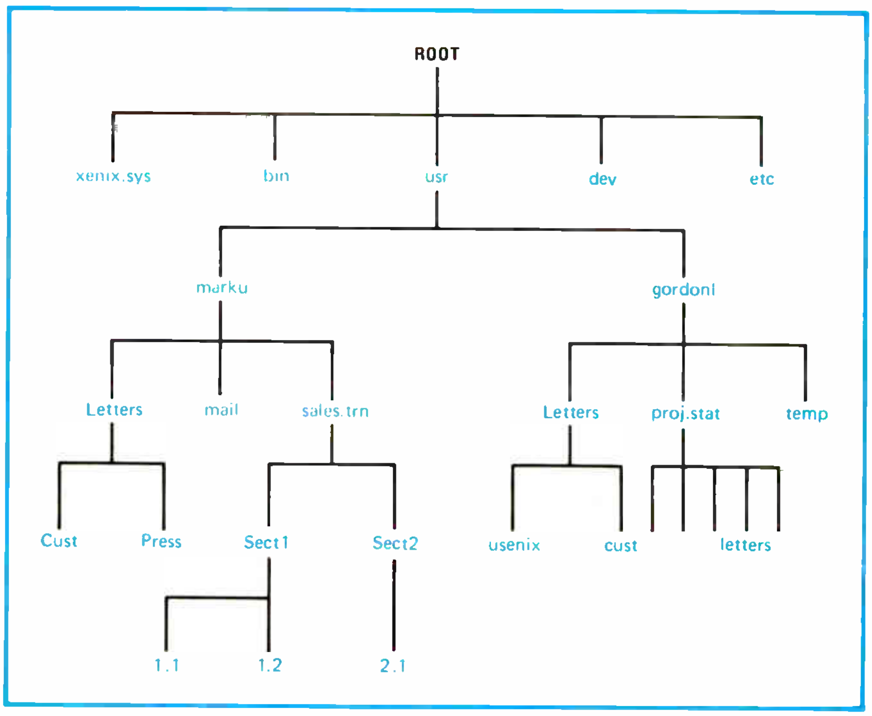
The magnitude of the problem convinced Microsoft that no single, magically clever package will solve it. After all, how likely is it that a single vendor could maintain strong relationships with all the vendors involved? The real solution will require all those—including in-house data-processing departments—who build software products to assume a share of responsibility. They will all have to build open architectures into the software they produce, and they will all have to generate appppropriate interfaces among the components they control. One part of Microsoft's share of this solution, SYLK (for SYmbolic LinK), will be discussed later, at the end of this article.

Physical communication between machines, and the passing of data between different operating systems, are two fundamental aspects of the integration problem. But even the physical connection between machines is hardly a trivial problem. And the tight coupling of mainframe systems and their communications hardware is an additional complication. So the burden of establishing the connection falls on the personal computer's operating software. What's more, mainframe systems tend to be wired to protocols sponsored by the mainframe manufacturer, and this too puts the burden on personal machines.

Fortunately, all the popular 16-bit operating systems for personal computers were developed by independent software vendors. Instead of the very specific operating systems of the mainframes, personal computers support a wide variety of architectures and can therefore communicate, without rigid predispositions, through integrated device drivers.

The problems of integration have also been simplified a bit by the communications level—in essence, message passing—permitted by classical operating systems. This simple mechanism allows personal-computer communications protocols to operate in tandem with device drivers.

Computer communications divide between two generic forms: telecommunications and local networks. General operating systems can interface with both forms. Whichever of them may be chosen, the operating system's



Tree structure. A typical hierarchical directory has a root and branches as shown. A directory, file, or peripheral on a network can be addressed by tracing a logical path through the tree branches. No knowledge of the network's architecture is needed, and both machines and users can change locations without disturbing the directory.

services should be defined at a level basic enough to eliminate the need to assume anything about the form's characteristics—even its performance. And the dynamic nature of the distributed information and resources in these networks means that they must be designed to allow logical addressing of data and services (see figure), independent of physical network address or the characteristics of a computer or a network (see "Where are you?" below).

A trio of classes

Integrating systems of differing functionality requires network services to be divided into three classes, set up as upwardly compatible layers to allow transparent networking between dissimilar systems and to avoid resort to the simplistic and inadequate—though normal—file-transfer and virtual-terminal protocols.

The first of these three classes, basic services, is the highest common factor. Basic services are so fundamental to computers that almost any machine can be given the protocol to join a network. There are no options, and all implementations provide all services. In effect, basic services consist of the facilities provided by a generic or pseudo operating system.

The second class, familial services, defines an extended functionality that is possible among operating systems of the same species. MS/DOS, Bell Laboratories' Unix operating system, and Xenix (and other Unix look-alikes and derivatives) are similar enough, architecturally, to be integrated at this level. Familial services allow these operating systems to merge files by supporting family-specific file-system operations, such as changing the files' protection "mode," altering the directory structure by adding and deleting directories, and accessing files on remote computers.

Finally, identical operating systems and identical extensions to different operating systems can have more functionality than operating systems of the same family. The third class of proprietary services—implementation-specific network extensions—takes advantage of hardware or software peculiar to a specific product.

Application integration

Integrating the application programs of mainframes and personal computers is even more difficult than integrating communications and system software. These days, the most celebrated form of program integration involves lashing up the productivity tools of personal computers to corporate data-processing resources or to commercially available information services. But this very limited definition of application-software integration solves only one limited problem.

Much work is being done to define "sockets" in personal-productivity tools and general application programs. These sockets provide a known and manageable interface that allows third parties to integrate applications from other vendors without modification. Mainframe data-base products have more or less been defined this way, since the data-base vendor must provide for the easy migration of data from oddly assorted application software into the data base.

Systems based on personal computers or work stations are following suit, at least in the sense that they are capable of reading and writing user-definable fixed-format records so as to load data from "foreign" sources. For example, data-base and application products generally incorporate a report writer that can also be used to provide this general interface.

The problem is harder with visually oriented productivity tools, like VisiCalc and Multiplan. Such visual tools interface with users more successfully than do applications that lack graphic displays; they give the data more meaning by presenting it, for example, as a function of position on a display. Of course, such data can always be dumped off as ASCII text and used in a text-only machine or application. But the user then loses the natural association of names, formulas, relative positions, and formats that describe the properties of the data and give it meaning. This diminishes the data's value to the application and creates a strained and unnatural association between packages.

Microsoft, for its part, has achieved a more intimate integration of its productivity tools—both among themselves and with "foreign" software—by defining a data interchange format called SYLK. The format not only dumps data but also adds extra properties that tell "reading" applications what it means. The format is designed for ease of generation, ease of parsing, and storage.

SYLK files, for example, can completely represent a Multiplan worksheet (like a program to build a cash-flow forecasting worksheet), so a program can generate one from a general-ledger chart of accounts. The resulting forecasts can then be "forwarded" for tracking to a budget-control system.

Where are you?

The most generally accepted way to provide an addressing interface is to extend the user and application file system. Since both the MS/DOS and Xenix operating systems have tree-structured (or hierarchical) directories, they can be pictured as an upward extension of the file system as it would appear on any machine. In other words, above the machine's top (or root) directory would be a network root.

Directories, files, and peripherals on any machine in the network can be addressed just by using the appropriate file system "path"—not the physical path that the system must travel, which is subject to architectural changes, but the logical directory path, which changes only as specified by a user or an application. The network file system removes the issue of network software and does so in a way that is general enough to allow networked applications to be developed without prior knowledge of the machines, communications mode, or media involved. Questions of file integrity, security, privacy, and reliability are resolved similarly. Thus, the end user has a uniform method of computer system control.

Cobol compiler fits micros and mainframes

by Glenn Embrey
Ryan-McFarland Corp., Rolling Hills Estates, Calif.

☐ Since companies, like people, have their own styles of using personal computers, there is probably no single, most effective way of integrating these machines into an organization's data-processing operations. Instead, companies should be given a tool with which to evolve their own solutions. So Ryan-McFarland has developed a Cobol-language compiler that produces identical source and object code on many different processors and different operating systems.

Once all computers in a company speak exactly the same language, many data-handling scenarios become possible. For example, most companies see the Ryan-McFarland Cobol product primarily as a means of giving their data-processing departments greater control over personal computers. Other firms, however, view it as a way of offloading some mainframe tasks—they discover they can develop more software more quickly by using personal computers in place of the overburdened mainframe, uploading programs into it only when they are complete and debugged. Still other companies find the product turns personal computers into training stations for beginning programmers, who no longer deplete mainframe resources.

Many possibilities

The same Cobol compiler, known as RM/Cobol, is available for IBM mainframes, as well as for most popular desktop systems. Consequently, identical application software will run on all these systems (to date 18 processors and 35 operating systems) without any code having to be rewritten. Such program portability is often difficult for mainframe specialists to grasp, accustomed as they are to the major changes usually required in application software when it migrates to a different operating system, let alone different hardware.

This approach also means software development for all the different machines in a company can be done on a single machine, under a single operating system. In effect, the use of personal computers can be managed and controlled by a single resource—ordinarily, a company's data-processing or management-information-systems organization. An application program can be developed on the company's mainframe, by mainframe personnel, in Cobol, the language in which most business programmers are most highly trained. The application is then downloaded with either a modem or a direct link to all the personal computers or work stations throughout the business. The identical code will run on all the machines.

Source or object?

When it makes sense to protect an application from revisions by its users, only the software object code is downloaded. When more flexibility is preferable—for example, to allow a user to customize a report format—the source code itself can be downloaded.

In much the same way, identical data files can be downloaded to personal computers throughout the company. Though such computers cannot usually read mainframe files, because of file structure differences, these files can be rewritten by a mainframe utility into a format compatible with a personal computer and then downloaded.

Clearly, the firm's data-processing department can control what files are available to the rest of the company, can protect the mainframe files from unauthorized updates, and can ensure that all departments have access to the latest figures. This approach is also flexible enough to accommodate transferring data back to the mainframe, if this is desirable.

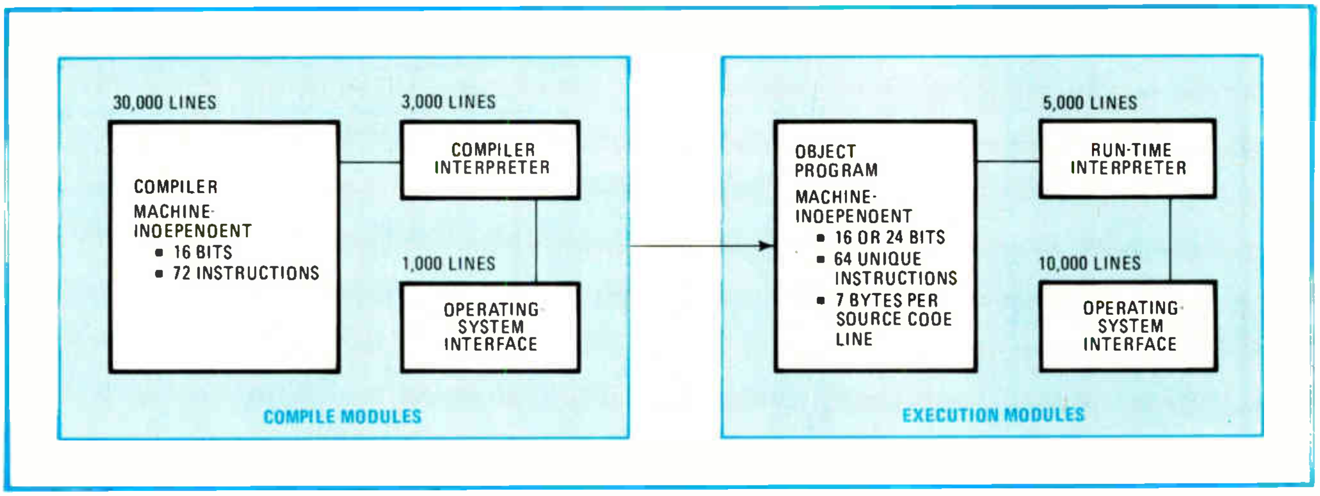
Independent instructions

The software technology of putting identical languages on a wide variety of computer environments is based on the use of machine-independent instruction sets tailored to very specific tasks. Fundamental here is the fact that the RM/Cobol compiler software consists of a number of modules, 70% of whose code is machine-independent. None of this 70% needs to be changed when the compil-

Small no longer

The size and complexity of Cobol programs that are capable of running on personal computers make their "small system" designation a misnomer. A case in point is a planning, scheduling, and control system for manufacturing, developed by Key Systems Inc., of Marathon, Fla. The 400,000 source-code lines of Key's mainframe package were developed by RM/Cobol on an IBM Personal Computer with only 56-K bytes of random-access memory.

Mainframe RM/Cobol is also being used on an IBM mainframe at Tandy Corp., in Fort Worth, Texas, for inventory and account applications. Once the application has been tested, it is turned into TRS-80–executable object code by a mainframe utility program and downloaded via Telenet to TRS-80 model 3s and 4s in Tandy's stores.



Portable. The RM/Cobol compiler is written in machine-independent, task-specific instruction sets, and applications written with it are portable at the source- and object-code level. Source code is compiled by a compiler module in conjunction with a compiler interpreter and operating-system interface. To be executed, the object code thus created requires a run-time system in a specific computer's machine code.

er is reconfigured to function on a different computer.

RM/Cobol can be put onto a new environment quickly, not only because so little of it needs to be changed, but also because the part that remains the same contains the scanning and translating algorithms of the compiler. Therefore, implementing the compiler on different machines is a rather straightforward task that does not require the man-years of work ordinarily needed to develop a distinct compiler.

Typically, the compiler module itself comprises 30,000 lines of code, all of it machine-independent. The module works in conjunction with two much smaller modules, usually totaling fewer than 5,000 lines of code, which are written in the assembly language native to the target machine (see figure).

Chief of three

The first of these modules, the operating-system interface, performs those compiler functions that depend on the operating system. These functions include allocating memory to data-base tables, reading a source record, writing an object record, writing a listing line, and loading a task-specific compiler overlay. The second module is the compiler interpreter. It handles data-management routines as well as interpreting each of the instructions in the compiler module.

Working together, these three modules compile source code into object code. The object code itself also includes machine-independent instructions. Thus, it can be moved from one machine to another without any alteration (or recompilation). In other words, an application can be run on any machine that supports the language.

Before the application object code can be executed, it requires two more modules, both written in the host machine's assembly language. The first is the run-time interpreter. It contains the implementation of the object-code instruction set and handles the instruction set's underlying data decoding and sequencing. Usually consisting of 3,000 to 6,000 lines of code, its size depends primarily on the input/output capability of the operating system. In some cases, nothing less than an entire indexed file manager must be included.

The second module is the run-time operating-system interface. It helps the operating system execute a Cobol program, and its functions include sequential, relative, and indexed input/output operations. The entire module can be quite small if the system file manager supports Cobol input/output in its entirety.

Minimal disadvantages

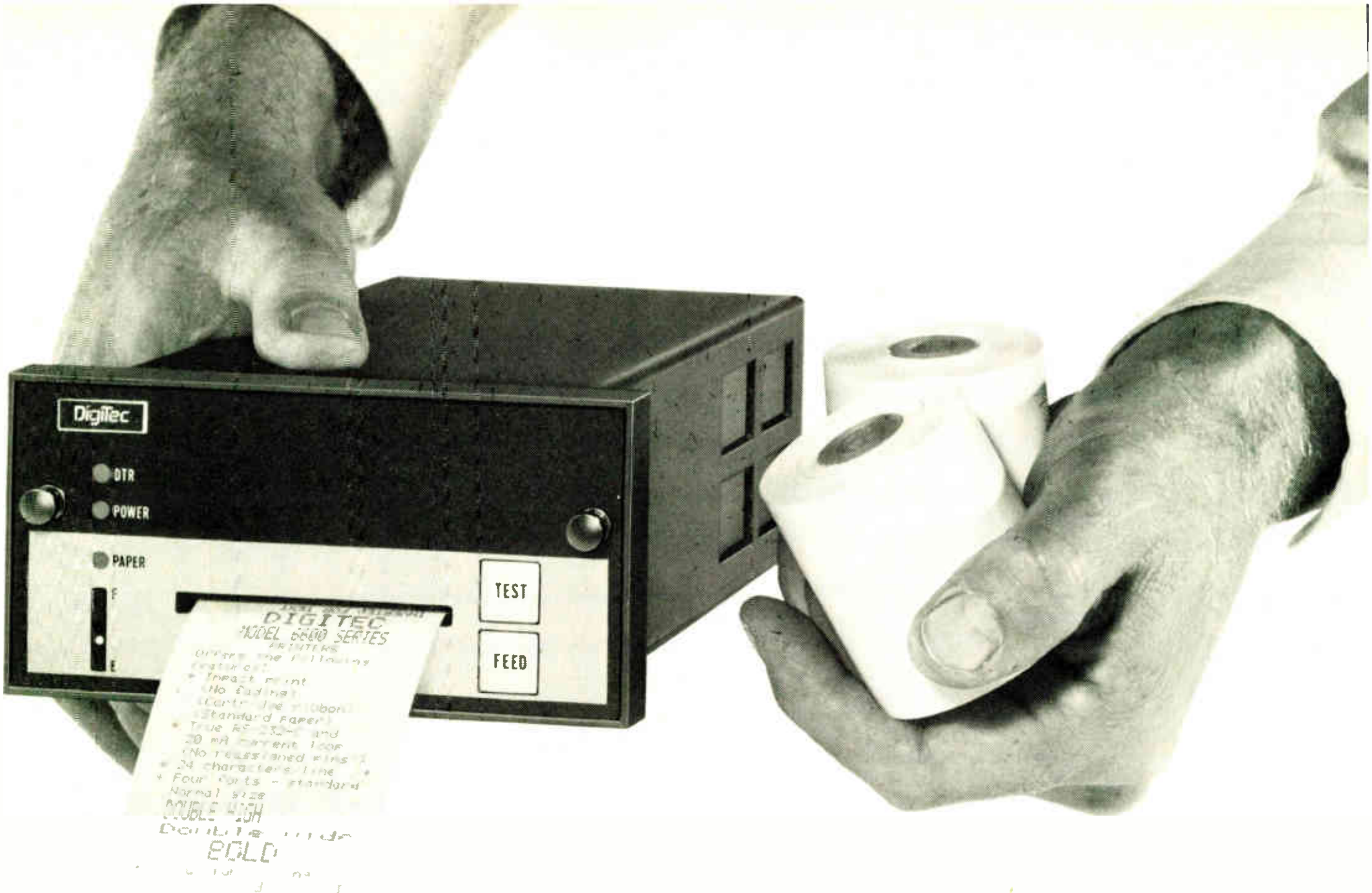
Traditionally, portable object code entails much slower program execution than does nonportable code. However, the Ryan-McFarland compiler minimizes this effect because its task-specific instruction sets are very compact. For example, the object code that represents a typical move statement requires only 4 bytes (16 bits per instruction). In contrast, a typical machine-language implementation would take about 10 bytes: a 3-byte branch-and-link instruction followed by a 2-byte argument A, followed by another 3-byte branch-and-link instruction and a 2-byte argument B.

On the average, the object code for each line of source code uses about 7 bytes, including instructions, data descriptions, variable storage, and literals. In contrast, typical mainframe versions of the Cobol language generate 25 to 35 bytes per source line.

Because of its compactness, the object program executes with much greater efficiency than do most pseudocode technologies, such as the p-system that is currently in vogue. These approaches do not tailor their instruction sets to the tasks required and consequently suffer from poor execution speed.

One segment at a time

RM/Cobol's compactness, coupled with its segmentation feature, allows sophisticated and large application programs to run on personal computers. Segmentation aids in this endeavor because it permits portions of a program to be designated as nonresident in main memory until the moment they are executed. Once executed, a segment is replaced by the next nonresident segment needed. □



New panel printers: ordinary paper is one of many smart benefits

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Pipelined structure overlaps microinstructions; two types of data chaining combine with command chaining

by Werner Boening and Sharad Gandhi, *Siemens AG, Munich, West Germany*

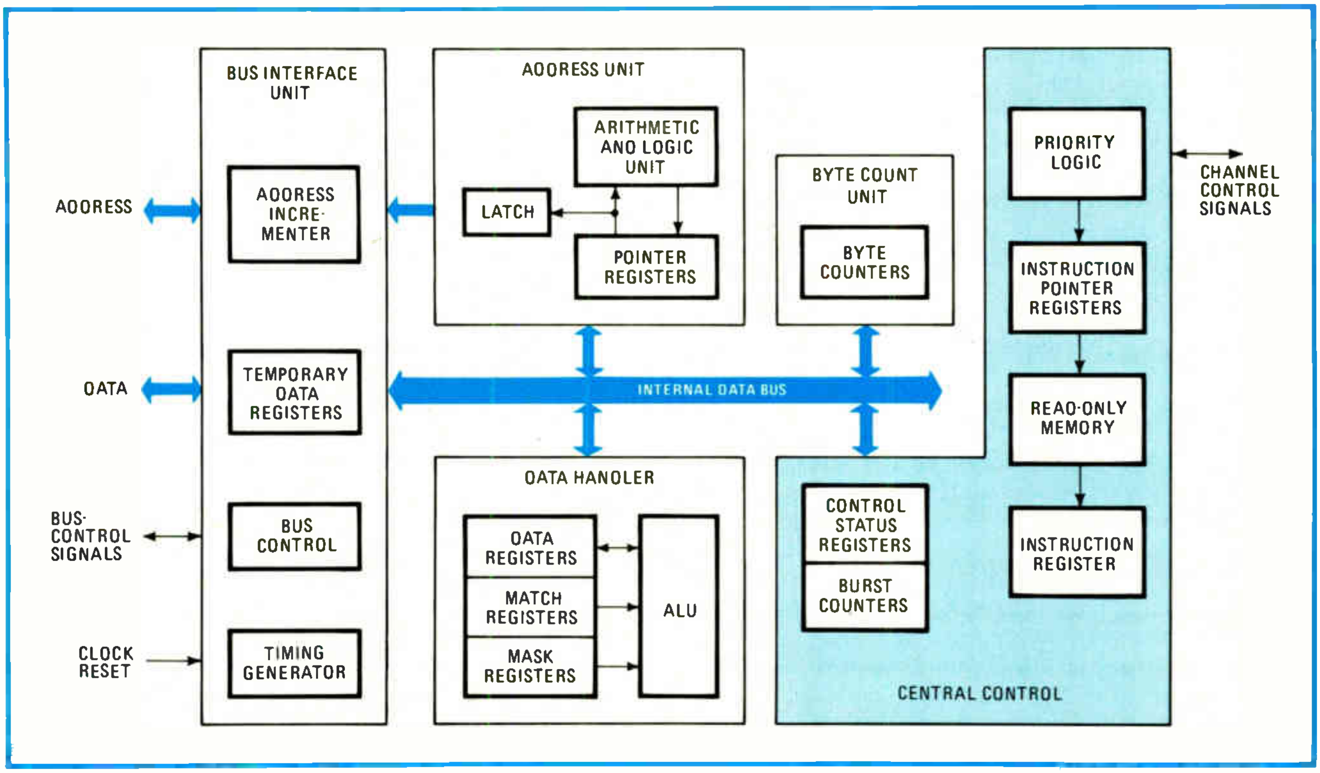
□ An advanced–direct-memory-access controller further fans the wildfire growth in processing power and speed of a variety of microprocessors. For one thing, its speed is heady—it transfers 8 million bytes a second from a single channel and even achieves the same overall throughput with four separately programmable channels working concurrently. For another, its ability to execute a sequence of individual commands independently of the central processing unit contributes directly to microsystem performance.

Nor does the SAB 82258 lack sophistication in its handling of data. It can assemble scattered blocks of data into a single chain, perhaps as a packet for data communications; conversely, it can distribute a chain of data blocks to diverse destinations. Also, it has two modes of operation for distributing data either rapidly and unchanged or more slowly but with some preprocessing. In the first mode, it passes data directly from source to destination in a single bus cycle. In the second mode, data takes two bus cycles to do so because on the way it passes through the controller; there it may undergo a variety of manipulations (such as a masked compare), be redirected to another location in system memory, or be reorganized from bytes into words and *vice versa*.

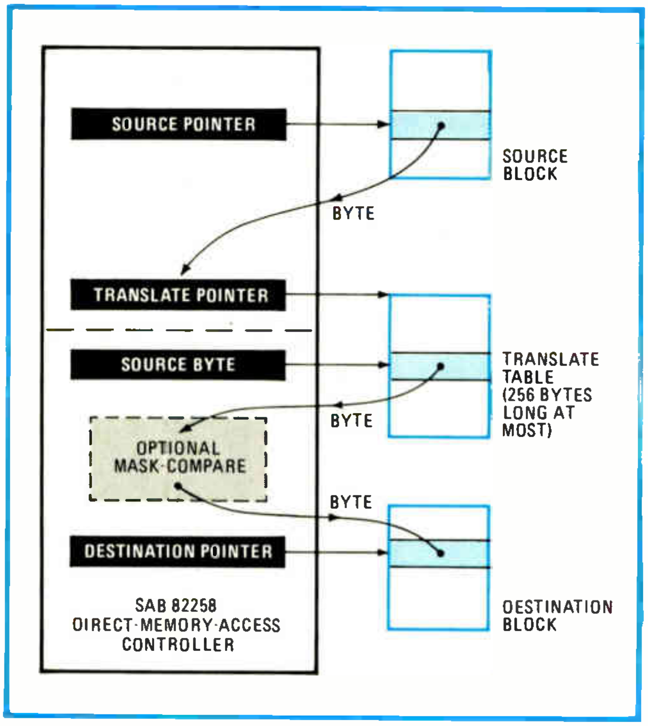
The blueprint

In structure, the SAB 82258 is a microprogrammed, pipelined 16-bit DMA controller with an internal architecture that makes it possible to overlap microinstructions for higher performance (Fig. 1). Siemens' advanced Mymos technology packs 50,000 transistor functions in a 48-square-millimeter die, housed initially in a 68-pin leadless chip-carrier but to be packaged later in a pin-grid array.

Although primarily designed for the 80286, which is a



1. Fast and flexible. Individual sections work autonomously in the SAB 82258 advanced–direct-memory-access controller. Microinstructions in the controller time-share the separate units so that microinstructions for different channels execute just as fast as those for a single channel.



2. Translator. During a DMA transfer, translations of source bytes may be performed (along with an optional mask-compare operation). In translation, the source byte is used as an index into a translation table, which is pointed to by the translate pointer.

16-bit microprocessor with five times the performance of the 16-bit 8086, the controller fits equally well in 8086/88- or 80186/188-based systems, thanks to its adaptive bus interface. The logic level on a specific pin on Reset configures the bus interface of the DMA chip either for the 80286's demultiplexed bus, with the necessary signals and timing, or for the 80186's multiplexed bus. The controller further provides the appropriate signals needed for use in the 8086/88 mode. This adaptive bus interface obviates the need for TTL glue to interface the SAB 82258 with different processor systems. Bus operations may be selected as 8 or 16 bits wide through software.

Paired for speed

The new advanced-DMA controller shows its best performance in the 80286 mode because that microprocessor has a very fast, pipelined bus—so fast that the two devices can read or write a word 16 bits long in just 250 nanoseconds when operating at the nominal 8-megahertz rate. In the 286 mode, the controller can transfer data at rates of 8 megabytes per second. In the 186 and the 8086 modes, the data-transfer rate is 4 megabytes/s since 500 ns is needed for one read or write operation at 8 MHz.

The 80286 can synchronously access the DMA controller through status lines. The HOLD/HOLDA protocol between it and the DMA chip ensures that only one of the two possesses the bus at any time. Such a local-mode combination of processor and DMA controller working through a shared bus is very compact and efficient.

To achieve a yet higher throughput than this setup allows, it is imperative that both the processor and the DMA controller possess a private bus. When operating in this mode, called the remote mode, the advanced-DMA chip can work in parallel with the main processor (which may also possess its own private bus), accessing resources on the resident bus most of the time and accessing the system bus only for communication with the processor. However, the DMA chip's registers are always accessible to the processor over the system bus.

The remote mode is also preferred for good system partitioning. For example, a subsystem dealing with Winchester and floppy disks could be put on a separate board holding the advanced-DMA chip, sufficient resident memory, and the necessary controllers.

Four-barreled

Whether in the remote or local mode, the DMA controller can handle a variety of high-speed data-transfer peripherals through its four independent channels. Each channel has three dedicated pins: DREQ (DMA request), DACK (DMA acknowledge), and EOD (end of DMA). A peripheral generates a request for DMA over the DREQ line. DACK is received by the peripheral from the SAB 82258 to tell it when data transfer may take place. The bidirectional EOD line is used by a peripheral to terminate the DMA or by the controller to generate an interrupt on the completion of a DMA operation.

The SAB 82258 is capable of doing single-cycle and two-cycle data transfers. In the faster, single-cycle transfer, the data is transferred between peripheral and memory in a single bus cycle. In the two-cycle operation, the data is always stored in the controller before being sent out to the destination. Although half as fast as a single-cycle transfer, it has several compensating advantages.

In a single-cycle transfer, the data being transferred generally does not enter the DMA controller, but goes directly from the source to the destination. In contrast, since the data does enter the DMA controller for a two-cycle transfer, it is possible to act upon the data and do on-the-fly operations during the transfer. For instance, the data can be translated before being sent to the destination (Fig. 2).

In the two-cycle transfer mode, data may also be transferred from one memory region to another—an impossibility with single-cycle transfer. Another feature of two-cycle transfer is automatic assembly and disassembly of data in bytes and words, meaning that data can be read as one 16-bit word and written as 2 bytes or *vice versa.* This is often desirable when using 8-bit-wide peripherals in a 16-bit system. For example, when data is being written to the peripheral from memory, it could be fetched as a 16-bit word and written out as two 8-bit bytes. The reverse is true for reading data out of an 8-bit peripheral. This feature saves time and reduces the number of bus cycles needed for a given block of data; it is also useful when transferring data between memory in a 16-bit-wide bus (for example, system bus) and that in an 8-bit-wide bus (for example, resident bus.).

In both the single-cycle and the two-cycle transfer modes, the data being transferred may be compared with a given pattern (mask-compare) and the DMA transfer optionally stopped either on encountering data of that pattern or on mismatch of data and pattern. This mask-compare feature may be used for search operations, but

SAB 82258 DIRECT MEMORY ACCESS CONTROLLER REGISTERS		
Name	**Width (in bits)**	**Description**
General registers		
Status	16	gives current status of all channels
Mode	16	sets system parameters such as priority and bus width
Command	8	sets start, stop, single-step operation
Burst	8	sets maximum number of contiguous bus cycles
Delay	8	sets minimum number of clocks between burst access
Channel registers (four sets; one per channel)		
Command pointer	24	holds address of command block being executed
Source pointer	24	holds address of source-address byte
Destination pointer	24	holds address of destination-address byte
Translate-table pointer	24	holds address of base of translation table
List pointer	24	holds address of next list entry for data-chaining operations (address of multiplexer table for multiplexer-channel operations)
Byte count	24	holds byte count, decremented during transfer
Channel command	24	contains current channel command
Mask	16	holds mask-bit pattern for mask comparison
Compare	16	holds bit pattern for comparison in a mask-comparison operation
Assembly	16	is used for data assembly and disassembly operations for data transfers with unequal bus widths
Channel status	8	indicates cause of transfer termination
Multiplexer channel registers		
Interrupt vector	8	identifies subchannel that interrupted or halted
Last vector	8	holds subchannel number of last subchannel that interrupted
Subchannel	8	holds subchannel number addressed by a multiplexer command to the general command register

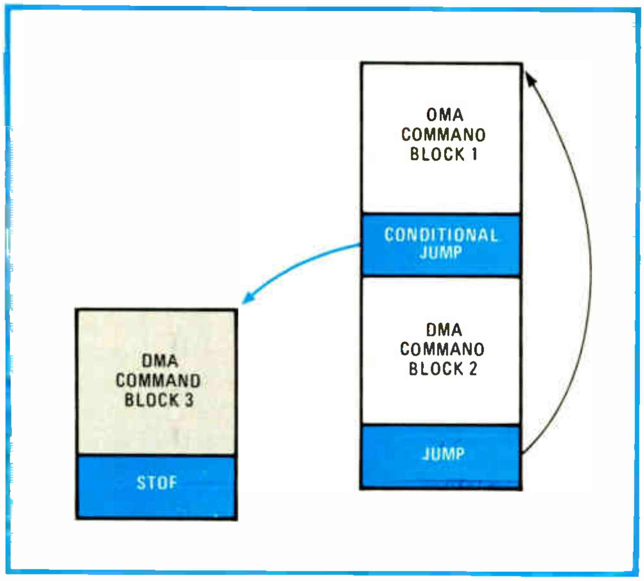
also for investigations of, say, a peripheral status register.

For high-speed DMA controllers with multiple channels, it is very important that no time penalty (no latencies) be imposed them when they are switching from one channel to another. The advanced-DMA chip features an 8-megabyte/s data-transfer rate for any one channel and yet retains a full 2-megabyte/s transfer rate for each of the multiple channels for a total of 8 megabytes/s. A microprogram-controlled machine, the chip accomplishes this through the use of overlapping microinstructions that are based on the critical requirements of the 80286 and its overlapping bus cycles.

An isolated 286 bus cycle needs three clock cycles—T_0, T_1, and T_2—each of 125 ns (assuming a nominal 8-MHz clock frequency). Within a stream of bus cycles, T_0 of a second bus cycle is executed concurrently with T_2 of a previous bus cycle. When coupled to this overlapped bus, the microprogrammed firmware of the advanced-DMA chip is consequently also able to overlap two microinstructions. Further, by dividing the internal logic into autonomous units and providing four separate copies of channel-specific registers and control flip-flops, these overlapping microinstructions can deal with totally different channels.

Thus, channel switching imposes no performance penalty on the SAB 82258. The autonomous logic units simply act like time-sharing execution units—accepting inputs and producing appropriate output signals—without caring which channel they are serving.

However, to determine which channel should be processed first when two or more have to be serviced simultaneously, various priority levels may be attached to



3. Commander. Conditional branching lets the DMA controller execute a series of commands based on the value of condition bits. Alternatively, a single command block could be repetitively executed by using a jump instruction back to itself.

these otherwise equivalent channels. Besides a fixed-priority scheme, two different rotating-priority schemes are available, in which priority may rotate among four channels, or among three channels with channel 3 fixed. Yet another scheme combines fixed with rotating priorities—channels 0 and 1 having higher priority than channels 2 and 3, and priority within each pair alternating.

A matter of access

The SAB 82258 DMA controller splits its user-visible registers into a single set of five general-purpose registers and four sets of channel-specific registers (see table). The set of five, called the general registers, serves all the four channels. In using the controller, the mode register, which describes such aspects of the controller's environment as bus widths and priorities, is written first after reset. The general command register is used by the CPU to start and stop the DMA transfer on different channels. The general status register shows the status of each of the four channels, such as if the channel is running or if an interrupt is pending. The burst and delay registers specify the bus load permissible for the SAB 82258.

With its 24-bit-wide source pointers, destination pointers, and byte-count registers, the advanced-DMA controller can address the 80286's full 16-megabyte address space as well as transfer data blocks as big as 16 megabytes. A large block size is often needed for graphics applications.

The SAB 82258 does not directly support the protected virtual addressing mechanism of the 80286, which contains on-chip memory-management and -protection functions. Yet the protection is not hurt, since the 80286 has to program the DMA with real (physical) addresses for source, destination, and other pointers. These real addresses are generated as such through the protection mechanism of the 80286 and hence are checked against protection violation. Usually, an input/output utility routine is provided by the operating system to service the SAB 82258—no direct user access should be allowed to the advanced-DMA chip from lower privileged levels. The operating-system utility has the job of converting the virtual addresses into real addresses and then programming the SAB 82258.

Blocks and pointers

In such a system utility, programming the advanced-DMA controller is a matter of creating a command block in memory containing all relevant data (parameters) for DMA transfer. The command pointer in the controller is loaded with the base address of the command block. On getting a start-channel command from the CPU, the controller loads the contents of the command block into its registers and starts the DMA operation. After completing operation on a command block, it writes back the channel status in the command block in memory for use by the operating-system utility. Optionally, source-pointer, destination-pointer, and byte-count registers may also be written out to the command block.

It is possible to have command blocks in a chain. After completing one block, the SAB 82258 starts processing the next block automatically. This operation, called command chaining, allows the chip to execute a sequence of different types of DMAs autonomously. Besides standard DMA command blocks, there are special command blocks that execute unconditional and conditional branching (depending on the type of DMA termination) and (un)conditional stop (Fig. 3).

These channel commands, contained in the channel command block, are up to 22 bits wide. Two types of channel commands are possible—type 1, for data movement, and type 2, for command-chaining control.

Type 1 command bits contain information on:

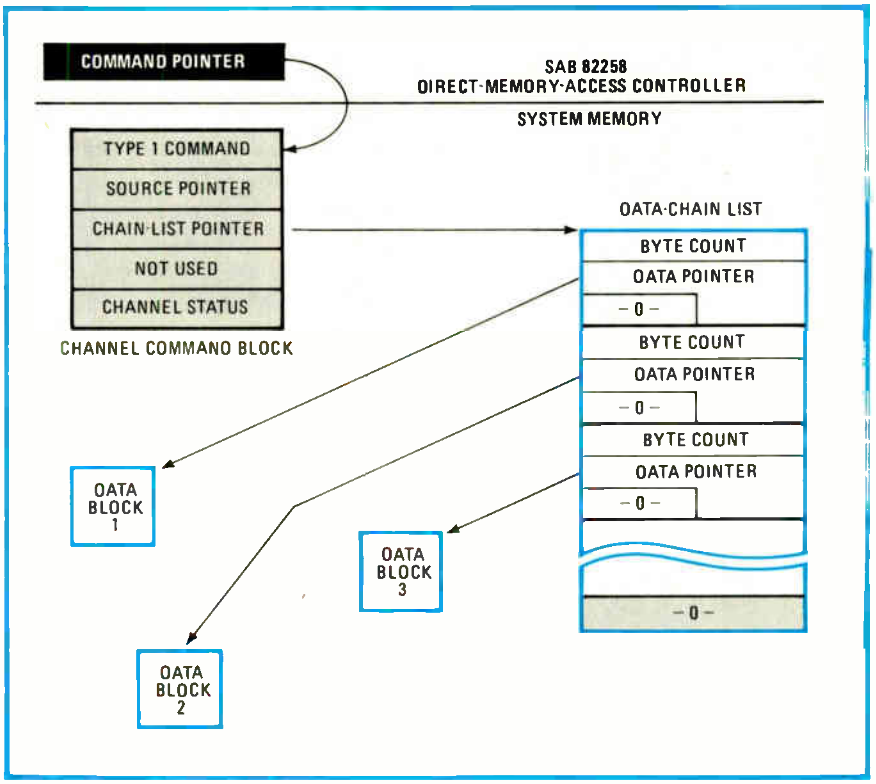
- The bus width of source and destination.
- Whether the source or destination address, or both, should be incremented, decremented, or kept constant during the transfer.
- Whether source or destination is in memory or I/O space (system or resident space in the remote mode).
- Whether data chaining (list or linked-list) is to be performed.
- Whether the data transfer is synchronized (source or destination) or free-running.
- Whether an on-the-fly match operation or translate operation has to be performed.
- Whether a verify operation has to be performed.

For certain type 1 transfers that, for example, do not use on-the-fly match, translate, or verify features, the command is only 16 bits wide and only a short command block is necessary.

Type 2 command blocks are 6 bytes long. Of these, the first 2 bytes form the command and the rest is either a relative displacement or an absolute address for the JUMP operation. The two basic type 2 commands—JUMP and STOP—may be conditional or nonconditional. The conditional case tests for either of the four condition bits that are altered at the termination of any DMA operation. These include termination due to the end of byte count, due to a successful mask compare operation, due to an external termination signal, or due to a verify operation resulting in a mismatch. Users are thus allowed to JUMP or STOP the further execution of commands based on any of these conditions and to optionally generate EOD or INTERRUPT signal.

Very often it is necessary to collect data from different data blocks and send the blocks out to a peripheral one after another. This can be done very efficiently by data chaining. Each block in a data chain is specified by a linked-list element consisting of a byte count, data pointer, and link pointer. As soon as the data from a block has been sent out to the destination, the next linked-list element addressed by the previous link pointer controls the next data block transfer.

This process continues until a 0 is encountered in the byte-count field. Thus data blocks can be included or removed or their sequence altered dynamically by manipulating the link pointers by means of the CPU. This feature can be used for serial–data-communications controllers, where different blocks represent different types of information like header, address, tail, and so on.



4. Pointed list. Requiring only 1 microsecond to access each new data block, the DMA chip can perform a specified operation on all the members of a list of data. The command block terminates when the controller finds a zero byte count somewhere down in the list.

Such linking of data blocks could also be implemented using command chaining, except that such chaining is much slower because the whole command block must be loaded before DMA can start.

Another form of data chaining—called list chaining, as opposed to the linked-list data chaining described above—is still faster (Fig. 4). In this case, there is only one list containing details on all the data blocks to be chained. This technique has the advantage of a very short latency of going from one data block to the next—on the order of 1 microsecond.

List chaining is preferred to linked-list chaining when the speed of going to the next block is of prime importance. Linked-list chaining offers greater flexibility, however. Data chaining makes it possible to gather data from various data blocks at one destination (source data chaining) and, conversely, to scatter data from one source to several data blocks (destination data chaining.)

Verify and save

Verifying the data read in from the peripheral—a commonly required function—is like a block-compare operation. A data block read in from a peripheral is compared byte for byte (or word for word) with a data block in the memory. The transfer can be halted if a mismatch occurs. It is very useful to compare the data on a disk sector with a memory block.

The verify and save mode of the SAB 82258 also supports a simultaneous data transfer (in a single-cycle mode) and verify. Each byte (or word) being transferred is read in by the SAB 82258 and compared with another byte or word fetched from the memory block.

Very often it is necessary to interface slow equipment like cathode-ray-tube terminals and line printers with computers. This can be easily done through a DMA channel to which the DMA controller can transfer a character or a block of characters as soon as it gets a request to do so. Since the slow equipment only rarely generates requests and since the timing of the response is also not so critical, it is more economical to multiplex several such slow devices onto one channel. And the controller's multiplexer channel, channel 3, can be programmed to serve just that function, supporting up to 32 peripheral devices.

32-line handler

The multiplexer network is implemented using SAB 8259A interrupt controllers in the master-slave mode. Upon receiving a request, the interrupt controller informs the DMA controller of it through the I/O request line. The DMA controller generates bus cycles similar to interrupt-acknowledge cycles, which read in the number of the subchannel that is requesting service (it is analogous to the vector numbers of interrupt controllers). On receiving the subchannel number, the controller executes a command block for that subchannel. Command chaining is permitted for the multiplexer channel, although data chaining is not.

Samples of the advanced-DMA controller will be available at the end of 1983, initially as the SAB 82257 only, without the multiplexer channel mode. The chip will be alternate-sourced by Intel Corp. □

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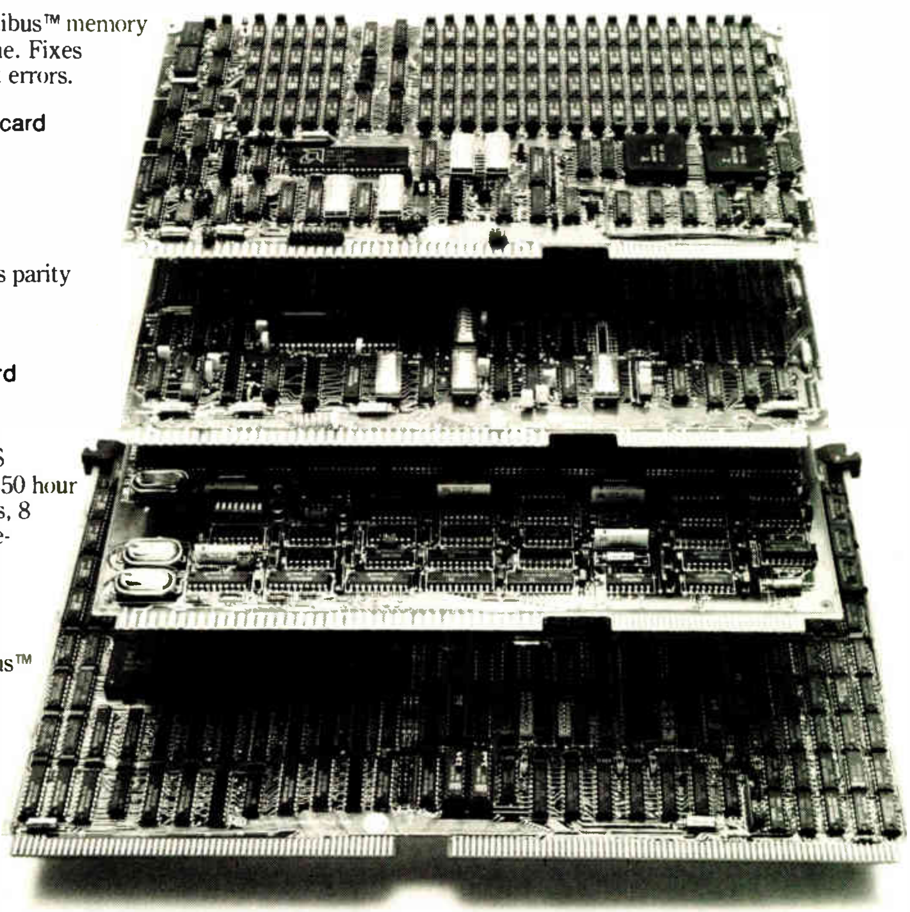

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Unix-based data base fits 16-bit systems

Multiple access methods boost performance in relational data-base management system

by Nicolas C. Nierenberg, *Unify Corp., Portland, Ore.*

☐ Scores of different brands of business "supermicrocomputers" are hitting the market. Based on the new generation of 16-bit microprocessor chips and using Bell Laboratories' Unix operating system, they magnify the need for both system and application software.

In particular, data-base–management systems will be essential both as a tool for end users and as a working foundation for program developers. One such system, called Unify, backs an innovative user interface with a unique high-performance architecture designed for just this new class of computers.

Software engineers who are creating programs for these machines are now faced with three choices. Programs can be adapted downward from large minicomputers running the Unix operating system, adapted upward from 8-bit personal computers running non-Unix software, or developed specifically for those computers running Unix. Since these business computers are based on 16/32-bit microprocessors, they have certain characteristics of both the 8-bit personal computer and also the 32-bit minicomputer.

On the face of it, therefore, drawing software from each environment is appealing. A closer look, though, indicates the disadvantages that such hybrid software may inherit from its 8- and 32-bit ancestors. Programs from the smaller systems will be deficient in such 16-bit system features as multiuser capability. On the other hand, software from the larger systems will be oversized for the smaller working environment of most 16-bit personal computers. Consequently, the best approach is to design software specifically for these machines.

In the case of the Unify data-base–management system, the design process had three primary objectives: Unify was to serve as a base for application development; it had to have rapid response and occupy as little system memory as possible; and it would have to be easily used by people who were not professional programmers.

Program support first

In its main function as a foundation for application development, Unify would be expected to interact with many end users through menus, screens, and reports—all of which would be designed once and then used repeatedly. In addition, a typical application program would require the support of high update rates, of the kind found in transaction systems for application programs written for insurance-claim processing, inventory control, accounting, and customer-contact and engineering-update tracking. The eventual end user of these applications should become aware of the existence of Unify only when performing an *ad hoc* query or when creating new screens or reports.

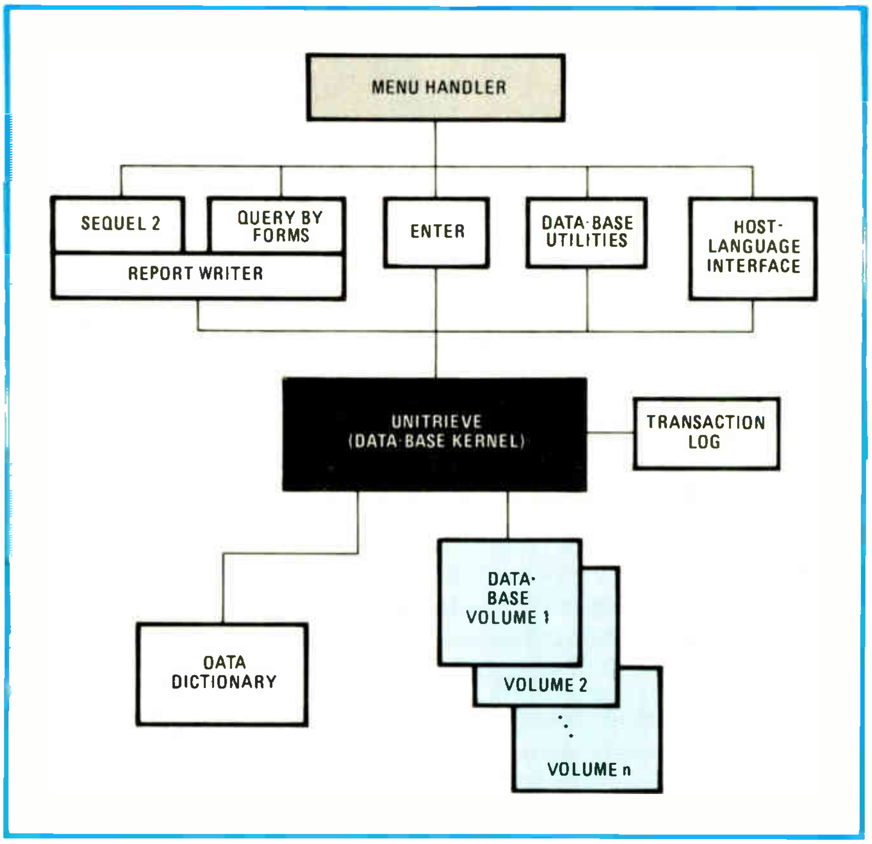
To provide this functional capability, the system would have to present a flexible user interface that could be modified to suit a particular application. Furthermore, to meet the demands of complex applications for sophisticated users and programmers, Unify would need powerful programming interfaces.

Of importance to applications that utilize a data-base management system is the latter's ability to respond interactively to users' queries, summarizing and distilling the information it has collected from the daily transac-

Data-base management unites with Unix operating system

Although operating systems like Bell Laboratories' Unix serve as an interface between application software and system hardware, they stop short of more conceptual levels of organization, such as providing a logical interface between the user and information stored in the system. Filling this gap, data-base–management systems help users organize and access data in meaningful ways, unlike operating-system file managers, which manipulate large amounts of data without regard to its information content.

With characteristics of both systems and application software, data-base–management systems are the keystone of large commercial data-processing systems. This third article in a series on the Unix operating system describes one company's approach to creating a high-performance data-base–management system within the Unix environment. —**Stephen Evanczuk**



1. At your service. In the Unify data-base–management system, user interaction passes through a menu handler (shaded), as well as directly through the host-language interface in application programs. The Unitrieve data-base kernel (black) manages the actual access that is made to the physical data-base volumes (tinted).

tions. For this reason, Unify had to provide powerful query capabilities aimed at both technical and nontechnical users.

Since few supermicrocomputers will be associated with a professional data-processing staff, various other people will be forced into the role of application developers. Besides their inexperience with data-base systems, many of these people will be neither able nor willing to write conventional programs. Consequently, the Unify tools for designing data-processing procedures must be as straightforward as possible. In fact, Unify should itself be a Unify application, so that it utilizes the same user interfaces as the final application. Users should be able to create various "obvious" parts of applications (such as menus, data-entry screens, reports, and updates) simply by configuring the various Unify utilities instead of having to develop conventional programs.

In transaction applications, the data-base–management system responds to external events, such as requests made by users in real time. In fact, it should respond at least as fast as do application programs written without a data-base–management system. More specifically, it should complete simple requests within 2 seconds, even with two or more users and with data files of more than 100,000 records.

Besides fast response time, a data-base–management system like Unify should not occupy more than 100 kilobytes of storage. Many of the new 16-bit personal computers are, after all, delivered with as little as 256-K bytes of system memory. In contrast, some earlier systems required at least 750 kilobytes to function in a single-user mode—and Unify is multiuser.

The third and last of the chief design goals—ease of use—dictated the adoption of the relational data-base model. Current implementations of such data bases have been plagued by performance problems, to such an extent that some designers have questioned whether the relational model is practical for transaction systems. As a result, the design of Unify extends current relational implementations and uses modifications where necessary to provide the required response time in a reasonable amount of memory.

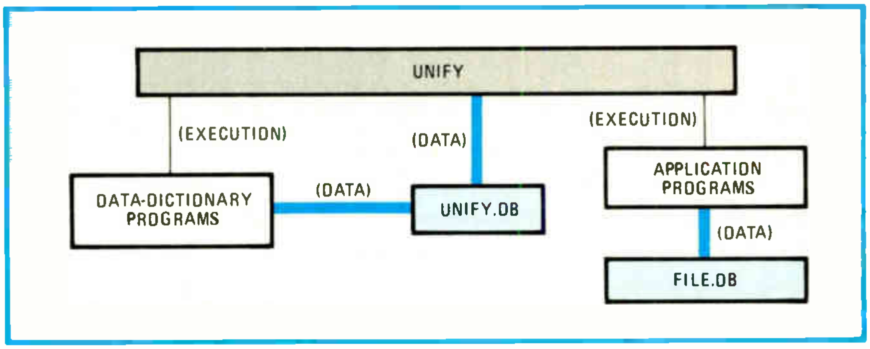
Over and above these performance problems of the conventional relational–data-base–management system model, the Unix operating system throws in its own stumbling blocks to efficient data-base management. For example, the Unix file system was not designed to be efficient with large files. In fact, the operating system often imposes two or three additional, or hidden, disk accesses in order to read a specific disk block. Since disk accesses are a critical aspect of data-base performance, this factor alone would have doubled response time unless Unify provided some alternative.

Unix lacks a general interprocess communication mechanism. This deficiency prevented the use of typical data-access optimization strategies, such as buffer pooling or reading disk blocks before they are actually needed. Overcoming these problems required innovative ways of working with Unix so that its many advantages would not be lost to applications needing high performance.

The solutions

Providing an environment powerful enough for the creation of complex applications, yet simple enough for nonprogrammers, is a challenge in any situation. Further constraining the system to 100 kilobytes of memory while maintaining rapid response adds another level of complexity to the design. Yet Unify (Fig. 1) meets these design objectives through a number of features, including a modular architecture, a menu handler, high-level query interfaces, a relational model, predefined relations, multiple on-line and programming access methods, reduced file overhead, and a run-time performance optimizer.

As one approach to satisfying the 100-kilobyte limit, Unify is segmented by function into a number of separately executable utility modules—data-dictionary update, data-base creation, data-base modification, and query (Fig. 2). This setup naturally means that data-base



2. Segments. Separate segments for individual functions in Unify allow the system to occupy only 100 kilobytes of system memory. Different segments handle data-dictionary update, data-base creation, data-base design modification, and query.

creation is not available from query but, given the assumptions listed above concerning Unify utilization, it is more than justified by the memory savings. This utility-program approach mirrors the implementation of the Unix system, which also prefers a few small interacting programs to having a single very large all-purpose utility.

A utility of particular importance to the data-base design process is Unify's menu handler. All the data-base utilities—such as data-base design maintenance, create data base, and reconfigure data base—may be selected by number or name. The menus are kept in the data dictionary and can be modified easily. The data dictionary also contains a matrix of each user's starting point in the menu hierarchy and the programs to which he or she has access. Each menu node also has associated on-line help documentation.

When Unify is first installed, the menus allow access to 28 programs. If the system were not menu-oriented, the user would be forced to memorize or look up numerous command sequences. Instead, the menus present the user with a simple list of options broken down by category. Once a utility is invoked, the user continues to interact in a structured full-screen mode. Designing a data base means just filling in the names and characteristics of tables and columns. Modifying a data-base design means just tabbing to the entry to be changed and replacing it. This style of interface reduces the knowledge needed to create and modify data structures.

Because menus may be modified and new functions easily added, menus also serve as the interface to application programs developed using Unify. All these programs can be registered with the menu handler and placed into an application hierarchy, with access assigned to each user according to individual need.

One important function supported by the menu system is Unify's high-level interface for data entry and query by forms. Using two Unify utilities, ENTER and SFORM, users create data-entry screens for Unify tables without programming. Because ENTER is fully integrated with the menu handler, forms users are limited to those combinations of update privileges (add, inquire, modify, or delete) specified by the system designer. Users can also employ these forms to query the data base by entering desired values into the fields on the screen.

Alternatively, Unify offers a Sequel query processor that is a substantial subset of the query and data-manipulation portion of IBM's Sequel language—an extremely powerful relational calculus that is the basis for IBM's relational data-base product, SQL/DS. Sequel is much more powerful and easier to use than relational algebras that employ separate select, project, and join operators. Results from either Sequel or ENTER queries can be passed to the Unify report processor, which creates formatted reports according to nonprocedural specifications provided by the user.

Relational model

Of course, it would be of little use to allow this type of easy access to the design tools if the data model itself were difficult to understand. For this reason, Unify employs the relational model, with its relatively simple structure, rather than more cumbersome network or hierarchical models.

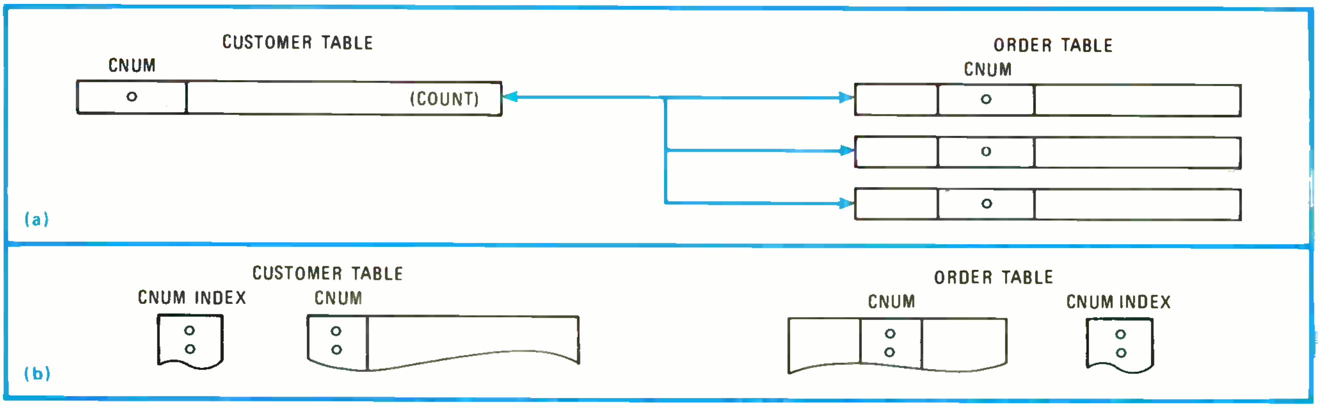
Unify extends the relational model in two important ways. First, it allows for the specification of a record key—a set of values unique to a table and contained in one or more columns of just one of its rows. Only one row in any table can contain a particular set of values in its key column(s). (Extra secondary keys can be specified, but these do not affect the data base's logical structure.) Second, Unify allows for the specification of links between tables. In a pure relational–data-base system, tables are laid out independently of one another and integrated only when a user specifies a join—a logical operation that combines information in the tables. With Unify's links, on the other hand, a user who knows that columns in two or more distinct tables are logically related can specify that relationship to the system.

For example, a value—a customer number—might appear as column entries in both customer and order tables. If, as in this case, the user knows that these columns in the separate tables are logically related, the columns can be tied together. The result is that only customer numbers that are stored in the customer table may be stored in the order table. Thus invalid data is kept out of the data base without its being necessary to carry out specific logic checks in each application program. Additionally, this "pre-join" greatly increases the speed of any subsequent join operations that involve these two columns.

Logical and physical links

The specification of links between tables has physical as well as logical ramifications. Unify uses this specification of the data-base structure to implement an access method that is unique among relational data bases. In this access method, relative row pointers reduce the number of disk accesses by a factor of two or three for some operations.

Figure 3a represents the pointers maintained by Unify when the user specifies a relationship between columns in two different tables. These pointers are completely trans-



3. Linked up. Unify lets user specify links between tables of data, as when a value in the customer table and order table are known by the user to be related (a). Conventional relational implementations maintain separate tables, as well as adding overhead for indexes into the tables.

parent to the user and are updated when the information in the columns is changed. One pointer runs from each row in the order table to the related row in the customer table. This pointer is used when the join sequence starts with the order table.

A second set of pointers begins in the customer table and brings together a list of related order rows. These pointers are used when the join sequence starts with the customer table. They are also used when selecting those order-table rows that contain a particular customer number. Associated with the pointer in the customer table is a count of the number of related order rows. This count is extremely useful in searches where several columns are specified, for it enables Unify to select the shortest possible search path.

For comparison purposes, the conventional approach is illustrated in Fig. 3b. Here two indexes (B trees, typically) are built—one for the cnum column in each table. This approach can be used with Unify by not specifying the link and by building two B trees. However, it uses at least twice the disk space of the pointers even in the best case (a 2-byte integer key). More importantly, it requires a B-tree search for each row of the join operation. The B-tree search can be up to 10 times slower in comparison with the use of pointers, when disk accesses and central-processing-unit utilization are taken into account.

Experiments have also shown that update of the links is only about 10% slower than update of the B trees. Join operations without either of these two approaches—using linear search—would be prohibitively slow. Consequently, the links are viewed not as more overhead but as a tradeoff with indexes.

Access methods

Equally important to Unify's link access method is the way Unify selects the most efficient of its three access methods—key, link, or B tree—for a given retrieval. This optimization is dynamic and can vary from search to search on the same data base.

Unify performs this optimization by evaluating the columns specified and the access methods available, based on a defined set of criteria. Scores are assigned and the best approach is accepted. The choices are listed in order from best to worst:

- An exact match on each one of the columns that make up the primary key of the table (hashing.)
- An exact match on a column that is in a pre-specified relationship. If several columns fit, then the one with the shortest list is chosen. (If the list is long relative to the number of rows in the table, then this may not be chosen if any of the three following choices appears to be better.)
- An exact match on a B-tree column.
- A numeric range on a B-tree column.
- An inexact match on a B-tree column where the first characters are specified.

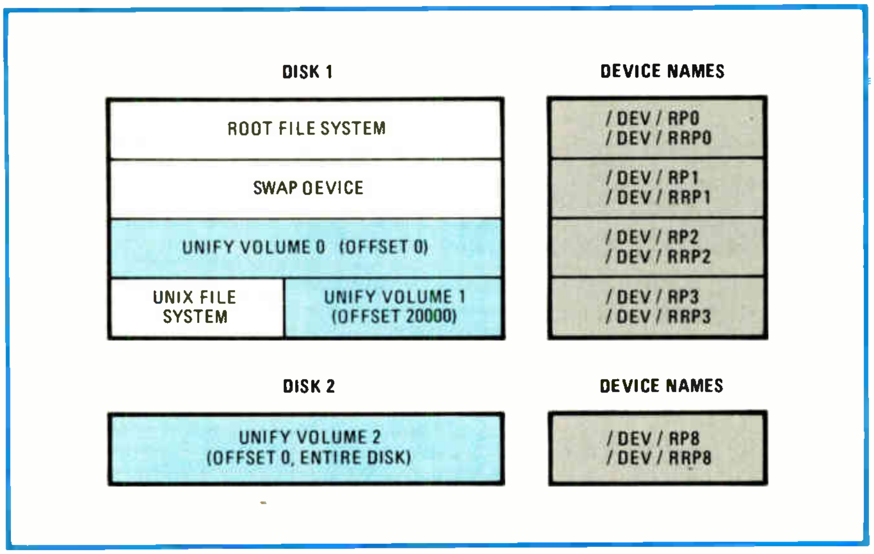
As an interesting note, a single column may have more than one access method applied to it, depending on the search criteria. For example, the primary key of record is always hashed, but the user may also build a B tree on it. If the key is specified precisely, then the hash method will be used, but otherwise the B tree will be utilized.

Because the Unify kernel itself performs these optimizations, they are independent of the way the query is written. Thus a Sequel query may operate in a completely different way, depending on how the physical access methods are configured or how the data base is loaded. The only difference perceived by the user is the length of time the system takes to respond.

Software developers building complex applications can select whatever level of access they desire through Unify's multilevel programming interface. At the highest level, the programmer is kept completely independent of the access methods used to fulfill the request. At the lowest level, the programmer may specify not only the access methods to be used but also how they are to be used.

UNISEL, the highest-level routine, optimally searches tables on the basis of criteria specified for various columns in the table. The programmer is free to mix criteria, such as exact, greater than, less than, ranges, and string-pattern matches. In addition, he or she can specify that the contents of a column must match the key of another table previously selected. If more complex computational or algorithmic tests are needed to complete a selection, UNISEL also allows for the specification of a user-written subroutine to perform the other tests.

UNISEL takes these inputs and selects an optimal



4. Speaking volumes. When, for example, Unify data volumes are laid out over two physical disk drives, the data base starts on the first disk and continues on the second. If this structure is not desired, the data base can reside in a single Unix file.

search strategy based on the physical access methods available. The rows that pass the criteria are returned in a specified sequence for processing by the program.

In cases where the programmers wish to direct the operation more precisely, they can access the B trees, hash keys, and links directly. Of course, programs using this option will be affected by changes in the physical configuration of the data base.

Once the desired rows have been selected, Unify allows the programmer to read and write them at the column level. To a considerable extent, this technique insulates programs from changes to the logical structure of the data base, as opposed to other techniques that require the entire record to be read or written. In addition, this low-level access capability greatly reduces the buffer space needed for data input/output operations.

At the system level, one of the Unix system's limitations *vis-à-vis* data-base management is its file system. Although work has been done recently to remedy this weakness, much block scattering and indirection (multiple physical reads for one logical read) still occur on large files. In addition, Unix has a tendency under some circumstances to allow files to be contaminated. For these reasons, Unify uses a specially designed file system, which can (at the user's discretion) run on portions of the disk outside conventional Unix file-system space. Tests have shown that this technique improves Unify's performance by over 40% compared with the standard Unix file-management scheme.

Figure 4 illustrates how the Unify file system is laid out on disk. In this case, the data base begins with two volumes on portions of the first disk and continues with the entire second disk. Up to eight disk extensions can be specified. These specifications are optional—without them, Unify resides in a single Unix file.

Within the Unify volumes, the rows of the tables are arranged as arrays within large segments. The block offset of each segment is kept in memory, so that, if the row number, the number of rows per segment, and the row length are known, a row can be read with one disk access. Additionally, since rows are stored contiguously, a great many of them can be read in a single disk request. Using this technique, sequential search speeds of 700 records a second have been observed.

In the conventional approach, each table is a separate Unix file within an ordinary Unix file system. Using this technique, most Unix systems restrict the size of the data base to a single Unix file system. Also, they lack control over block placement, so that the disk head travels excessively even on sequential access. Finally, the Unix file system imposes an average overhead of two disk accesses, in addition to any indirection imposed by the data-base system itself.

An extra benefit of using raw disk files is the speed at which backup and recovery can be done. Unify utilities perform these operations using multisectored raw I/O at a fraction of the time needed by other systems.

Rapid row replacement

To provide the response time needed for multiuser on-line operations, Unify stresses run-time performance in other areas besides disk organization—in certain cases even at the expense of data compaction and dynamic change. The two key areas are fixed versus variable physical row lengths and dynamic reconfiguration.

Unify uses fixed physical row lengths both for direct computed access to rows (as discussed above) and for improved free-space recovery. With fixed row lengths, a newly inserted row can always take the place of a previously deleted one. In systems where row length is not guaranteed to be a certain size, all the rows in an arbitrary area, or page, must be deleted before the space can be reused. Since an entire page is rarely freed at random in reasonably stable data bases, compression runs are inevitably needed to reclaim space available on partially deleted pages. Consequently, direct row access and elimination of compression runs more than make up for the extra space needed for fixed-length rows.

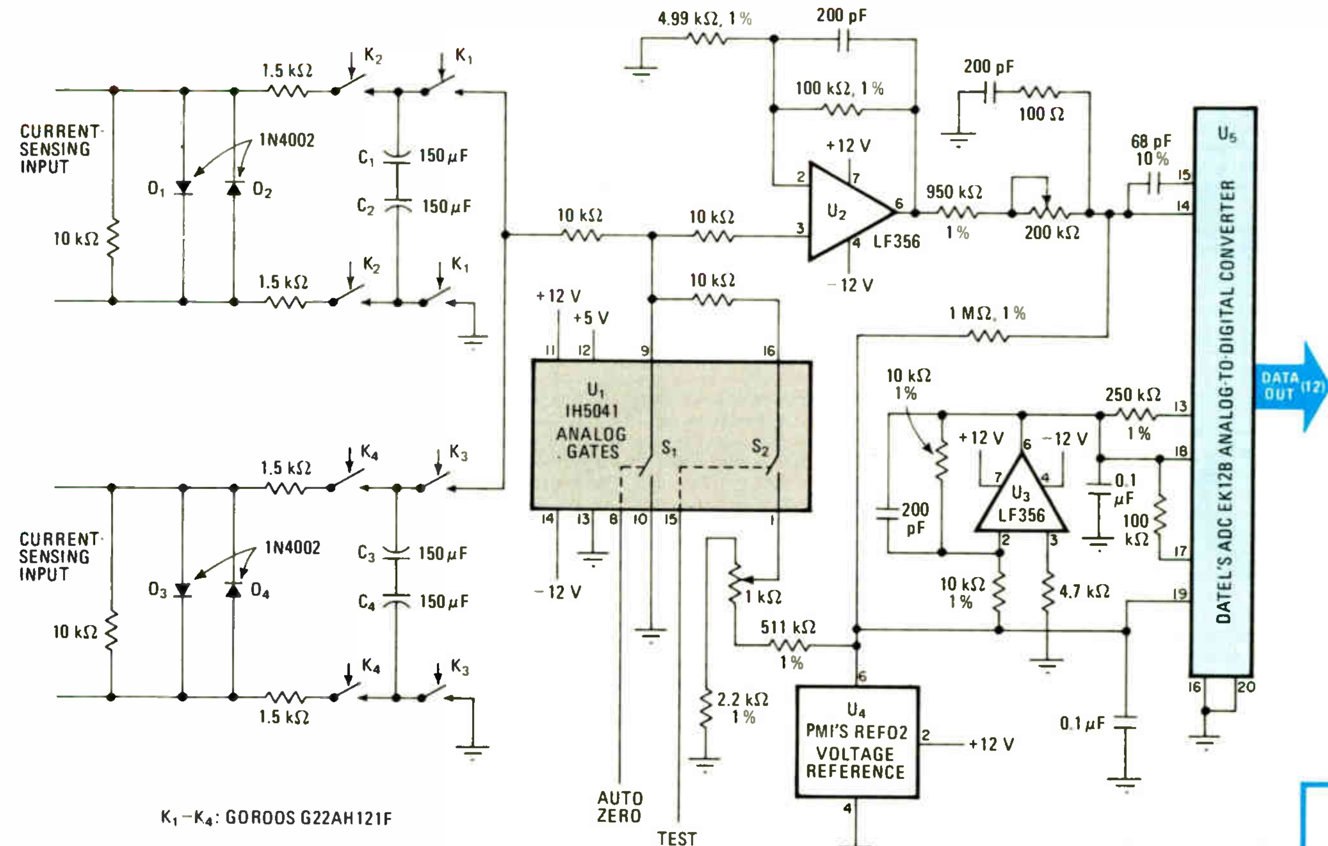
Some data-base–management systems are also able to add tables and columns dynamically. Unify, on the other hand, requires a reconfiguration process to accomplish this. Although the ability to modify the logical data structures dynamically may be desirable, its benefits are outweighed by the penalties associated with it. For instance, since such data-base–management systems scatter data over the disk, they require the user to execute a lengthy process—the performance maintenance run, which reorganizes the data—in order to avoid performance degradation. During the life of a typical application, this requirement takes the system off line frequently, whereas Unify requires no maintenance runs to avoid performance degradation. □

8039 monitors motor's operating conditions

by Steven Woelfle
Analog Precision, Tucson, Ariz.
and M. N. Szilagyi
Department of Electrical Engineering, University of Arizona, Tucson, Ariz.

Down in the mines, trucks and trains get stuck in the mud—and when that happens to vehicles with electric wheel motors, high current is drawn because the wheels cannot move. The excessive heat generated by the high current causes burnout, so these motors must have wheel-motion sensing to prevent it. The 8039 microprocessor circuit monitors operating conditions and warns of faulty parameters, thus alleviating the problem.

A shunt-and-isolation network—diodes D_1–D_4, relays K_1–K_4, and capacitors C_1–C_4—achieves the input-current sensing. At first, to permit the capacitors to charge to the shunt value, relays K_2 and K_4 are closed. They are then opened, and relays K_1 and K_3 are closed to present the input voltage to analog-to-digital converter U_5. Before reaching U_5, this voltage passes through operational amplifier U_2 and solid-state switch U_1. U_5 is designed to



(a)

Resistor gives high gain to Sallen-Key lowpass filter

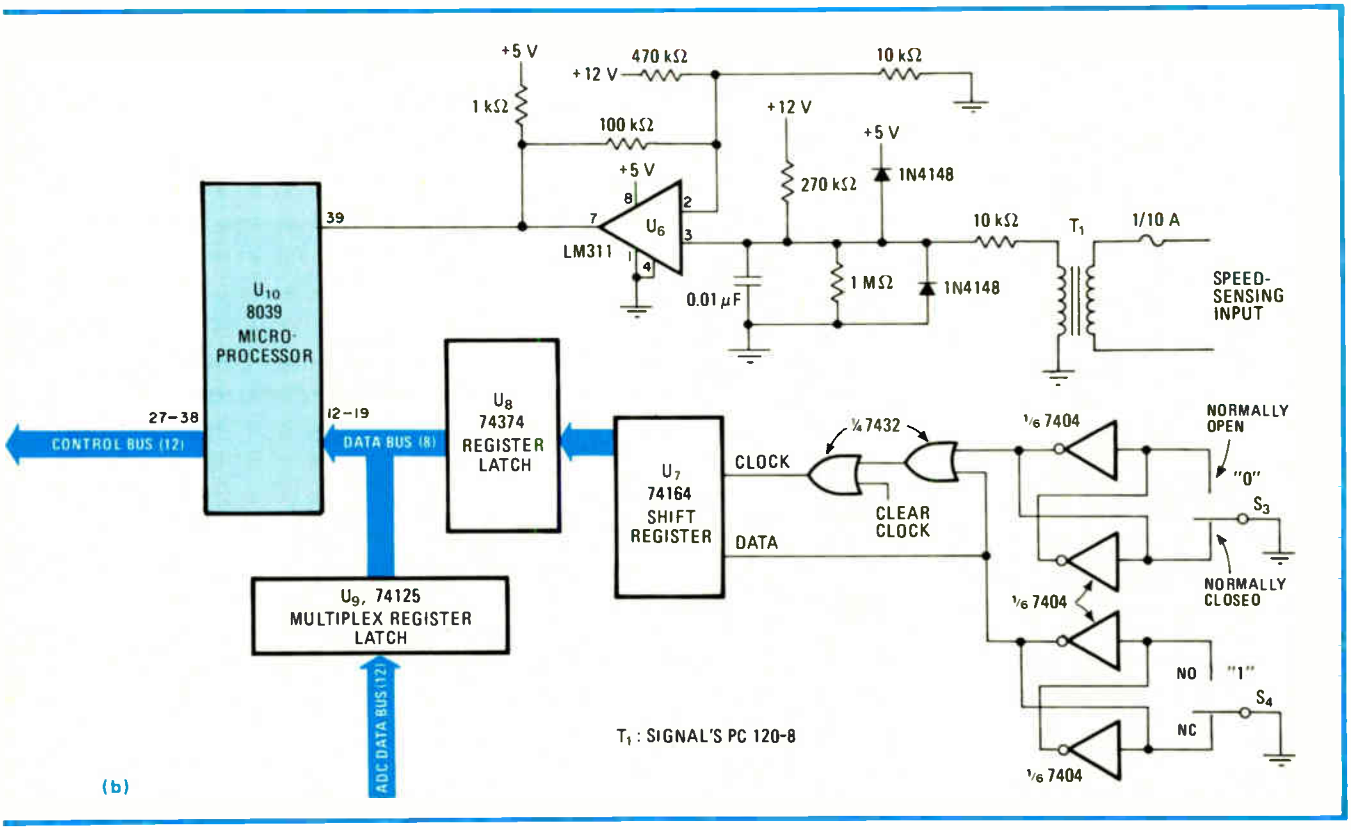
by Ralph A. Giffone
New England Research Laboratory, ADT, Cambridge, Mass.

Because the Sallen-Key low-pass active-filter circuit has a maximum gain of only 3, an extra amplifier must be provided to get a high-gain response from this circuit, shown in (a) on page 135. Typically, the gain is between 1 and 2.5. This design, however, acquires more gain from the Sallen-Key circuit by introducing an additional feedback element into the standard configuration. And it does so without altering the desired frequency response convert both positive voltages and negative voltages, thereby allowing polarity insensitivity at the current-sensing inputs.

To compensate for the op amp's thermal drift, the circuit uses an auto-zeroing technique. It closes analog gate S_1, feeds op amp U_2 with a digital sample of zero input, and subtracts it from the shunt value sample. The microprocessor then provides a difference value free of thermal drift. S_2 permits circuit calibration by connecting a fixed reference voltage to a-d converter U_5.

A magnetic pickup senses the wheel's motion, which is supplied to the monitor circuit through isolation transformer T_1 (b). The magnetic pickup produces a sinusoidal voltage whose amplitude and frequency are proportional to the speed. This signal is then clipped to meet the input requirements of comparator U_6, which converts it into TTL logic levels.

For easy integration of current on any pair of rotor contacts—needed to spot failure conditions—U_{10} samples the current and motion-sensing data at a rate of 1 Hz. The control data at the CPU's output directs two additional relays. One warns the operator about undesirable conditions, while the other shuts off the generator in the event of hazardous conditions. The electronic key—switches S_3 and S_4—permits the machine to be inspected before operation resumes. □



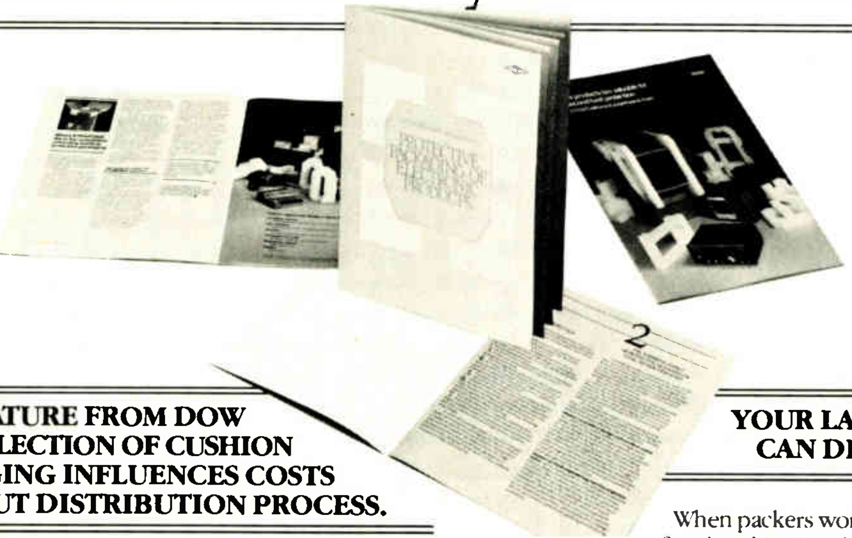
Monitor. This microprocessor-based monitor circuit automatically shuts off the generator of a mine truck or train when its rotor contacts draw excessive current. The circuit (a) senses the current and feeds it to analog-to-digital converter U_5, whose output is sampled by the central processing unit U_{10}. A magnetic pickup senses the wheel's motion and feeds it to the processor through T_1 and U_6 (b). Undesirable conditions cause the control bus output to shut down the generator.

and without adding another active component. Only one extra resistor is needed to boost the filter's gain.

With the addition of resistor R_3 to the Sallen-Key circuit, the new low-pass filter (b) provides a gain $K_f = V_A/V_i = 1+R_2/R_1$ in the passband. The overall amplifier gain, which has an influence on the filter gain in the passband, is given by $K_a = (R_1+R_2+R_3)/R_1$, and its transfer function, $V_o/V_i = K_a/(s^2/w^2+2\zeta s/w+1)$ where $w = 1/RC$ and $\zeta = (3-K_f)/2$, is the damping ratio. Only the gain-bandwidth limitation of operational amplifier U_1 limits the gain. For the component values that shown here, the filter's 3-decibel cut-off frequency works out at 18 kilohertz, while its overall gain is measured to be 11.7.

Impedance Z_a, looking into the operational amplifier at reference terminal A, is about $K_f R_3/A$, where A is

If your damage rates are near zero, your distribution costs may be needlessly high.



NEW LITERATURE FROM DOW SHOWS HOW SELECTION OF CUSHION PACKAGING INFLUENCES COSTS THROUGHOUT DISTRIBUTION PROCESS.

When packaging fragile, high-value electronic products, any cushioning material that keeps damage low is usually considered cost-effective.

What's often overlooked, though, is that the protection can cost more than the damage it prevents.

Packagers of electronic products are discovering that it is indeed possible to achieve adequate protection while reducing distribution costs.

They've learned it is more cost-effective to select cushioning materials on the basis of *efficiency,* rather than depending on sheer bulk for cushioning performance. The result is not only better product protection, but a chain-reaction of savings from one end of the distribution process to the other.

MATERIAL COSTS MAY DROP BECAUSE YOU USE LESS CUSHIONING FOR EQUAL OR BETTER PROTECTION.

High-efficiency cushioning products such as ETHAFOAM* brand polyethylene foam usually allow the use of considerably less material. You not only save on the amount of cushioning, you're often able to use lighter, smaller, less expensive cartons. You may also be able to dispense with additional taping, blocking and strapping, further lowering your material costs.

AS CARTON SIZE SHRINKS, SO DO SHIPPING COSTS. BUT PAYLOAD GOES UP.

Perhaps the biggest benefit of an efficient cushioning material like ETHAFOAM is its ability to improve the dimensional weight of the package. It's not unusual for shippers who switch to a more efficient material to achieve significant dimensional weight improvements which translate directly into significant shipping savings. Especially with air freight.

YOUR LABOR COSTS CAN DROP, TOO.

When packers work with ready-made, form-fitted cushioning devices, there's little guesswork when assembling the package. And no special training is required. Packers can complete packages quickly and correctly every time. So labor costs should drop while productivity stays up.

NO NEED FOR EXPENSIVE EQUIPMENT.

Because your fabricator supplies the finished cushion packaging pieces that are ready for use immediately, you avoid the cost of fabrication equipment and labor when manufacturing cushioning pads on site. You're also spared the costs of maintenance, downtime, structural alterations, and ventilation systems associated with such equipment.

CUSHION PACKAGING THAT CAN BE REUSED KEEPS RIGHT ON SAVING YOU MONEY.

Cushioning products, like ETHAFOAM, that are resilient and relatively unaffected by temperature, moisture, and chemical attack can be reused. Many packagers insist that returned products be shipped in the original custom-fabricated cushions...so the product is protected and packaging expense is further reduced.

FOR A MORE THOROUGH LOOK AT HOW CUSHION PACKAGING INFLUENCES DISTRIBUTION COSTS...

You and your Packaging Supervisor may benefit from the wealth of information published by Dow including a factual report entitled "A General Management Guide to Protective Packaging of Electronic Products" and case history reports from six leading electronics firms who are profiting in many ways from the use of ETHAFOAM plastic foam. For your free copies simply contact Dow Chemical U.S.A., Inquiry Services, P.O. Box 1206, Midland, MI 48640, or circle the number below on the reader service card.

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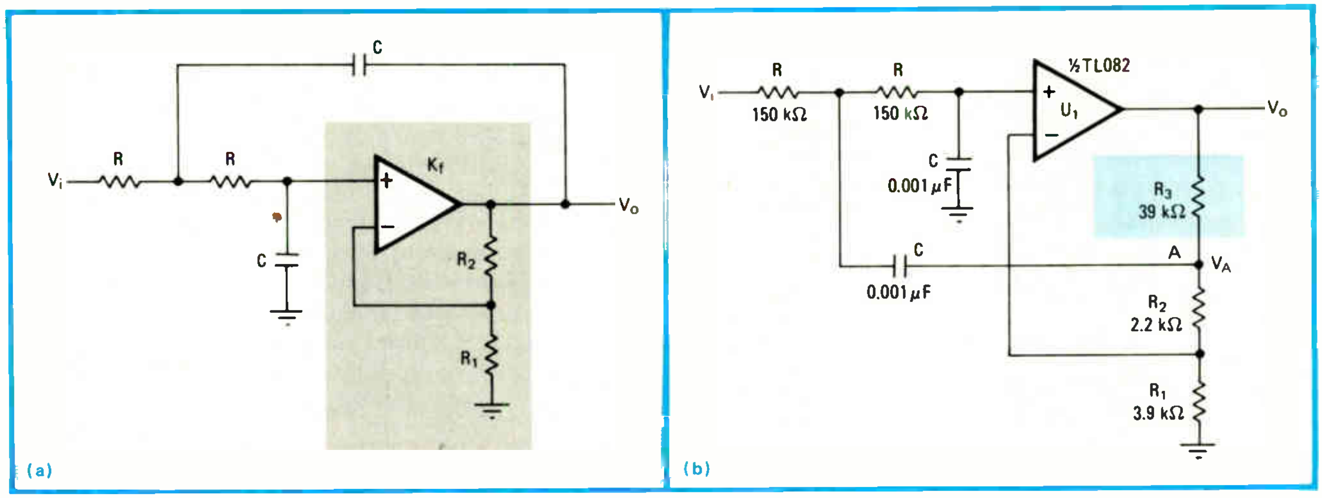


High gain. To get more gain from the filter, without altering its frequency response, this design modifies the fundamental Sallen-Key low-pass filter configuration (a). The new low-pass filter (b) needs only one additional resistor R_3 to add gain to the Sallen-Key circuit. Using the components shown, the filter provides a gain of 11.7, with a 3-dB cutoff at 1.18 kHz.

U_1's open-loop gain. For the filter to be accurate to within a few percentage points, the impedance of capacitor C must be a good deal greater than Z_a at the frequencies of interest.

Another version of the Sallen-Key circuit uses $K_f = 1$ and adjusts the ratio of the capacitors to obtain the desired damping ratio. This version can be realized, with high overall circuit gain, by setting $R_2 = 0$. □

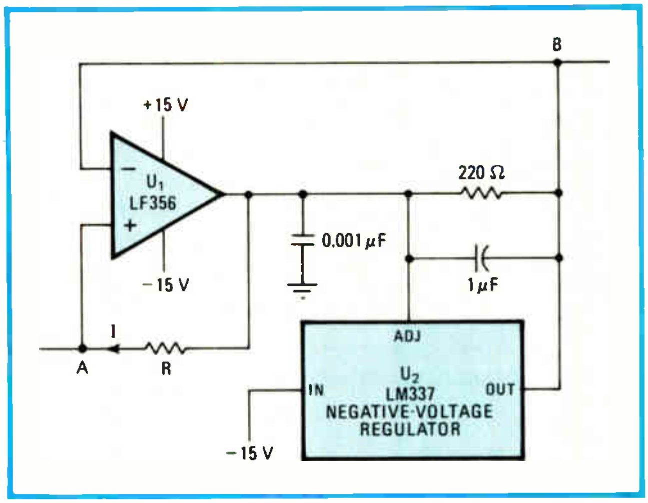
Accurate constant-current source can be adjusted

by Donald Scarl
Polytechnic Institute of New York, Farmingdale, N. Y.

This constant current source, which combines a three-terminal voltage regulator with an operational amplifier, is useful for making precise measurements of components like thermistors and resistance-temperature detectors. It quite accurately furnishes 1 nanoampere to 10 milliamperes of constant current, which flows through an external resistor whose voltage is then available with relatively low output impedance. As a result, the resistor can be measured accurately. Over a voltage range of 0 to 10 volts the current is constant to within 100 parts per million, and the current temperature coefficient is 100 ppm per degree Kelvin.

The three-terminal negative voltage regulator U_2 produces a constant 1.25 V between its adjustment and output terminals (see figure). This voltage makes the inverting input of operational amplifier U_1 1.25 V more negative than its output terminal. U_1's output, in turn, forces the voltage at its noninverting input to equal the voltage at its inverting input, within the 1-millivolt offset voltage, thus ensuring that 1.25 V appears across precision resistor R. Therefore, a current $I = 1.25/R$ flows out of terminal A, and the voltage at point B equals the voltage at point A.

A current of 5 mA, generated at the amplifier's output, flows through the 220-ohm resistor and into the voltage



Current source. Using a three-terminal negative voltage regulator and an operational amplifier, this circuit provides a constant current source with an accuracy of 100 parts per million. The current is determined by the relation $I = 1.25/R$ ampere, where R is in ohms. For the circuit shown, the current range is between 1 nA and 10 mA.

regulator's output. Since only 1 mA is required to keep U_2 active, 4 mA are available at point B to drive external circuitry. The voltage compliance, 0 to 10 V, is determined by the operational amplifier's maximum output, which is +12 V.

A complementary version of this circuit—a version that would use a positive regulator—is built using similar ideas. □

Electronics invites readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose and send to Ashok Bindra, Circuit Design Editor. We'll pay $75 for each item published.

Silicon-gate C-MOS chips gain immunity to SCR latchup

Improved processing deprives parasitic silicon controlled rectifiers of the current that unleashes their destructive tendencies

by Larry Wakeman
National Semiconductor Corp., Santa Clara, Calif.

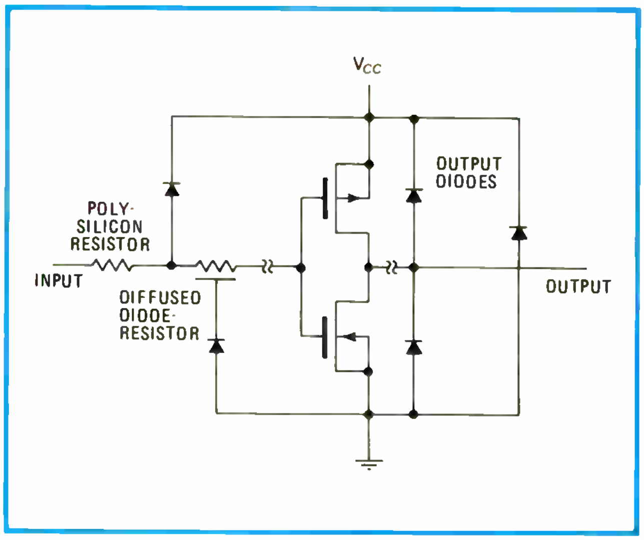
☐ Silicon-gate complementary-MOS integrated circuits, noted for achieving higher speeds than conventional metal-gate C-MOS ICs, can now boast of immunity to SCR latchup. This self-destructive mode is caused by parasitic silicon controlled rectifiers that are triggered by transients on signal lines or an out-of-bounds operating voltage. But in a new line of silicon-gate C-MOS circuits, the parasitic SCRs are so weak that they cannot be triggered in worst-case operating tests.

The new MM54HC and MM74HC high-speed C-MOS logic series have been immunized against SCR latchup by a combination of process and layout upgrades that will solve the problem in future chips as well. As C-MOS transistors become smaller, faster, and more tightly packed, the parasitic SCRs also shrink. They could become more susceptible to high-speed transients on external connections and to current generated internally by parasitic capacitors. The upgrades that now stop external triggering and self-triggering are also expected to prevent them in future scaled-down designs.

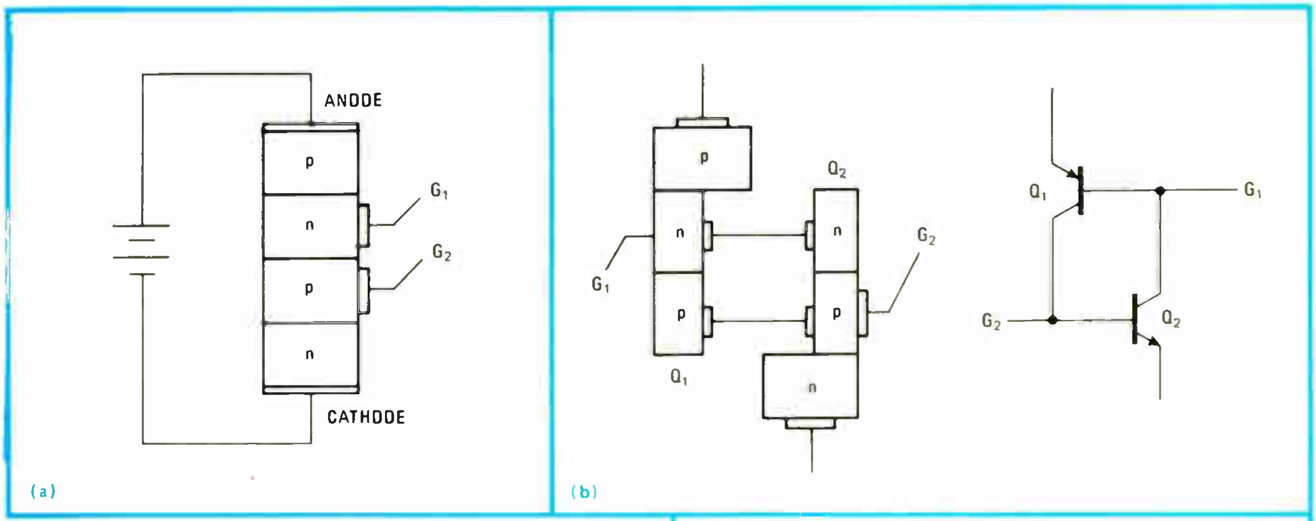
Starving the SCR

Tests show that the upgrades eliminate both dynamic and static triggering—the first resulting from high-speed pulses and transients, the latter from slower variations in operating voltages and the accompanying trigger currents. In effect, the parasitic SCR becomes so starved for current that it cannot turn on. Moreover, it starves itself—current that might otherwise trigger latchup is returned directly to the power supply or ground—a cure that should work at future densities and switching speeds as well.

It is safe to say that these C-MOS circuits require no more protection from SCR latchup than do the TTL circuits they replace. That is, they can survive on their own when used in low-power logic and memory systems, instead of depending on other circuits to limit currents and stabilize signal and supply voltages. Without such protection in high-power applications, however, a conventional



1. Extra protection. A C-MOS circuit's I/O protection diodes become forward-biased if the I/O voltages go higher or lower than the supply. A new process prevents this condition from triggering the parasitic SCRs in the substrate below the complementary transistors.



C-MOS circuit is likely to latch up, thereby shorting the power supply, burning itself out, or at least causing logic malfunctions.

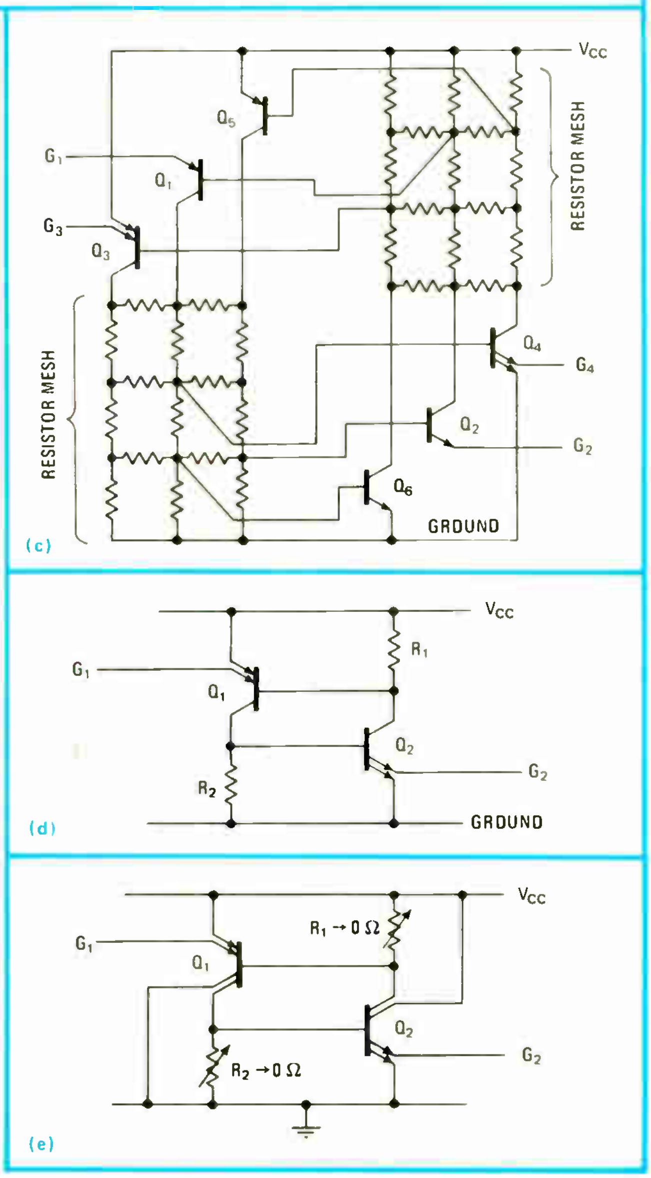
The MM54/74HC circuits are low-power counterparts of standard 5400/7400 TTL circuits. They are fabricated in a high-speed, silicon-gate C-MOS technology that increases the frequency response of parasitic SCRs in the silicon substrate. Along with other design changes, this increased frequency response could make high-speed C-MOS parts more susceptible to high-speed transients on signal lines, unless SCR latchup is prevented.

Transients, whether fast or slow, are usually blamed for SCR latchup, but the blame really belongs to the complex parasitic circuits created by the many complementary diffusions that appear in the bulk silicon during normal circuit operation. They operate between the collector supply voltage, V_{cc}, and ground in TTL-compatible C-MOS (or between the source supply voltage, V_{ss}, and the drain supply voltage, V_{dd}, in conventional CD4000 C-MOS). They are a problem only if allowed to latch up and become a short circuit between the supply pins.

The problem is called SCR latchup because the parasitic circuits behave like the thyristors (pnpn diodes) of real, controllable silicon controlled rectifiers. Such devices conduct power when a triggering current is applied to an SCR gate terminal or when the anode-to-cathode voltage is increased until triggering current flows through the thyristor. C-MOS parasitic SCRs are similarly activated—but, being uncontrolled, may not turn off until the circuit blows out like a fuse.

Metal-gate C-MOS devices, such as MM54C/74C ICs, are most commonly latched up by an input or output voltage greater than V_{cc} or less than ground (CD4000 parts by voltages greater than V_{dd} or less than V_{ss}). Whether caused by signal or supply variations, such voltages forward-bias the input or output protection diodes that are on the C-MOS chip. If the diodes also conduct sufficient current to trigger the parasitic SCR, latchup occurs.

Silicon-gate C-MOS circuits generally have inputs protected by polysilicon resistors that limit currents (Fig. 1). Unfortunately, an output resistor would degrade the drive current needed for high-speed operation, so the



2. Equivalent circuits. A real silicon controlled rectifier's thyristor (a) is equivalent to cross-coupled bipolar transistors (b). A C-MOS parasitic SCR behaves like a complex thyristor (c), but it contains parasitic resistances (d) that must be minimized to prevent latchup (e).

circuits have only diodes for output protection. Also, because high-speed parts like the 54/74 series operate in faster systems, they are exposed to more line-signal ringing, power-supply transients, and industrial or automotive noise. Such transients are not only more prevalent in high-speed systems but are more likely to come within the frequency-response range of the smaller, faster parasitic SCRs in these circuits.

A supply voltage high enough to break down diodes within the chip may also cause latchup in combination with input or output current—or, if large enough, by itself. Raising the supply voltage is comparable to raising a thyristor's anode voltage. Silicon-gate C-MOS parts do not break down often, because their typical breakdown voltage is above 10 volts, or more than twice the nominal V_{cc} voltage of 5 V. The specified worst-case limit is usually 7 V at maximum operating temperature.

Not that SCR latchup has destroyed many C-MOS circuits lately, because system designers usually take pains to prevent triggering by adding protection circuitry. For example, a designer may protect a low-power memory system by stabilizing the power supply, decoupling supply noise, and clamping both ends of the bus lines to supply and ground rails with Schottky, zener, or germanium diodes. Some designers prefer diode-resistor networks, and some develop special circuits to stop transients from entering C-MOS systems.

However, C-MOS systems would be more reliable and easier to design with if they needed no more protection than a TTL system does. There is also the future to consider. Protective circuits will become less and less effective with increases in parasitic-SCR density and speed. It is up to the chip designer to make sure that neither internal nor external current sources can trigger today's high-speed C-MOS parts or the very high-density parts of the future.

Blame the complementary parasites

Surer cures than diode and resistor networks become apparent when equivalent transistor circuits are examined. The real thyristor is normally biased in a forward-blocking state, ready for triggering through a gate (Fig. 2a). The equivalent circuit is a feedback circuit triggered by a current applied to either gate (Fig. 2b). Its complementary pnp and npn bipolar transistors produce collector currents equal to the current gain (B) times their base currents and feed these currents into each other's bases. If the circuit's current-gain product ($B_1 \times B_2$) exceeds 1, the feedback is regenerative and the circuit can latch up.

If any gate or emitter sees enough current to sustain feedback, the transistors will saturate and remain on after the gate current is removed. This feedback must be prevented in C-MOS circuits because the power supply can provide enough sustaining current to burn up the circuit.

A C-MOS parasitic SCR's equivalent circuit is similar in principle to that of a true SCR. Any C-MOS diffusion can become part of a parasitic SCR, and all these parts are interconnected by the bulk silicon's resistance (represented by the resistor mesh in Fig. 2c). When the parasitic SCR is triggered, a small part of the structure may latch up and carry current, causing localized heating and increased current flow. Then, the latching action may spread through the intertwined structure until the whole chip is in jeopardy.

The parasitic SCR model also indicates the variety of equivalent transistors involved. Q_1 and Q_2 represent transistors formed by input-protection diodes. Q_3 and Q_4 are output-transistor diffusions (the second emitter of each corresponds to a bonding-pad connection). Q_5 and Q_6 are parasitic elements associated with p- and n-channel MOS transistors but not connected directly to pins. G_1 through G_4 are external voltage nodes that can gate the SCR. Since the SCR is in the bulk silicon, "external" usually means the protection diodes in Fig. 1 or other elements on the chip surface that may carry trigger current.

A complete model would include a variety of parasitic capacitances. Circuit-switching operations change junction-depletion capacitances, generating small currents that also contribute to latchup (these are the parasitics that could cause self-triggering in very high-density designs). A full equivalent circuit would be a mind-boggling three-dimensional structure with more components than a large-scale IC.

However, a simple two-transistor model of the parasitic SCR circuit can still show how to prevent latchup (Fig. 2d). Because of the multiple diffusions in the C-MOS circuit, transistors Q_1 and Q_2 have multiple emitters, and any emitter can turn on the SCR. The circuit is triggered by raising G_1 high enough above V_{cc} to turn on Q_1 or by dropping G_2 enough below ground to turn on Q_2 (as with the diodes in Fig. 1). But now resistors R_1 and R_2 represent troublesome substrate resistances. Since they are part of the problem, they must be accounted for in the solution, which lies in process changes.

Special C-MOS devices comparable to this latchup-prone model were fabricated and tested before the upgrades were designed to determine what made SCR latchup more likely in high-speed silicon-gate designs. From the trigger-current measurements, it is clear that high-temperature environments—or localized chip heating—multiplies the hazard (Fig. 3a). Also, the high-frequency pulse trains common in logic and memory systems are at least as big a threat as the relatively large but infrequent transient pulses (Fig. 3b).

Obviously, susceptibility to latchup can be reduced by processing techniques that reduce parasitic transistor gains. However, unless the process is carefully engineered, such techniques can degrade the performance of the real circuit's transistors without eliminating SCR latchup. Chip designers are now focusing on the parasitic resistances that develop the circuit's operating currents. Current is not injected directly into a parasitic transistor base but into one of the many emitters. Latchup comes when parasitic resistances develop the voltages that turn on the parasitic transistors.

Suppose the voltage at gate 1 in Fig. 2d is higher than V_{cc}. It causes transistor Q_1's collector current to feed both the base of Q_2 and resistor R_2. Since R_2 steals base current from Q_2, it causes a voltage to appear at Q_2's base. Once this voltage reaches a threshold (typically 0.6 V), Q_2 turns on and feeds current from its collector back into R_1 and Q_1. If this current generates at least 0.6 V across R_1, Q_2 turns on even more. Conversely, if the voltage at G_2 (an output diode) drops below ground, a similar feedback process begins at Q_2.

With the knowledge gained from the test devices, the SCR-stifling approach modeled in Fig. 2e was pursued in the 54/74HC design. Dummy collectors—the second collector on each transistor—shunt input and output currents around the transistors and collect internal currents to V_{cc} or ground. Any current not collected will flow through R_1 and R_2, but if these are minimized, much more current will be needed to develop the transistor turn-on voltages. However, reducing the resistances is not enough, so the final step is to enhance the semiconductor process so that transistor gains, shunt resistances, and parasitic resistances can all be reduced to less than the values needed to cause latchup under worst-case operating conditions, without hampering the performance of the real circuit.

Before and after

What happens in the bulk silicon can be seen more clearly in "before and after" cross-sections of a C-MOS circuit. Before the corrective changes are incorporated, Q_1 is a lateral pnp transistor in the substrate and Q_2 is a vertical npn transistor in the well. One's base is the other's collector; the emitters are diffusions; and the resistors are parasitic resistances in the substrate and well (Fig. 4a). Afterwards, they are both lateral transistors in the substrate; dummy collectors lead to V_{cc} and ground connections; and there are low-resistance substrate contacts for the parasitic resistances (Fig. 4b).

These cross-sections are simplified representations of p-well designs, since most C-MOS logic circuits are p-well designs. In such a process, the p-MOS transistors are fabricated on an n-type silicon substrate. Large p-type diffusions called wells serve as the substrates for the n-channel transistors. However, the same considerations apply to n-well processes: the silicon and transistor types are reversed, but the model circuits are the same.

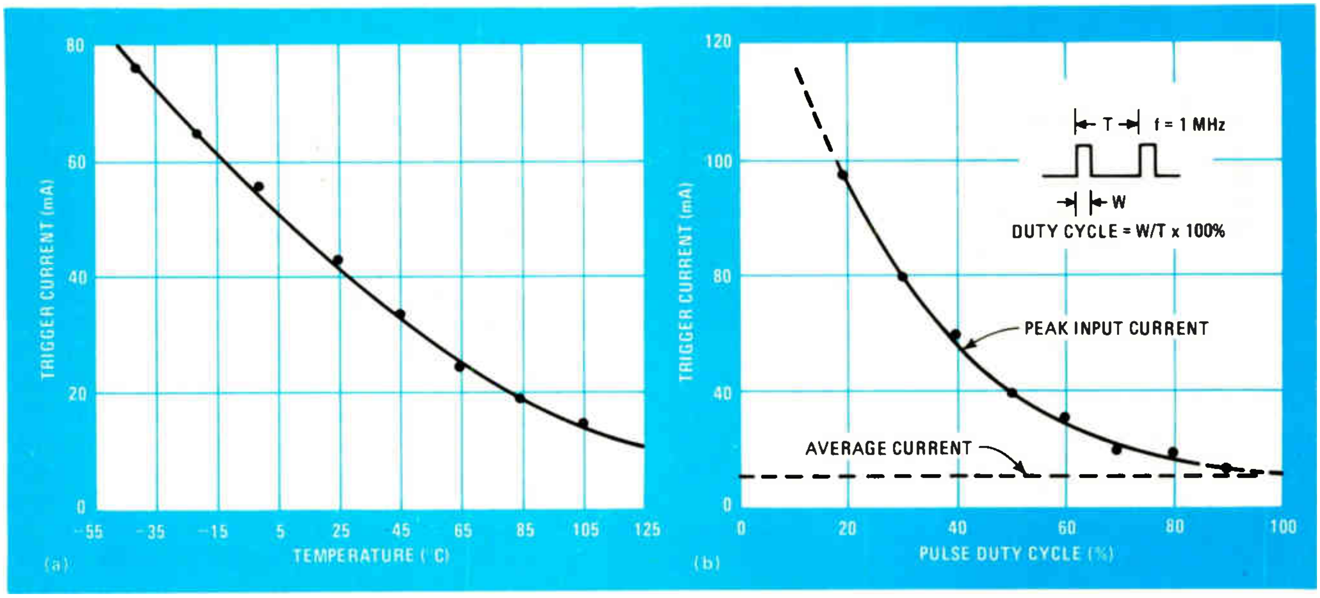
In the latchup-prone p-well process (Fig. 4a), parasitic transistors Q_1 and Q_2 have a current-gain product $(B_1 \times B_2)$ well above 1. Q_1's gain is usually reduced by raising substrate doping concentrations to reduce minority-carrier lifetimes. However, this method is of limited usefulness because it also increases parasitic capacitances and may degrade the performance of the p-MOS transistors. Increasing the space around the input and output diodes helps reduce gain but adds to chip area.

Q_2's gain is generally reduced by increasing the well's doping level to reduce its minority-carrier lifetimes. This move also reduces substrate and base-emitter resistances. However, parasitic junction capacitances increase, and the n-channel transistor's threshold voltage and carrier mobility may be affected. Gain can also be reduced by driving the well diffusion deeper, but that move increases processing time, lateral diffusion, and chip area.

For current reduction, guard rings connected to V_{cc} and ground may be diffused around the input and output diodes to short out the parasitic SCR (Fig. 4b). Guard-ring diffusions create additional parasitic transistors and reduce effective substrate resistance, which make it harder for parasitic SCRs to turn on. They also act as dummy collectors that collect charges directly through V_{cc} and ground, rather than through active circuitry, thereby shunting the parasitic transistors.

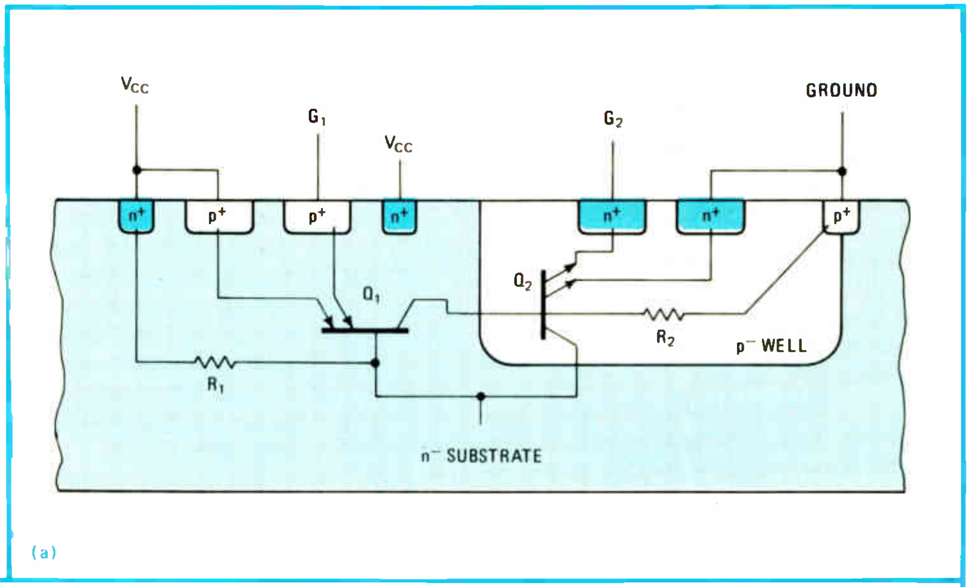
However, guard rings increase chip area considerably and do not always work well. Because they only reduce surface resistance, there may still be parasitic transistors deep in the substrate and under the well (as in Fig. 4b). Carriers can still be injected deep into the substrate, where they cannot be collected by the relatively small dummy collectors on the surface. They can go under the collectors and be collected by the relatively large p-well and thus hamper the active circuit. The collector diffusions can be deepened along with the well diffusions, but with the same drawbacks as before.

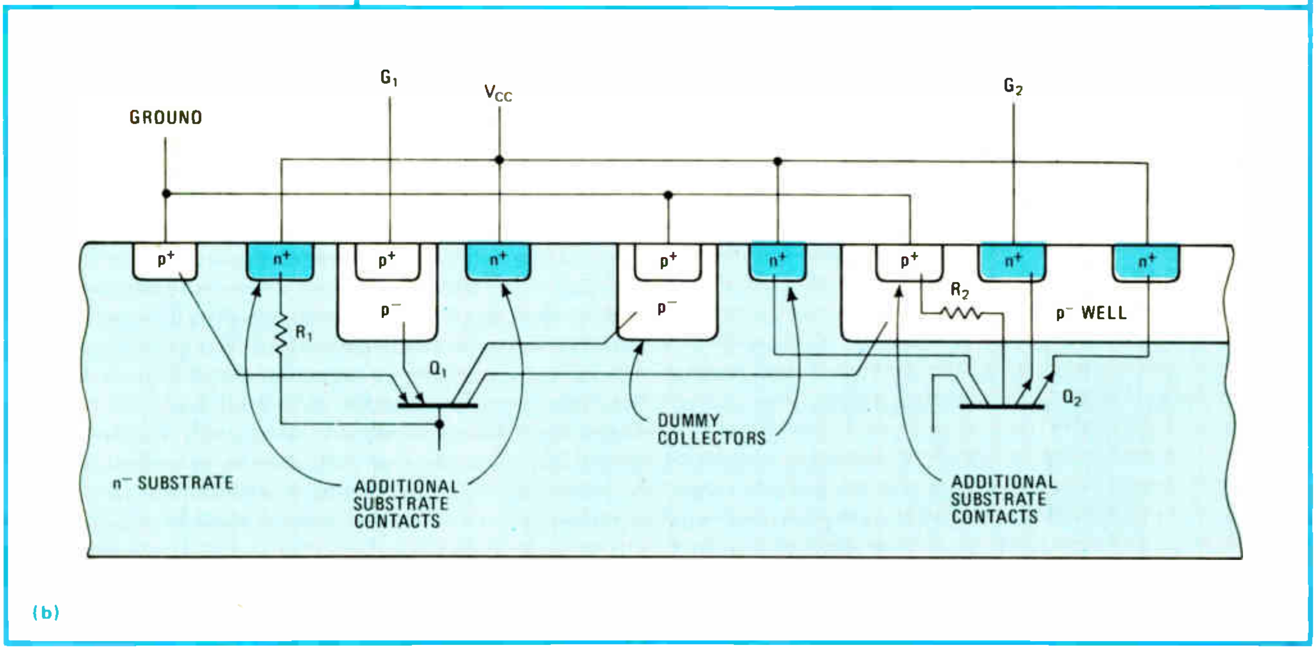
However, it is important to eliminate SCR latchup completely, not just to reduce it with guard rings and other techniques that cost chip area. If, as usual, the



3. Some of the causes. Chip heating (a) and repetitive pulse noise (b) can increase the risk of SCR latchup in high-speed C-MOS circuits. These tests were made with special, latchup-prone devices during a study of ways to prevent latchup in silicon-gate C-MOS circuits.

4. Before and after. The difference between these simplified cross-sections of C-MOS devices that are latchup-prone (a) and latchup-resistant (b) is layout changes that affect parasitic currents. National also adds extra diffusions that carry current away from parasites to power supply or ground.





system must still be protected by non-C-MOS circuits, the extra area needed may not be cost-effective in many applications.

Therefore, enhancements of these techniques were needed. With the MM54/74HC circuits, the solution is fabrication on a substrate with reduced conductivity and a light surface-doping concentration. This and related changes deliver the final blow to the latchup problem.

Preventive actions

The low-conductivity substrate allows large reductions of minority-carrier lifetimes, down to where the other techniques have, in effect, cornered the parasites. The light surface-doping concentration allows optimization of the p- and n-channel transistors and the guard rings. Near the surface, it maintains carriers that lower parasitic resistances and make the dummy collectors more efficient. The surface contacts can now clean up the charges and stray currents.

As part of the characterization testing of the family, many typical devices have been tested for latchup under worst-case conditions (V_{cc} = 7 V, 125° C). They cannot be latched up by forcing triggering current into or out of the input or output protection diodes. The input resistors, output diodes, or metalization can be destroyed by grossly excessive trigger currents, but there is no sign of latchup. To keep latchup tests relatively nondestructive, input current must be limited to 70 milliamperes, and output current to less than 200 mA.

Parasitic circuit elements cannot be tested one by one, but it is clear that there is not enough gain left in the equivalent circuit for triggering. In the present p-well process, most of the gain reduction is in the pnp types of parasitic transistors, since these are always in the substrate in p-well processes. However, the same general considerations and solutions can be applied to n-well processes and, as noted previously, to future higher-density designs. □

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Software notebook

Fortran program designs compensating network

by A. K. Goyal and M. U. A. Siddiqui
R&D Division, Indian Telephone Industries Ltd., Allahabad, India

This Fortran program simplifies the design of a compensation-series-resonant network that reduces the reflection coefficient at the input port of a frequency-band separation circuit comprising low- and high-pass filters connected in parallel. In addition, the program analyzes the reflection coefficients of compensated and noncompensated networks at frequencies of interest.

L_0 and C_0 are the physical values of the compensation-circuit elements connected in parallel with the input port, as shown in (a) on page 145. They are calculated from the mean admittance value, $Y = (Y_{01} + Y_{02})/2$, where Y_{01} and Y_{02} are imaginary parts of the driving-point admittance at frequencies f_1, a low-pass cut-off frequency, and f_2, a high-pass cut-off frequency.

Since $Y_{01} = -1/W_0(j2\Pi f_1)$, $Y_{02} = 1/W_0(j2\Pi f_2)$, and f_0

TABLE 1 A FORTRAN PROGRAM FOR DESIGNING A COMPENSATING NETWORK

```
      DIMENSION C1 (10), C2 (10), CC1 (10), CC2 (10), TITLE (19), FREQ (30)
      COMMON N1, N2, CL, LL, COUT, LOUT, C1, C2, CC1, CC2, LL1 (10), LL2 (10)
      COMMON S, W, IMPD, PII, R
      COMPLEX S, X, YL, YH, YO, YO1, YO2, ADMT, IMPD, YCMPNW
      REAL LOUT, LL, LL1, LL2, LO
      PII = 4. *ATAN (1.)
      WRITE (6, 83)
      READ (5, 82)  (TITLE (I), I = 1, 19)
C
C     READS LOW PASS FILTER COMPONENTS
C
      WRITE (6, 99)
      WRITE (6, 98)
      READ (5,*) FREQ1
      WRITE (6, 97)
      READ (5,*) N1
      WRITE (6, 96)
      READ (5,*) R, CL
      DO 10 I = 1, (N1-2) / 2
           WRITE (6, 95)
           READ (5,*) LL1 (I), CC1 (I)
           WRITE (6, 94)
           READ (5,*) C1 (I)
   10 CONTINUE
      WRITE (6, 93)
      READ (5,*) LOUT
C
C     READS HIGH PASS FILTER COMPONENTS
C
      WRITE (6, 92)
      WRITE (6, 98)
      READ (5,*) FREQ2
      WRITE (6, 97)
      READ (5,*) N2
      WRITE (6, 91)
      READ (5,*) R, LL
      DO 20 I = 1, (N2-2) / 2
           WRITE (6, 94)
           READ (5,*) C2 (I)
           WRITE (6, 95)
           READ (5,*) LL2 (I), CC2 (I)
   20 CONTINUE
      WRITE (6, 94)
      READ (5,*) COUT
```

```
C
C     READS FREQUENCIES FOR ANALYSIS
C
         WRITE (6, 90)
         READ (5,•) NFREQ
         WRITE (6, 89)
         READ (5,•)  (FREQ (I), I = 1, NFREQ)
C
C     COMPUTES COMPENSATING NETWORK
C
         CALL ADMIT (FREQ1, Y01)
         CALL ADMIT (FREQ2, Y02)
         Y = (AIMAG (Y02) —AIMAG (Y01)) / 2.
         L0 = 1. / (2•PII•Y•(FREQ2—FREQ1))
         C0 = 1. / (4•PII••2•FREQ1•FREQ2•L0)
         F0 = SQRT (FREQ1•FREQ2)
         WRITE (6, 87)
         WRITE (6, 88) L0, C0, F0
C
C     ANALYSES UNCOMPENSATED AS WELL AS COMPENSATED NETWORK
C
         WRITE (6, 86)
         DO 30 J = 1, NFREQ
              F = FREQ (J)
              CALL ADMIT (F, ADMT)
              IMPD = 1. / ADMT
              RCOEF1 = 100.•ABS ((IMPD—R) / (IMPD + R))
              YCMPNW = S•C0/(1—W••2•L0•C0)
              IMPD = 1. /(ADMT + YCMPNW)
              RCOEF2 = 100.•ABS ((IMPD—R) / (IMPD + R))
              WRITE (6, 85) F/1000., RCOEF1, RCOEF2
              IF (F. EQ. FREQ1 . OR . F . EQ . FREQ2) WRITE (6, 84)
   30    CONTINUE
   99    FORMAT (1H0, 'ENTER DATA FOR THE LOWPASS FILTER FROM INPUT SIDE'/)
   98    FORMAT (1X, 'ENTER CUTOFF FREQUENCY IN HZ')
   97    FORMAT (1X, 'ENTER DEGREE OF THE FILTER')
   96    FORMAT (1X, 'ENTER VALUE OF R & C')
   95    FORMAT (1X, 'ENTER VALUE OF L & C')
   94    FORMAT (1X, 'ENTER VALUE OF C')
   93    FORMAT (1X, 'ENTER VALUE OF L')
   92    FORMAT (1H0, 'ENTER DATA FOR THE HIGHPASS FILTER FROM OUTPUT SIDE'/)
   91    FORMAT (1X, 'ENTER VALUE OF R & L')
   90    FORMAT (1H0, 'ENTER NUMBER OF FREQUENCIES FOR ANALYSIS')
   89    FORMAT (1X, 'ENTER FREQUENCIES IN HZ')
   88    FORMAT (1H0, 'L0 = ', E14.8, 'H', / 1X, 'C0 = ', E14.8, 'F',/ 1X,
        •'F0 = ', E14.8,' HZ')
   87    FORMAT (1H1, 'COMPUTED VALUES FOR THE COMPENSATING NETWORK')
   86    FORMAT (1H0, 'FREQUENCY REF_COEFF. (%)   REF_COEFF. (%)',
        •/5X, '(KHZ)', 4X, 'WITHOUT CMP_NET WITH CMP_NET' /)
   85    FORMAT (3X, F8.3, 7X, F6.2, 10X, F6.2)
   84    FORMAT (3X, '---------', 7X, '------', 10X, '------')
   83    FORMAT (1X, 'JOB:  ', $)
   82    FORMAT (19A4)
         STOP
         END
         SUBROUTINE ADMIT (FREQ, Y0)
C        ••••••••••
         DIMENSION C1 (10), C2 (10), CC1 (10), CC2 (10)
         COMMON N1, N2, CL, LL, COUT, LOUT, C1, C2, CC1, CC2, LL1 (10), LL2 (10)
         COMMON S, W, IMPD, PII, R
         COMPLEX S, X, YL, YH, Y0, Y01, Y02, ADMT, IMPD, YCMPNW
         REAL LOUT, LL, LL1, LL2, L0
```

```
C
C    LOWPASS FILTER PROCESSING
C
         W = 2.*PII*FRQ
         S = CMPLX (0.0, W)
         YL = 1. / (CL*S + 1 / R)
         DO 10 I = 1, (N1-2) / 2
             X = LL1(I)*S/(1-LL1(I)*CC1(I)*W**2)
             YL = 1 / (X + YL)
             X = C1 (I)*S
             YL = 1 / (X + YL)
    10   CONTINUE
         X = LOUT*S
         YL = 1 / (X + YL)
```

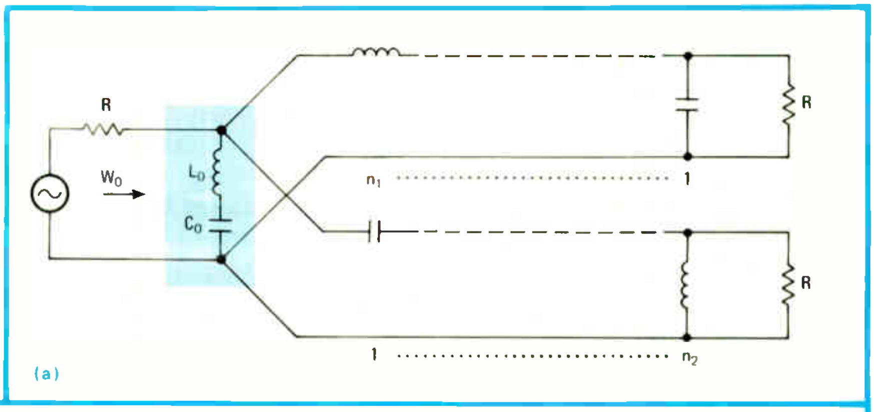
```
C
C    HIGHPASS FILTER PROCESSING
C
         YH = R*LL*S/(R + LL*S)
         DO 20 I = 1, (N2-2) / 2
             X = 1/(C2 (I)*S)
             YH = 1 / (X + YH)
             X = CC2(I)*S/(1-LL2(I)*CC2(I)*W**2)
             YH = 1 / (X + YH)
    20   CONTINUE
         X = 1 / (COUT*S)
         YH = 1 / (X + YH)
         Y0 = (YL + YH)
         RETURN
         END
```

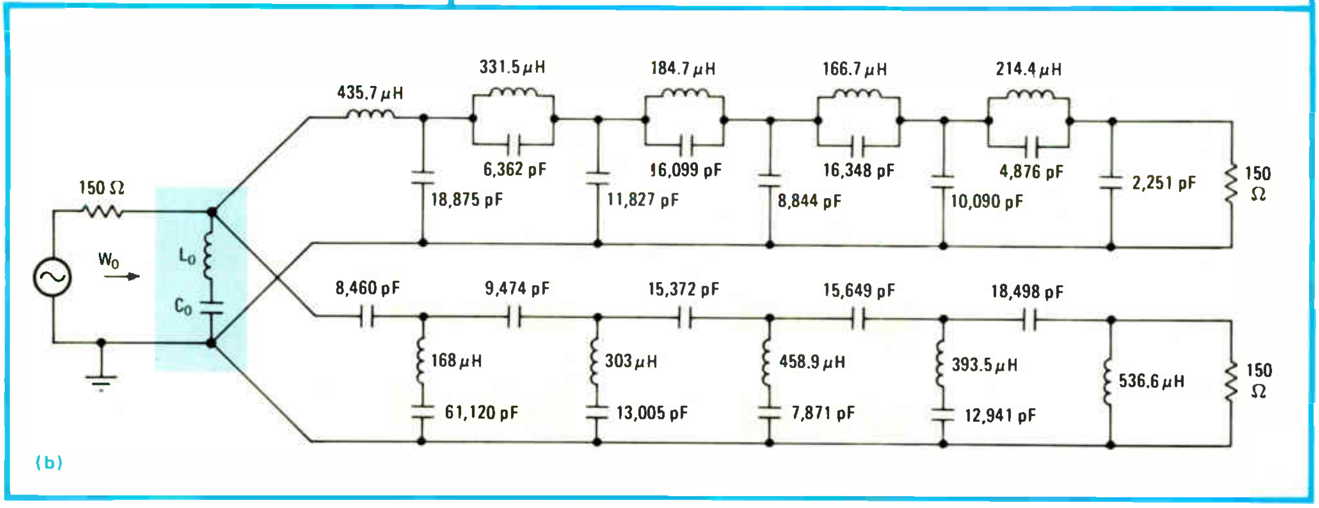
TABLE 2 PROGRAM EXAMPLE COMPENSATION NETWORK FOR A DIRECTIONAL FILTER

```
$ FORTRAN COMPEN

$ LINK COMPEN

$ RUN COMPEN

JOB: SAMPLE RUN

ENTER DATA FOR THE LOWPASS-FILTER
FROM INPUT SIDE

ENTER CUTOFF FREQUENCY IN HZ
84E3
ENTER DEGREE OF THE FILTER
10
ENTER VALUE OF R & C
150,2251E-12
ENTER VALUE OF L & C
214.4E-6, 4876E-12
ENTER VALUE OF C
10090E-12
ENTER VALUE OF L & C
166.7E-6, 16348E-12
ENTER VALUE OF C
8844E-12
ENTER VALUE OF L & C
184.7E-6, 16099E-12
ENTER VALUE OF C
11827E-12
ENTER VALUE OF L & C
331.5E-6, 6362E-12
ENTER VALUE OF C
18875E-12
ENTER VALUE OF L
435.7E-6
```

```
ENTER DATA FOR THE HIGHPASS-FILTER
FROM OUTPUT SIDE

ENTER CUTOFF FREQUENCY IN HZ
92E3
ENTER DEGREE OF THE FILTER
10
ENTER VALUE OF R & L
150,536.6E-6
ENTER VALUE OF C
18498E-12
ENTER VALUE OF L & C
393.5E-6, 12941E-12
ENTER VALUE OF C
15649E-12
ENTER VALUE OF L & C
458.9E-6, 7871E-12
ENTER VALUE OF C
15372E-12
ENTER VALUE OF L & C
303E-6, 13005E-12
ENTER VALUE OF C
9474E-12
ENTER VALUE OF L & C
168E-6, 61120E-12
ENTER VALUE OF C
8460E-12
ENTER NUMBER OF FREQUENCIES FOR ANALYSIS
16
ENTER FREQUENCIES IN HZ
60E3, 72E3, 78E3, 80E3, 81E3, 82E3, 83E3, 84E3,
92E3, 93E3, 94E3, 95E3, 96E3, 98E3, 104E3, 116E3
```

Compensation. Practical values, L_0 and C_0, of a compensation-series-resonant network (a) can easily be obtained with this Fortran program. The program computes the network's element values for a directional filter (b) comprising low- and high-pass filters in parallel, with cut-offs at 84 kHz and 92 kHz.





COMPUTED VALUES FOR THE COMPENSATING NETWORK

LO = 0.70764292E-02 H
CO = 0.46318979E-09 F
FO = 0.87909047E+05 HZ

FREQUENCY (KHZ)	REF_COEFF.(%) WITHOUT COMPENSATION NETWORK	REF_COEFF.(%) WITH COMPENSATION NETWORK
60.000	2.14	0.32
72.000	4.02	0.80
78.000	6.53	1.46
80.000	8.50	1.64
81.000	10.07	1.58
82.000	12.06	1.62
83.000	14.80	1.71
84.000	20.46	0.38
------	-----	------
92.000	20.71	0.16
------	-----	------
93.000	15.31	1.54
94.000	12.67	1.54
95.000	10.81	1.47
96.000	9.32	1.52
98.000	7.28	1.51
104.000	4.89	0.79
116.000	2.68	0.75

FORTRAN STOP
$

$= \sqrt{(f_1 f_2)} = 1/2\Pi\sqrt{(L_0 C_0)}$, it follows (after simplification) that $L_0 = 1/2\Pi Y(f_2 - f_1)$ and $C_0 = 1/4\Pi^2 f_1 f_2 L_0$. All standard filter-design handbooks give element values for the desired low- and high-pass filters. After denormalization, the filters are connected in parallel and the compensation network is computed.

Table 1 shows the complete listing of the Fortran program. Although it is implemented on a VAX 11/780, it can be used, as well, with any microcomputer or minicomputer that supports Fortran. To obtain the compensation network's component values, users must enter the component values of the low-pass and high-pass sections branch by branch. If the reflection coefficient should violate the specifications at the desired f_1 and f_2, the degree of the filters must be increased to extend the pass bands.

Table 2 shows a sample run of the program for a directional filter (b) that is composed of a low-pass filter with cut-off at 84 kilohertz connected in parallel to a high-pass filter with cut-off at 92 kHz. The directional filter provides stop-band attenuation greater than 55 decibels, with a maximum reflection coefficient (within the pass bands of both the filters) lower than 8% at the input port. From the table, it can also be seen that a noncompensated directional filter network has a reflection coefficient of more than 20%, a value that is not suitable for most applications. □

Electronics invites readers to submit short, original, unpublished programs and software solutions to engineering problems. Explain briefly and thoroughly the program's operation and send to Ashok Bindra, Circuit Design Editor. We'll pay $75 for each item published.

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. . . and check world environment standards

For more detail on world standards for environmental testing, you might also check with publication 68-2-47 from the International Electrotechnical Commission. The publication describes **standard procedures for mounting components for dynamic testing for shock, bumps, vibration, and steady-state acceleration.** The 25-page booklet is available for 34 Swiss francs from the Information Officer, Central Office of the IEC, 3, Rue de Varembé, 1211 Geneva 20, Switzerland.

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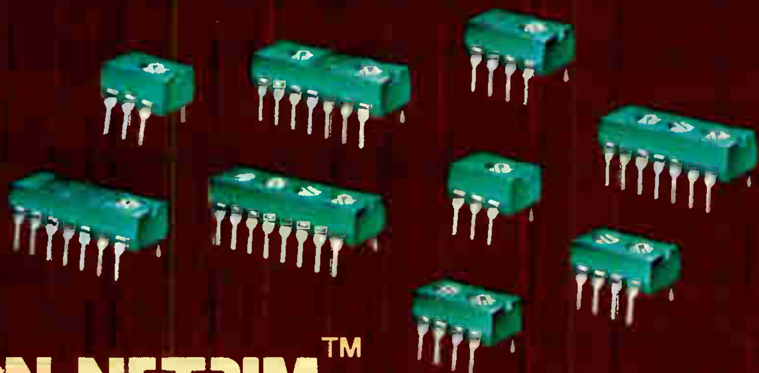
nine reasons to be choosy



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RISC supermini has stellar performance

Use of register-to-register operations makes 32-bit reduced-instruction-set computer a speedster

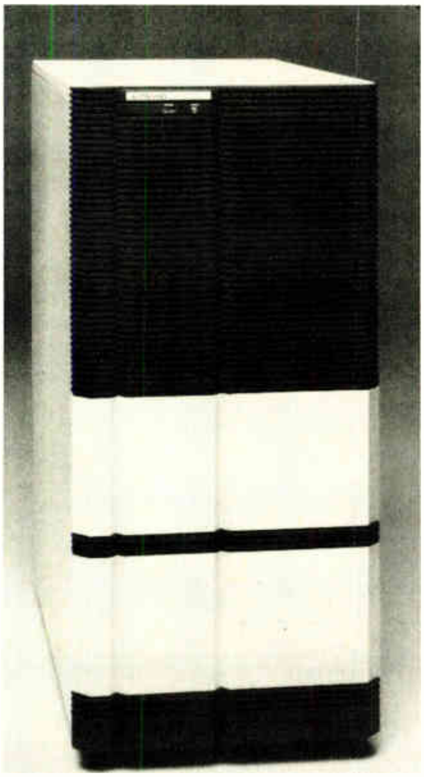
by Clifford Barney, Palo Alto bureau

The first commercial computer designed with the high-performance reduced-instruction-set–computer RISC architecture that can outspeed conventional computers by as much as 2:1 has been introduced by Pyramid Technology Corp. Called the Pyramid 90x, the new machine [*Electronics,* July 28, p. 41] is an expandable 32-bit superminicomputer with 8 megabytes of main memory. Tailored to the Unix operating system, it is organized around a 32-megabyte/s bus and supports up to 128 users over intelligent input/output processors.

A firm less than two years old, Pyramid will market the system to original-equipment manufacturers and large end users through its own direct sales force and through independent sales organizations. "We want to be the premier supplier of high-performance Unix systems," says Pyramid cofounder and president Edward W. Dollinar, a former Rolm executive. "There are a lot of Unix-based micros, but these do not meet the almost insatiable demand for more performance in the high end of the marketplace."

Price range. The Pyramid system will be priced at $100,000 to $300,000, depending on configuration. The company expects to sell about half its production into the OEM market, the rest into the scientific and academic communities.

High performance was one of the reasons that Robert Ragan-Kelley, the other cofounder and Pyramid's vice president of architecture and planning, chose to design the computer around the register-intensive RISC architecture, developed at the University of California, Berkeley. The 90x has a total of 528 registers—16 global registers and a 16-level stack with 32 registers (4 bytes apiece) on each level. The stack format of the registers makes it easier to keep track of subroutine calls, which is important for a procedure-intensive operating system like Unix.



All operations except memory loads and stores are register to register. Ragan-Kelley says register-to-register operations are 2 to 4 times faster than cache operations and 8 to 10 times faster than memory operations. Only 15% to 20% of instructions executed require memory loads and stores on the 90x, he adds, giving it about twice the performance of a conventional system, which may have to access memory 50% of the time. Pyramid says that its system has outperformed a VAX-11/780 by factors of 2 to 5 on several benchmark tests.

Overlapping registers. Ragan-Kelley also adopted the structure of overlapped logical registers invented by Berkeley's David Patterson [*Electronics,* Nov. 17, 1982, p. 101]. In this structure, data that is passed from one procedure to another remains in the same physical register. This is important because the simple RISC instructions, though they make compiler-writing easier, do require subroutine procedures where conventional architecture can get by with a complex instruction.

"We did relax some of Patterson's constraints," Ragan-Kelley says. "He assumed a hardwired machine, because he was designing a VLSI chip; our instructions are microcoded.

"He also assumed that all instructions were one word long and executed in one machine cycle. Some of our instructions take two words, and we use two cycles. But the important aspect is that at the same time we decode one instruction, we can prefetch the next one."

TTL-based. The Pyramid 90x has about 90 instructions; some of them, such as those for multiplication and division, are more complex than the Berkeley RISC chip's instructions. Unlike the Berkeley design, the Pyramid is implemented in conventional Schottky TTL medium-scale integrated circuits. "Our alternatives were to go to low-performance off-the-shelf microprocessors, or design a VLSI chip prematurely," Ragan-Kelley

New products

says. "TTL is fast, cheap, and available from many suppliers, and it is the modeling clay for the next-generation VLSI chip."

Pyramid tailored its own Unix port to the RISC architecture, including several kernel enhancements and incorporating the Berkeley 4.1C demand-paged–virtual-memory and networking software. Compilers are provided for three languages: C, Pascal, and Fortran 77.

Support processors. All I/O operations are offloaded to intelligent terminal processors, which are built with bit-slice circuits and have an average instruction time of under 200 ns. Each I/O module controls 16 asynchronous ports, and the system will support up to eight modules. A dedicated system-support processor, based on the Motorola 68000 chip, is used to handle all system configuration, diagnostics, and on-line software changes.

All of these processors sit on Pyramid's proprietary XTEND bus, which also has slots for floating-point processors and other performance-enhancement modules. The architecture also provides for a 4-K-byte instruction cache and a 32-K-byte data cache with a 125-ns access time.

A basic Pyramid system has 5 slots for memory, 7 for the central processing unit and subsystems, and 14 for any mix of terminal, disk, and other controllers. In theory, there is no limit to the amount of disk memory the system can support; in practice, Pyramid has tested it at a maximum of 3.6 gigabytes—eight drives of 450 megabytes each.

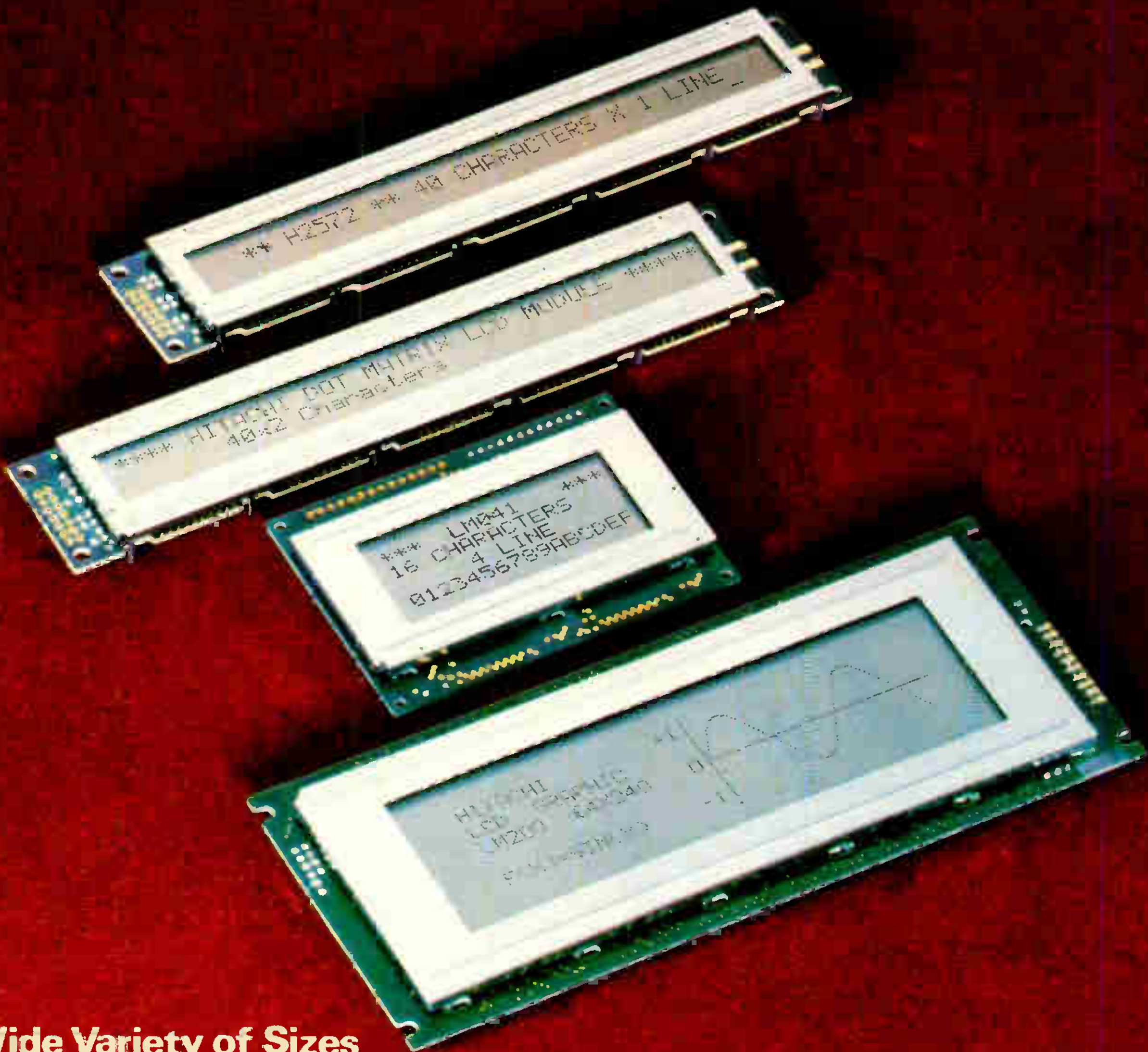
Main-memory boards are designed so that 256-K random-access memories can be plugged in to the same sockets that now contain 64-K chips. This would permit an upgrade to 32 megabytes of main memory when the larger RAMs become generally available next year, with no hardware modification necessary.

The first shipments of the Pyramid 90x are scheduled to be made in October, from the company's new 100,000-ft² manufacturing facility.

Pyramid Technology Corp., 1295 Charleston Rd., Mountain View, Calif. 94043. Phone (415) 965-7200 [338]

Gems Among LCDs

When only the best is good enough, Hitachi's the LCD module you can depend on. For bright and high-contrast display, thanks to twist-nematic type liquid crystal. For low power consumption and drive voltage. For a complete range of sizes, including extra-small, lightweight models. And for high quality in a wide variety of applications, from measuring instruments and scientific calculators to POS and portable data terminal equipment, personal computers, word processors, and other top-end display devices.



Wide Variety of Sizes

Type No	No. of display characters	External dimensions W×H×T (mm)	Weight (g)	Power consumption (mW)
H2572	Single-line × 40-character display	182 × 33.5 × 13 (max.)	65	10
LM018	Double-line × 40-character display	182 × 33.5 × 13 (max.)	65	15
LM041	Four-line × 16-character display	87 × 60 × 14 (max.)	60	15
LM200	64 × 240 dot graphic display	180 × 75 × 15 (max.)	150	20

Note: Shown here are just four of the many types of LCDs available from HITACHI.

HITACHI

For more information:
Hitachi America, Ltd.
Chicago Office, 500 Park Boulevard, Suite 805, Itasca, Illinois 60143
Telephone: (312) 773-0700
TWX: 910-651-3105

Circle 151 on reader service card

Computers & peripherals

SMD controller bows for IBM PC

Board lets Personal Computer control more than 1 gigabyte of high-density disk drives

Interphase Corp. is bringing to the market a controller board that enables the International Business Machines Corp.'s Personal Computer to take advantage of fast, high-density drives using the storage-module-device interface. To do so meant teaming low-power complementary-MOS chips with a high-performance architecture that, in turn, combines a microcomputer with a custom-designed state machine.

Given the wide range of SMD-compatible drives, Interphase says its SMD PC-80 controller opens up the possibility of giving an IBM Personal Computer control of well over 1 gigabyte of storage—such that a whole new range of applications usually requiring a minicomputer or mainframe can be implemented using the popular PC or the compatible microsystems surfacing in its wake.

Fast Maverick. Nicknamed the Maverick, Interphase's SMD PC-80 controller can handle two SMD units and data rates of up to 20 Mb/s. Currently, high-performance SMD-compatible drives offer rates of up to 16 Mb/s, but Interphase designed its controller to support what it anticipates to be the upper SMD range within a year.

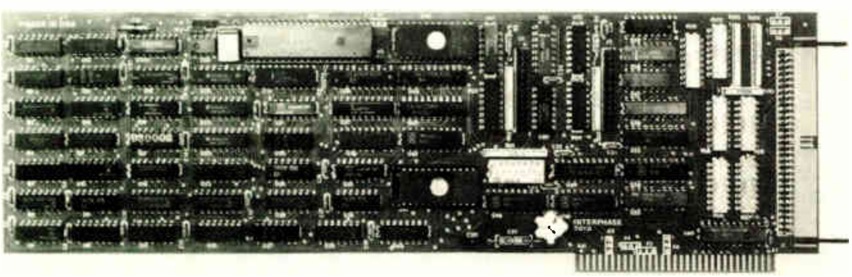
The trick to offering high-performance SMD compatibility for the IBM unit was in packing the necessary control circuitry onto a standard 4.188-by-13.125-in. expansion card, says Tom Thawley, vice president of engineering who headed the design effort. In addition, power dissipation had to be kept at a minimum so that the board could operate inside the PC, he adds.

State machine too. Approximately 60 devices are used on the controller board, which is based on an Intel 80C31 C-MOS microcomputer. (About 90 integrated circuits are used on Interphase's Multibus SMD controller.) The 8-bit microcomputer works in tandem with a bipolar state machine made from a number of components such as latches, programmable read-only memory, and other logic chips.

Control functions are divided up between the microcomputer and state machine according to speed requirements. A vast majority of them can be performed by the microcomputer chip, but, when needed, the state machine can handle sub-instructions 10 to 20 times faster than the standard C-MOS part, Thawley says.

To handle the 20-Mb/s data rate, the buffered control board uses high-speed TTL components. The flow is so fast that both the microcomputer and state machine must perform their control duties outside the main data stream.

Interphase elected to use high-speed C-MOS logic on the board to keep the power consumption within an acceptable range for the desktop unit. "I'd say about 80% of the entire board is C-MOS," estimates Thawley, adding that the controller board can support two SMD disk drives while drawing a nominal 0.8 A, or 1.2 A maximum. Because of the limited availability of negative-voltage power in the IBM unit, the board has been designed to run off a 5-V-only power supply, ±5%. Operating temperature range is 0° to 55°C.



The controller supports both fixed and removable SMD-compatible drives, as well as dual-ported units. Sector sizes may be programmed up to 960 bytes. Data transfers over the system bus may be implemented at high speed through the Personal Computer's direct-memory-access scheme or set by programmed input/output. Interphase has optimized the unit's DMA system to offer a 50% speed improvement over IBM's own programs, Thawley states.

In addition to use with the PC, the board can be installed in a number of units that employ similar system architecture and a central microprocessor, including Compaq's portable computer and systems from Victor, Columbia, and Eagle. Currently, the board operates under PC-DOS, MS-DOS, and Lantech Systems Inc.'s uNETix operating systems. (Dallas-based Lantech's uNETix is a Unix-like multitasking operating system that sells for $99.)

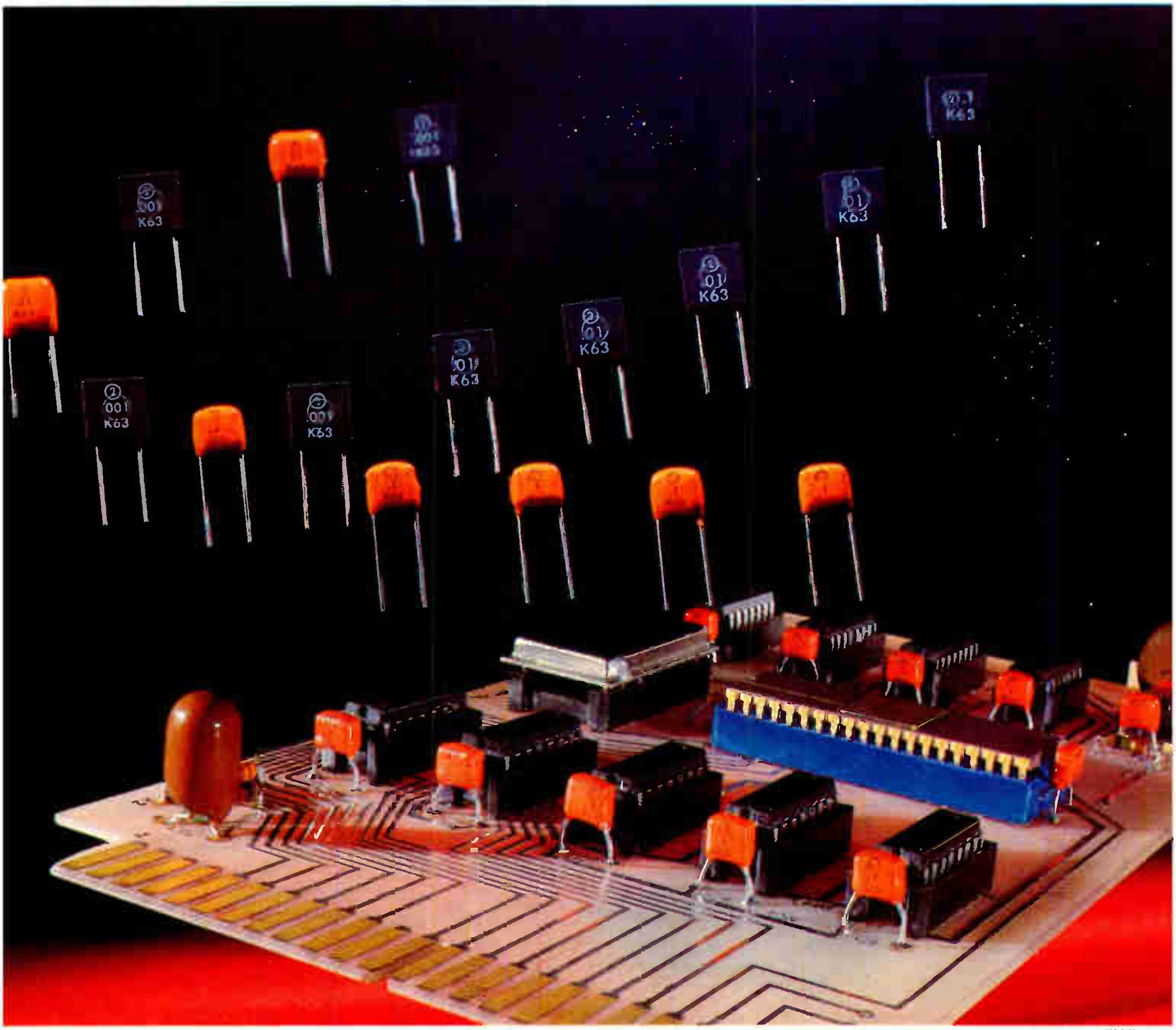
The SMD PC-80 supports overlapped seeks between two drives and has automatic 32-bit error checking and correction. It also handles bad-track and -sector replacement.

The controller is priced at $1,895 in single quantities and $1,200 each in 100-piece lots. Volume deliveries are slated to begin in September. Interphase also plans to make available an SMD subsystem for the IBM market using the same Maverick controller, says A. Edward Turner, vice president of marketing.

More to come. Initially, the subsystem—which will include an enclosure and power supply—will feature a 50-megabyte Amcodyne Arapaho drive with 25 megabytes removable. Other subsystems also in the prototype stage will offer similar fixed-and-removable schemes and high performance.

"While it may seem a bit much to consider an IBM Personal Computer

RESOURCEFULNESS.



458 3100

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THE MARK OF RELIABILITY
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Circle 153 on reader service card

with well over a gigabyte of storage, we believe the wide range of SMD densities as well as fixed and removable types will open up many new applications for the PC," explains Turner. Leading examples of such applications include: large data bases; file servers for local networks; and a number of business applications requiring the storage of massive records, such as accounting.

As an example, Control Data Corp. plans to begin offering samples of its SMD-compatible 9771 expanded module drive this quarter. The 14-in. XMD drive, which will cost $9,840 each in volume quantities, stores 825 megabytes. Interphase says two of these could be controlled by its Maverick drive.

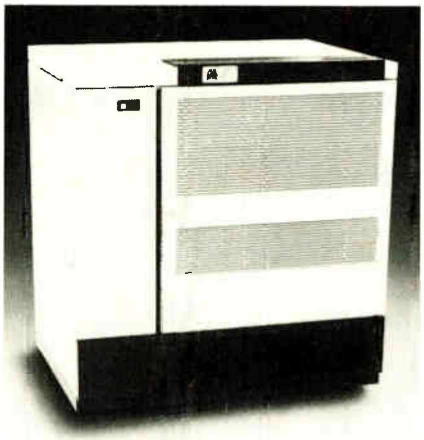
Broadening the range. Currently, those manufacturers wishing to use high-performance drives on the unit are for the most part limited to ST506-compatible 5¼-in. Winchesters. A number of SMD-compatible drives offer potential speed improvements of four to five times that of IBM's Winchester-based XT model, Turner points out.

"We believe the combination of greater density and speeds, coupled with the potential of removable and fixed storage, will prove to be very popular in this growing market," says Turner, noting that the controller board marks Interphase's initial entry into the IBM PC field. Until now, the nine-year-old firm has specialized in Multibus-compatible disk controllers.

Interphase Corp., 2925 Merrell Rd., Dallas, Texas 75229. Phone (214) 350-9000 [361]

Satellite computer gives mainframes interactive abilities

The Dialogic/One system implements what its developer calls layered interactive processing to integrate the Dialogic/10 satellite computer into a large IBM or IBM-plug-compatible mainframe environment. The distributing of different computer tasks between the two machines, or layers, promotes efficient, cost-effective interactive processing.



Each machine performs the tasks it does best, while users view both machines as a single, familiar system from a 3270-type terminal. The mainframe, for example, performs batch processing and data-base management, while the Dialogic/10 performs interactive processing.

The Dialogic/One system comprises hardware and software packaged for simple installation in any IBM or plug-compatible environment that uses the MVS operating system. As for the Dialogic/10 satellite computer, its hardware architecture is based on multiple microprocessors working in parallel. Through a wideband communications channel, the processors share access to a high-performance hard-disk–drive system.

The user software consists of a superset of Time Sharing Option (TSO) and an operating system distributed between the mainframe and the Dialogic/10, a set of application packages, and a high-level command language for developing applications. Available now, Dialogic/One systems start at $198,000.

Dialogic Systems Corp., 1335 Bordeaux Dr., Sunnyvale, Calif. 94089. Phone (408) 745-1300 [363]

19-in. color terminal draws 25,000 vectors/s

Two raster-scanned–display terminals—a 14- and a 19-in.–diagonal model—support such software packages as Disspla and Tell-A-Graf, for business applications, and Template, for engineering applications.

The 14-in. GR-1104 desktop terminal has a resolution of 1,024 by 780 picture elements and can display any eight colors from a palette of 512 through a user-loadable video look-up table. The screen has a 60-Hz noninterlaced display to achieve bright, nonflickering images. An alphanumeric overlay capabilitiy permits independent file listings to be superimposed and scrolled over a graphics display.

The 19-in. GR-2414, designed to meet the high-level graphics-design needs of the scientific and engineering community, has been clocked at 25,000 vectors/s. It has a displayable resolution of 1,280 by 1,024 pixels and can simultaneously display 1,024 colors from a palette of 32,768. Its local interactive processing supports basic two-dimensional transformations for scale, rotation and translation, clipping functions with window and viewport, true zoom and scroll, positioning, rubber banding, drag, and hit test.

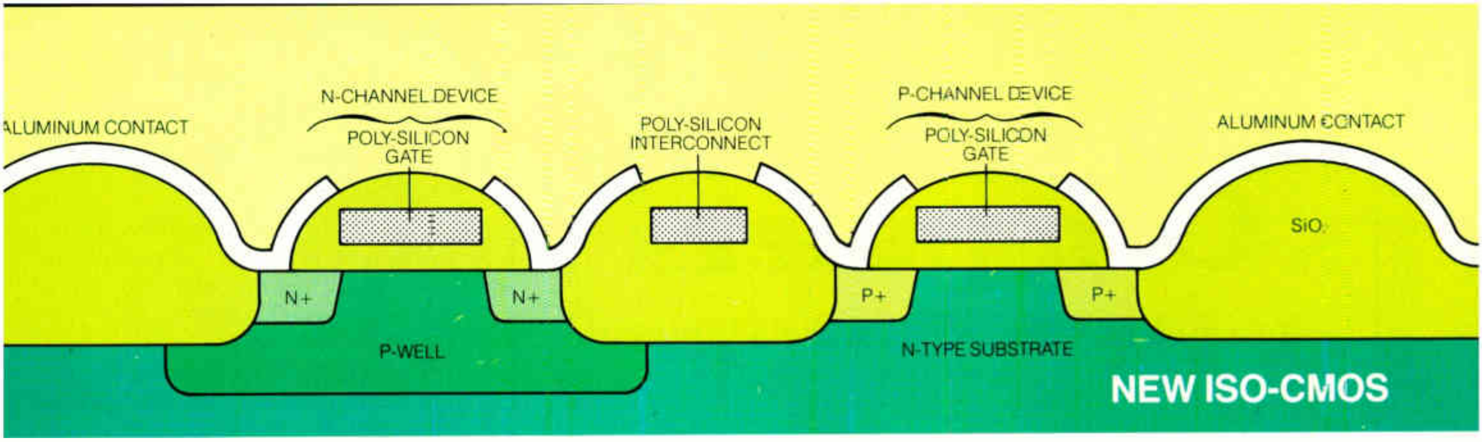
In addition, the bigger terminal's graphics processor generates a wide variety of graphics primitives—including circles, arcs, rectangles, polygons, grids, fans, hatchings, and paintings. Its local functions operate on data from the 128-K-byte display list segment memory.

The 14-in. terminal costs $4,950, the 19-in. one, $18,950.

Seiko Instruments USA Inc., Graphic Devices & Systems, 1623 Buckeye Dr., Milpitas, Calif. 95035. Phone (408) 943-9100 [364]

Thrifty APL computer uses an array processor

A stand-alone general-purpose computer with an array processor architecture "speaks" the APL language with the same performance as a mainframe but at a fraction of the cost: as little as $44,000 for a basic system with ½ megabyte of memory. A typical configuration of the APL Machine consists of a 4-megabyte array processor, an IBM Personal Computer serving as the programmer's work station, a 124-megabyte hard



IF YOUR BOARDS ARE GOING CRAZY, MAYBE THEY NEED A SHRINK.

Problems with PC boards? As you add function to your PC boards, you add complexity, power supplies, chances for failure and . . . cost. What's more, it's hard to "hide" a system that's built with discretes. So, maybe you're considering an expensive custom chip. There's an alternative: GTE Microcircuits semicustom gate arrays, the GTE 50000 Series.

The GTE solution. GTE's ISO-CMOS process gate arrays offer you many of the advantages of custom circuits; but you won't have to wait years to get your parts. And you won't be saddled with custom circuit costs. Best of all, you can shrink your boards and your production costs into a single package.

Who needs it? Anyone who can benefit from greater efficiency, reduced real estate, greater dependability, low power requirements and fast turnaround.

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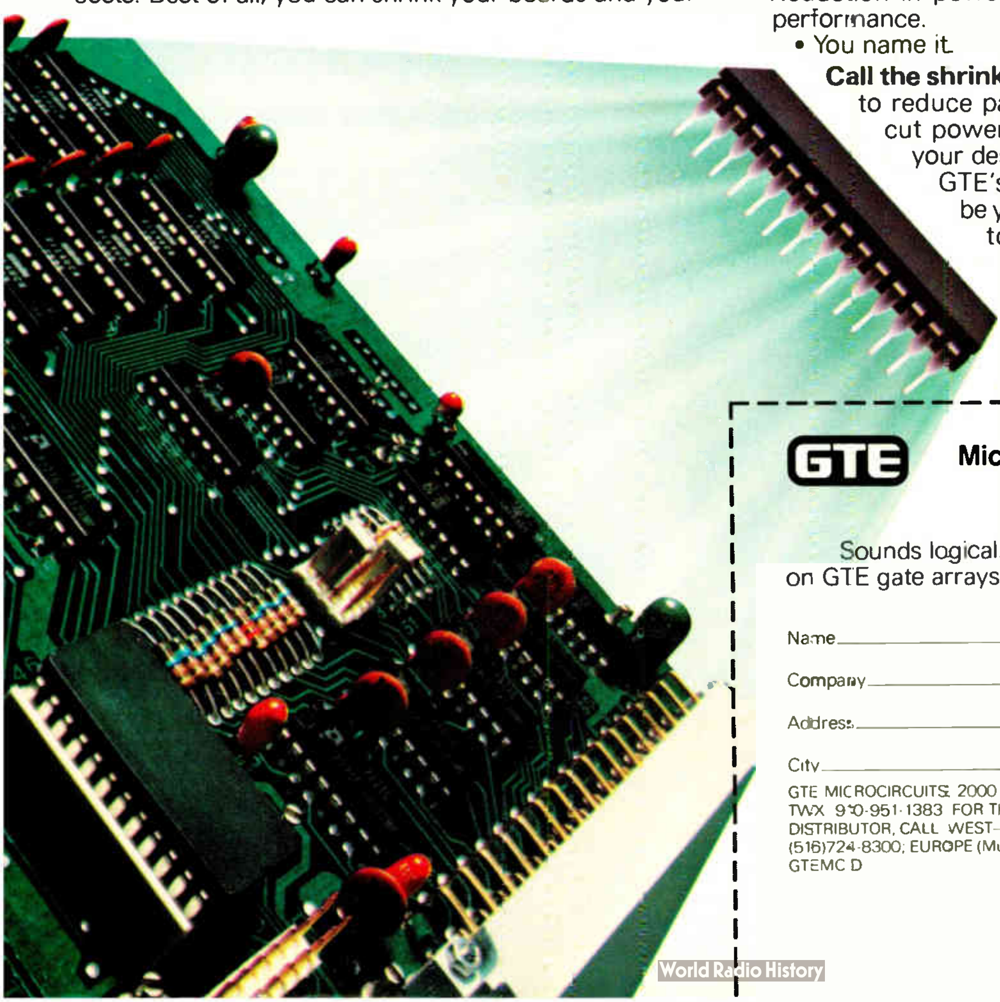
- Industries where reduced assembly, maintenance and labor costs are important.
- Proprietary designs where confidentiality is a marketing consideration.
- Telecom products where gate arrays can reduce system costs.
- Reduction in power and size without sacrificing performance.
- You name it.

Call the shrink. That's us. We'll work with you to reduce parts count, increase reliability, cut power requirements and sequester your designs. And we'll show you how GTE's semicustom gate arrays can be your most cost effective answer to more efficient systems. Call for information. Or fill in the coupon below. We'll send you our G50000 Series gate array product data.



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Circle 155 on reader service card

New products

disk, a dual-mode tape drive, an input/output processor supporting up to eight terminals, and the firm's software. This system sells for $85,000.

The APL interpreter runs in the 12.5-MHz 16-/32-bit control processor, which handles all aspects of syntax and conformance checking. Arithmetic and logical expressions are executed by the machine's array portion. As many as 10 million floating-point operations/s can by executed by the APL's array processor.

This 32-bit floating-point array processor is programmed directly in APL. Since the primitive functions and operations of APL reside in pipeline microcode, in most applications high-speed execution is achieved directly from APL. A sophisticated PC operating environment called In-Sight, designed by Analogic, allows users to display up to 10 concurrently running tasks on overlapping and sliding windows. The system will be available in September.

Analogic Corp., Audubon Road, Wakefield, Mass. 01880. Phone (617) 246-0300 [365]

Winchester disk quadruples storage in Vector 4/60 computer

Thanks to an integrated 5¼-in., 46-megabyte Winchester disk drive, the Vector 4/60 stores four times as much data as previous Vector 4 systems. The 8-/16-bit business computer also has a 5¼-in. floppy-disk drive with a 630-K-byte capacity. The Winchester's average access time is 39 ms.

Priced at $9,995, the Vector 4/60 includes the CP/M-86 operating system and the Memorite III word-processing and ExecuPlan II financial-planning packages, as well as GSX-86 graphics software. It supports pen plotters from Hewlett-Packard Co. and Houston Instrument.

The standard Vector 4/60 comes with 128-K bytes of random-access memory. A 256-K-byte version sells for $10,490.

Vector Graphic Inc., 500 N. Ventu Park Rd., Thousand Oaks, Calif. 91320. Phone (805) 499-5831 [368]

THE AGONY & THE ECSTASY

FutureNet's DASH-1 Revolutionizes Schematic Design and Documentation!

Perfect Schematics on Your IBM*PC

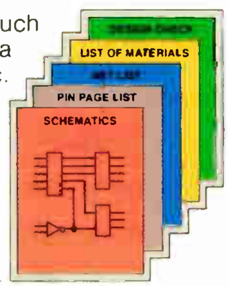
Imagine, sitting at your IBM Personal Computer, producing perfect schematics in a fraction of the time it would take using normal design techniques. Gone forever are the tedium and agony associated with manual design, drafting, and documentation.

FutureNet's DASH-1 Schematic Designer is the only system tailored specifically to the needs of the electronics engineer. It can make you five times more efficient as a designer, and nearly eight times more efficient when it comes to revisions.

Parts Libraries Included

No more sweating over IC data books. The DASH-1 Parts Library (on disk) includes TTL, popular microprocessors, memory and support chips, plus discrete components, complete with pinouts and pin functions. With a keystroke you can call up the symbols you need or quickly create new symbols. Using the mouse you can move symbols or areas of a drawing and interconnect them. And annotation is a snap. Typically, a schematic that would take eight hours to produce manually can be completed in one to two hours on the DASH-1. Ah, the ecstasy of it all!

Captures Data for Documentation



DASH-1 does much more than create a perfect schematic. With your design data captured automatically on disk, essential documents — Net Lists, Lists of Materials, Design Check Reports — can be produced at will. Think of the hours of drudgery you'll save by eliminating these time-consuming, error-prone tasks. Plus, you'll have peace of mind knowing that DASH-1 will locate many common design errors before they reach the hardware stage.

DASH-1 Talks to Other Systems

The DASH-1 interfaces with other computer or CAD systems, transferring all your schematic data in a flash. Direct connection to VAX's or PDP-11's is especially easy.

The $5,980 Miracle

After seeing DASH-1 in operation, engineers from large and small companies alike have said, "We need this!" They're pleased by the price, too. Just $5,980 for the Add-on Package to your IBM PC. Complete turnkey systems including the IBM PC and the new IBM XT with 10 Mb Winchester hard disk and printer are available at prices starting at $12,960. Call FutureNet today for more information on the amazing DASH-1. You'll become a far more efficient designer overnight!

So long Agony... hello Ecstasy.

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(213) 700-0691

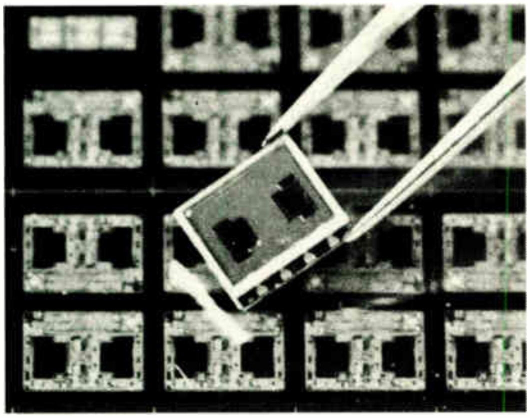
Circle 158 on reader service card

Industrial

Chip senses heat, pressure

Silicon sensor carries circuitry that multiplexes measurements onto a single output line

Silicon sensors that measure temperature have been around for a while and offer size, power-consumption, and reliability advantages over their mechanical relatives. But merging the ability to measure both pressure and temperature on one silicon chip is something that has only just been done—by Transensory Devices Inc. in its IS2002 sensor.



The IS2002 is a pressure-temperature transducer that may be configured by either the manufacturer or the user to measure differential and absolute pressure in the range of 0 to 1,500 torr. Temperature may be measured between –40° and +125°C.

Powered by a 5-V source, the chip has its three outputs—differential and absolute pressure, plus temperature—multiplexed on a single output line. When an output is requested, the sensor gives all three values, separating each with a voltage frame-reference marker.

The pressure readings of the sensor are accurate to within 0.5 torr for short periods of time and 1 torr per month. On the other hand, the temperature portion of the sensor is accurate to 0.1°C for short periods of time and has a maximum error of 5°C. The sensor has a power consumption of 1.5 mW, and has outputs of 300 μV/torr and 2 mV/°C.

Current measurement techniques typically use a mechanical sensor that is coupled to separate signal-processing electronics and calibration or compensation modules. With this approach, additional signal-processing electronics is often needed.

According to Transensory Devices' president, James Knutti, the sensor is unusual in the amount of signal processing that is incorporated on the chip along with the precision sensing element. This circuitry is used to generate a buffered signal that is calibrated and referenced. The buffering inside the sensor, which makes the sensor appear more as a transmitter to an interface, helps to minimize its sensitivity to noise. In addition, thanks to the proximity of the electronics to the sensor, there are no connecting wires to create the parasitic effects inherent in other approaches. The result is higher accuracy and stability.

The sensor has its own internal clock, which acts as an external control line. Although it is not accurate enough to be used for timing, says Knutti, it can allow users to access any sensor reading easily and will also send out the signals at certain times.

The unit is particularly suited for use in computer or digital systems. In fact, because of the signal-processing circuitry contained on the sensor chip, the computer can poll a specific parameter on a sensor by just sending out the appropriate address.

The particular housing that is selected for the sensor determines its uses. Perhaps the most classic application of differential and absolute pressure is taking a reading from two branches of a Y-shaped pipe. In this case, the housing would be specially made to suit the pipe and the placement of the sensors.

The device will be available in September and will sell for between $80 and $500 depending upon the housing chosen.

Transensory Devices Inc., 44060 Old Warm Springs Blvd., Fremont, Calif. 94538. Phone (415) 490-3333 [371]

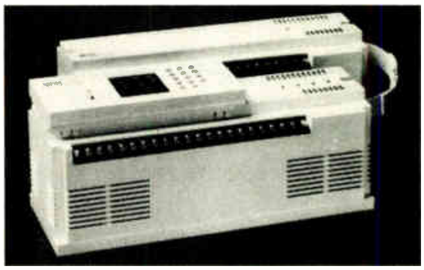
Small programmable controller runs 80 input/output lines

A compact programmable controller measures only 12 by 4.3 by 4.3 in. yet handles up to 80 input/output lines. Programs stored in complementary-MOS random-access memory or erasable programmable read-only memory enable the basic unit, the F-40M, to offer as many as 40 I/O lines. Two expansion units, the F-20E and F-40E, provide an additional 20 or 40 I/O points, respectively, for a maximum of 48 inputs and 32 outputs.

The output, unlike that of other controllers, has no voltage contact relays. The F-40M does, however, permit the use of triacs or transistors, depending on the application.

A portable programming panel, the F-20P-E, allows users to create control sequences with 14 different commands, entered through keys that relate directly to relay symbols. The panel also provides several function keys that help construct program sequences.

A digital readout and light-emitting diodes for the 14 commands also help in programming. Stored programs can be downloaded from either the ROM or an optional program loader into the C-MOS memory, which is powered by lithium batteries.



Priced at $1,369, the F-40M is available from stock. The programming panel sells for $214, and the F-

20E and F-40E expansion modules go for $393 and $893, respectively.
Mitsubishi Electric Sales America Inc., 3030 E. Victoria St., Rancho Dominguez, Calif. 90221. Phone (800) 421-1132 [373]

Proximity sensors can work even near welding electrodes

The E54 line of inductive proximity sensors—available in front-, right-, left-, and top-sensing models, with pin or cable connectors—can perform even when mounted ¼ in. from welding electrodes. The sensors—whose encapsulated solid-state circuitry and corrosion-resistant housing shrug off moisture, dust, contaminants, heat, shock, and vibration—are protected against short circuits and resist electrical and electromagnetic noise.

Some models are equipped with three light-emitting diodes, which indicate when power is on, when a target is present, and when short-circuit protection has been activated. The third LED is activated when hard or soft short-circuit conditions (from 5.2 to 10 A of instantaneous load current) occur in the presence of a metal target. If the target is removed, the LED is automatically reset.

The units' voltage range extends from 24 to 120 V ac, and their operating-temperature range, from –20° to +70°C. Priced from $85 to $130, the sensors are available now.
Eaton Corp., Cutler-Hammer Products, 4201 N. 27th St., Milwaukee, Wis. 53216. Phone (414) 449-6000 [374]

Card links standard industrial I/O panels to HP-IB computers

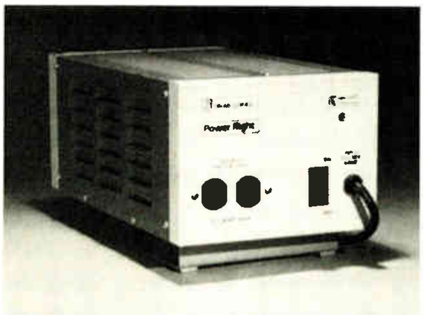
Hewlett-Packard Co.'s series 200 computers and the industrial-automation applications they control have been targeted by Electrologic Inc.'s HP01 interface card, which suits the computer to real-world industrial input/output requirements. The HP01 provides an IEEE-488 bus interface to connect any HP-IB-compatible computer to industry standard I/O module racks made by Opto-22, Crydom, Guardian of California, and other manufacturers.

The card is equipped with a Z8-type processor and firmware for handling and generating interrupts, including programmable interrupt response. Other features include a self-testing routine initiated at power-up, a power-on interrupt, and an on-board digital display to indicate which operating mode and command is currently in process.

Available now in sample quantities, the HP01 sells for $475. Special application firmware is also available, the firm says.
Electrologic Inc., 1359 28th St., Signal Hill, Calif. 90806. Phone (213) 595-0551 [376]

Voltage regulator holds output within 3%, cuts noise 120 dB

The Power Right series of voltage regulators provides accurate voltage regulation, complete isolation from



the power line, and common- and transverse- (normal-) mode noise attenuation for large and small computers, point-of-sale terminals, word processors, and microprocessor-based industrial-control equipment. Available in portable and hard-wire models, the regulators can be used as a dedicated line. They suppress transients and are current-limiting and thereby protect against overloading.

Noise attenuation of the regulators is more than 120 dB, common-mode and more than 60 dB, transverse-mode. The waveform is sinusoidal, with less than 3% harmonic distortion. Output regulation is ±3%, and input line voltage can be as high as ±15%. Even for inputs outside this range, claims the company, Power Right regulators will maintain output voltage.

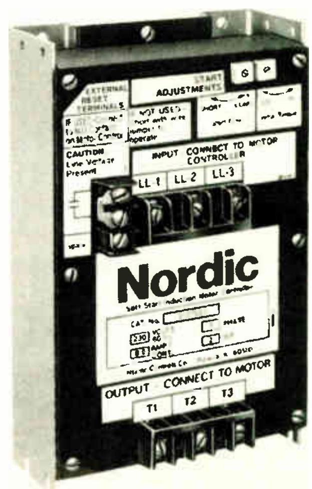
Portable units handle up to 2,000 VA single phase; hard wire models can handle single- and three-phase power up to 30,000 VA. Prices start at $250, and the regulators are available from stock.
Triad-Utrad, 1124 E. Franklin St., P. O. Box 1147, Huntington, Ind. 46750. Phone (219) 356-6500 [377]

Three-phase motor controller provides a soft start-up

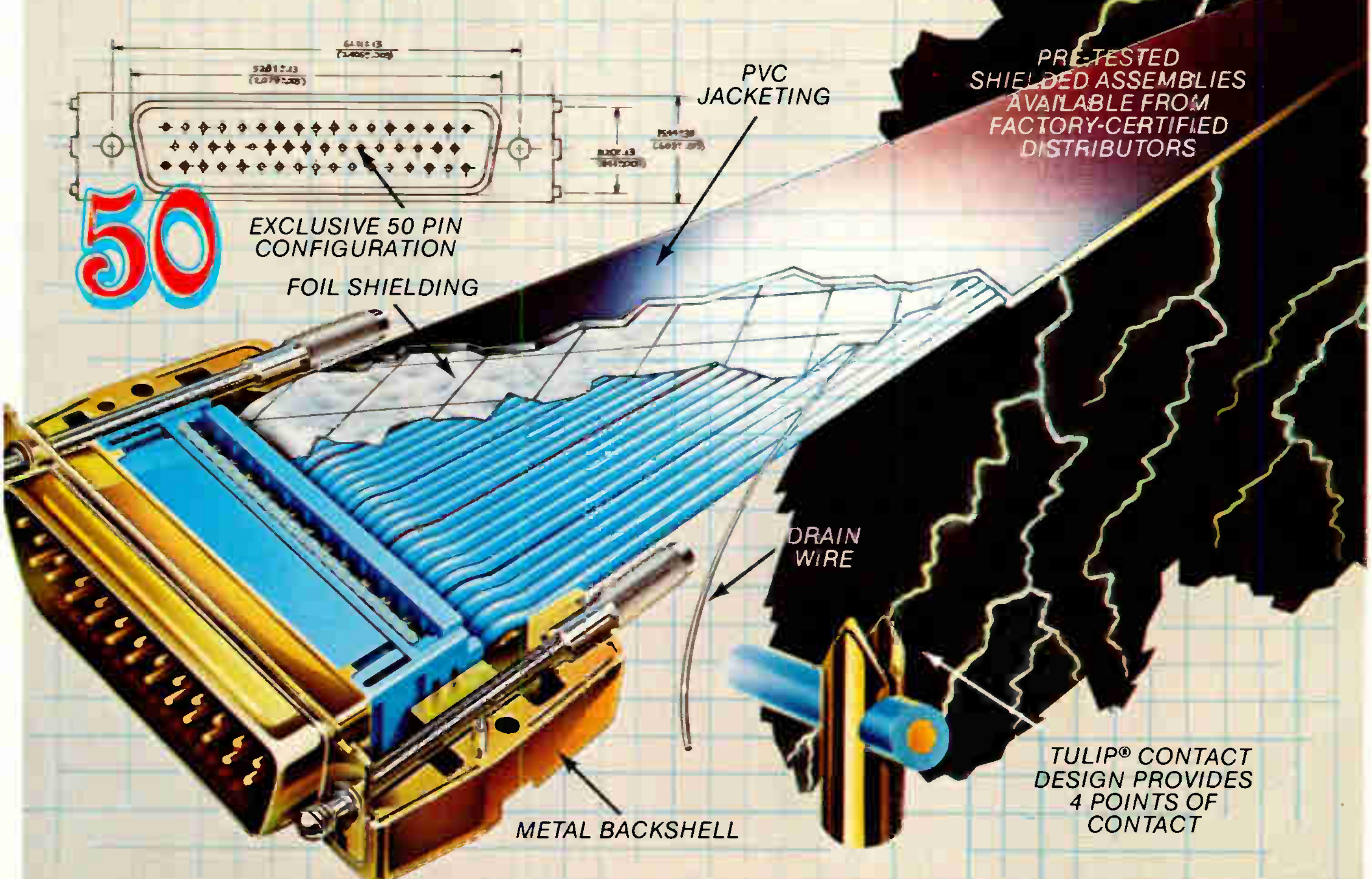
A compact, open-frame, three-phase motor controller gives a reduced-voltage soft start-up to applications in which high starting torques may damage the load or other power-transmission components. Offered for use with any three-phase ac induction motor (of up to 2 hp), in voltages from 200 V to 575 V, the series 21 is suited for machine-tool and materials-handling applications that demand limited starting torque.

The controllers are not sensitive to phase rotation and can be used for reversing, plugging, jogging, and multispeed applications. Series 21 models can easily be installed on a panel between the starter and the motor.

Available from stock, the models range in price from $300 to about $600.
Nordic Controls Co., 155 N. Van Nortwick Ave., Batavia, Ill. 60510. Phone (312) 879-7500 [378]



The Ansley® shielded I/O package: Effective suppression of EMI/RFI spurious signals – today, tomorrow and into the next century.



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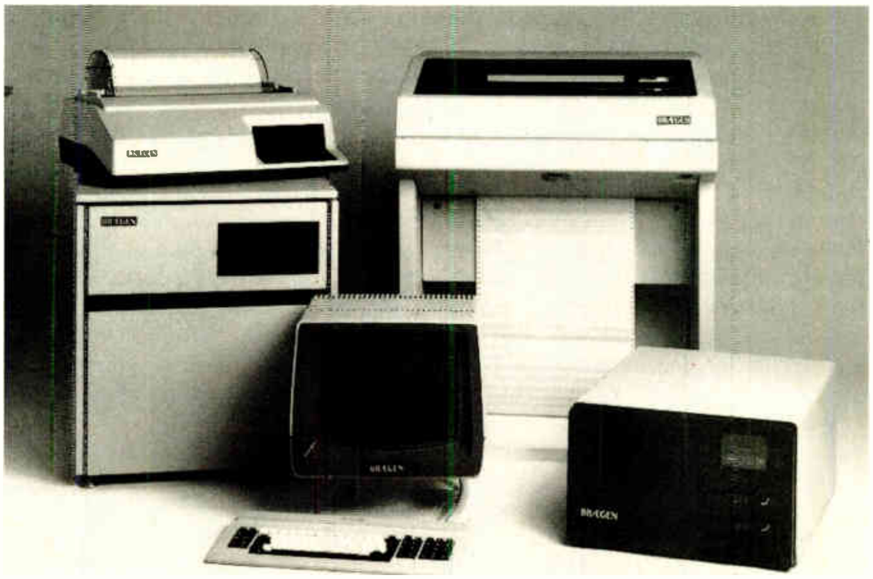
System integration

Controller forms net of terminals

System services up to four host computers and as many as 120 IBM-compatible terminals



Altogether 120 terminals or printers can be supported by a 3270-compatible terminal-cluster controller with its own local network. Made by the Braegen Corp., a supplier of IBM-compatible peripherals, the 8500 controller is a 750,000-instruction/s machine based on a proprietary processor that services up to four host computers and supports remote devices on up to 16 coaxial cables. Each cable can be up to 10,000 ft long.

Also being introduced is a terminal for this network. Called the 8520, it replaces models 2 through 5 of IBM's 3278 series and may be configured from the keyboard by Braegen-supplied software.

The local network implemented by the controller uses a carrier-sense multiple-access protocol with collision avoidance and transmits data at 1.5 Mb/s. Braegen supports the connection of devices with RS-232-C, IBM CIX, and Systems Network Architecture (local type) interfaces.

The controller also extends the personal-computing capability announced earlier by Braegen [*Electronics*, March 24, p. 154] from remote devices that communicate with the host over phone lines to terminals on the local coaxial network. Up to eight users of terminals attached to the local network can operate their terminals as personal computers by making use of the 8500's internal 8086-based microsystem, which runs under the MS-DOS, MP/M, or Xenix operating systems.

But the principal advantage of the 8500, Braegen says, is that it supports more terminals. A user with 120 terminals, for instance, would need four 3270 controllers, at approximately $15,000 each, since each will support only 32 terminals; however, a single 8500 could handle them all.

Collision-proof. The CSMA protocol used by the Braegen local network has been popularized by the Ethernet and Ethernet-type local networks. However, instead of providing collision detection, which requires frequent repeaters in the line, Braegen developed its own collision-avoidance protocol, in which a 20-μs time guard is provided after each message packet to allow for acknowledgment by the receiving station.

In this scheme, any station may transmit at any time. If no return signal is received, the sending station infers that a collision has occurred and resends the packet after a random interval. Braegen says that the technique allows for 70% to 80% line utilization.

Versions of the 8500 controller are available to support all IBM 3274 devices, models A, C, and D. A standard version of the 8500 controller provides a single local network, supporting up to four standard RG62A coaxial lines. Up to four controllers and 60 devices can be connected to the network, and an extra four coaxial lines can be added to it. Moreover, a second logical network can be added to support a maximum of 16 runs of coaxial cable and 120 connected devices.

The 8520 terminal has a 15-in. antiglare tube, refreshed at 30 Hz. The convection-cooled station has a detachable keyboard, and controls on its keyboard allow adjustment of brightness and contrast. A keyword may be assigned to each terminal to allow for security in accessing the host computer.

Prices for the 8500 controller, including the local network, start at $8,500 for a unit supporting four cables and up to 60 attached devices. The 8520 terminal starts at $1,900. However, system prices will vary widely depending on the configuration chosen by the user. The products will be available in the fourth quarter of this year.

The Braegen Corp., 20740 Valley Green Dr., Cupertino, Calif. 95014. Phone (408) 255-4200 [401]

Card lets IBM PCs emulate System 36 remote terminals

Linking a Personal Computer instead of a dumb terminal to an IBM System/34, 36, or 38 can greatly extend these systems, many of which are near the end of their useful lives. Quite a few functions formerly performed on the mainframe can now be transferred to the PC and then uploaded through short-term telephone links to the mainframe.

Blue Lynx, a hardware and software combination that permits the PC to be used in place of a 5251 model 12 remote dumb terminal, makes the connection through synchronous modems or modem eliminators. It requires no other protocol converters or modifications to the operating system. Communications move through switched, leased point-to-point, or multipoint lines at speeds from 1,200 to 9,600 bits/s. The PCs can coexist with clusters of 5251 terminals in a communications network.

What's more, Blue Lynx permits PCs equipped with color graphics to emulate the IBM 5292's color display. A PC must have 64-K bytes of memory if running under PC-DOS release 1.1, a disk drive, a monochrome or color monitor capable of displaying 24 lines of 80 characters each, and a printer connected to a parallel port—and it must have 96-K bytes if running release 2.0.

A second version of Blue Lynx allows the PC to be substituted for 3270 series terminals in a bisynchronous environment. Yet a third lets it replace 3276 model 12 work stations in a Systems Network Architecture/Synchronous Data Link Control environment.

Available from stock, any version costs $690 for the interface card and software, delivered on a disk.

Techland Systems Inc., 25 Waterside Plaza, New York, N.Y. 10010. Phone (212) 684-7788 [403]

Software lets Kaypro computer read disks from other units

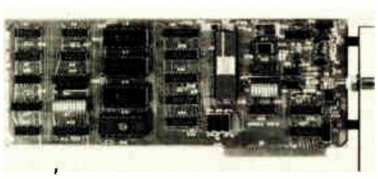
Non-Linear Systems Inc. has introduced software that lets its Kaypro computers read and write disks in 15 different CP/M formats like those of the Osborne I, the Xerox 820 and 820 II, and the TRS-80 model I. The two programs, called UniForm, give Kaypro access to software written for the other machines. Non-Linear Systems, which has licensed the systems from Micro Solutions Inc., of DeKalb, Ill., will package them with Kaypro's CP/M disk.

The first program, Initdisk, allows the user to initialize, or change, a disk to any of the supported formats. These disks can then be used on the appropriate machines. The other, Setdisk, is used to select the desired disk format for the Kaypro's drive B. Once it is used to change a disk to a different format, familiar commands can be used to manipulate the data. Files are easily copied from Kaypro's disk format to the selected format by using the CP/M PIP command. UniForm is available on Kaypro's CP/M S-Basic 5¼-in. disks, retailing for about $25.

Non-Linear Systems Inc., Kaypro Division, P. O. Box N, Del Mar, Calif. 92014. Phone (619) 481-3424 [409]

Controller puts IBM PCs onto Arcnet, supports 2.5-Mb/s rate

The ARC-PC local-network controller module lets users put IBM Personal Computers on the Arcnet modified-token-passing network. The ARC-PC will support up to 255 nodes per network segment while running at a 2.5-Mb/s data rate.



To tuck complete Arcnet protocol handling onto a single board that fits in the PC, the module incorporates the single-chip COM 9026 local-network controller and COM 9032 local-network transceiver circuits. A 2-K on-board data-packet buffer provides four pages of packed storage, and an on-board 8253-programmable interval timer simplifies the software interface by providing user-programmable timeouts. Users can run their own programs thanks to sockets that accommodate an 8-K programmable read-only memory and a 2-K RAM.

Available from stock, the controller costs $495.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, N. Y. 11788. Phone (516) 273-3100 [405]

Gateway device links as many as 8 remote Ethernet networks

The GS/3 internetwork router, a network-gateway device, uses a number of common point-to-point connection media to link as many as eight remote Ethernet networks. This communications-processing system, which supports from two to eight communications lines, has a maximum aggregate data rate of 304 kb/s when fully configured.

The GS/3 can use leased lines, fiber-optic links, point-to-point broadband modems, microwave links, switched lines, or any other point-to-point connection method accessible through an RS-232-C, RS-423, or RS-422 synchronous communications port. Ethernet's distance limitations would seem to make the GS/3 especially useful for linking geographically separate facilities.

The unit comprises three logical modules, each incorporating its own dedicated 68000 microprocessor. The central communications processor contains the XNS Ethernet protocol software, and the Ethernet interface module interfaces the network at the data-link level. The serial interface module contains one to four 68000-based serial input/output boards, each containing a pair of high-speed ports supporting an aggregate data rate of 76 kb/s. When four I/O boards—the maximum—are installed, eight communications lines are available.

Priced at $9,900 with one I/O board, the GS/3 is available now. Each additional board and line adapter costs $1,900. A starter pack-

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Betatronix Inc. is the US-affiliate of novotechnik

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age, including two GS/3 units and transceivers, goes for $17,000.

Bridge Communications Inc., 10440 Bubb Rd., Cupertino, Calif. 95014. Phone (408) 446-2981 [406]

Broadband token-passing net handles video, data, voice

The Videodata LAN/1 local network simultaneously handles video, data, and audio signals. It communicates over a mid- or equal-split broadband cable system that uses the standard Electronic Industries Association 40.2 frequency offset, and its communicating elements are connected to the broadband cable through microprocessor-based Network Interface Units. Two-, four-, and eight-port versions are available.

For network traffic control, the LAN/1 uses a token-passing protocol; individual NIUs capture the circulating token for a preset time slot, when data packets are transmitted. Although it is a broadband system, it operates as a logical-ring or circular-message network. As many as 10,000 users on five channel pairs can be supported by the network, with data rates of up to 2.5 Mb/s. The maximum terminal data rate is specified at 19.2 kb/s.

The LAN/1, available now, costs about $360 per port.

3M Co., P. O. Box 33600, St. Paul, Minn. 55133. Phone (612) 733-9817 [408]

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Tokyo, Japan

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Software

C compiler targets 16032

Code generators, cross compiler, and cross linker virtually eliminate assembly-language programming

With the future in mind, the creators of National Semiconductor's 16000 family of microprocessors designed the architecture to provide compact code generation from compilers for high-level languages. Seizing that opportunity, JMI Software Consultants Inc. will begin shipping next month a C cross compiler with facilities for writing machine-dependent software, including device drivers and interrupt handlers. According to Edward Rathje, the company's vice president, "the C compiler eliminates the need for almost all assembly-language programming."

The C cross compiler comprises both a native-code generator for the host development machine and a code generator for the 16032. Initial support is for computer systems running Bell Laboratories' Unix operating system, Idris, and RSX-11M, as well as VAX computers running VMS, but versions for other popular development systems are planned.

The compiler package also includes a cross assembler that optionally produces complete assembly listings, including addresses, object code, and assembler source code. What's more, the assembler has full macro assembly capabilities. A cross linker that facilitates the construction of random-access and read-only memory combination systems rounds out the package.

Floating-point support is provided in conjuction with the 16081 floating-point unit, currently available in sample form. A cross-reference listing capability, initially unavailable, will be ready within the next six months, Rathje points out.

The cross compiler is based on the family of C compilers from Whitesmiths Ltd., which support the complete C language as defined by Kernighan and Ritchie. It has been used to adapt the C executive [*Electronics*, Jan. 27, p. 134], also available from JMI, to National's 16000 development board. The implementation under the 16032 is one of six different central processing units supported by the C executive. (The others are the LSI-11; the 68000; the 8080, 8085, and Z80; the 8086 and 8088; and the 6809.)

This C executive real-time monitor, itself written in portable C language, incorporates a complete portable run-time library, including formatted input/output, string handling, dynamic memory allocation, and data-conversion routines. "The exercise of porting a real-time operating system along with an extensive library provides a clear demonstration of the advantage of using C as a portable system-implementation language," argues Rathje (see table).

When available next month, the C cross assembler will sell for $2,500, including documentation, media, and shipping. The compiler can also be used with JMI's recently announced Bastoc, a Basic to C translator, to provide support for multiple dialects of Basic on the 16032.

JMI Software Consultants Inc., 1422 Easton Rd., Roslyn, Pa. 19001. Phone (215) 657-5660 [381]

SIZE OF C EXECUTIVE AND RUN TIME LIBRARY FOR VARIOUS HOST PROCESSORS

Central processing units	Minimum kernel size (bytes in decimal)	C portable library size (bytes in decimal)
68000	6,490	5,936
16032	5,765	5,130
LSI-11	5,024	5,160
6809	5,861	6,220
8080	9,165	10,214
VAX/780	not available	4,944

Accounting package for VAX lets users set conventions

A general-accounting package based on accounting principles rather than on a limited number of rigid conventions is now available for VAX computers running the VMS operating system. Called Dolars (for Distributed On-Line Accounting and Reporting System), the system permits users to formulate their own conventions, and in virtually limitless combinations, the company says.

The Dolars packages include financial planning and reporting, general ledger, capital-items accounting, accounts receivable and payable, and facilities, property, or relational–data-base management. Each system may also be used with Digital Equipment's popular layered products, like All-In-One and Datatrieve.

Dolars packages are available individually and range in price from $19,000 to $60,000.

Landmark Software Systems, 155 W. Main St., Somerville, N. J. 08876. Phone (201) 722-5100 [385]

Optimized Pascal compiler for Unix meets ISO specs

An optimizing compiler that is fully integrated into the Unix operating system on the 68000, Pascal-2 produces smaller, faster code than C, Fortran 77, or other Pascal compilers on Unix. It performs nine types of code optimizations usually performed only by language compilers on large machines.

Pascal-2 programs may call subroutines written in C, Fortran 77, or assembler, enabling the user to take advantage of existing Unix software. Also, the compiler's language extensions provide sophisticated input/output handling and access to low-level Unix operations.

An interactive source-level debugger, an execution profiler, program and text formatters, and cross references provide additional program development tools. The debugger sim-

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plifies program development, allowing the programmer to solve logic errors in applications interactively, at the level of the source program. The profiler produces a source listing showing the number of times each statement of code is executed to help identify execution bottlenecks.

Pascal-2 supports all capabilities of standard Pascal and is written to conform to Level 1 of the draft international Pascal standard (International Standards Organization's dp7185.1), which includes conformant array parameters. Checks on type compatibility during compilation ensure that data types conform to the ISO standard.

The license fee for the Pascal-2/Unix system, including the debugger, other tools, and a year of software support, is $1,650. The compiler alone sells for $600. It will be available next month.

Oregon Software, 2340 S. W. Canyon Rd., Portland, Ore. 97201. Phone (503) 226-7760 [383]

Unix programs proofread writer's work, analyze its style

Western Electric is licensing for use under its Unix operating system a set of computer programs, called Writer's Workbench, that proofreads and edits copy. More than two dozen different Writer's Workbench programs check spelling and punctuation, analyze the writer's style, and provide information about principles of good writing. The programs can be used separately or in various combinations, or they can be used together, by means of a single command.

Writer's Workbench programs fall into four major categories: proofreading, style-analysis, information, and utility programs, the last of which allow writers to tailor programs to fit special needs. For example, the models with which writing is compared can be individually selected.

Proofreading programs check spelling, punctuation, wordy phrasing, misused words, split infinitives, and repetitive words. Style analysis is based on advice from reference books and on the results of research on the psychological bases of comprehension, according to the firm.

The word-use program, for example, explains the difference between the words "effect" and "affect" and when to use "which" and "that." The prose program compares a writer's style with one of two sets of standards, one derived from well-written training materials and the other from good technical reports. Priced at $4,000 for the first central processing unit and $1,600 for each subsequent CPU at the same site, the Writer's Workbench is available now. A 50% discount is offered to educational institutions.

Western Electric Software Sales and Marketing Group, P. O. Box 25000, Greensboro, N. C. 27420. Phone (919) 697-6530 [384]

CAD package translates schematics into VLSI circuits

Employing silicon-cell–compiler technology, an integrated computer-aided engineering and design package is capable of translating schematics into custom very large-scale integrated circuits. The Logicomp compiler system includes all the tools needed to enter a system schematic, verify the design through simulation, build a corresponding physical layout by the use of its Cell Compiler library, and verify that the interconnection and function of the physical layout correspond to the schematic.

Other major elements in the system include a schematic editor and a logic and timing simulator. The first provides the basis for design synthesis, network entry, and documentation. The second verifies the correctness of designs created with the schematic editor or those created directly from the physical layout.

The software sells for $100,000 for use on VAX computers or for $50,000 for use on Apollo computer systems. The company can provide a turnkey CAD system including the software on an Apollo Domain work station.

VLSI Technology Inc., 1101 McKay Dr., San Jose, Calif. 95131. Phone (408) 942-1810 [389]

Sperry leads the way in ruggedized computer technology

engineering careers

Through 1983, Computer Systems and the Defense Systems Division have added substantially to their base of new business. As an industry leader in the development, manufacture and marketing of ruggedized computers, communications and signal processing equipment featuring advanced LSI, VLSI and VHSIC technologies, this Sperry division is really on the move.

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- software - software development, CAD/CAM, software tools and technology development, ATE/diagnostics, and microprogramming

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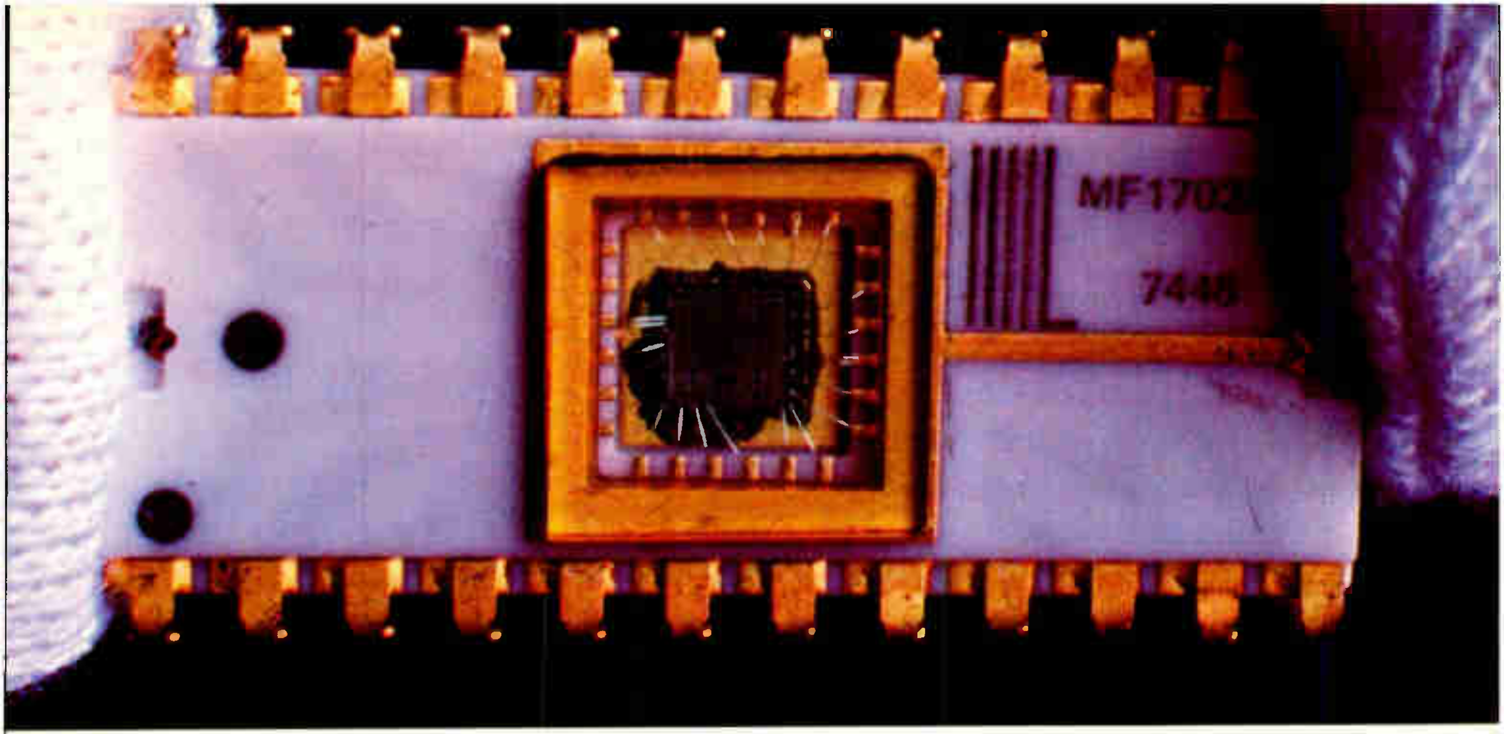

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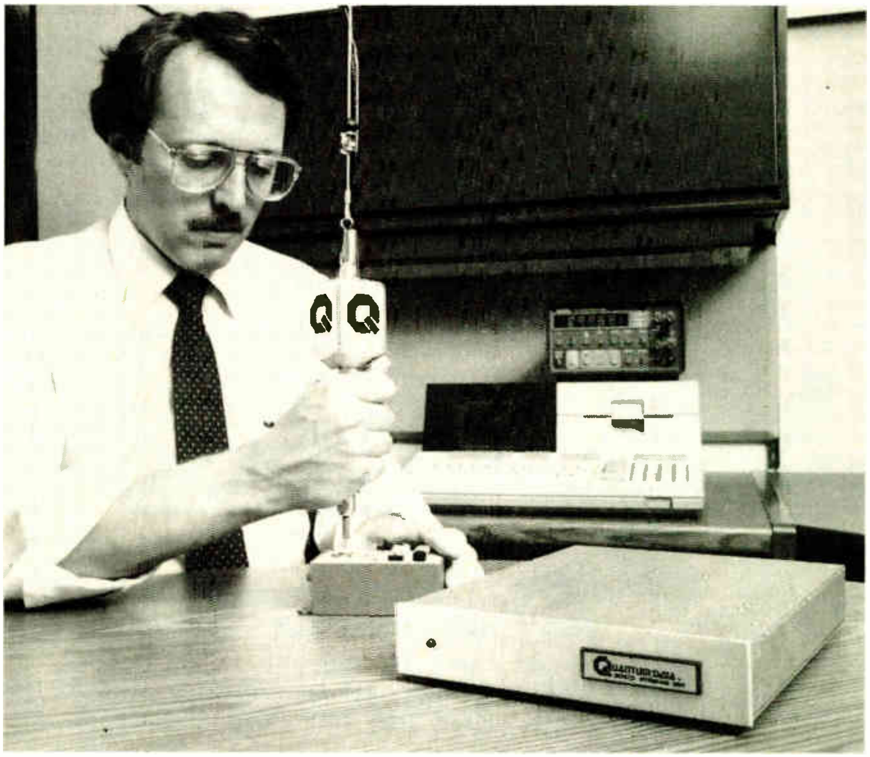
Packaging & production

Smart tool sets up pots

Motorized screwdriver adjusts trimmers and tuners under control of computerized test-system



Testing and precise final adjustment of potentiometers, trimmer capacitors, and tunable coils in power supplies and other control devices can be very time-consuming. All too often, the tasks cause a bottleneck in factory operations involving electronic equipment.

Addressing that problem is the CAT 2000 (for computerized alignment tool) from Quantum Data Inc. Consisting of a motorized hand-held screwdriver, a foot switch control, and a rack-mounting interface box for connecting both to an IEEE-488 bus, the system makes possible automated adjustment under microprocessor control.

At $2,295 in single-unit quantities, the CAT 2000 is a cheaper solution than the development of a custom automatic adjustment system and will provide a quick return on investment, the company contends. Indeed, according to Quantum Data president Al Jorgensen, a similarly priced but less capable unit offered by the firm since 1981 has paid for itself in direct labor savings within 60 days at many customer locations.

In one case, the output of adjustment station operators reportedly increased by 65% using the earlier system, called the RS 1000, while the rate of misadjusted pots dropped from 20% to 5%. Depending on the application, even better results can be expected with the CAT 2000, says Mark Stockfisch, Quantum Data vice president of engineering.

The CAT 2000 relies on a 16-bit 8088-2 microprocessor to control the screwdriver tip, directed by the user's in-house computer over an IEEE-488 bus. After checking measurements made by instruments also on the bus, the computer tells the CAT 2000 in which direction and how many degrees the tip should turn for proper adjustment of a device. An adjustment station operator uses the foot pedal to operate the CAT 2000, which makes the adjustments at speeds of up to 5 revolutions/s to an angular resolution within 0.1°. This is five times faster and nearly four times more precise than the RS 1000, which used an 8-bit Z80A for control, a less precise stepper motor, and mechanical gearing.

Limiting torque. Thanks in part to the improved software capabilities of the 16-bit microprocessor, the CAT 2000 uses direct-drive electronic gearing to eliminate backlash and improve reliability. Additional CAT 2000 features not found on the earlier system include variable speed control and torque limiting from 0 to 20 oz-in. Dynamic torque on the CAT 2000 is specified at 15 oz-in. continuous and 20 oz-in. momentary.

CAT 2000 users will be required to write their own software to integrate the unit into their system. But in most cases where a computerized measurement system already exists, that job will be small, typically requiring only about 20 lines of Basic code, says Stockfisch.

The rack-mounting CAT 2000 interface box comes with cord attachments for the foot pedal and hand-held tool and measures 1.75 by 8.5 by 11.5 in. The CAT 2000 will be available in September.

Quantum Data Inc., 455 E. Kehoe, Suite 104, Carol Stream, Ill. 60188. Phone (312) 668-3301 [391]

Seven modular units build conveying and handling system

Built from seven standard modules, an automated conveying and handling system can be used with either carrier or pallet-type production lines for continuous, on-line assembly of printed-circuit boards, wave soldering, lead cutting, cleaning, and inspection. The conveying and handling system can be tailored to small assembly operations or to large, full-factory, multi-assembly lines under complete computer control.

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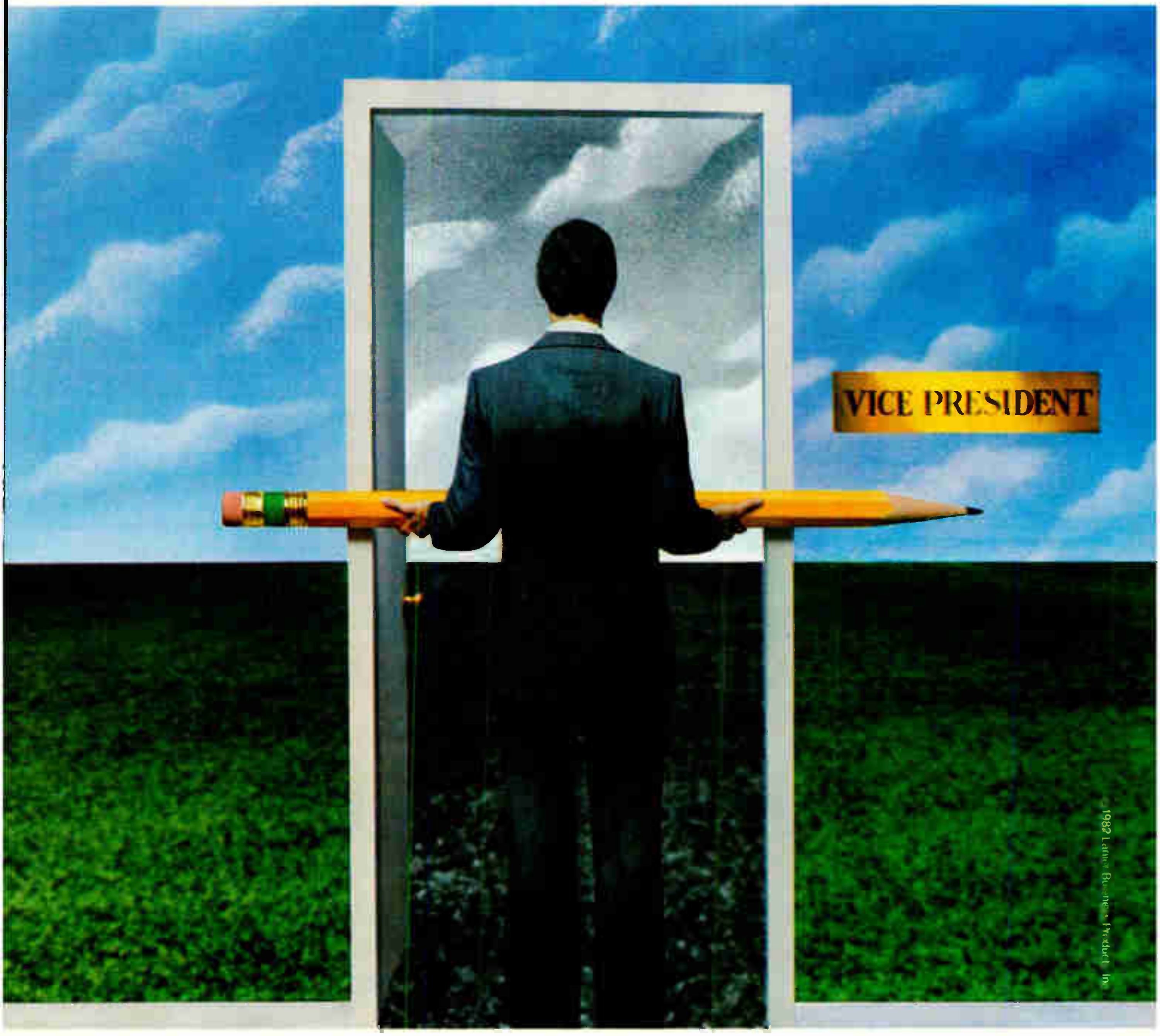

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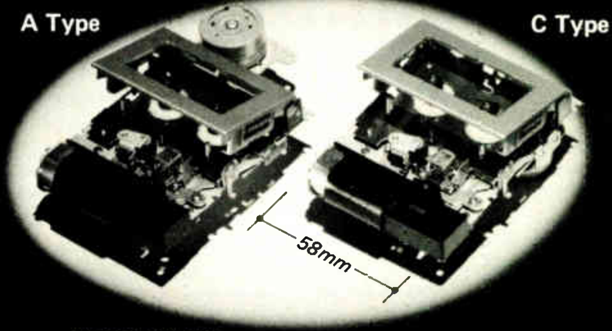

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  B Type 78 x 86 x 22.5 mm
  C Type 78 x 58 x 33.5 mm
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Circle 176 on reader service card

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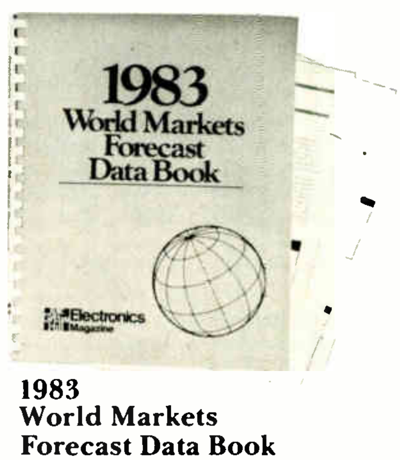

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cumulator, and inclinable transfer—are available in four standard widths to accommodate boards up to 12, 15, 18, and 24 in. Except for the inclinable transfer, which is mechanical, all modules are completely automated and electronically controlled by a logical sequence of limit switches located within an independent central control station.

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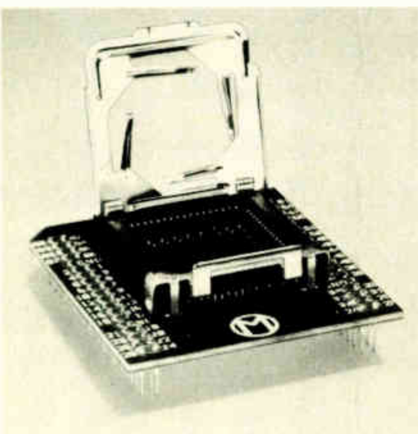
Electrovert USA Corp., 399 Executive Blvd., Elmsford, N. Y. 10523. Phone (914) 592-7322 [393]

Adapters hold chip-carriers on wire-wrapped boards

Aided by the series 300 adapter plugs, 68-pin leadless chip-carriers of Joint Electron Device Engineering Council type A can plug into printed-circuit boards or wrap-type universal logic boards. The adapter plugs are compatible with a number of the firm's logic boards, including its Multibus, Q-bus, and VME-bus versions.

A specially designed socket with grounded cover and an on-board pin-side ground plate is said to reduce noise. The adapter has four terminals that are dedicated to grounding only. Gold-plated brass terminals on increments of 1/10 in. have a built-in standoff to prevent short-circuiting terminals or circuit traces beneath the device.



Priced at $43 each in lots of 100, the adapter plugs are available in two to four weeks.

Methode Electronics Inc., Logic Board Division, 7444 West Wilson Ave., Chicago, Ill. 60656. Phone (312) 867-9600 [395]

Glass plate allows viewing of wave-soldering process

The Lev Chek, a 3/16-in. tempered borosilicate glass panel, similar in size and shape to a printed-circuit board, permits topside observation of the actual wave-to-board contact for precise analysis of wave-soldering operations. The diagnostic tool aids the user in monitoring flux coverage, wave shape and turbulence, and conveyor leveling. It also helps keep tabs on the angle of contact, the intermixing of flux or oil across the board, the displacement fluxing action, the direction of solder flow, and the meniscus velocity at the breakaway trailing edge of the solder contact.

Heat-resistant gauge markings are printed on the top surface of the Lev Chek glass in ½- or 1-in. grid patterns on the small and large models, respectively. The specially tempered glass is designed for wave-soldering temperatures of 500° to 525°F. Normal transport speeds across preheaters are acceptable, and stationary dwell time on a wave, for observation, can last up to 5 min.

Lev Chek gauges are available in sizes ranging from 6 to 18 in., but custom sizes can be delivered. A standard 8-by-10-in. model sells for $24.15 and can be delivered in two weeks.

Assembly & Production Aids, 399 Executive Blvd., Elmsford, N. Y. 10523. Phone (914) 592-7322 [394]

Electron microscope works under low-voltge conditions

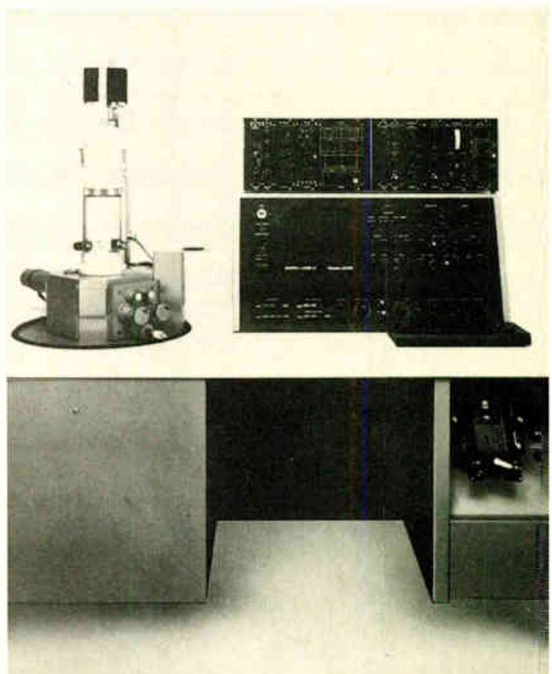
Focused on semiconductor researchers, the Nanolab LE2100 scanning electron microscope, a low–beam-energy instrument, conducts nondestructive, routine examinations of materials that previously required sample coating with conductive metals. The LE2100's magnification accuracy and image linearity have extended to 750 V, which permits quantitative image measurements under low-voltage conditions.

The microscope's lanthanum hexaboride single-crystal emitter electron gun provides 10 times the electron emission of conventional tungsten sources, allowing for high-resolution inspection of semiconductors, glasses, photographic film, polymer coatings, plastics, and other insulating or easily damaged materials.

A microprocessor-controlled digital magnification system, full-screen alphanumerics, and an integral feature-measuring system allow the microscope to work accurately at beam energies of less than 1,000 V. Low-voltage compensation, independent condenser lenses, and a constant–emission-current circuit further enhance the microscope's abilties.

Micrograph resolution is guaranteed to 50 Å and magnification ranges are from 25× to 300,000×.

Bausch & Lomb, 2930 Baseline Rd., Nepean, Ont., Canada K2H 8T5. Phone (613) 820-9437 [397]



advancing the technologies

MOS and bipolar

At Computer Systems we've shown the ability to blend imagination with practicality and cost effectiveness. We've invested heavily in human resources and laboratory and test equipment for the development and fabrication of integrated circuit technology for use in Sperry applications. Our Semiconductor Operations in Minnesota now spearheads high density MOS and high performance bipolar silicon circuitry activities.

We've recently expanded into a new 250,000 sq. ft. facility in the Sperry Park complex and there are currently a number of key positions available. If you are currently involved in a semiconductor environment and are interested in joining a team that's over 500 strong and growing, consider the following opportunities:

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- PRODUCT ENGINEER
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SPERRY

Products newsletter

An intelligent recorder with 17,990 speeds uses a thermal print head

Thermal–print-head and microprocessor technologies team up in Gulton Instruments' Computrak 6100, an intelligent recorder that plots wave patterns from as many as six analog signals. With the 6100, users can select **any speed from 0 to 5 mm/s, in 1- mm/hr increments—17,990 discrete chart speeds in all.** They can also program chart speed, engineering units, sensitivity, scale, and even the dimensions of the grid matrix on which data is charted, thus eliminating the need for preprinted forms. A 4-in. ceramic print head with a 100-dot/in. resolution prints thermally on 5-in. paper. The East Greenwich, R. I., firm will show its recorder at October's Instrument Society of America show. A three-channel version will sell for $2,900.

Function generators claim accuracies within 0.1%

Wavetek, in San Diego, has introduced two closed-loop frequency-stabilized function generators, the first members of a new family of simplified instruments. For less than $1,000, models 21 and 22 offer frequencies that range from 100 μHz to 11 MHz and are accurate to within 0.1%—**an order of magnitude better than any comparable instrument, claims Wavetek.** The units' output varies less than ±0.1% of the full-scale range at 0.5°C for more than 10 min. A counter and an error-correction circuit called Delta F control the 3½-digit liquid-crystal digital readout.

Thermocouple amp handles temperatures from −200° to +1,200°C

Analog Devices Inc.'s monolithic AD595 thermocouple amplifier, which can monitor temperatures from −200° to +1,250°C, accepts K-type thermocouple signals and delivers an output of 10 mV/°C. **Adding to the part's accuracy and reliability are on-chip features like cold-junction compensation,** an instrumentation amplifier with differential inputs for rejecting common-mode noise on the thermocouple leads, and a circuit that flags broken thermocouple connections. Packaged in a 14-pin Cerdip, the AD595 comes in two versions, one calibrated for initial accuracy of ±1°C and another for ±3°C. In lots of 100, the two models cost $14.50 and $9.50, respectively. Delivery from the Norwood, Mass., firm is from stock.

Wang's latest mini has 2.5 gigabytes of storage

The newest addition to Wang Laboratories Inc.'s VS family of minicomputers offers 32-bit processing in a compact package whose base price is $63,000. Fully compatible with all the Lowell, Mass., company's VS products, **the basic VS85 system comes equipped with 1 megabyte of main memory,** the VS operating system, a 16-port serial input/output processor, and a 48-K-byte archiving work station and compiler. The VS85 supports up to 32 concurrent users and can be configured with as much as 4 megabytes of main memory and 2.5 gigabytes of mass storage.

Software evaluates wafer's topography

A software option for Tencor Instruments' Flatgage wafer-flatness test system allows the user to determine which part of a wafer should lie within an automated stepper's field of focus. In 60 seconds, the Mountain View, Calif., firm's program, called Local Slope, **checks a 100-mm wafer and accepts or rejects the wafer** for further processing. The program sells for $4,500 and is available in 60 days.

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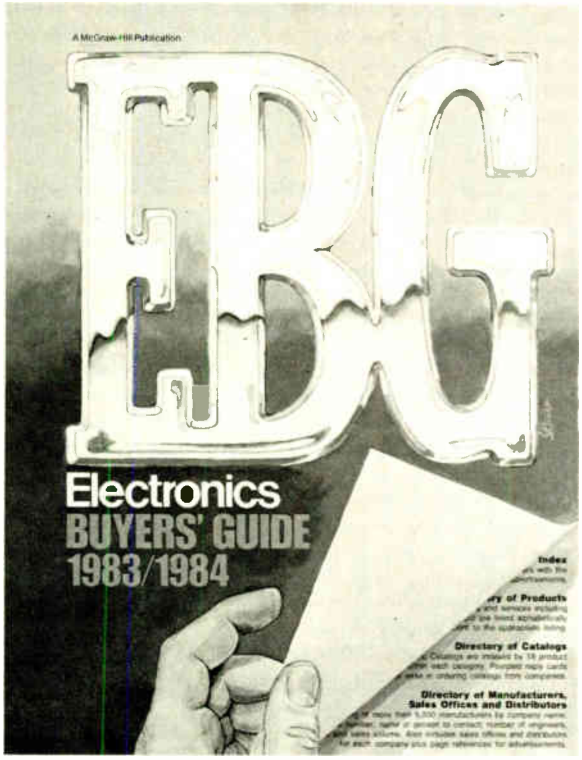

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Career outlook

Sales: novices need not apply

For electronics engineers who may be eyeing the sales department as a way out of a career rut, a veteran recruiter specializing in this field has good news and bad news. First, the good news: "There are many jobs—at least twice as many as I can fill," counsels Joel Rice, based in Los Angeles for Sales Consultants International. And now the bad news: "You will have to take a 50% pay cut to start, until you prove you can sell."

Gone, gone are the days when electronics manufacturers were so eager to find technically qualified sales representatives that anyone with a bachelor of science degree in electrical engineering or a scientific degree could get a good job, Rice adds. Moreover, the recession, as well as the high cost of converting engineers into sales reps or of giving salesmen some technical polish, have killed off the training courses most firms operated for years. "No companies are doing that today," he explains.

As a result, "companies are looking for and demanding experience. For example, minicomputer firms want specific minicomputer background. OEMs [original equipment manufacturers] won't have any part of end-user salespeople." Rice believes that the demand for specialized experience reflects a maturing marketplace—and also the recession, which has given employers a wider choice.

It takes time. One aspect of computer marketing that technical people do not understand is the amount of time it takes to sell a mainframe, as opposed to a minicomputer or a personal computer—a year or longer for a mainframe, about six months for a mini, and three months or less for a personal computer. "It makes a lot of difference how salesmen manage their own time," says Rice. Selling a personal computer takes many more calls, but a mainframe deal requires a more detailed technical presentation and permits a leisurely schedule.

Demand for sales reps largely reflects hot business. At the moment, the largest numbers of new hires are being snapped up by software companies of all kinds. These outfits can take on so many people because their net profit margins run at 18% to 20% of sales, about double those of hardware companies. Printers make up another lively sales area. Dramatic improvements in the print quality of less expensive units have opened up many user doors.

In addition, now that equipment for the office of the future is finally coming to market—after years of promises—Rice expects strong demand for sales personnel who understand how these separate terminals, electronic-mail components, and telecommunications gear operate as a system.

Small will prosper. Although such major firms as IBM, Wang, and Hewlett-Packard will lead, smaller companies offering replacements for individual pieces of equipment look forward to growing fat, too. They are preparing for the feast by hiring seasoned sales personnel, says Rice.

Starting jobs bring in $22,000 to $35,000, depending on the field and the new hire's record, but these salaries can escalate quickly—for reps who hit their stride quickly. Employment-agency fees are paid by the employer and usually run about 30% of a year's salary.

Rice deals with computer-oriented firms, from the largest down to start-up operations, from vice president to entry level. He regularly puts in 12-hour days and personally earns more than $250,000 a year.

Sales Consultants International is the sales-recruiting arm of Management Recruiting International, which has some 400 offices and grosses $125 million a year. Claiming that "we never have a recession in this business," he notes that activity is up some 40% over a year ago, with nearly 70 positions left to go begging in his office alone.

Although he deals with technically educated people in a field marked by rapid technological development, Rice says that success still depends on old-fashioned salesmanship and on qualities that are instinctive, not learned. "Charisma is still very important," he says. —**Larry Waller**

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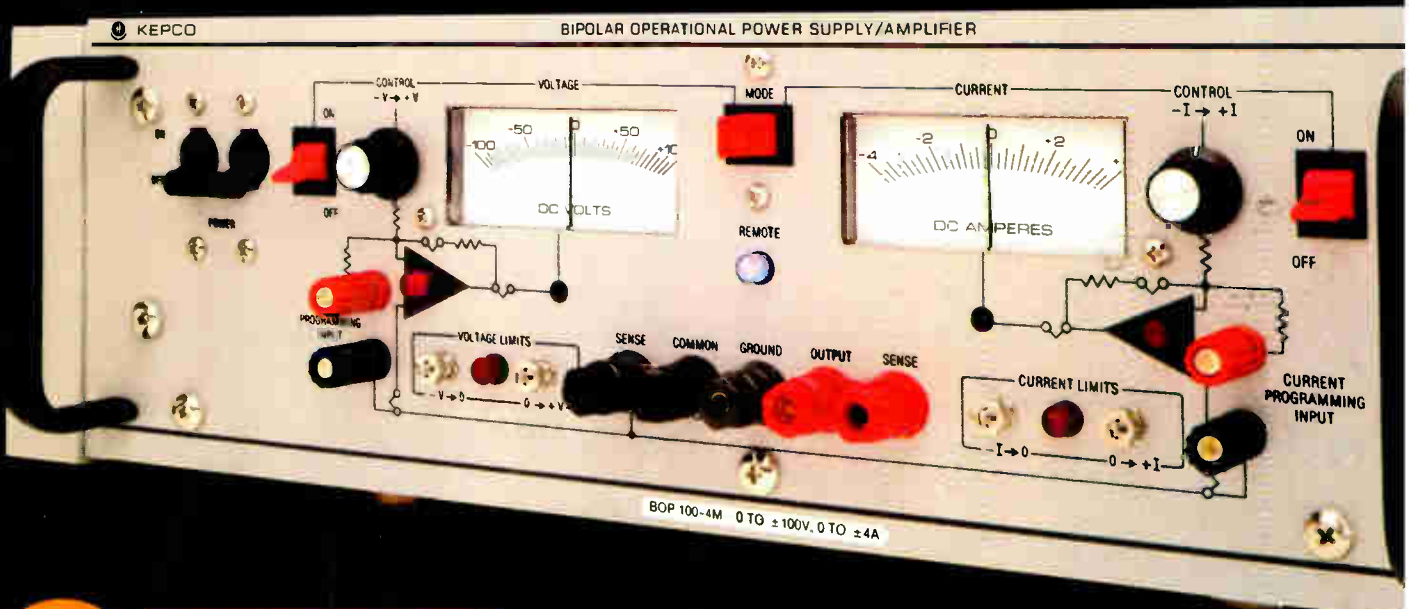

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