ADQ36-PXIE Datasheet

The ADQ36-PXIE is a high-end 12-bit quad-channel flexible data acquisition board optimized for high channel-count scientific applications. The ADQ36-PXIE features:

- **Two analog channels at 5 GSPS included**
- **Four analog channels at 2.5 GSPS per channel included**
- **12 bits resolution**
- **7 GByte/s sustained data transfer rate to GPU**
- **7 GByte/s sustained data transfer rate to CPU**
- **Two external triggers**
- **General Purpose Input/Output (GPIO)**
- **Open FPGA for real-time signal processing**
- **Firmware option for averaging of records**
- **Firmware option for pulse analysis**
- **Synchronization of large installations through daisy chain concept**

1 ORDERING INFORMATION

ADQ36-PXIE is available with a set of options. Follow the procedure to configure the ADQ36-PXIE. Start with the hardware configurations. These are factory installed and cannot be changed through software commands.

1. DC-coupled analog front-end is standard.
2. Analog bandwidth 2.5 GHz is standard
3. PXIe interface is standard.

Select the firmware options. The firmware FWDAQ is always included. Additional firmware files are distributed as files and can be loaded into the board at any time.

4. Data acquisition firmware **-FWDAQ** is always included
5. Select one or several of available firmware packages, **-FWATD**, **-FWPD**.
6. Select to activate channel combination option for dual-gain pulse detection, **-LICPDRX**.
7. Select accessories, open FPGA development kit **DEVDAQ**, **-DEVPD**[1].
8. Select extended warranty **-W5Y**[2].

The open FPGA is accessed through the design project for each firmware. For **-FWDAQ**, the development kit is **DEVDAQ**. For **-FWPD**, the development kit is **DEVPD**. The **DEVDAQ** is a one-time purchase. The FPGA bit files built from the design project can be used on any ADQ36-PXIE with a valid FWDAQ license (included on all units).

[1] DEVPD is available in 2024. Contact Teledyne SP Devices for more information.

[2] Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. The option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices. Warranty extension must be ordered before included 3 years warranty is expired.

2 ADQ36-PXIE INTRODUCTION

2.1 Features

- Two and four analog input channels
- 5 and 2.5 GSPS sampling rate per channel
- 12 bits resolution
- DC-coupled with 2.5 GHz bandwidth
- Programmable DC offset
- Internal and external clock reference
- Internal and external sampling clock
- Clock reference output
- Internal and external triggers
- 8 Gbyte data memory
- 7 GByte/s sustained data streaming to CPU and GPU
- Data interface PCIe Gen3 x8
- Averaging firmware FWATD
- Pulse analysis firmware FWPD

2.2 Applications

ADQ36-PXIe is intended to be used primarily in high channel-count systems.

- LIDAR
- Beam Position Monitor
- High energy physics
- Scientific instruments

2.3 Advantages

- A compact high-performance digitizer that optimize the system solution
- Real-time processing and high data throughput
- Teledyne SP Devices' design services are available for fast integration to reduce time-to-market

2.4 System design optimization; open FPGA and streaming to CPU and GPU

High-performance data acquisition systems require high speed real-time analysis. ADQ36-PXIE offers a variety of options for efficient system design:

Streaming to GPU
ADQ36-PXIE supports up to 7 GByte/s peer-to-peer streaming and streaming via pinned buffer to GPU. A GPU offers a powerful platform for implementing application-specific signal processing algorithms.

Streaming to CPU
ADQ36-PXIE supports up to 7 GByte/s to host computer. Implementing the application-specific algorithms in the CPU results in an efficient system.

Open FPGA for real-time processing
ADQ36-PXIE offers an open FPGA for implementation of the application-specific computations in the FPGA. This gives the most compact system design. Firmware development kit is ordered separately.

3 TECHNICAL DATA

Technical parameters are valid for ADQ36-PXIE operating with firmware FWDAQ. All parameters are typical unless otherwise noted.

Table 1 Analog input (front panel label A, B, C, and D)

Parameter	Condition	Min	Typical	Max	Unit
Basic parameters					
Number of channels	4 channels mode		4		
Sampling rate per channel	4 channels mode		2.5		Gsample/s
Number of channels	2 channels mode		2		
Sampling rate per channel	2 channels mode		5		Gsample/s
Bandwidth -3dB	Standard config.		2.5		GHz
Input range			0.5		Vpp
Input impedance			50		Ω
Coupling			DC		
Connector type		SMA			
Programmable DC-offset					
DC-offset range		-0.25		+0.25	V
Dynamic performance 4 channels mode at 2.5 GSPS					
Cross talk	< 800 MHz		-70		dBFS
Noise power density	0 to 1.25 GHz		-148		dBFS/√Hz
SNR	260 MHz, -1dBFS		54		dBc
SFDR	260 MHz, -1dBFS		65		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.8		bits
ENOB relative full scale	260 MHz, -1dBFS		8.8		bits
ENOB relative full scale	810 MHz, -1dBFS		8.8		bits
ENOB relative full scale, using FIR filter[3]	260 MHz, -1dBFS		9.0		bits
Dynamic performance 2 channels mode at 5 GSPS					
Cross talk	< 800 MHz		-80		dBFS
Noise power density	0 to 2.5 GHz		-150		dBFS/√Hz
SNR	260 MHz, -1dBFS		53		dBc
SFDR	260 MHz, -1dBFS		60		dBc
ENOB relative full scale	10 MHz, -1dBFS		8.7		bits
ENOB relative full scale	260 MHz, -1dBFS		8.6		bits
ENOB relative full scale	1625MHz,-1dBFS		8.1		bits
ENOB relative full scale, using FIR filter[3]	260 MHz, -1dBFS		9.0		bits

[3] Programmable FIR filter enabled. Coefficients [57,92,–279,21,704,–720,–1163,4127,10784]/2^14

Table 2 Clock generator and front panel CLK connector.

Parameter	Condition	Min	Typical	Max	Unit
Internal clock reference					
Frequency			10		MHz
Accuracy			±3 ±1/year		ppm
Internal sampling clock generator					
Frequency range 1	2 channels	2440	2500	2500[4]	MHz
Frequency range 2	2 channels	1473		1627	MHz
Frequency range 1	1 channel	4880	5000	5000	MHz
Frequency range 2	1 channel	2946		3254	MHz
External clock reference input (from front panel CLK connector)[5]					
Frequency		1	10	500	MHz
Frequency [6]	Jitter cleaner enabled	10 -10 ppm	10	500 +10 ppm	MHz
Frequency	Delay line used		10	100	MHz
Delay line tuning range			500		ps
Signal level		0.5		3.3	Vpp
Input impedance	AC		50		Ω
Input impedance	DC		10k		Ω
Input impedance (high) [7]	AC		200		Ω
Clock reference output (on front panel CLK connector)					
Frequency			10		MHz
Signal level	Into 50-Ω load		1.2		Vpp
Output impedance	AC		50		Ω
Output impedance	DC		10k		Ω
External direct sampling clock input (from front panel CLK connector)[8]					
Frequency [9]		1000		2505	MHz
Signal level		0.5		3.3	Vpp
Impedance	AC		50		Ω
Impedance	DC		10k		Ω
Physical connector label CLK					
Connector type		SMA			

[4] The software setting limit. The tolerance with external clock reference is up to 2505 MHz.
[5] Using a reference from an external source to synchronize the ADQ36-PXIE to the external source.
[6] The jitter cleaner requires the reference frequency to be a multiple of 10 MHz within ± 10ppm.
[7] Software-selectable high-impedance mode.
[8] Using an external clock while bypassing the internal clock generator.
[9] In single-channel mode, the sampling frequency is 2 times the external clock frequency.

Table 3 Front panel TRIG connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type		SMA			
Used as input (or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [10]	DC		500		Ω
Signal level	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [11]	As trigger		50		ps
Update rate [11]	As GPIO			156.25	MHz
Used as output (or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

Table 4 Front panel SYNC connector (may be used as a trigger source with larger timing grid)

Parameter	Condition	Min	Typical	Max	Unit
Connector type			SMA		
Used as input (or GPIO)					
Impedance	DC		50		Ω
Impedance (high) [10]	DC		500		Ω
Signal range	50-Ω mode	-0.5		3.3	V
Adjustable threshold	50-Ω mode	0		2.8	V
Signal level	High impedance	-0.5		5.5	V
Adjustable threshold	High impedance	0		2.3	V
Pulse repetition frequency	As trigger			10	MHz
Time resolution [11]	As trigger		3.2		ns
Update rate [11]	As GPIO			156.25	MHz
Used as output (or GPIO)					
Impedance	DC		50		Ω
Output level high VOH	Into 50-Ω load	1.8			V
Output level low VOL	Into 50-Ω load			0.1	V
Pulse repetition frequency				156.25	MHz

[10] Software-selectable high-impedance mode.

[11] Timing properties are valid for 2.5 GSPS in 2 channel mode and 5 GSPS in 1 channel mode. Timing properties scale linearly with sampling frequency.

Table 5 Front panel GPIO connector

Parameter	Condition	Min	Typical	Max	Unit
Connector type			HD-DSUB 44		
Single-ended GPIO signals					
Number of signals			12		
Input level high		2			V
Input level low				0.8	V
Output level high	100 uA	3.1			V
Output level low	100 uA			0.1	V
Output level high	8 mA	2.5			V
Output level low	8 mA			0.6	V
Update rate per pin [12]				156.25	MHz
Differential LVDS signals					
Number of inputs			4		
Number of outputs			3		
Update rate per pin [12]				156.25	MHz

Table 6 Environment and mechanical parameters

Parameter	Condition	Min	Typical	Max	Unit
Power and temperature					
Power consumption [13]	FWDAQ		60		W
Power supply		10.8	12	13.2	V
Operating temperature	At fan inlet	0		45	°C
Size					
Width			2		slot
Height			3U		
Mechanical standard			PXIe Type 2		
Compliances					
RoHS3			Yes		
CE			Yes		
FCC	Exclusion according to CFR 47, part 15, paragraph 15.103(c).				

[12] Timing properties are valid for 2.5 GSPS in 2 channel mode and 5 GSPS in 1 channel mode. Timing properties scale linearly with sampling frequency.

[13] Power consumption depends on firmware option and use case. Power consumption is measured during acquisition and streaming of data at 5 Gbyte/s to PC.

Table 7 Data acquisition

Parameter	Condition	Min	Typical	Max	Unit
Rearm time[14]				20	ns
Acquisition memory (Data FIFO)	Shared by all channels		8		Gbyte
Record length	4 channels mode in steps of 1	2		2^{32}-1	samples
	2 channel mode in steps of 1	2		2^{32}-1	samples
Pretrigger[15]	4 channels mode in steps of 8	0		16 360	samples
	2 channel mode in steps of 16	0		16 336	samples
Trigger delay[16]	4 channels mode in steps of 8	0		2^{35}-8	samples
	2 channel mode in steps of 16	0		2^{36}-16	samples

Table 8 Data transfer

Parameter	Value	Unit
Supported versions of data transfer standard PCIe	Gen1 / Gen2 / Gen3	
Supported number of lanes	1 / 4 / 8	
Data rate to CPU sustained with headers	5	GByte/s
Data rate to CPU sustained without headers	7	GByte/s
Data rate to GPU sustained without headers	7	GByte/s
Data rate peer-to-peer to GPU sustained without headers	7	GByte/s

Table 9 Software support

Parameter	Value
Operating system[17]	Windows / Linux
GUI	Digitizer Studio
Example code	C, Python
API	C / C++

[14] Minimum time from the last sample of a record to the next trigger.

[15] Pre-trigger is set by assigning the parameter “horizontal offset” a negative value

[16] Trigger delay is set by assigning the parameter “horizontal offset” a positive value

[17] See 15-1494 Operating system support for a detailed listing of supported distributions.

4 FEATURES FOR DATA FLOW CONTROL, SYNCHRONIZATION AND PROCESSING

The ADQ36-PXIE features an advanced machine for flow control, synchronization, and signal processing. The block diagrams are shown in Figure 1 and Figure 2. The features are described in the following tables.

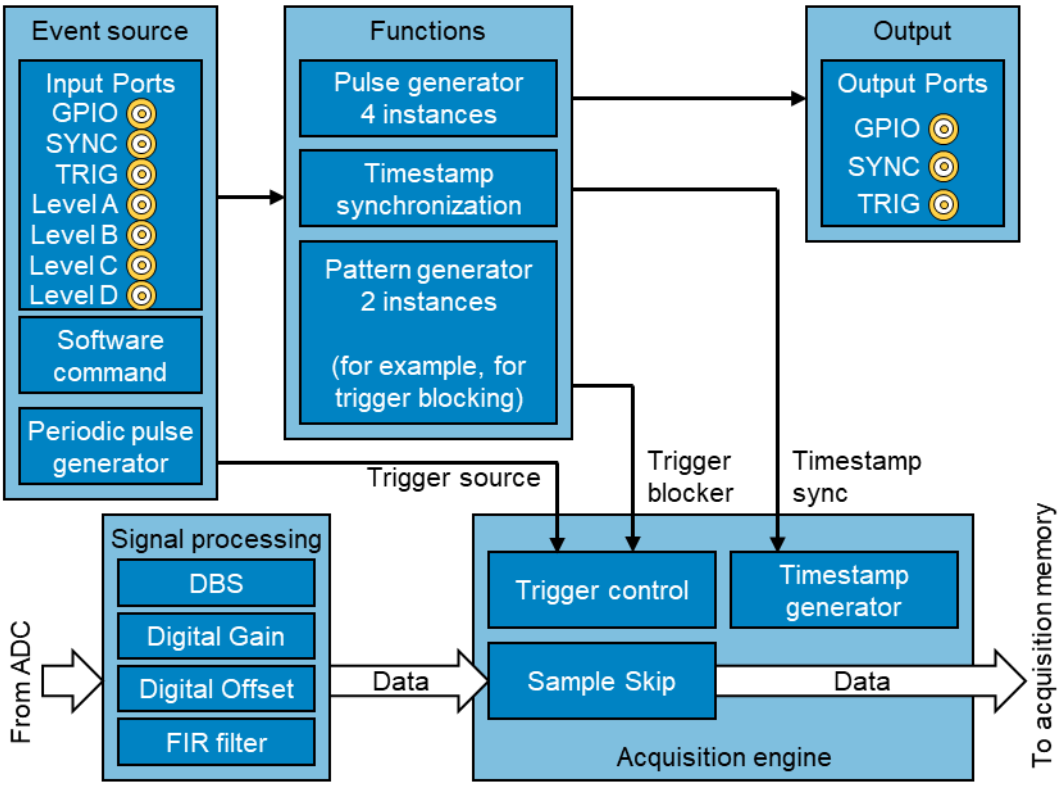


Figure 1 Flow control and synchronization block diagram.

Table 10 Digital signal processing blocks

Object type	Available selections
Digital Signal Processing Included signal processing in the data path for enhanced signal quality.	Digital Baseline Stabilizer (DBS) Digital gain Digital offset Digital FIR filter

Table 11 Flow control blocks

Object type	Available selections
Input ports Electrical connections to the ADQ36-PXIE for real-time operation (excluding the PCIe data interface) Used as event source.	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference or clock input only) Analog channel A Analog channel B Analog channel C Analog channel D
Event sources Signals for real-time control of activities in the firmware of ADQ36-PXIE.	Software command External TRIG External SYNC External GPIO Internal periodic event generator Level analog channel A Level analog channel B Level analog channel C Level analog channel D
Functions Included operations for real-time control of activities in the firmware of ADQ36-PXIE.	Pattern generator for timestamp synchronization Pattern generator general purpose, 2 instances Pulse generator, 4 instances
Output ports Electrical connections to the ADQ36-PXIE for real-time operation (excluding the PCIe data interface).	Front panel TRIG Front panel SYNC Front panel GPIO Front panel CLK (clock reference output only)

Table 12 Firmware functions for flow control

Function	Modes/selections	Event sources as stimuli
Pattern generator for timestamp synchronization Control the time of the ADQ36-PXIE.		Software command External TRIG External SYNC Internal periodic event generator
Pulse generator Control output pulse shapes. Three instances.	Rising edge Falling edge Pulse length Polarity	Software command External TRIG External SYNC Internal periodic event generator
Pattern generator general purpose For example, used for trigger blocking.	Once Window Gate Trigger counter	Software command External TRIG External SYNC Internal periodic event generator

Table 13 Firmware functions for acquisition

Function	Modes	Event Sources as stimuli / control
Trigger Initiate the acquisition of a data record.		Software command External TRIG External SYNC Internal periodic event generator Level analog channel A Level analog channel B
Data acquisition modes Configurations for sending digital data to the host PC.	Fixed record length Dynamic record length (zero suppression)	Selected **Trigger**
Data transfer modes Transport to CPU / GPU	Streaming with header Streaming without header	User set-up

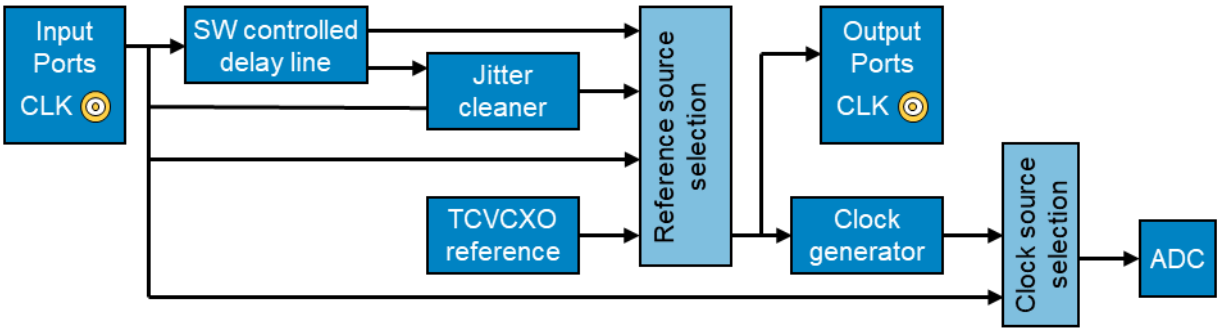


Figure 2 Clock generation block diagram.

Table 14 Clock generation

Function	Modes
Clock reference source Phase and frequency reference for the clock system.	Internal External External with jitter cleaner and/or delay line
Sampling clock sources Actual clock for taking the samples of the analog data.	Internal clock generator Direct external clock
Clock output	Selected clock reference

5 FIRMWARE

5.1 FWDAQ

The FWDAQ is included with all digitizers. The firmware includes control of the hardware and recording of data.

5.2 FWATD

The FWATD is optional. It includes thresholding for noise suppression and accumulations of waveforms. See datasheet 22-2912 for more details.

5.3 FWPD

The FWPD is optional. It includes detection and analysis of pulses. See datasheet 23-3028 for more details.

5.4 Managing firmware

The digitizer supports multiple firmware images. Note the following about managing firmware images:

- The non-volatile memory on the digitizer can store up to four different firmware images (including the active firmware). Use the tool ADQAssist to change firmware and to upload new images to the digitizer.
- Each hardware can include a license for multiple firmware options. If all firmware images cannot be stored on the device, some may need be stored on the host computer for manual reprogramming via ADQAssist.
- The digitizer (and the enclosing host computer) must be power cycled for the firmware switch to be completed. This is required to let the PCIe bus enumerate with the new firmware.
- Some firmware features require a valid license key to activate. See the ordering information section for details about available firmware features.
- Switching mode between one channel at 5 GSPS and two channels at 2.5 GSPS requires switching the digitizer firmware image.

6 ABSLOUTE MAXIMUM RATINGS

Table 15 Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
Power supply to GND		-0.4	14	V
Operating temperature		0	45	ºC
Analog in to GND		-1.75	+1.75	V
TRIG to GND	50-Ω mode	-2	5	V
SYNC to GND	50-Ω mode	-2	5	V
TRIG to GND	500-Ω mode	-2	6	V
SYNC to GND	500-Ω mode	-2	6	V
CLK REF to GND AC amplitude			5	Vpp
CLK REF to GND DC-level		-5	5	V
GPIO to GND		-1.5	5	V

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the digitizer. The digitizer with PCIe format has a built-in fan to cool the device. The built-in temperature monitoring unit will protect the digitizer from overheating by temporarily shutting down parts of the device in an overheat situation.
The SMA connectors have an expected lifetime of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

7 TYPICAL PERFORMANCE

7.1 Frequency response

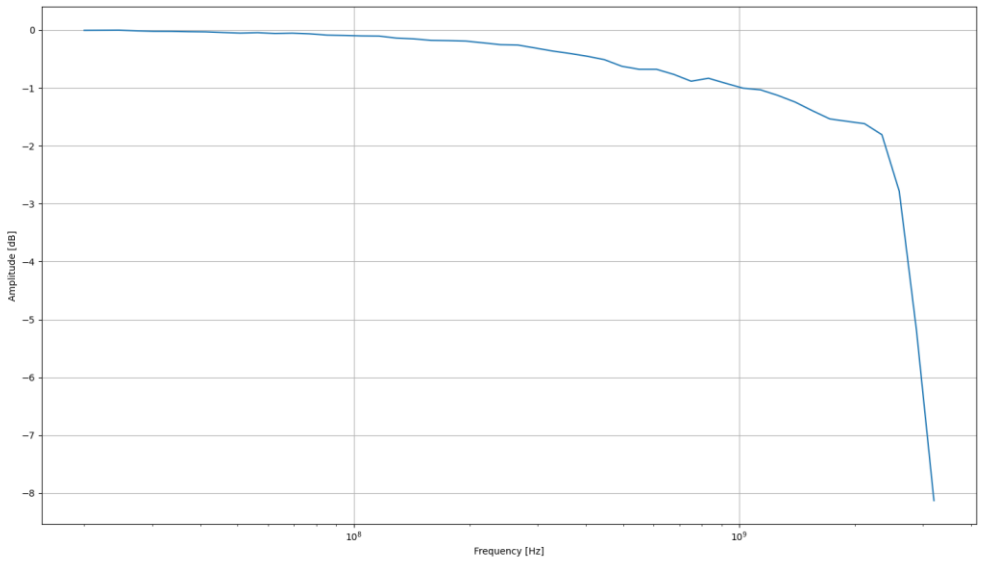


Figure 3 Typical frequency response.

7.2 Crosstalk

Figure 4 Typical crosstalk in 4-channel mode. Channel A to B, C and D.

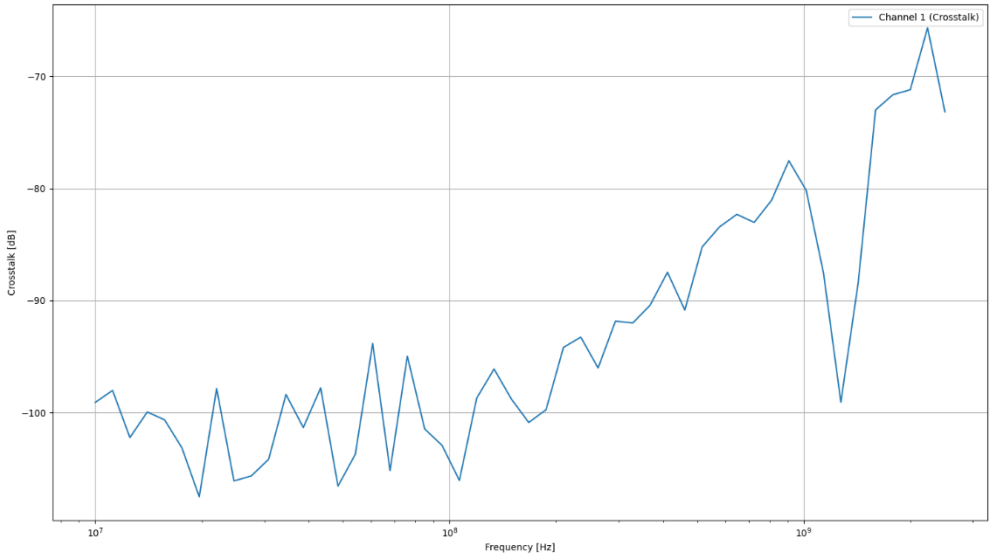


Figure 5 Typical crosstalk in 2-channel mode.

7.3 Frequency domain 4-channel mode

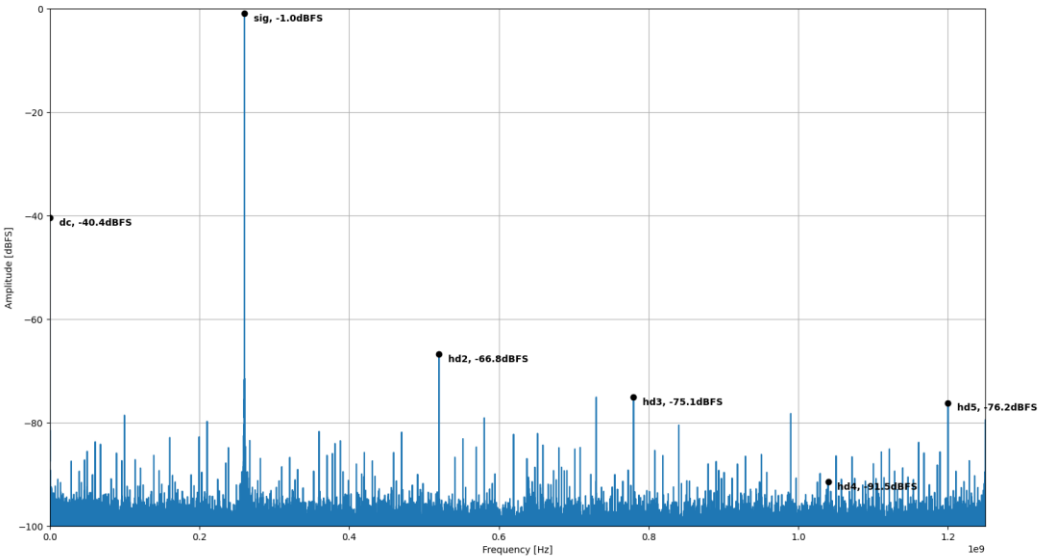


Figure 6 FFT typical single tone performance, 4-channel mode at 2.5 GSPS

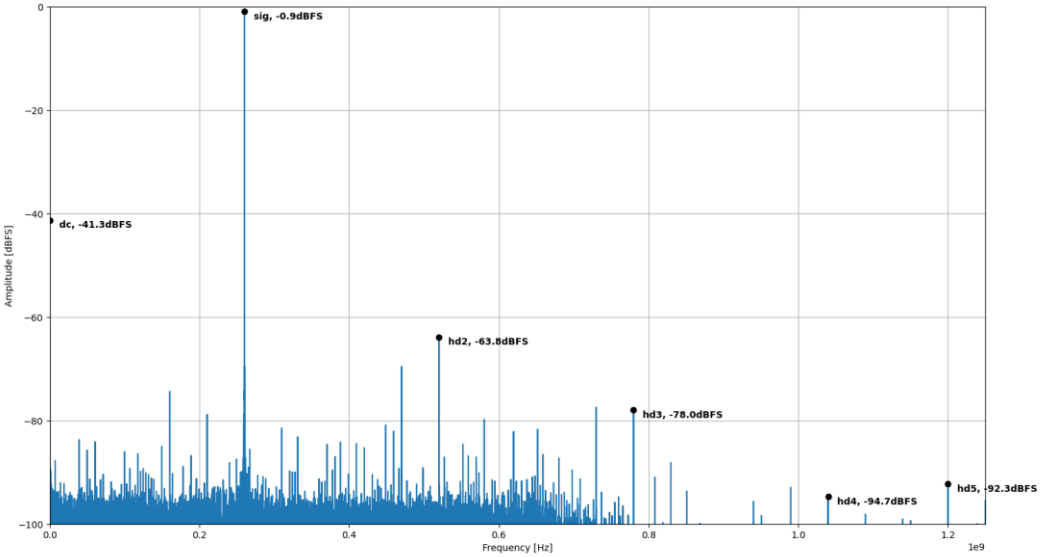


Figure 7 FFT using built in programmable FIR, 4-channel mode at 2.5 GSPS

7.4 Frequency domain 2-channel mode

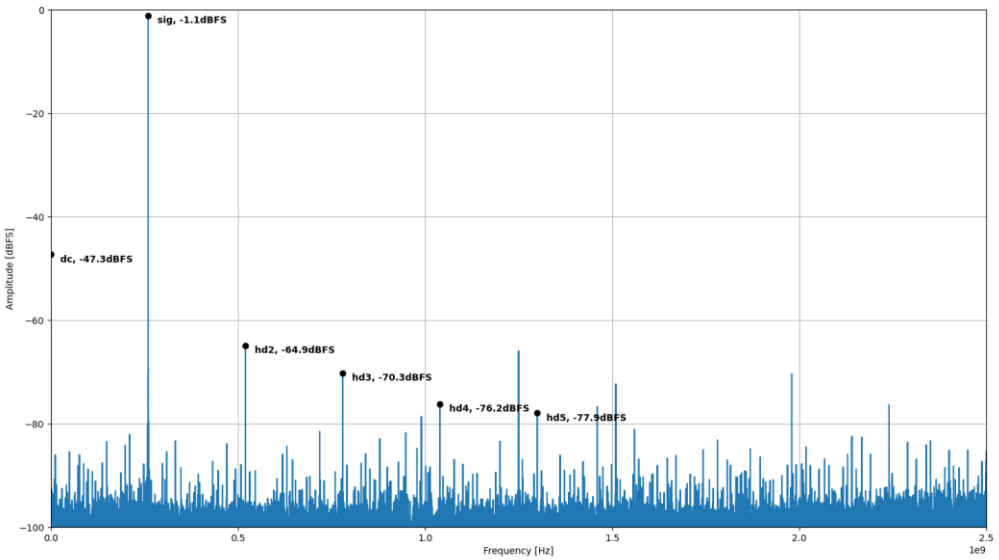


Figure 8 FFT typical single tone performance, 2-channel mode at 5 GSPS

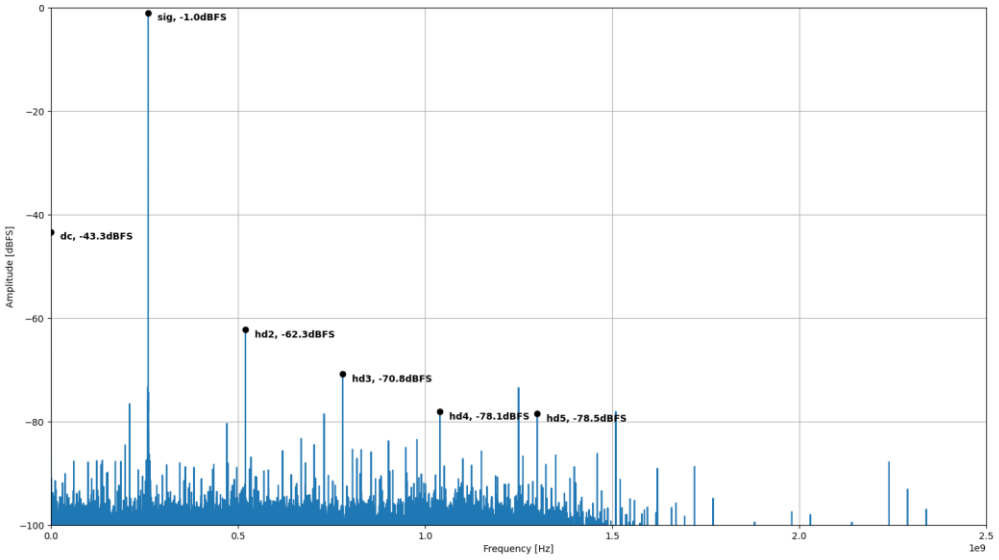


Figure 9 FFT using built in programmable FIR, 2-channel mode at 5 GSPS

8 BLOCK DIAGRAM

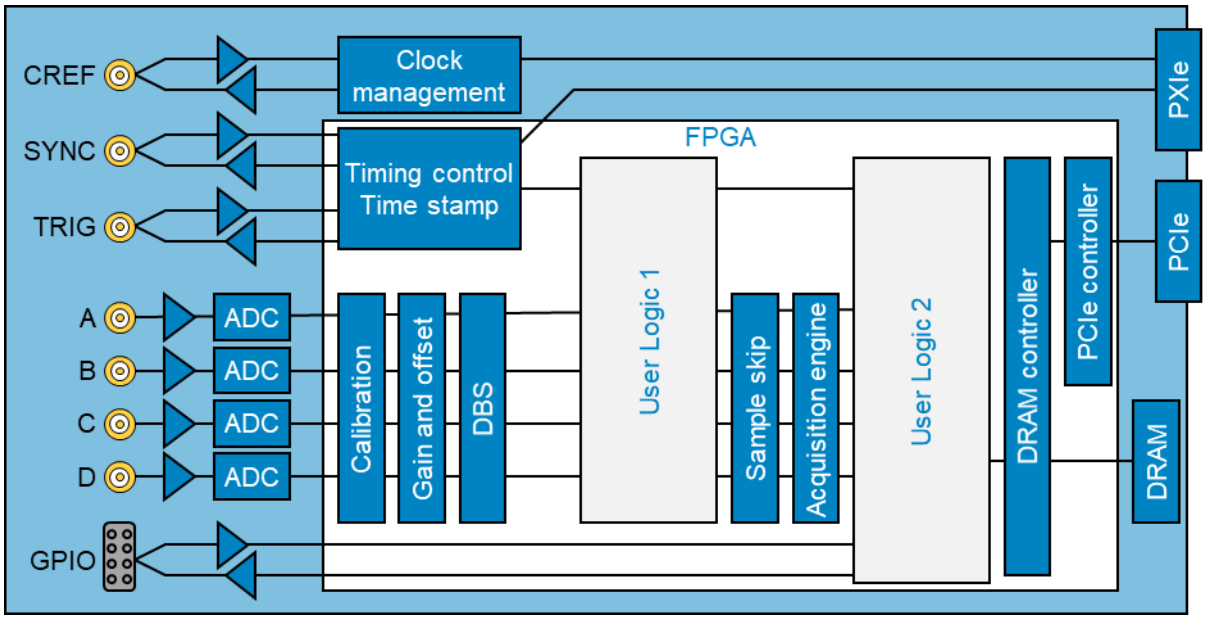


Figure 10 Block diagram.

Figure 10 shows a block diagram of ADQ36-PXIE in 2channels mode. The boxes “User Logic” are open for custom real-signal processing thought the firmware development kit (purchased separately).

9 REFERENCES

Refer to TSPD’s web site spdevices.com for the latest version of documents.

15-1494 Supported operating systems

18-2059 ADQUpdater user guide

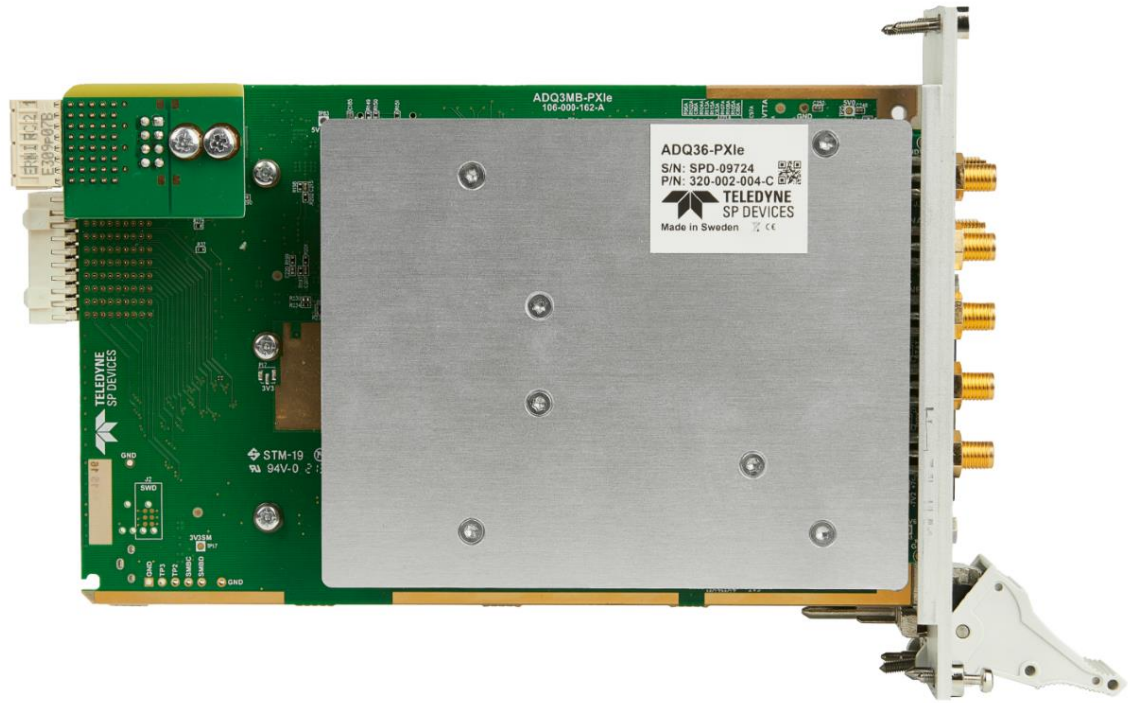
20-2507 ADQ3 series development kit user guide

20-2521 ADQAssist user guide

21-2539 ADQ3 series user guide

22-2912 ADQ3 FWATD datasheet

23-3028 ADQ3 FWPD datasheet


ADQ3MB-PXIe
106-009-162-A
ADQ36-PXIe
S/N: SPD-09724
P/N: 320-002-004-C
TELEDYNE
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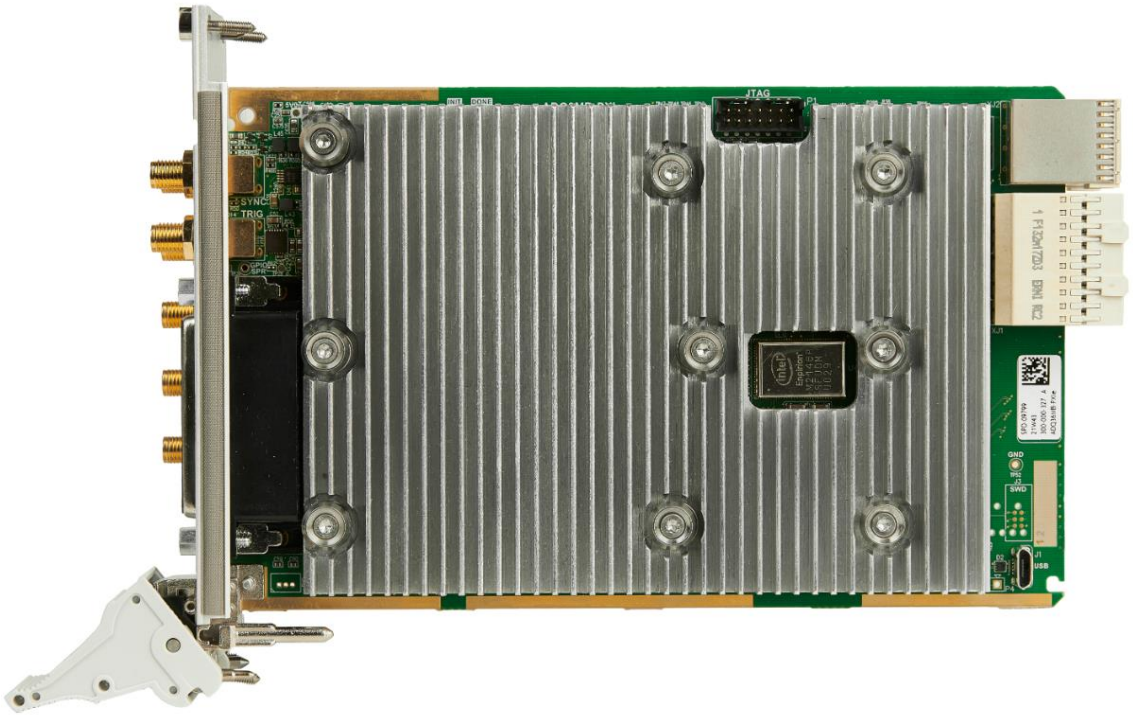
Made in Sweden
TELEDYNE
SP DEVICES
STM-19
94V-0


JTAG
SYNC
TRIG
USB

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