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NRW-FPGA-Based PRM System Qualification Project

Document Title

Final Technical Evaluation Report

CUSTOMER NAME	None
PROJECT NAME	NRW-FPGA-Based PRM System Qualification Project
ITEM NAME	PRM Equipment
ITEM NO.	C51
JOB NO.	FPG

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0	Apr 21,2008	First issue	N.Oda	Y.Goto	T.Miyazaki
1	See cover sheet	See cover sheet	See cover sheet	See cover sheet	See cover sheet

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Acronyms

CC: Critical Characteristic
CCD: Critical Characteristic for Design
CCA: Critical Characteristic for Acceptance
CGD: Commercial Grade Dedication
CGI: Commercial Grade Item
CGS: Commercial Grade Service
FTER: Final Technical Evaluation Report
NRW-FPGA: Non-Rewritable Field Programmable Gate Array
PTER: Preliminary Technical Evaluation Report

1. Introduction

1.1. Purpose

As stated in the Qualification Plan (Reference (1)) of this project, the process of Commercial Grade Dedication (CGD) is intended to ensure that all design requirements and safety functions are satisfied. This was accomplished by identifying the Critical Characteristics for Design (CCDs) which, when satisfied provide reasonable assurance that the design requirements and safety functions are satisfied. To ensure that the Commercial Grade Item (CGI)/Commercial Grade Service (CGS) satisfies the CCDs, Critical Characteristics for Acceptance (CCAs) were identified which, when satisfied provide reasonable assurance that the item/service is as specified and satisfies the CCDs and thus satisfies the design requirements and safety functions. To document the CCDs and CCAs, a Preliminary Technical Evaluation Report (PTER) (Reference (2)) was prepared.

The purpose of the PTER is to describe results of the preliminary technical evaluation to ensure that the Non-Rewritable Field Programmable Gate Array (NRW-FPGA)-Based Power Range Monitor (PRM) System meets all safety design and quality requirements for US nuclear plant applications as one of major activities for CGD. The preliminary technical evaluation includes identification of the requirements to be imposed on Fuchu Complex as part of the commercial grade procurement of the test system, and required qualification activities by NED. Note that since this project should be sufficient for the establishment of the qualification envelope for PRM System that will be provided to US market; therefore, qualification testing and analysis are performed in accordance with IPSNE 10 CFR50 Appendix B QA Program.

After completing procurement and qualification activities (including qualification testing and analysis, and software qualification), a Final Technical Evaluation Report (FTER) was established based on the PTER, and the results of qualification activities.

The purpose of this FTER is to document results of confirmation of the procurement, acceptance, and qualification of the Test System for NRW-FPGA-Based PRM System Qualification Project.

1.2. Definition

(1)Critical Characteristics for Acceptance (CCAs) - Identifiable and measurable attributes/variables of a CG items and CG services, which once selected to be verified, provide reasonable assurance that the items and services received is the items and services specified.

(2)Critical Characteristics for Design (CCDs) - Those properties or attributes which are essential for the items and services's form, fit, and functional performance. CCDs are the identifiable and/or measurable attributes which provide assurance that the items and services will meet its design requirement or safety function.

2. Approach

The PTER categorizes all Critical Characteristics (CCs) by the activities that will be performed to verify that each is satisfied. The following activities were performed to verify CCs in this project:

- Requirements to be imposed on the commercial vendor as CGI.
- Requirements to be imposed on the commercial vendor as CGS.
- The analyses that will be performed to ensure that the system to be specified is representative or bounds the system configuration for US customer orders, and for the EPRI TR-107330 qualification requirements.
- The testing that will be performed to ensure that the system to be specified is representative or bounds the system configuration for US customer orders, and for the EPRI TR-107330 qualification requirements.
- Software qualification activities to be performed by NED.

This FTER reports the result of verification of CCs identified in PTER.

The results of verification are summarized in Appendix A of this FTER.

3. Result of Final Technical Evaluation

As a result of final technical evaluation, all CCs identified in PTER have been verified through procurements, qualification tests, qualification analysis, and software qualification of this project.

4. Conclusion

All CCs have been verified in this project, so Toshiba concludes that Toshiba NRW-FPGA-Based PRM System meets all safety design and quality requirements for US nuclear plant applications.

5. References

(1) FPG-PLN-C51-0003 Rev.3
Qualification Plan
(2) FPG-DRT-C51-0001 Rev.10
Preliminary Technical Evaluation Report
(3) Toshiba FPG-PLN-A70-0001 Rev.2
Project Quality Assurance Manual
(4) Toshiba FPG-RQS-C51-0001 Rev.7
Equipment Requirement Specification of FPGA-based Units
(5) FPG-DRT-C51-0023 Rev.0
Software Qualification Report
(6) FPG-TRT-C51-1001 Rev.0
Qualification Test Summary Report
(7) FPG-TRT-C51-0002 Rev.0
Availability/Reliability Analysis Report
(8) FPG-TRT-C51-0003 Rev.0
Setpoint Support Analysis Report
(9) FPG-PLN-C51-0005, Rev.3
Master Test Plan
(10) FPG-TPRC-C51-1001, Rev.6
System Set-up and Check-out Test Procedure
(11) FPG-TPRC-C51-1009, Rev.5
Operability Test Procedure
(12) FPG-TPRC-C51-1010, Rev.5
Prudency Test Procedure
(13) FPG-TPRC-C51-1010, Rev.5
Environmental Test Procedure
(14) FPG-TPRC-C51-1003, Rev.3
Seismic Test Procedure
(15) FPG-TPRC-C51-1004, Rev.7
EMI/RFI Test Procedure
(16) FPG-TPRC-C51-1005, Rev.4
EFT/B Test Procedure
(17) FPG-TPRC-C51-1005, Rev.4
Surge Withstand Capability Test Procedure
(18) FPG-TPRC-C51-1007, Rev.5
ESD Test Procedure
(19) FPG-TPRC-C51-1008, Rev.5
Class 1E to Non-1E Isolation Test Procedure
(20) FPG-DRT-C51-0018, Rev.0
Requirement Definition Phase Preliminary Hazard Analysis Report
(21) FPG-CFM-C51-0001, Rev.7
Master Configuration List
(22) FPG-DRT-C51-0005, Rev.1
NICSD's Critical Digital Review Report
(23) FPG-DRT-C51-0006, Rev.0

Actel's Critical Digital Review Report
(24) FPG-VDN-C51-0047, Rev.9
Schematic Diagrams (PRM System for Qualification)
(25) FPG-VDN-C51-0136, Rev.0
Users Manual for Current Monitor Box
(26) FPG-VDN-C51-0135, Rev.0
Users Manual for Test Rack
(27) FPG-06-ESVR-0001 Rev.0
Source Verification Check Sheet and Record for Commercial Grade Dedication
(28) FPG-06-ESVR-0002 Rev.0
Source Verification Check Sheet and Record for Commercial Grade Dedication
(29) FPG-06-ESVR-0003 Rev.0
Source Verification Check Sheet and Record for Commercial Grade Dedication
(30) FPG-07-ESVR-0001, Rev.0
Source Verification Check Sheet and Record for Commercial Grade Dedication
(31) FPG-07-ESVR-0002, Rev.0
Source Verification Check Sheet and Record for Commercial Grade Dedication
(32) FPG-07-ESVR-0003, Rev.0
Source Verification Check Sheet and Record for Commercial Grade Dedication
(33) FPG-07-ESVR-0004, Rev.0
Source Verification Check Sheet and Record for Commercial Grade Dedication
(34) E05SC-001-R0
CG Survey Check List
(35) E05SC-003-R0
CG Survey Check List
(36) E06SC-001-R0
CG Survey Check List
(37) E05SR-001-R1
CG Survey Report
(38) E05SR-003-R1
CG Survey Report
(39) E06SR-001-R1
CG Survey Report
(40) E06SR-004-R0
CG Survey Report
(41) FPG-PLN-A70-0003 Rev.0
Process Control Sheet (System Validation testing at Fuchu)
(42) FPG-PLN-A70-0004 Rev.3
Process Control Sheet (Qualification testing at [ ])^{a,c}

Appendix A

Comparison Table of ERS/PQAP Requirements and Qualification Activities for Ensured Satisfaction

[Note]
X: Applicable,
---: Not Applicable

EPRI TR-107330 CTM ITEM NO.	Document	Section of Document	ERS/PQAM Requirement to be confirmed by					Post-Qualification Activities	Remarks on selection of Methods for Ensuring ERS/PQAP requirements are satisfied	CCDs for CGI	CCAs for CGI	Verified by
			Procurement of the CG Items	Procurement of the CG Services	Qualification Analyses	Qualification Tests	Software Qualification					
---	CG Survey Report (E05SR-001-R1)	Observation No.5	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Verification of design tool	CG Suvey Check List (E06SC-001-R0), Section 9
---	CG Survey Report (E05SR-001-R1)	Observation No.6	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	V&V activities in accrdance with IEEE1012, R.G1.168.	CG Suvey Check List (E06SC-001-R0), Section 9
4.5.4 4.5.6.A 4.5.6.B 4.9.3	ERS	5.1.1 Basic Design Requirements	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Unit Model Numbers Quality of Design and Manufacture	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1
4.2.3.7.C 4.4.1.2.D 4.4.1.2.I 4.4.6.3	ERS	5.1.2 System Initialization Requirements	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Unit Model Numbers Quality of Design and Manufacture	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1
4.2.4 4.5.2.B	ERS	5.1.3 Nominal System Setpoints	X	---	X	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied. In addition, qualification analysis provides reasonable assurance that the setpoint analysis requirement (from the EPRI TR) is satisfied.	X	Unit Model Numbers Configuration Identifications of Units Quality of Design and Manufacture Trip set point of each module Performing correct action upon reaching setpoint	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1, Section 2, Section 5, and Section 6 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules Setpoint Support Analysis Report (FPG-TRT-C51-0003 Rev.0), All Sections
4.2.1.A 4.3.4.1 4.3.4.3.F	ERS	5.1.3.1 Response Time Requirements	X	---	---	X	---	---	Qualification testing provides reasonable assurance that the total system response time requirement (from the ERS) is satisfied. CGI procurement acceptance includes activity to reasonably assure that all other ERS response time requirements (except total system response time) are satisfied.	X	Unit Model Numbers Configuration Identifications of Units Quality of Design and Manufacture	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1, and Section 2 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules Qualification Test Summary Report (FPG-TRT-C51-0101, Rev.0), Section 6
4.3.2.1.2.B	ERS	5.1.4 Drift and Accuracy Requirements	X	---	X	X	---	---	CGI procurement acceptance includes activity to reasonably assure that this performance/design requirement is satisfied. Qualification testing provides reasonable assurance that the linearity requirement (from the EPRI TR) is satisfied. Qualification analysis addresses the drift analysis requirement and overall accuracy requirement(from the EPRI TR).	X	Unit Model Numbers Configuration Identifications of Units Quality of Design and Manufacture Accuracy of APRM Upscale (High-High) trip/reset Accuracy of Simulated Thermal Power Upscale trip/reset	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1, and Section 6 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules Qualification Test Summary Report (FPG-TRT-C51-0101, Rev.0), Section 6 Setpoint Support Analysis Report (FPG-TRT-C51-0003 Rev.0), Section 4
4.9.2	ERS	5.1.5 Instrument Modes	X	---	---	X	---	---	CGI procurement acceptance includes activity to reasonably assure that this performance/design requirement is satisfied. Qualification testing provides reasonable assurance that the mode function requirement (from the ERS) is satisfied.	X	Unit Model Numbers Configuration Identifications of Units Quality of Design and Manufacture Change of state of signal when mode is changed	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1, Section 2, and Section 7 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules Qualification Test Summary Report (FPG-TRT-C51-0101, Rev.0), Section 6

EPRI TR-107330 CTM ITEM NO.	Document	Section of Document	ERS/PQAM Requirement to be confirmed by					Post-Qualification Activities	Remarks on selection of Methods for Ensuring ERS/PQAP requirements are satisfied	CCDs for CGI	CCAs for CGI	Verified by
			Procurement of the CG Items	Procurement of the CG Services	Qualification Analyses	Qualification Tests	Software Qualification					
4.2.3.6 4.2.3.7.A 4.3.4.7.B 4.3.4.7.C 4.4.1.2.G 4.4.6.1 4.4.6.1.1 4.4.6.1.5 4.4.6.1.8 4.4.6.1.9	ERS	5.1.6 Failure Detection and Self Test Requirements	X	---	---	X	---	---	CGI procurement acceptance includes activity to reasonably assure that this performance/design requirement is satisfied.	X	Unit Model Numbers Configuration Identifications of Units Quality of Design and Manufacture Fault condition signal generated during faults	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1, Section 2, and Section 8 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules Qualification Test Summary Report (FPG-TRT-C51-0101, Rev.0), Section 6
4.2.3.2 4.2.3.3 4.2.3.4 4.2.3.5 6.4.1	ERS	5.1.7 Availability/Reliability Requirements	X	---	X	---	---	---	CGI procurement acceptance includes activity to reasonably assure that the MTBF requirement is satisfied. Qualification analysis addresses the availability/reliability analysis requirement (from the EPRI TR)	X	Unit Model Numbers Quality of Design and Manufacturer Documentation	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1 and Section 13 Qualification Test Summary Report (FPG-TRT-C51-0101, Rev.0), Section 6
4.3.1.4 4.3.2.1	ERS	5.2.1 Unit Configuration Requirements	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Configuration Identifications of Units	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 2 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules
ERS4.3.1 ERS4.4.1 ERS4.1.2 ERS4.1.3 ERS4.2	ERS	5.2.2 Unit Input/Output Requirements	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Unit Model Numbers Configuration Identifications of Units	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1 and Section 2 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules
4.3.2.1.C 4.3.2.1.D 4.3.2.1.E 4.3.2.1.2.A 4.3.2.1.2.C 4.3.2.1.2.D 4.3.2.1.2.E 4.3.2.1.2.J 4.3.2.2 4.3.2.2.2.A 4.3.2.2.2.B 4.3.2.2.2.C 4.3.2.2.2.D 4.3.3.1	ERS	5.2.3 Module Requirements	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Configuration Identifications of Units -- Module Model Numbers -- Revision Number -- Serial Number Module Documentation Output Linearities APRM Inoperable Trip Accuracy of Trip/Reset LVPS Power output Display Linearity for Modules	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 2, Section 6, Section 9, Section 11, and Section 13 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules
4.3.4.6	ERS	5.2.4.1 Chassis Requirements	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Quality of Design and Manufacture Chassis structure Chassis type, dimensions Weight	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 10
4.6.5	ERS	5.2.4.2 System Cables and Connectors	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Quality of Design and Manufacture Cable Type and length Connecter Type	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 4 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Connector Type of LPRM Modules
4.3.4.2	ERS	5.2.4.3 Data Retention Capability Requirements.	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	FPGA type ROM type	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 11 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), FPGA type and ROM type

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			Procurement of the CG Items	Procurement of the CG Services	Qualification Analyses	Qualification Tests	Software Qualification					
4.3.4.3	ERS	5.2.4.4 Transferring information between modules and modules	X	---	---	X	---	---	Procurement of the CGI, with special requirements for loss of power to chassis interconnect, provide reasonable assurance that transfer requirements are satisfied. Qualification testing provides reasonable assurance that the requirements are met.	X	Unit Model Numbers Quality of Design and Manufacture	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1
4.6.8	ERS	5.2.4.5 Grounding/Shielding Requirements	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Unit Model Numbers Provision of Grounding Points Provision of Shielding Points	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1and Section 11
4.6.6	ERS	5.2.4.6 Termination Requirements	X	---	---	X	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied. Qualification testing provides reasonable assurance that the requirements are met.	X	Unit Model Numbers Connector type	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1and Section 11
	ERS	5.2.4.7 Requirement for Power Supply line	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Varistor Type Number Noise Filter Type Number	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 12
4.2.2 4.4.5.2.E 7.2.G 7.4 7.5.2 7.5.3 7.7.3 8.7.E	ERS	5.3 Software Requirements	X	---	---	---	X	---	Software qualification by NED provides reasanable assurance that the requirement is satisfied. Procurement of the CGI provides reasonable assurance that the requirements is satisfied., including providing necessary V&V information from vendor.	X	Quality of Design and Manufacture Documentation that work is performed in accordance with a program that has: -- Lifecycle V&V requirements (documents such as FE specs, FPGA design specs, implementation records, testing records, etc.) -- Traceability Requirements (of the boards, etc.) -- Document and Coding Control Requirements -- Configuration Control requirements -- Change Control Requirements -- Design Language and Tool Control Requirements -- Labelling requirements for logic revision number on chips Design Requirements -- Synchronous design -- Modular design using completely tested FEs -- Lengths of train of the FEs FPGA model number (for size, non-rewritable, retention capability)	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 11 Software Qualification Report (FPG-DRT-C51-0023, Rev.0), Section 4

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			Procurement of the CG Items	Procurement of the CG Services	Qualification Analyses	Qualification Tests	Software Qualification					
4.7.8.2	ERS	5.4 Design Life	X	---	---	X	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied, including providing modular design, bypass capability and redundancy within the units. Qualification testing provides reasonable assurance that the requirements are met.	X	Unit Model Numbers Quality of Design and Manufacture	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1
4.3.6.1 4.3.6.2 4.3.6.3	ERS	5.5.1 Environmental Requirements	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the environmental requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101 Rev.0), Section 6
4.3.9	ERS	5.5.2 Seismic Requirements	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the seismic requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101 Rev.0), Section 6
4.3.7	ERS	5.5.3 EMI/RFI Requirements	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101 Rev.0), Section 6
4.6.2	ERS	5.5.4 Surge Withstand Requirement	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101 Rev.0), Section 6
4.6.2	ERS	5.5.5 ETF/B Withstand Requirement	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101 Rev.0), Section 6
4.3.8	ERS	5.5.6 ESD Withstand Requirement	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101 Rev.0), Section 6
4.6.4	ERS	5.5.7 Isolation Requirement	X	---	---	X	---	---	Procurement for CGI ensures that vendor provides items that NED has selected based on the requirements. Qualification testing provides reasonable assurance that the requirements are met.	X	Unit Model Numbers Configuration Identification of Units Quality of design and manufacture	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1 and Section 2 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
4.3.1.4 4.3.4.7.A 4.6.1.1.D 4.6.1.1.F 4.6.1.1.I 4.3.4.7.D 4.6.1.1.A	ERS	5.5.8 Power Supply	X	---	---	X	---	---	Procurement for CGI ensures that vendor provides items that NED has selected based on the requirements. Qualification testing provides reasonable assurance that the requirements are met.	X	Unit Model Numbers Configuration Identification of Units Quality of design and manufacture	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1 and Section 2 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6

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7.2.A	ERS	5.6 Classification	X	X	X	X	X	---	The ERS contains requirements throughout which invoke the Appendix B QA program. There are many CCs specific to this ERS requirement.	(See many other sections)	(See many other sections)	(See many other sections)
4.7.3 4.7.5 4.7.8.1	ERS	5.8 Maintenance Requirements	X	---	X	---	---	---	Procurement for CGI ensures that vendor provides items that NED has selected based on the requirements. Qualification analyses provides reasonable assurance that the MTBF requirement is met.	X	Unit Model Numbers Quality of Design and Manufacture	CG Survey Check List (E05SC-001-R0), Section 1, Section 5, and Section 8 CG Survey Check List (E06SC-001-R0), Section 9 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1 Availability/Reliability Analysis Report (FPG-TRT-C51-0002), Section 3
7.2.A	ERS	5.9 Design Method	X	---	---	---	X	---	Software qualification by NED provides reasanable assurance that the requirement is satisfied. Procurement of the CGI provides reasonable assurance that the requirements is satisfied., including providing necessary V&V information from vendor.	(See many other sections)	(See many other sections)	(See many other sections)
4.9.4	ERS	5.10 Material Requirements	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	---	---	--- (Hazadous materials are not used)
4.8	ERS	5.11 Requirements for Third Party/Sub-Vendor Items	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	---	---	--- (No item is provided from Sub-vendor or Third Party to NED)
7.2.A	ERS	6 Fabrication Requirements	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	(See many other sections)	(See many other sections)	(See many other sections)
5.2.A	ERS	7.1 Unit and Module tests	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Documentation	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 13

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			Procurement of the CG Items	Procurement of the CG Services	Qualification Analyses	Qualification Tests	Software Qualification					
5.2.B 5.2.C 5.2.D 5.2.E 5.2.F	ERS	7.2.1 System Tests	X	X	---	X	X	---	The requirement is satisfied by NED's acceptance activity for CGI. The procurement for CG services provides associated services for performing the test such as wiring design of test system and Test Equipment. Qualification testing provides reasonable assurance that the requirements are met. System validation tests are performed in software qualification activities.	(See many other sections)	(See many other sections)	(See many other sections for CGI and Modules) CG Survey Check List (E05SC-001-R0), Section 1, Section 2, Section 5, CG Survey Check List (E06SC-001-R0), Section 9 CG Survey Check List (E05SC-003-R0), All Section Schematic Diagrams (PRM System for Qualification) (FPG-VDN-C51-0047, Revision 9), All Section Users Manual for Current Monitor Box (FPG-VDN-C51-0136, Revision 0), All Section Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0002, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0003, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0004, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0001, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0003, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6 Software Qualification Report (FPG-DRT-C51-0023 Rev.0), Section 4
5.3	ERS	7.2.2 Operability Test Requirements	---	X	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met. The procurement for CG services provides wiring design of test system and Test Equipment.	---	---	(See many other sections for CGI and Modules) CG Survey Check List (E05SC-001-R0), Section 1, Section 2, Section 5, CG Survey Check List (E06SC-001-R0), Section 9 CG Survey Check List (E05SC-003-R0), All Section Schematic Diagrams (PRM System for Qualification) (FPG-VDN-C51-0047, Revision 9), All Section Users Manual for Current Monitor Box (FPG-VDN-C51-0136, Revision 0), All Section Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0002, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0003, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0004, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0001, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0003, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
5.4	ERS	7.2.3 Prudency Testing Requirements	---	X	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met. The procurement for CG services provides wiring design of test system and Test Equipment.	---	---	(See many other sections for CGI and Modules) CG Survey Check List (E05SC-001-R0), Section 1, Section 2, Section 5, CG Survey Check List (E06SC-001-R0), Section 9 CG Survey Check List (E05SC-003-R0), All Section Schematic Diagrams (PRM System for Qualification) (FPG-VDN-C51-0047, Revision 9), All Section Users Manual for Current Monitor Box (FPG-VDN-C51-0136, Revision 0), All Section Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0002, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0003, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0004, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0001, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0003, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
5.5	ERS	7.2.4 Operability and Prudency Tests Applicability	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6

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			Procurement of the CG Items	Procurement of the CG Services	Qualification Analyses	Qualification Tests	Software Qualification					
6.2.1.A 6.2.1.B 6.2.1.C 6.2.1.D 6.2.1.E 6.2.1.F 6.2.1.G 6.2.1.H 6.2.1.I 6.2.1.1	ERS	7.3.1.1 Test specimen Hardware Configuration and Arrangement Requirements	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Unit Model Numbers Configuration Identification of Units	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1, and Section 2 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules
6.2.2.	ERS	7.3.1.2 Test Specimen Software Requirements	X	---	---	---	---	---	Procurement of the CGI provides reasonable assurance that the requirements is satisfied.	X	Unit Model Numbers Configuration Identification of Units	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 1, and Section 2 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0002, Revision 0), Identification of Modules
6.2.3	ERS	7.3.1.3 Test Support Equipment Requirements	—	X	---	X	---	---	Procurement for CG services provides reasonable assurance that the requirements are met. Control of test equipment is part of the qualification testing scope.	—	---	CG Survey Check List (E05SC-001-R0), Section 1, Section 2, Section 5, CG Survey Check List (E06SC-001-R0), Section 9 CG Survey Check List (E05SC-003-R0), All Section Schematic Diagrams (PRM System for Qualification) (FPG-VDN-C51-0047, Revision 9), All Section Users Manual for Current Monitor Box (FPG-VDN-C51-0136, Revision 0), All Section Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0002, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0003, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0004, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0001, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0003, Revision 0), All Section Master Test Plan (FPG-PLN-C51-0005, Revision 3), Appendix 1
6.3	ERS	7.3.2 Qualification Tests and Analysis requirements	—	---	---	X	---	---	Qualification testing provide reasonable assurance that testing meet the ERS requirements.	—	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.3.1	ERS	7.3.2.1 Aging Requirement	—	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	—	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.3.2	ERS	7.3.2.2 EMI/RFI Test Requirement	—	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	—	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.3.2.1	ERS	7.3.2.3 EMI/RFI Test Mounting Requirement	—	X	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met. Procurement for CG services provides reasonable assurance that Test Equipment meets the requirements.	—	---	Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0003, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.3.3	ERS	7.3.2.4 Environmental Test Requirement	—	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	—	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.3.3.1	ERS	7.3.2.4.1 Environmental Test Mounting Requirement	—	X	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met. Procurement for CG services provides reasonable assurance that Test Equipment meets the requirements.	—	---	Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0003, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0]), Section 6

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			Procurement of the CG Items	Procurement of the CG Services	Qualification Analyses	Qualification Tests	Software Qualification					
6.3.4	ERS	7.3.2.5 Seismic Test Requirement	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.3.4.1	ERS	7.3.2.5.1 Seismic Test Mounting Requirement	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.3.4.2	ERS	7.3.2.6 Seismic Test Measurement Requirement	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.3.4.3	ERS	7.3.2.6.1 Seismic Test Performance Requirement	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.3.4.4	ERS	7.3.2.6.2 Seismic Test Spectrum Analysis Requirement	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.3.5	ERS	7.3.2.7 Surge Withstand Capability Test Requirement	---	X	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met. Procurement for CG services provides reasonable assurance that Test Equipment meets the requirements.	---	---	Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0003, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.3.6	ERS	7.3.2.8 Class 1E to Non-1E Isolation Test Requirement	---	X	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met. Procurement for CG services provides reasonable assurance that Test Equipment meets the requirements.	---	---	Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0003, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
-	ERS	7.3.2.9 EFT/B Test Requirement	---	X	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met. Procurement for CG services provides reasonable assurance that Test Equipment meets the requirements.	---	---	Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.4.2	ERS	7.3.2.10 ESD Test Requirement	---	X	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met. Procurement for CG services provides reasonable assurance that Test Equipment meets the requirements.	---	---	Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0003, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.4.3	ERS	7.3.2.11 Power Quality Tolerance Requirement	---	X	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met. Procurement for CG services provides reasonable assurance that Test Equipment meets the requirements.	---	---	Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0003, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
6.4.4	ERS	7.3.3 Requirements for Compliance to Specifications	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Master Test Plan (FPG-PLN-C51-0005, Revision 2), Appendix 1-10)

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			Procurement of the CG Items	Procurement of the CG Services	Qualification Analyses	Qualification Tests	Software Qualification					
4.10.1.A 4.10.1.B 4.10.1.C 4.10.1.D 4.10.1.E 4.10.1.F 4.10.1.G 4.10.1.H 4.10.1.J	ERS	8.1 Packaging Requirements	---	X	---	X	---	---	Procurement for CG services provides reasonable assurance that the packing for shipment to [redacted] is in accordance with the requirements. Qualification testing requirements provide reasonable assurance that the packaging by [redacted] is in accordance with these requirements.	---	---	CG Survey Check List (E05SC-001-R0), Section 1, Section 4, and Section 6 Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0003, Revision 0), All Section Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0004, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
4.10.2	ERS	8.2 Shipping Requirements	---	X	---	X	---	---	Procurement for CG services provides applicable shipping requirements for Test Specimen. Qualification testing requirements provide reasonable assurance that shipping by NED to and from [redacted] and by [redacted] within the US, is in accordance with these requirements.	---	---	CG Survey Check List (E06SC-004-R0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101 Revision.0), Section 6
4.10.3	ERS	8.3 Storage Requirements	---	X	---	X	---	---	Procurement for CG services provides applicable storage requirements for Test Specimen. Qualification testing requirements provide reasonable assurance that the storage will be in accordance with these requirements.	---	---	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-07-ESVR-0001, Revision 0), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
8.1.A 8.1.D 8.1.E 8.1.F 8.1.G	ERS	9.1.1 Equipment General Overview Documentation	X	---	---	---	---	---	Procurement for CGI provides reasonable assurance that the requirements are met.	X	Documentation	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 13
4.7.3 4.7.4 4.7.9.B 4.7.9.C 8.3 8.5	ERS	9.1.3 Users Manual	X	---	---	---	---	---	Procurement for CGI provides reasonable assurance that the requirements are met.	X	Documentation	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 13
8.6.1.A 8.6.5	ERS	9.2.1 Programmatic Documentation A.	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Master Test Plan (FPG-PLN-C51-0005, Revision 0), Appendix 1-10
8.6.1.B 8.6.1.C	ERS	9.2.1 Programmatic Documentation B.	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	System Set-up and Check-out Test Procedure (FPG-TPRC-C51-1001, Revision 6), All Section Operability Test Procedure (FPG-TPRC-C51-1009, Revision 5), All Section Prudency Test Procedure (FPG-TPRC-C51-1010, Revision 5), All Section Environmental Test Procedure (FPG--TPRC-C51-1002, Revision 3), All Section Seismic Test Procedure (FPG-TPRC-C51-1003, Revision 3), All Section EMI/RFI Test Procedure (FPG-TPRC-C51-1004, Revision 7), All Section EFT/B Test Procedure (FPG-TPRC-C51-1006, Revision 4), All Section Surge Withstand Capability Test Procedure (FPG-TPRC-C51-1005, Revision 4), All Section ESD Test Procedure (FPG-TPRC-C51-1007, Revision 5), All Section Class 1E to Non-1E Isolation Test Procedure (FPG-TPRC-C51-1008, Revision 5), All Section
8.6.1.D	ERS	9.2.1 Programmatic Documentation C.	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), All Section

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			Procurement of the CG Items	Procurement of the CG Services	Qualification Analyses	Qualification Tests	Software Qualification					
8.6.1.E	ERS	9.2.1 Programmatic Documentation D.	X	X	---	X	X	---	Audits are performed during CGI, CGS, testing (and to approve [redacted] FPGA development (per the SQAP), and of third parties. These activities provide reasonable assurance that the audit requirements are satisfied.	---	---	CG Survey Report (E05SR-001-R1) CG Survey Report (E05SR-003-R1) CG Survey Report (E06SR-001-R1) CG Survey Report (E06SR-004-R0)
8.6.1.F	ERS	9.2.1 Programmatic Documentation E.	---	---	X	---	---	---	Qualification analyses provides reasonable assurance that the requirements are met.	---	---	Availability/Reliability Analysis Report (FPG-TRT-C51-0002 Revision 0), All Section Setpoint Support Analysis Report (FPG-TRT-C51-0003 Revision 0), All Section Requirement Definition Phase Preliminary Hazard Analysis (FPG-DRT-C51-0018, Revison 0), Appendix
8.6.2.A 8.6.2.B 8.6.2.D	ERS	9.2.2 Technical Items	X	---	---	---	---	---	Procurement for CGI provides reasonable assurance that the requirements are met.	X	(See many other sections)	(See many other sections)
8.6.3 8.6.3.A 8.6.3.B 8.6.3.C 8.6.3.D 8.6.3.E 8.6.3.F 8.6.3.H 8.6.3.J 8.6.3.K 8.6.3.L 8.6.3.M 8.6.3.N 8.6.3.O 8.6.3.P 8.6.3.Q 8.6.3.R 8.6.3.S	ERS	9.2.3 Application Guide.	---	---	---	---	---	X	After all qualification activities, NED performs this activity.	---	---	(Application Guide wil be provided in the Topical Report of NRW-FPGA-Based Power Range Monitor (PRM) System Qualification)
8.6.4	ERS	9.2.4 Supporting Analyses Documentation	---	---	X	---	---	---	Qualification analyses provide reasonable assurance that the requirements are met.	---	---	Availability/Reliability Analysis Report (FPG-TRT-C51-0002 Revision 0), All Section Requirement Definition Phase Preliminary Hazard Analysis Report (FPG-DRT-C51-0018, Revison 0), Appendix
8.7.B 8.7.C	ERS	9.2.5 V&V Documentation	X	---	---	---	X	---	Procurement of CGI provides required documents to be prepared by Fuchu-IP. Software qualification provides required documents to be prepared by NED.	X	Documentation	Source Verification Check Sheet and Record for Commercial Grade Dedication (FPG-06-ESVR-0001, Revision 0), Section 13
8.8	ERS	9.2.6 Test System Description	---	---	---	---	---	---	This information is covered by ERS section 9.2.3; software design description does not apply, since the PRM system does not have programmable software. The hardware description of ERS 9.2.3 is sufficient.	---	---	---
8.9	ERS	9.2.7 Critical Characteristics	---	---	---	---	---	---	The PTER provides required information.	---	---	Preliminary Technical Evaluation Report (FPG-DRT-C51-0001, Revision 10), Appendix A
8.10.A 8.10.B 8.10.D 8.10.E 8.10.F	ERS	9.2.8 Test System Drawing	---	X	---	---	---	---	Procurement of CG service provides required documents.	---	---	Schematic Diagrams (PRM System for Qualification) (FPG-VDN-C51-0047, Revision 9), All Section Users Manual for Test Rack (FPG-VDN-C51-0135, Revision 0), All Section
8.11	ERS	9.2.9 System Software/Hardware Configuration Document	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Master Configuration List (FPG-CFM-C51-0001, Revision 7), All Section
8.13	ERS	9.2.10 System Setup/Calibration/Checkout Procedure	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0]), Section 5

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			Procurement of the CG Items	Procurement of the CG Services	Qualification Analyses	Qualification Tests	Software Qualification					
8.14 8.6.2.E	ERS	9.2.11 System Test Documentation	---	---	---	X	---	---	Qualification testing provides reasonable assurance that the requirements are met.	---	---	System Validation Test Procedure (FPG-TPRC-C51-0001, Revision 2), All Section Qualification Test Summary Report (FPG-TRT-C51-0101,Rev.0), Section 6
7.2.F	PQAM	6.4 Critical Digital Review	---	---	---	---	X	---	Software qualification by NED provides reasonable assurance that the requirement is satisfied	---	---	NICSD's Critical Digital Review Report (FPG-DRT-C51-0005, Revision 1), All Section Actel's Critical Digital Review Report (FPG-DRT-C51-0006, Revision 0), All Section
6.5.D	PQAM	6.3 Commercial Grade Dedication (CGD)	X	---	---	---	---	---	NED prepared PTER. NED performed CG Survey. Procurement for CGI provides reasonable assurance that the requirements are met.	(See many other sections)	(See many other sections)	(See many other sections for CGI) Preliminary Technical Evaluation Report (FPG-DRT-C51-0001, Revision 10), Appendix A CG Survey Report (E05SR-001-R1) CG Survey Report (E05SR-003-R1) CG Survey Report (E06SR-001-R1) CG Survey Report (E06SR-004-R0)
6.5.B (1) 7.2.D	PQAM	9 Control of Purchased Material, Equipment, and Services	X	X	---	---	---	---	Procurement of CG items and Services provides reasonable assurance that procurement QA requirements are satisfied.	(See many other sections)	(See many other sections)	(See many other sections)
6.5.D 7.2.H	PQAM	13.3 Qualification Testing	---	---	---	X	---	---	NED performs the qualification testing, which provides reasonable assurance that the requirement for test QA and witnessing are met.	---	---	Process Control Sheet (System Validation testing at Fuchu) (FPG-PLN-A70-0003 Revision 0) Process Control Sheet (Qualification testing at [ ]3,c FPG-PLN-A70-0004 Revision 3)
7.3 7.8	PQAM	16 Nonconforming Materials, Parts or Components	X	X	X	X	X	---	CG procurement requirements for problem reporting provide reasonable assurance that problem reporting requirements are met. Work under the NED QA program provides reasonable assurance that problem reporting requirements are met.	---	---	NNR-06-001-I NNR-06-002-I/II NNR-06-003-I/II NNR-07-002-I NNR-08-001-I NNR-08-002-I/II VNNR-06-012 VNNR-06-013 VNNR-07-001 VNNR-07-002
6.4.4.H 7.2.E 7.2.F 8.15	PQAM	19 Reviews, Audits and Surveilance	X	X	---	X	X	---	This requirement is met by the following activities: -- CG survey of Fuchu-IP -- App B Audit of [ ]3,c -- In-process audits of Fuchu-IP (Job Order will state requirement that NQAD shall have access to Fuchu-IP for audits)	---	---	CG Survey Report (E05SR-001-R1) CG Survey Report (E05SR-003-R1) CG Survey Report (E06SR-001-R1) CG Survey Report (E06SR-004-R0)

PSNN-2016-0382

■Safety-related
□Non-Safety-related
□ASME CODE
□Others ( )

Document No.	FPG-PLN-C51-0006	Rev	5

NRW-FPGA-Based PRM System Qualification Project

Document Title
Verification and Validation Plan

CUSTOMER NAME	None
PROJECT NAME	NRW-FPGA-Based PRM System Qualification Project
ITEM NAME	PRM Equipment
ITEM NO.	C51
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Rev. No.	Issue Date	Description	Approved by	Reviewed by	Prepared by
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5	See cover sheet	See cover sheet	See cover sheet	See cover sheet	See cover sheet

Table of Contents

1 Purpose

This Verification and Validation (V&V) plan is prepared by Toshiba Nuclear Energy Systems & Services Division (NED) for the NRW-FPGA (Non-Rewritable Field Programmable Gate Array) -Based Power Range Monitor (PRM). This plan has the following purposes:

(1) This V&V plan (VVP) specifies V&V activities performed by NED and Toshiba Nuclear Instrumentation & Control Systems Dep. (NICSD).

(2) This VVP defines the envelope of the NICSD VVP.

For the V&V of NRW-FPGA-Based PRM System, NICSD shall prepare its own VVP describing their V&V activities in detail.

This VVP is based on NED AS-200A128 "Digital System Life Cycle Procedure," AS-200A129 "Digital System Development Procedure," AS-200A130 "Digital System Verification & Validation Procedure," AS-200A132 "Digital System Safety and Hazard Analysis Procedure," and Control & Electrical Systems Design & Engineering Dept. (ICDD) P-101 "NICSD Manufacture of FPGA-Based Equipment."

2 Reference Documents

2.1 Code of Federal Regulations

This VVP does not refer to the Code of Federal Regulations (CDR) directly, but does indirectly through the TOSHIBA internal standards in section 2.4.

2.2 Regulatory Guides and NRC Documents

2.2.1 US NRC Regulatory Guide 1.168 - Verification, Validation, Reviews, And Audits For Digital Computer Software Used in Safety Systems of Nuclear Power Plants, Revision 1 Feb. 2004.

2.2.2 US NRC Regulatory Guide 1.152 - Criteria for Programmable Digital Computer System Software in Safety related Systems of Nuclear Power Plants, Revision 1 Jan. 1996

Other regulatory guides and NRC documents are referenced through the TOSHIBA internal standards in section 2.4.

2.3 Industry Standards and EPRI Reports

2.3.1 IEEE Std 1012-1998, "IEEE Standard for Software Verification and Validation"

2.3.2 IEEE Std 829-1983, "IEEE Standard for Software Test Documentation"

2.3.3 IEEE Std 7.4.3.2-1993, "IEEE Standard Criteria for Digital Computers in Safety Systems of Nuclear Power Generating Stations"

2.4 Toshiba Internal Documents

2.4.1 AS-200A002, "Design Verification Procedure"

2.4.2 AS-200A005, "Design Review Meeting Convening Standard"

2.4.3 AS-200A010, "Control Procedure of vendor generated documents"

2.4.4 AS-200A015, "Design Change Control Procedure"

2.4.5 AS-200A128, "Digital System Life Cycle Procedure"

2.4.6 AS-200A129, "Digital System Development Procedure"

2.4.7 AS-200A130, "Digital System Verification & Validation Procedure"

2.4.8 AS-200A131, "Digital System Configuration Management Procedure"

2.4.9 AS-200A132, "Digital System Safety and Hazards Analysis Procedure"

2.4.10 AS-300A006, "Nonconformance Control Procedure for Procured Items and Services"

2.4.11 AS-300A008, "Nonconformance Control and Corrective Action Procedure"

2.4.12 AS-300A103, "Test Control Procedure"

2.4.13 P-101, "NICSD Manufacture of FPGA-Based Equipment"

2.4.14 FPG-PLN-A70-0001, Project Quality Assurance Plan

2.4.15 FPG-PLN-C51-0002, Software Quality Assurance Plan

2.4.16 FPG-RQS-C51-0001, Equipment Requirement Specification

2.4.17 FPG-PRD-A11-0002, Master Engineering Schedule

2.4.18 FPG-DRT-C51-0002, Preliminary Hazard Analysis Report

2.4.19 NICSD D-68016, "NICSD Procedural Standard for FPGA Products Development"

2.4.20 NICSD D-68017, "NICSD Procedural Standard for FPGA Device Development"

2.4.21 NICSD D-68018, "NICSD Procedural Standard for Functional Element Development"

2.4.22 NICSD D-68019, "NICSD Procedural Standard for FPGA Configuration Management"

2.4.23 NICSD D-68020, "NICSD Procedural Standard for Control of Software Tools Used with FPGA Based Systems"

2.4.24 NICSD D-67003, "NICSD Procedural Standard for Software Media Registration and Change"

Notice: Upon application of above NED, NICSD and other Toshiba internal standards, the latest version shall be used.

3 Definitions and Abbreviations

3.1 Definitions

Functional Element (FE): A Functional Element is a component of digital logic that shall be completely verified and validated through full pattern tests. i.e. tests that are performed for every possible input combination. An FE is written in Very High Speed Integrated Circuit Hardware Definition Language (VHDL). All VHDL source for the NRW-FPGA-Based PRM System shall solely consist of FEs and interconnects between FEs.

hazard: A source of potential harm or a situation with a potential for harm in terms of human injury, damage to health, property, or the environment, or some combination of these (Reference 2.3.1).

module: A part of a unit. Modules have the specific functions, for example, circuit board(s), AC-DC converter, connector assembly etc. See unit.

Netlist: Description of logics created by the logic synthesis tool. A design engineer describes FPGA logic in the form of VHDL source codes. The logic synthesis tool converts the VHDL source code into forms of digital circuits and outputs the resulting circuit in the form of a Netlist. The layout tool transforms the Netlist into physical placement of interconnects on the FPGA, which are represented as an FPGA fuse-map.

unit: NRW-FPGA-Based PRM System consists of the LPRM units, the LPRM/APRM units, and the FLOW units. Each unit is a drawer type chassis which houses the individual plug-in modules.

validation: Confirmation by examination and provisions of objective evidence that the particular requirements for a specific intended use are fulfilled. The process of evaluating a system or component during or at the end of the development process to determine whether it satisfies specified requirements.

verification: Confirmation by examination and provision of objective evidence that specified requirements have been fulfilled. The process of evaluating a system or component to determine whether the products of a given development phase satisfy the conditions imposed at the start of that phase.

3.2 Abbreviations

APRM: **A**verage **P**ower **R**ange **M**onitor

DCN:	**D**esign **C**hange **N**otice
DRS:	**D**ocument **R**eview **S**heet
DVR:	**D**esign **V**erification **R**eport
EDIF	**E**lectronic **D**esign **I**nterchange **F**ormat
ERS:	**E**quipment **R**equirement **S**pecification
FPGA:	**F**ield **P**rogrammable **G**ate **A**rray (a programmable logic device)
ICDD:	Control & Electrical Systems Design & Engineering Department
IPSNE:	Toshiba Corporation, **I**ndustrial and **P**ower Systems & Services Company, **N**uclear **E**nergy
IR:	**I**ndependent **R**eviewer
LPRM:	**L**ocal **P**ower **R**ange **M**onitor
MCL:	**M**aster **C**onfiguration **L**ist
NED:	**N**uclear **E**nergy Systems and Services **D**ivision
NICSD:	**N**uclear **I**nstrumentation & **C**ontrol **S**ystems **D**epartment
NRW-FPGA:	**N**on-**R**ewritable **F**ield **P**rogrammable **G**ate **A**rray
PHA:	**P**reliminary **H**azard **A**nalysis
PRM:	**P**ower **R**ange **M**onitor
PRS:	**P**roblem **R**eporting **S**heet
QA:	**Q**uality **A**ssurance
RTM:	**R**equirements **T**raceability **M**atrix
SCSI:	**S**mall **C**omputer **S**ystem **I**nterface
SDD:	**S**oftware **D**esign **D**escription
SER:	**S**afety **E**valuation **R**eport
SIL:	**S**oftware **I**ntegrity **L**evel
SQAP:	**S**oftware **Q**uality **A**ssurance **P**lan
SRS:	**S**oftware **R**equirements **S**pecification
VDCL:	**V**endor generated **D**ocument **C**heck **L**ist
VHDL:	**V**ery High Speed Integrated Circuit **H**ardware **D**efinition **L**anguage (A hardware description language that defines the FPGA circuit)
V&V:	**V**erification and **V**alidation
VFS:	**V**erification **F**ollow **S**heet
VVP:	**V**erification and **V**alidation **P**lan
VVR:	**V**erification and **V**alidation **R**eport

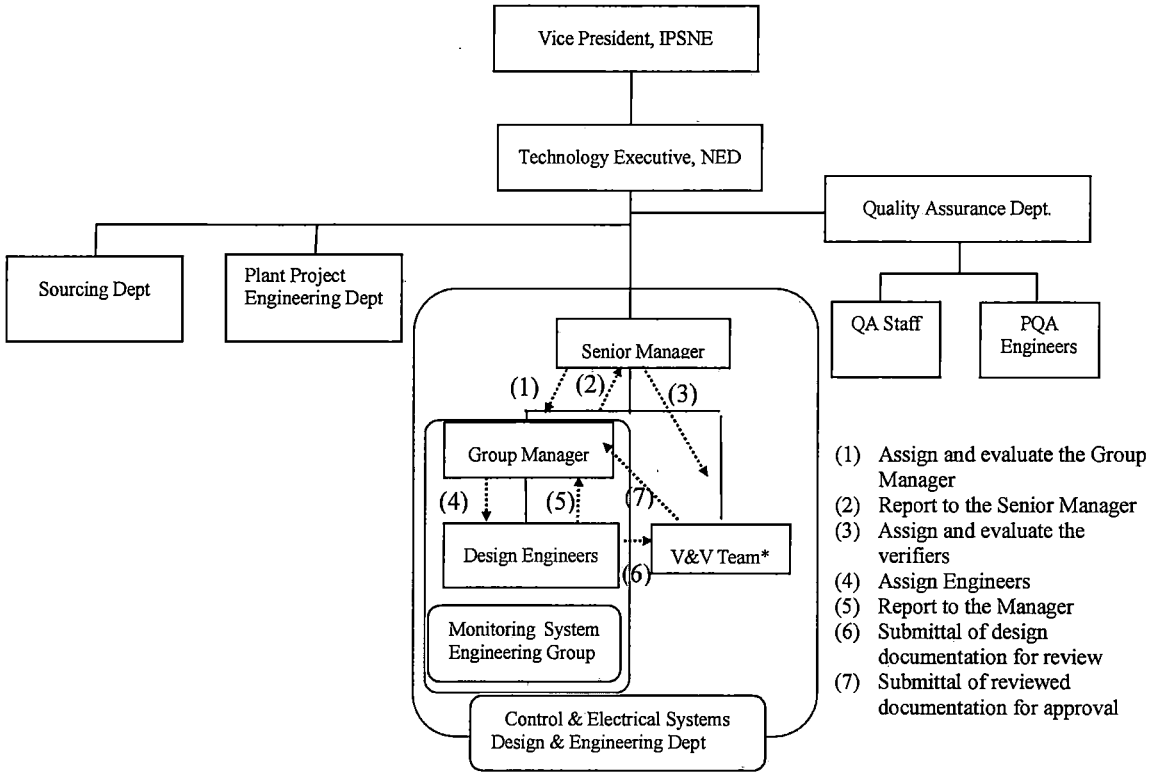
4 Verification and Validation Overview

4.1 Organization

The NRW-FPGA-Based PRM System Software Quality Assurance Plan (SQAP) (Reference 2.4.15) describes the V&V Team organization. Figure 4-1 is excerpted from the SQAP and depicts the NED V&V Team organization.

Both design and V&V activities shall be performed by Control & Electrical Systems Design & Engineering Dept. (ICDD). However, as shown in the figure above, the Monitoring System Engineering Group (which consists of the Design Engineers lead by the Group Manager) shall perform design activities, and the V&V team (that is independent from the Design Engineers) shall perform V&V activities which require independence.

NICSD shall describe its V&V organization in the NICSD VVP.



* The V&V team consists of persons who belong to the Control & Electrical Systems Design & Engineering Department, and who are independent from the Monitoring System Engineering Group with separate cost, schedule and resources.

Figure 4-1 NED Organization associated with this Plan

4.2 Master Schedule

Activities described in this VVP shall be performed according to the Master Engineering Schedule (Reference 2.4.17) that was established by NED at the beginning of the NRW-FPGA-Based PRM System Qualification Project (FPGA/SER Project).

For the V&V activities performed by NICSD, NICSD shall establish its master schedule based on NED's Master Engineering Schedule. NICSD shall provide its schedule to NED with the NICSD VVP (See section 5.2).

4.3 Software Integrity Level Scheme

The software integrity level (SIL) scheme shall be determined based on Table A-1 of AS-200A129 Digital System Development Procedure (Reference 2.4.6), which is considered to be equivalent to the Appendix B of IEEE Std 1012 (Reference 2.3.1).

The SIL shall be 4 for the PRM safety software and 3 for the PRM non-safety software as documented in the Appendix A of the SQAP. Note that all the V&V activities defined in section 5 shall be applied for both SIL-3 and SIL-4 PRM software.

4.4 Resource Summary

The Senior Manager of ICDD of NED shall assign appropriate persons for the V&V team to perform the NED V&V activities. The V&V team members shall meet the following restrictions:

- Be independent of the design activities in schedule, cost, and resource.
- Be technically qualified for the work performed.

NICSD shall assign appropriate persons for the NICSD V&V team to perform the NICSD V&V activities. NICSD shall state more detail about the resources for activities in the NICSD VVP. The NICSD V&V team members shall meet the following restrictions:

- Be independent of the design activities in schedule, cost, and resource.
- Be technically qualified for the work performed.

The NICSD Senior Manager or a Group Manager who is independent of the design activities shall be responsible for the assignment of the NICSD V&V team members.

This VVP includes some special procedural requirements to NICSD. NICSD shall prepare necessary resources including facilities and tools in order to meet the requirements.

4.5 Responsibilities

For the NED part of the V&V activities, the responsibilities of the V&V activities are defined in AS-200A130 Digital System V&V Procedure (Reference 2.4.7) as follows:

The Preparer(s) of documentation of V&V activities must:

- Be in the V&V team which is independent of the Engineering/Design Group that has responsibility for the software development activities, with separate cost, schedule and resources.
- Not have contributed to the design.
- Be technically qualified for the work performed.

The Independent Reviewer of documentation of V&V activities must:

- Be in the V&V team which is independent of the Engineering/Design Group that has responsibility for the software development activities, with separate cost, schedule and resources.
- Not have contributed to the design.
- Be independent of the Preparer of the V&V Activity Output Document (that is, the Independent Reviewer must not have collaborated on the preparation of the document).
- Be technically qualified for the work being reviewed.

The independent review of documentation of V&V activities, as well as design documentation, shall be performed by V&V personnel. As shown in Figure 4-1 the V&V personnel are independent of the Monitoring System Engineering Group.

All safety related development documents must also be approved in writing prior to use. The Approver is usually the Group Manager.

For the Preparer, the Independent Reviewer, and the Approver for specific documents, Table 3 of ICDD P-101 (Reference 2.4.13) shall be applied.

For the NICSD part of the V&V, NICSD shall assign NICSD V&V team for the NICSD V&V activities. The responsibilities of the Preparer, the Independent Reviewer, and the Approver of NICSD must be equivalent to those of NED stated above.

The NICSD V&V team shall be responsible for the following activities:

- Establishing the NICSD VVP
- Independent review of design documents
- Reviewing the Requirements Traceability Matrix (RTM) that is prepared based on the concept phase RTM, which is to be received from NED.
- Issuing the NICSD V&V report (VVR) at the end of each V&V phase.

The NICSD V&V team shall submit the NICSD VVP and NICSD VVRs to the NED V&V team without delay. The NED V&V team reviews those documents to determine whether they are acceptable for NED. If those documents are not acceptable, the NED V&V team

shall prepare Nonconformance Notice Report (NNR) in accordance with the SQAP (Reference 2.4.15).

NED V&V personnel may also perform witness activities on the works of NED and NICSD design engineers to verify that they are working in compliance with applicable internal standards. For NICSD design engineers, they are required to work in accordance with the special provisions from NED, especially provisions to avoid security risks. Results of these reviews if necessary, shall be documented in NED's VVR for each phase..

4.6 Tools, Techniques, and Methodologies

For tools, techniques, and methodologies, refer to Section 9 of the SQAP. The following is additional information about the tools that NICSD uses for its V&V activities:

1. Synplify Tool
   The Synplify tool synthesizes logic from VHDL source codes and produces Netlists. As by-products of logic synthesizing, Synplify performs syntactic check of the VHDL source codes and adequacy check of the synthesized logic.

2. Netlist Viewer tool
   The Netlist Viewer tool depicts the logic block diagrams according to the Netlists. The Netlist Viewer tool is used to inspect the Netlist to ensure the correct conversion of the logic, i.e. ensure that functional elements (FEs) are correctly connected in the Netlists. The Netlist Viewer tool is integrated as a function in the Actel Libero tool, which is an FPGA development package. (See 5.5.2)

3. Designer tool
   The Designer tool is a layout tool. It converts gate-level Netlists into a Fuse Map file. To generate the Fuse Map file, the Designer tool determines which cells in an FPGA chip are to be used, and makes connections to obtain the desired circuit defined by the Netlist. The Designer tool is used to generate the gate-level delay information.

4. ModelSim tool
   ModelSim tool is used for simulation of an FPGA using the gate-level Netlists and gate-level delay information generated by Designer tool, for generation of test signals for the PinPort device to test FPGAs, and for measurement of the toggle coverage rate for given test vectors.

5. Silicon Sculptor tool
   Silicon Sculptor tool embeds Fuse Maps generated by the Designer tool on the FPGA chips.

6. PinPort device
   The PinPort device has a small computer system interface (SCSI), which is connected by an SCSI cable to a personal computer containing the ModelSim tool.

For each test, the ModelSim tool generates inputs to, and monitors outputs from, the FPGA chip. For this testing, the FPGA chip is mounted in a socket in the PinPort device.

NICSD shall use these tools in accordance with NICSD procedure D-68020 (Reference 2.4.23). In addition, NICSD shall prepare an appropriate procedure meeting the requirements in section 3.2.3 of SQAP, in particular personnel training to use the tools. The procedure can be prepared as a part of the NICSD VVP.

NICSD may use test equipment for the validation testing of Units/Modules. This equipment includes a signal generator and a data recorder. The signal generator generates inputs to the Units/Modules, while the data recorder records outputs from the Units/Modules. To control the signal generator and the data recorder, test equipment software may be used.

To develop new test equipment software, or use legacy software, NICSD shall follow the SQAP including the requirements for configuration management, and D-68020. NICSD shall explain the V&V activities associated with the use of their tools in the NICSD VVP.

NED shall assess the controls of the tools and test equipment software as a V&V activity. See section 5.5.6, 5.6.4, and 5.7.4.

For system validation testing, NED may use test equipment software similar to that used for Unit/Module testing. To develop new equipment software, or use legacy software, NED shall follow the SQAP including the requirements for configuration management. Specifically:

- For newly developed test equipment software, NED shall follow the life cycle approach in accordance with AS-200A128 through AS-200A132. The SIL shall be 2 for the software, and the scope and rigor of V&V for the software are determined in accordance with SIL 2. The developed software shall be controlled under the configuration management requirements of section 10 of the SQAP.

- For legacy test equipment software, NED shall perform the following activities for the software:
  - Define the Test Equipment software functions required in the project.
  - Establish the equipment software acceptance criteria.
  - Establish the procedure to use the equipment software. This procedure includes the methods to record errors in accordance with the configuration management process.
  - Perform hazard analysis to ensure that the software causes no harm to the product.
  - Train the personnel to use the test equipment software.

Section 5.5 of SQAP defines the metrics that should be maintained for each NRW-FPGA-Based PRM system.

5 Verification and Validation Activities for This Project

(1) Management of V&V

IEEE Std 1012 (Reference 2.3.1) defines tasks for the management of V&V. Table 5-1 shows the corresponding activities in the project.

Table 5-1 V&V Tasks for Management of V&V

Task defined in IEEE Std 1012	Activity in this VVP
1) Software Verification and Validation Plan (SVVP) Generation	Establishment of this VVP
2) Baseline Change Assessment	The configuration management activities in section 5.10 covers the requirements of the Baseline Change Assessment
3) Management Review of V&V	V&V personnel shall review the V&V efforts at the end of each V&V phase, and summarize the results in the VVR.
4) Management and Technical Review Support	V&V personnel shall attend the design review meetings, which is prescribed in AS-200A005 (Reference 2.4.2), for management and technical support, if necessary.
5) Interface With Organizational and Supporting Processes	V&V personnel shall attend the project meeting to coordinate V&V effort with organizational and supporting processes.

(2) V&V Phases

Required V&V activities for the NWR-FPGA-Based development are defined in AS-200A130 "Digital System Verification & Validation Procedure" (Reference 2.4.7).

ICDD P-101 (Reference 2.4.13) describes how the requirements of the AS-200A128 (Reference 2.4.5) through AS-200A132 (Reference 2.4.9) are to be implemented in the development and procurement of FPGA-based systems from NICSD.

P-101 decomposes the V&V phases in AS-200A130 to the following, as shown in Figure 5-1:

(1) Project Planning and Concept Definition phase

(2) Requirements Definition phase

(3) Design phase

(4) Implementation and Integration phase

(5) Unit/Module Validation Testing phase

(6) System Validation Testing phase

(7) Operation and Maintenance (O&M) phase.

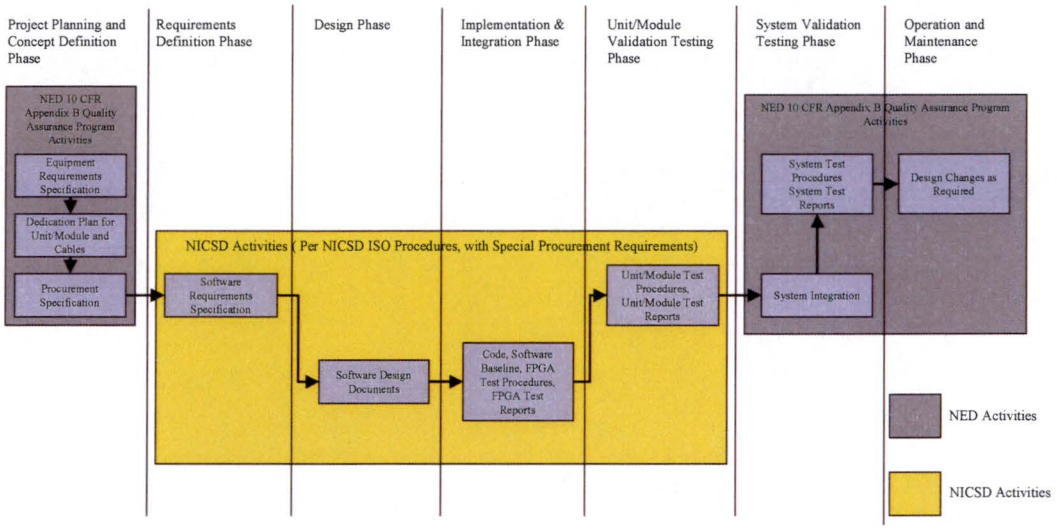


Figure 5-1 Process for Development and Procurement of FPGA-based systems

In addition, P-101 prescribes which parts NED shall perform and which parts NICSD shall perform. Further information for V&V activities for each phase is described in the following sections. In this project, the O&M phase is considered to correspond to the qualification testing phase. Note that the scope of this VVP does not include the O&M phase.

The following sections, V&V inputs and outputs are defined for each V&V phase. The source and format of the inputs and outputs are defined in relevant NED and NICSD standards.

5.1 Project Planning and Concept Definition Phase

NED V&V personnel shall perform all Project Planning and Concept Definition Phase (Concept Phase) V&V activities.

V&V Inputs:

(1) ERS (Review Document) (Reference 2.4.16)
(2) SQAP (Review Document) (Reference 2.4.15)
(3) Preliminary Hazard Analysis (PHA) Report (Review Document) (Reference 2.4.18)

V&V Outputs:

(1) VVP (This document)
(2) Document Review Reports
(3) Project Planning and Concept Definition Phase RTM
(4) Project Planning and Concept Definition Phase VVR

5.1.1 Preparation of VVP

NED V&V personnel shall prepare NED VVP in accordance with AS-200A130 and the SQAP.

5.1.2 Document Reviews

NED V&V personnel shall perform an independent review of the following documents for completeness, correctness, consistency, and accuracy:

- SQAP, including the Project Specific Configuration Management Plan.
- Equipment Requirement Specification (ERS)
- Preliminary Hazard Analysis Report (PHA)
- VVP (This document)
- Concept Phase RTM
- Concept Phase VVR

Note that the section 6 of the SQAP states the reviews for the ERS and VVP, and Appendix A of the SQAP defines the SIL applied to the PRM Systems.

All documents listed above will be independently reviewed. Document review is a method of verification to assure that the design output is correct and satisfactory by addressing that, the design inputs were correctly incorporated into the design, and the design output is reasonable compared to the design input. If the document includes design, the review shall be performed in accordance with AS-200A002 (Reference 2.4.1), the review result shall be documented on the Design Verification Report (DVR), and when applicable the Verification Follow Sheet (VFS) shall be used for identification of comments and following up the comments to close. Otherwise they may be documented using the DRS that is the exhibit of P-101.

For the review of the RTM, the Independent Reviewer shall review to ensure all entries made contain sufficient detail, complete and unambiguous.

5.1.3 Project Planning and Concept Definition Phase RTM effort

(1) Preparation of the RTM

NED design engineer shall prepare the Project Planning and Concept Definition Phase RTM, to track implementation of requirements.

The requirements shall be taken from the input documents of the Project Planning and Concept Definition, which are listed as "input" at the beginning of this section.

All the requirements entered in the RTM shall be collected and compiled by the RTM Preparers. The entries in the RTM should be limited to requirements which are verifiable (testable or measurable) but must completely cover all the functionality of the product under development.

The Preparer shall summarize any open items revealed by the RTM effort. The Design /Engineering Group must resolve these items to the satisfaction of the RTM Preparer and the Reviewer.

(2) Compilation of the Project Planning and Concept Definition Phase RTM report

NED design engineer shall prepare and release the Project Planning and Concept Definition Phase RTM report for internal use, with a summary of open items revealed by the RTM effort.

5.1.4 Concept Phase VVR

NED V&V personnel shall produce this VVR including:

(1) References to the reviewed documents.
(2) References to the DVRs.
(3) References to the Concept Phase RTM.
(4) Any findings, recommendations, or suggestions to reduce any risks identified in the V&V activities.

5.2 Establishment of NICSD V&V Plan

The NICSD V&V team shall establish its own VVP conforming to the NED VVP (this document) and submit the NICSD VVP to the NED V&V team. The NED V&V personnel shall review the NICSD VVP to assure that the NICSD VVP meets the requirements of the NED VVP. The review shall be performed in accordance with Section 6.4 of the SQAP, and recorded in a Vendor generated Document Check List (VDCL) in accordance with AS-200A010 (Reference 2.4.3). The NED V&V Team shall notify NICSD in writing about the results of this review and whether the NICSD VVP is acceptable. The Group Manger of the Monitoring System Engineering Group shall approve the NICSD VVP based on the review.

The NICSD VVP may be written in Japanese.

5.3 Requirements Definition Phase

NICSD shall perform the Requirements Definition Phase (Requirements Phase) V&V activities in accordance with the NICSD VVP. In addition, NED V&V personnel will perform the independent review of the updated PHA, and prepare an NED Requirement Phase VVR. This section states the minimum requirements for the NICSD VVP, which shall specify the details of the NICSD V&V activities.

V&V Inputs:

(1) ERS (Base Document)
(2) Project Planning and Concept Definition Phase RTM (Base Document)
(3) Unit/Module Design Specifications (Review Document)
(4) PHA Report (Review Document)

V&V Outputs:

(1) Document Review Reports (by NICSD and NED)
(2) Requirements Definition Phase RTM (by NICSD)
(3) NICSD Requirements Phase VVR (by NICSD)

(4) Requirements Phase VVR (by NED)

5.3.1 Document Reviews

The NICSD V&V team shall perform the following independent reviews:
Review of the Software Requirements Specification (SRS) included in the Unit Design Specifications and Module Design Specifications, for completeness, correctness, consistency, and accuracy. The review includes a check that the requirements are unambiguous, testable or observable, and that the requirements provide acceptance criteria or acceptable ranges of values. The functional requirements, interface requirements and functional allocation written in the SRS shall be reviewed.

The reviewers shall document results of the review in accordance with NICSD D-68016 (Reference 2.4.19).

The NED V&V personnel shall independently review the Requirements Definition Phase PHA, and document the results of the review in accordance with AS-200A002.

5.3.2 Requirements Definition Phase RTM effort

(1) Preparation of Requirements Phase RTM

NICSD design engineer shall generate the Requirement Definition Phase RTM to trace the requirements collected during the Concept Phase RTM effort to the requirements in the Unit/Module Design Specifications.

The NICSD V&V team shall independently review this RTM, and verify the following:

- The requirements are traceable "forwards" from the base requirements (from the Concept Phase RTM) to the SRS; that is, that all the requirements from the Concept Phase appropriately correspond to the functions described in the Unit/Module Design Specifications. In addition, the SIL requirements from the Concept Phase are addressed in the SRS.
  It should be noted that since NED prepares the ERS based on the vendor package, the requirements in the Concept Phase RTM should be consistent with those in the SRS.
- The requirements are traceable "backwards" from the SRS to the Concept Phase. That is, all the requirements listed in the SRS are covered by the Concept Phase requirements, and no new requirements have been created in the Unit/Module Design Specification.

The NICSD Design Group and V&V team shall report any open items or nonconformance items revealed by the Requirements Definition Phase RTM effort.

The NICSD VVP shall specify the method to track the completion of open items.

(2) Compilation of the Requirements Definition Phase RTM report

NICSD shall compile the Requirements Definition Phase RTM report. The RTM report must include the RTM, how each requirement is addressed in the Unit/Module Design Specifications, the open items, and any resolutions to the open items.

5.3.3 Issuance of the Requirements Definition Phase V&V Report

The NICSD V&V team shall issue the NICSD Requirements Definition Phase VVR. The report includes:

(1) Copies of or references to Document Reviews.
(2) Reference to the Requirements Definition Phase RTM
(3) Any findings, recommendations, or suggestions to reduce risks identified in the V&V activities.

NED V&V personnel shall establish the Requirements Definition Phase VVR based on the NICSD VVR. The report includes any findings, recommendations, or suggestions to mitigate any V&V risks in this phase. The NICSD VVR shall be attached to the NED VVR.

5.4 Design Phase

In the design phase, NICSD produces the FPGA Design Specifications including the Software Design Description (SDD) for each FPGA. Because FPGAs are independent from each other, most of the activities in this phase and the implementation phase can be performed independently.

NICSD shall perform the Design Phase V&V in accordance with the NICSD VVP. In addition, NED V&V personnel will perform the independent review of the updated PHA, and prepare an NED Design Phase VVR. This section states the minimum requirements for the NICSD VVP, which shall specify the details of the NICSD V&V activities.

It should be noted that the logic design is made using FEs and interconnects between FEs. All the FEs used in design are registered in the FE library through the life-cycle activities defined in the NICSD procedure D-68018 (Reference 2.4.21).

V&V Inputs:
(1) Unit/Module Design Specifications (Base Document)
(2) Requirements Definition Phase RTM (Base Document)
(3) FPGA Design Specification (Review Document)
(4) PHA Report (Review Document) (Reference 2.4.18)

V&V Outputs:
(1) Document Review Reports (by NICSD and NED)
(2) Design Phase RTM (by NICSD)
(3) NICSD Design Phase VVR (by NICSD)
(4) Design Phase VVR (by NED)

Note: NICSD V&V activities for FEs are described separately in Section 5.8.

5.4.1 Document Reviews

The NICSD V&V team shall perform an independent review of the SDD included in the FPGA Design Specifications for completeness, correctness, consistency, and accuracy. The FPGA design shall comply with the design rules of FPGA logic in Appendix A of NICSD procedure D-68017 (Reference 2.4.20). The special instruction to be applied in the review is that the logic of FPGA shall be constructed of previously tested FEs, and the interface to each FE shall be consistent with that specified in FE specifications.

The review includes the check of FE documents. (See section 5.8.)

The reviewers shall document results of the review in accordance with NICSD D-68016.

The NED V&V personnel shall independently review the Design Phase PHA, and document the results of the review in accordance with AS-200A002.

5.4.2 Design Phase RTM effort

(1) Preparation of Design Phase RTM

NICSD shall perform the Design Phase RTM effort to trace the design as documented in the FPGA Design Specifications to the Requirements Phase RTM effort.

The NICSD V&V team shall independently review this RTM, and verify the following:

- The requirements are traceable "forwards" from the base requirements in the Requirements Phase to the FPGA Design Specifications; that is, each FPGA in the FPGA Design Specifications addresses the functions and interfaces of the FPGA requirements described in the Module Design Specifications. In addition, the SIL requirements from the Requirements Phase are addressed in the FPGA Design Specifications.
- The requirements are traceable "backwards" from the FPGA Design Specifications to the Requirements Phase.

The NICSD Design Group and V&V team shall report any open items revealed by the Design Phase RTM effort. The report shall be issued in accordance with the official document procedure of NICSD. The Design Group must resolve these items to the satisfaction of the RTM Preparer and the Reviewer. Any open items not resolved during this phase must be carried to the next phase.

The NICSD VVP shall specify the method to track the completion of open items.

(2) Compilation of the Design Phase RTM report

NICSD shall compile the Design Phase RTM report. The Design Phase RTM report must include the RTM, how each requirement is addressed in the FPGA Design Specifications, the open items, and any resolutions to the open items.

5.4.3 Issuance of Design Phase V&V Activities Report

NICSD shall issue the NICSD Design Phase VVR. The report includes:

(1) Copies of or references to Document Reviews.

(2) Copies of or references to the results of the checks of the FE document, the FE library control, and the software tool control. (See 5.8)
(3) Reference to the Design Phase RTM.
(4) Any findings, recommendations, or suggestions to reduce any risks identified in the V&V activities.

NED V&V personnel shall establish the NED Design Phase VVR based on the NICSD VVR. The report includes any findings, recommendations, or suggestions to mitigate any V&V risks in this phase. The NICSD VVR shall be attached to the NED VVR.

5.5 Implementation and Integration Phase

NICSD shall perform the Implementation and Integration Phase (Implementation Phase) V&V in accordance with the NICSD VVP. In addition, NED V&V personnel will perform the independent review of the updated PHA, and prepare an NED Implementation Phase VVR. This section includes the minimum requirements for the NICSD VVP, which will specify the details of the NICSD V&V activities.

The development activities in the implementation and integration phase are divided into the following steps as illustrated in P-101.

Step (1): VHDL Source Coding
Step (2): FPGA Implementation
Step (3): FPGA Validation

In step (1), NICSD design engineers generate VHDL source codes implementing the functional requirements from the SDD using editor tools. In the coding, verified functional elements (FEs) are used to implement specific logic steps. Although editor tools are software, errors in the editor tools are likely to be obvious to the NICSD design engineers.

In step (2), the VHDL source codes are compiled into gate-level Netlists by the Synplify tool. To verify that the gate-level Netlists are correctly converted, the Netlists are drawn in logic diagrams, and visually compared with the VHDL source codes. The gate-level Netlists are converted to Fuse Maps by the Actel Designer tool, then the NICSD design engineers embed the Fuse Maps into FPGA chips by the Silicon Sculptor tool. Test vectors used in step (3) and FPGA Validation test procedures are prepared in this step. The test vectors shall be prepared so that every operative connection between FEs is tested. More detailed explanation is described in section 5.5.2.

Note that "FPGA Validation test procedure" is equivalent to "FPGA Test Procedure" in NICSD procedure D-68017. Similarly, "FPGA Validation test report" is equivalent to "FPGA Test Report" in NICSD procedure D-68017.

In step (3), the NICSD design engineers test the FPGA chips with embedded Fuse Maps using the PinPort device and ModelSim tool. The ModelSim tool generates inputs to the FPGAs according to the test vectors, which are generated prior to the FPGA validation testing.

For steps (2) and (3), software tools are used where the results of software tool errors may not be obvious to the NICSD design engineers. So, the verification and testing are carefully considered.

The V&V in this phase includes activities (discussed below) to mitigate software tool errors, such as incorrect compilation of VHDL source codes, incorrect gate assignment, or faulty connections between FEs.

V&V Inputs:
(1) FPGA Design Specifications (Base Document)
(2) Design Phase RTM (Base Document)
(3) FPGA Source Code written in VHDL language (Review Document)
(4) Log files produced by software tools (Review Document)
(5) FPGA validation test procedure (Review Document)
(6) FPGA validation test reports (Review Document)
(7) Software Baseline (Review Document)
(8) PHA Report (Review Document)

V&V Outputs:
(1) Document Review Reports (by NICSD and NED)
(2) Implementation Phase RTM (by NICSD)
(3) NICSD Implementation Phase VVR (by NICSD)
(4) Implementation Phase VVR (by NED)

5.5.1 VHDL Source Codes

The NICSD V&V team shall review the VHDL source codes for FPGA logics with the depth and intensity commensurate with the SIL of the source codes.
The review includes:

- Tracing the source code to the FPGA design specifications to verify correctness, consistency, completeness, and accuracy.
- Reviewing the source code for compliance with the design rules of FPGA logic in Appendix A of NICSD procedure D-68017.

In particular, the logic for the safety system FPGA must consist of combinations of the FEs. The review shall check to ensure that the interfaces between FEs are correct.

5.5.2 Logic Synthesis and Layout Verification

The NICSD design engineers use the Synplify tool to compile a VHDL source code to gate-level Netlists. A Netlist is stored in an EDIF (Electronic Design Interchange Format) file.

The Netlist Viewer tool integrated in the Actel Libero tool depicts logic diagrams according to the Netlist. The NICSD design engineers compare the original VHDL files with the logic diagrams to verify the correctness of the compilation. In the comparison, checks shall be made for the block connections and the FE interfaces. Note that FEs are seen as elementary logic blocks on the logic diagrams.

Since VHDL source codes implement logics using FEs, the Netlist includes "calls" for the FEs. The Designer tool integrates the Netlist file and the FE Netlists withdrawn from the FE library into a single Fuse Map

The NICSD V&V team shall perform the verification, which includes:

(1) Checking the message files produced by Synplify tool and Designer tool, to confirm that the logic synthesis and layout are performed normally. The software tool options and tool warning messages shall be checked.
(2) Review the results of comparison between the logic block diagrams and VHDL files.

The NICSD VVP shall state the method to be used in performing the verification.

5.5.3 FPGA validation testing

FPGA validation testing shall be performed in accordance with NICSD procedure D-68017, using test purpose FPGAs that are prepared in the same manner as those FPGAs to be implemented in the modules.

The design engineers who perform FPGA testing shall prepare Problem Reporting Sheets (PRS) in accordance with NICSD procedure D-68017, to document any test failures, any product or configuration nonconformance, or any errors in the test procedure itself. The PRS shall be resolved by modifying design documentation, logic, or testing plans and procedures as necessary, revising all previous materials and performing reviews as necessary to incorporate the changes. NICSD shall document the amount of retest required for these changes, and shall perform retests as needed to resolve all PRSs.

5.5.4 Document Reviews

The NICSD V&V team shall perform an independent review of the following items:

(1) FPGA validation test procedures

Review the FPGA validation test procedures prepared by the NICSD Design Group for completeness, correctness, consistency, and accuracy. The FPGA Validation tests shall achieve 100% toggle coverage of the active FE connections using the toggle coverage scheme provided by the ModelSim tool.

The FPGA Validation tests shall be performed to assure that every operative connection between FEs is toggled. Note that not all connections in a FPGA can be toggled, because some connections are connected to ground level or power level directly.

NICSD shall evaluate the test coverage ratio, i.e. the number of toggled connections in the test to the number of operative connections, and confirm that the ratio achieves 100%.

In addition, experience has shown that 100% toggle testing may not fully test all connections between FEs. For example, in testing an OR gate that inputs signal A and B, and outputs signal X, toggling the signal A while the signal B is set to "1" has no meaning, since the signal X keeps "1" regardless of the signal A value. NICSD design engineers shall review the circuit performance using the Netlist Viewer tool to determine if additional

tests are needed to check all connections. When needed, these additional tests are added to the test vector. The final test vector is fully verified to assure the completeness of the logic of the FPGA circuit design.

(2) FPGA validation test reports

After NICSD design engineers (who are independent of the design engineers of the FPGA product being tested as required by D-68016) will perform these tests, the NICSD V&V Team shall reviews the FPGA validation test reports to verify:

- The tests have been appropriately performed according to the test procedures.
- There are sufficient tests records, including the findings during the validation testing
- The tests results are acceptable.
- If above issues are not satisfied, the test shall be performed again.

(3) Software Baseline

The NICSD design engineers shall establish the Software Baseline after FPGA Validation Testing is finished. The NICSD V&V Team shall review the Software Baseline to confirm that the items required by the NICSD procedure D-68019 (Reference 2.4.22) have been appropriately established.

(4) Implementation Phase PHA

The NED V&V personnel shall independently review the Implementation Phase PHA, and document the results of the review in accordance with AS-200A002.

5.5.5 Implementation Phase RTM effort

(1) Preparation of Implementation Phase RTM

NICSD shall perform the Implementation Phase RTM effort to trace the FPGA validation test procedures to the preceding phases of the RTM effort.

The NICSD V&V team shall independently review this RTM, and verify the following:

- The requirements are traceable "forwards" from the base requirements to the FPGA; that is, that all the requirements in the Design Phase are correctly addressed in the FPGA validation test cases and the test results are acceptable.
- The requirements are traceable "backwards" from the FPGA validation procedures to the Design Phase.

(2) Compilation of the Implementation Phase RTM Report

- The Implementation Phase RTM report must include the RTM, how each requirement is addressed in the FPGA validation test procedures, the open items, and any resolutions to the open items.

5.5.6 Assessment of Software tools

NED V&V personnel shall assess the NICSD control of the software tools used in the design and V&V activities.

NED V&V personnel shall review NICSD's records for software tool control to ensure:

- FPGAs used for the project are manufactured using the correct tool versions.
- NICSD is controlling the software tools in accordance with procedures that NED has reviewed and approved.

NED may also perform in-process audits and witness activities to verify that NICSD is working in compliance with these controls and procedures. Results of these reviews, and audits if necessary, shall be documented in NED's VVR for this phase.

5.5.7 Issuance of Implementation Phase V&V Report

NICSD shall issue the NICSD Implementation Phase VVR. The report includes:

(1) Copies of or references to Document Reviews.
(2) Copies of or references to the source code reviews.
(3) Copies of or references to the software tools message file checks
(4) Copies of or references to the logic block diagram checks
(5) Reference to the Implementation Phase RTM
(6) Any findings, recommendations, or suggestions to reduce risks identified in the V&V activities.

NED V&V personnel shall establish the Implementation Phase VVR based on the NICSD VVR. The report includes any findings, recommendations, or suggestions to mitigate any V&V risks in this phase. The NICSD VVR shall be attached to the NED VVR.

5.6 Unit/Module Validation Testing Phase

After the FPGA testing has finished, the validated FPGA logics are embedded into new FPGAs, which are soldered on the printed circuit boards. Finally, the printed circuit boards are assembled as the modules. NICSD shall perform Unit/Module Validation Testing Phase V&V in accordance with the NICSD VVP. In addition, NED V&V personnel will perform the independent review of the updated PHA, and prepare an NED Unit/Module Validation Testing Phase VVR. This section states the minimum requirements for the NICSD VVP, which will specify the details of the NICSD V&V activities.

V&V Inputs:

(1) Module validation test procedures (Review Document, Base Document)
(2) Unit validation test procedures (Review Document, Base Document)
(3) Module validation test reports (Review Document)
(4) Unit validation test reports (Review Document)
(5) User Documentation for Unit and Module (Review Document)
(6) Requirements Phase RTM (Base Document)
(7) PHA Report (Review Document)

V&V Outputs:

(1) Document Review Reports (by NICSD and NED)
(2) Unit/Module Validation RTM (by NICSD)

(3) NICSD Unit/Module Validation Testing Phase VVR (by NICSD)
(4) Unit/Module Validation Testing Phase VVR (by NED)

5.6.1 Unit and Module validation testing

(1) NICSD shall perform the Module validation testing and Unit validation testing by personnel who are independent of the Design Group. The tests shall be performed following the Module validation test procedures and Unit validation test procedures respectively. NICSD shall establish these test procedures prior to the testing.
(2) NICSD shall prepare Problem Reporting Sheets (PRS) in accordance with NICSD procedure D-68016 (Reference 2.4.19), to document any test failures, any product or configuration nonconformance, or any errors in the validation test procedure itself. The NICSD Test Group shall forward the PRS to the NICSD Design Group for resolution. The PRS shall be resolved by modifying design documentation, logic, or testing plans and procedures as necessary, revising all previous materials and performing reviews as necessary to incorporate the changes. NICSD shall document the amount of retest required for these changes, and shall perform retests as needed to resolve all PRSs.

5.6.2 Document Reviews

(1) Module validation test procedures
The NICSD V&V team shall review the Module validation test procedures prepared by the NICSD design engineers for completeness, correctness, consistency, and accuracy.

(2) Unit validation test procedures
The NICSD V&V team shall review the Unit validation test procedures prepared by the NICSD design engineers for completeness, correctness, consistency, and accuracy.

(3) Module validation test reports
The NICSD design engineers shall prepare the Module validation test reports including the signed validation test procedures, and any PRSs written as results of the testing. The NICSD V&V personnel shall perform an independent review of the Module validation test reports. The validation test reports shall be prepared and reviewed in accordance with NICSD procedure D-68016. In this review, the Module validation test procedures are considered to be base documents.

(4) Unit validation test reports
The NICSD design engineers shall prepare the Unit validation test reports including the signed validation test procedures, and any PRSs written as results of the testing. The NICSD V&V personnel shall perform an independent review of the Module validation test reports and the Unit validation test reports. The validation test reports shall be prepared and reviewed in accordance with NICSD procedure D-68016. In this review, the Unit validation test procedures are considered to be base documents.

(5) User Documentation for Unit and Module
The NICSD design engineers shall prepare the Unit and Module user documentation, which includes the contents stated in Section 4.1.6 of SQAP at minimum. The NICSD V&V personnel shall perform an independent review of the user documentation.

(6) Unit/Module Validation Testing Phase PHA
The NED V&V personnel shall independently review the Unit/Module Validation Testing Phase PHA, and document the results of the review in accordance with AS-200A002.

5.6.3 Unit/Module Validation Phase RTM effort

(1) Preparation of Unit/Module Validation Phase RTM
NICSD shall perform Unit/Module Validation Phase RTM effort to trace the requirements from Requirements Phase RTM, and report any open items revealed by this RTM effort.

The NICSD Design Group must resolve these items to the satisfaction of the RTM Preparer and the Reviewer. NICSD must resolve all open items before the end of Unit/Module Validation Testing Phase. NICSD and NED shall confirm that the validation tests comprehensively validate all the entries in the RTM from the Requirements Phase.

(2) Compilation of the Unit/Module Validation Phase RTM report
The NICSD V&V team shall compile the Unit/Module Validation Phase RTM report

5.6.4 Assessment of Test Equipment Software
NED V&V personnel shall assess the NICSD control of the test equipment software, if used in the Unit/Module Validation Testing.

NED V&V personnel shall review NICSD's records for test equipment software control to ensure:

- Test equipment software used for the project tests is prepared in accordance with procedures that NED V&V personnel have reviewed and approved.
- NICSD is controlling the software tools in accordance with NICSD procedure D-67003 (Reference 2.4.24).

NED may also perform in-process audits and witness activities to verify that NICSD is working in compliance with these controls and procedures. Results of these reviews, and audits if necessary, shall be documented in NED's VVR for this phase.

5.6.5 Issuance of the Unit/Module VVR
The NICSD V&V team shall establish the NICSD Unit/Module VVR. The report includes:

(1) A description of how the V&V activities were completed.
(2) A description of how adherence to each software life cycle requirements and system requirements were demonstrated,
(3) Copies of or reference to the NICSD VVRs issued for requirements phase through implementation phase.
(4) References to the independent reviews of the unit and module hardware review. (See 5.9)

(5) Copies of or references to Unit/Module Validation Test Reports, including the configuration of the test specimen.
(6) Reference to the Unit/Module Validation Phase RTM.

Approval of this phase VVR confirms that all required reviews and testing were performed completely and that no unresolved anomalies (PRSs) or issues remain.

NED V&V personnel shall establish the Unit/Module Verification and Validation Final report based on the NICSD VVR, when the NICSD VVR is acceptable to NED. The report includes any findings, recommendations, or suggestions on using the NICSD Unit/Module VVR. NICSD and NED shall confirm that the validation tests comprehensively validate all the entries in the RTM from Requirements Phase.

5.7 System Validation Testing Phase

NED V&V personnel shall perform the System Validation Testing Phase V&V activities.

V&V Inputs:
(1) ERS (Base Document)
(2) System Validation test procedure (Review Document)
(3) System Validation test report (Review Document)
(4) System Validation Testing Phase RTM (Review Document)
(5) Concept Phase RTM (Base Document)
(6) Hazard Analysis Report (Review Document)

V&V Outputs:
(1) Document Review Reports (by NED)
(2) System Validation Testing Phase RTM (by NED)
(3) System Verification and Validation Final report (by NED)

5.7.1 System Validation Testing

(1) NED PQA (see Figure 4-1) shall perform the system validation testing.
(2) NED PQA shall prepare nonconformance notice reports (NNRs) to document any test failures, any product or configuration nonconformance, or any errors in the validation test procedure itself. NED PQA shall forward the NNRs to the Design Group for resolution, and perform retests as needed to resolve all NNRs.
See sections 5.7.2 through 5.7.5 for NED V&V activities.

5.7.2 Document Reviews

NED V&V personnel shall review the system validation testing procedures (which are prepared by NED design engineers) and the System Validation Test Reports (which are prepared by NED design engineers), and any NNRs written as a result of the testing.

The NED V&V personnel shall independently review the final hazard analysis report, and document the results of the review in accordance with AS-200A002.

5.7.3 System Validation Testing Phase RTM effort

(1) Preparation of System Validation Testing Phase RTM

NED V&V personnel shall perform the System Validation Testing Phase RTM effort to trace the requirements from Concept Phase RTM for the System. NED shall confirm that the validation tests comprehensively validate all the entries in the Concept Phase RTM.

(2) Compilation of the Final RTM report

The NED design engineers prepare the Final RTM report. The Final RTM report must include the RTM, how each requirement is addressed in the test results, and resolutions to all open items. The Final RTM shall be reviewed by NED V&V personnel, and approved by the Group Manager of the Monitoring System Engineering Group.

5.7.4 Assessment of Test Equipment Software

NED may use Test Equipment Software for the System Validation Testing. In that case, NED test personnel shall use the software in accordance with the requirements for test equipment software in section 4.6.

NED V&V personnel shall review the records for test equipment software control to ensure:

- Test Equipment Software used for the tests is prepared in accordance with the SQAP and section 4.6.
- The test equipment software is controlled using Master Configuration List (MCL) in accordance with AS-200A131.

If NED PQA uses the test equipment software that NICSD developed for Unit/Module testing for system testing, the test equipment software shall be considered as legacy software discussed in section 4.6.

5.7.5 Issuance of the final VVR

The NED V&V Team shall prepare, review and approve the Verification and Validation Final report. The report includes:

- A description of how the V&V activities were completed,
- A description of how adherence to each software and system requirement was demonstrated,
- System configuration tested,
- Version data for all test equipment software used in the testing.

Approval of the final VVR confirms that all required reviews and testing are performed completely and that no unresolved anomalies or issues remain.

5.8 Functional Element V&V

NICSD design engineers control a library of general purpose FEs. For the FEs used in the FPGAs for the PRM system, V&V effort from the requirements phase through the implementation phase shall be applied. The depth and intensity of the V&V effort shall be in accordance with the SIL of the target FPGAs.

NICSD shall follow NICSD procedure D-68018 (Reference 2.4.21) for NICSD activities related to the design, V&V, testing or modification of FEs.

The following is the outline of the procedure prescribed in D-68018:

(1) FE Requirements Definition

The FE Requirements Specification is established to address at a minimum:

- FE functional requirements,
- Input/Output Signals,
- Interface/Interaction with other FE

(2) FE Design

The FE Specification (also referred to as a Software Design Document or SDD) is established. The FE Specification specifically states how all of the requirements specified in the FE Requirements Specification for this FE will be implemented. The FE Specification should contain sufficient criteria to support verification testing of the FE when performing FE testing.

The RTM is prepared to trace the design features in the FE Specification to the requirements shown in the FE Requirements Specification.

The FE test procedure that documents the following process is prepared:

- Make a VHDL source code which only indicates the connection to I/O pins and call the FE EDIF File.
- Convert the VHDL source code into an EDIF File with the synthesis tool and convert the EDIF File into a Fuse map with the layout tool.
- Implement the Fuse-map into the FPGA chip with the implementation tool.
- Mount the implemented FPGA chip on the signal test tool.
- Test the FE embedded in the FPGA chip for all possible input patterns to determine the correctness on the signal test tool.

The RTM is prepared to trace the tests in the FE test procedure to the requirements shown in the FE Requirements Specification.

(3) FE Coding

The coding of FEs is performed in VHDL. FEs are designed in accordance with the design rules shown in D-68017 Appendix A.

VHDL source code is translated into FE EDIF File with the logic synthesis tool.

(4) FE Testing

The tests are performed in accordance with the FE Test Procedure, and the Test Report is produced.

(5) Final FE Acceptance/Release

The FE is registered into the FE library after the confirmation of the issuance of the Test Report.

(6) Maintenance Phase
FE logic modifications are approved, documented, verified and validated, and controlled.

Above activities corresponds to the FE life cycle phases in SQAP (Reference 2.4.15) as shown in Table 5-1.

Table 5-2 The Relation between FE Life Cycle Phase and Activities for FE per D-68018

Expected FE Life Cycle Phase in SQAP	Activities for FE per D-68018
Requirements Definition Phase	FE Requirements Definition
Design and Implementation Phase	FE Design, FE Coding,
Testing Phase	FE Testing, Final FE Acceptance/Release
N/A	Maintenance Phase

NICSD shall perform the following V&V activities in the FPGA/SER project.

5.8.1 Document Check

The NICSD V&V team shall check the following documents to ensure that NICSD procedure D-68018 is appropriately applied for FEs placed in the FE library and used in the PRM project:

- FE Requirements Specification
- FE Specification
- RTM between the FE Specification and the FE Requirements Specification
- FE test procedure
- RTM between the FE Specification and the FE test procedure
- FE test report

In the check, the NICSD V&V team shall ensure that the full pattern tests have been appropriately performed for each FE.

The NICSD VVP shall document the procedure for the check. The NED V&V Team shall review this procedure as part of the review of NICSD's VVP.

The results of the check shall be documented and included in the Design phase VVR, and shall be reviewed by NED V&V personnel. See section 5.4.

5.8.2 Check of the FE library control and the software tool control

The NICSD V&V team shall check that appropriate control activities have been performed as follows:

- The FE library is being controlled in accordance with NICSD procedure D-68019.
- The software tools are being controlled in accordance with NICSD procedure D-68020 (Reference 2.4.23)

The results of the check shall be documented and included in the NICSD Design phase VVR, and shall be reviewed by NED V&V personnel. (See section 5.4)

5.9 Hardware V&V

The NICSD V&V team shall perform the independent review of the unit and module hardware design in accordance with NICSD procedure D-68016. The results of the review shall be documented and reported as a part of Unit/Module Validation Testing Phase VVR.

5.10 Configuration Management

SQAP Section 10 describes the Configuration Management Plan to be used by NED and NICSD in this project. Required V&V activities throughout the project are as follows:

- The NED V&V Team shall perform V&V activities on the NED MCL throughout the project life cycle in accordance with the requirements of Procedure AS-200A130. Specifically, this includes performing an independent review of the software baseline (when applicable) throughout the project. The NED V&V Team shall document the results of these activities in the NED VVR for each phase.
- The NICSD V&V Team shall perform V&V activities on the NICSD MCL throughout the NICSD effort in accordance with NICSD VVP. The NICSD V&V team shall document the results of NICSD V&V activities in the NICSD VVR for each phase. The specific activities to be performed by NICSD V&V personnel will be described in NICSD's VVP.
- The NED V&V Team shall review the NICSD V&V Team VVR to ensure that NICSD is performing the appropriate V&V activities for the NICSD MCL. NED shall document the results of this review in the NED VVR for each life cycle phase.

Note that the Project Specific Configuration Management Plan is contained in the SQAP; accordingly, independent review of the SQAP adequately completes the AS-200A130 and AS-200A131 procedure requirement for independent review of the Project Specific Configuration Management Plan.

6 Software Verification and Validation Reporting

The NICSD VVP shall state that the reports to be issued by NICSD include the followings:

- Problem Reporting Sheet (PRS)
  Problem Reporting Sheet shall be prepared to document any test failures, any product or configuration nonconformance, or any errors in the test procedure itself during FPGA and Unit/Module validation testing. See D-68016 (Reference 2.4.19) and D-68017 (Reference 2.4.20).
- NNR
  An NNR shall be issued if NICSD finds any problems in documents, equipment, or activities, for which an NICSD VVR has been already issued. See AS-300A006 (Reference 2.4.10).
- RTM Reports for Phases in NICSD's Scope
  RTM Reports shall be prepared to trace the requirements in the previous phase to the current phase documents.
- VVR for each phase
  A VVR shall be prepared at the end of each V&V phase. The report shall include the results of documents reviews, copies of or references to PRS or NNR, and RTM Reports.

These NICSD reports shall be written in Japanese.

The reports issued by NED include:

- NNR
  An NNR shall be issued if NED finds any problems in documents, equipment, or activities, for which a VVR has been already issued. In addition, an NNR shall be issued to document any test failures, any product or configuration nonconformance, or any errors in the test procedure itself during system validation testing. See AS-300A008 (Reference 2.4.11).
- RTM Reports in NED's Scope
  RTM Reports shall compare the results of the System Validation Testing Phase with the requirements in the Project Planning and Concept Definition Phase.
- Hazard Analysis Report
  The Hazard Analysis Report shall be prepared and updated to determine if the design and associated activities throughout the life cycle are established in a manner that minimize risk and design errors. The PHA Report shall be first prepared at the Concept Phase, and be updated from the Requirements Definition Phase through System Validation Testing Phase.
- VVR for each phase
  A VVR shall be prepared at the end of each V&V phase. The report includes the results of documents reviews, copies of or references to PRS or NNR, NICSD VVRs, and references to the PHA Report and RTM Report.
- V&V Final Report
  The V&V Final Report shall be established at the end of V&V activities. The Report includes copies or references to all VVRs from the life cycle phases.

These NED reports shall be written in English and available in NED offices for audit. For preparation of Hazard Analysis Reports, see section 4.2.4 of SQAP.

7 V&V Administrative Requirements

7.1 Problem Reporting and Corrective Action

If NED or NICSD finds any problem in documentation, equipment, or design and V&V activities after the Software Baseline has been established in the Implementation Phase, the problems shall be reported, and corrective action shall be taken in accordance with section 8 of SQAP (Reference 2.4.15).

7.2 Task Iteration Policy

Affected V&V tasks or activities shall be repeated if design documents are changed in accordance with AS-200A015 (Reference 2.4.4) or if this VVP is updated. AS-200A015 prescribes a change control procedure consisting of change proposal, evaluation of the change, and authorization of change. In a change proposal, the design change is specified in a Design Change Notice (DCN) which includes the change item, current design, previous design, and the reason of the change.

If design documents are changed, the independent review shall be performed for the affected documents. Further, the design engineer shall update the RTM and the PHA to reflect the design change. This requires another independent review of the RTM. As a result, the VVR of the phase for the updated documents shall be updated.

For RTMs, design engineers shall revise the RTM even if there is nothing affected by the design change. V&V personnel shall verify that the decision of the design engineers as to the need for documentation change is correct.

Note that the change of the RTM may affect the next phase RTM. The design engineers shall follow the propagation of the effects of change through RTMs. All changes of RTMs shall be reviewed by V&V personnel.

The above policy applies to both the NED and the NICSD V&V activities.

For the case of this VVP update, see the next section.

7.3 Deviation Policy

If the NED V&V personnel determine that this VVP must be changed, the change shall be made in the same manner in which this plan has been established, i.e. the update shall be reviewed independently, and approved by the Project Manager.

For the approval of the VVP change, the Project Manager may need to know the impact on the quality of the project, the schedule, and the resources. The V&V personnel must explain this information to the Project Manager along with the reason of the change.

When the VVP is updated, the NED V&V personnel shall perform the following actions:

- The NED V&V personnel shall assess the effect of the change to determine if there are any V&V activities to be repeated.
- The NED V&V personnel shall repeat the needed V&V activities.
- The NED V&V personnel shall notify the NICSD V&V team about the change to the NED VVP.

When the VVP is updated, the NICSD V&V team shall perform the following actions:

- The NICSD V&V team shall update the NICSD VVP so that it conforms to the updated NED VVP. The changes to be made to the NICSD VVP shall be approved by the NED V&V personnel.
- The NICSD V&V personnel shall assess the effect of the change to determine if there are any V&V activities to be iterated.
- The NICSD V&V personnel shall repeat the needed V&V activities.

If the NICSD V&V team change the NICSD VVP, the change shall be made in the same manner in which the initial NICSD VVP has been established, i.e. NICSD shall submit the updated VVP to the NED for approval. The NED V&V personnel shall review the updated NICSD VVP for its conformance to the NED VVP, and the Group Manager of the Monitoring System Engineering Group shall approve the updated NICSD VVP based on the review.

The NICSD V&V team may change the NICSD VVP of their necessity, as long as the change is submitted to and approved by the NED.

The V&V activities affected by the change shall be updated in accordance with the updated VVP.

7.4 Control Procedures

The documents that resulted from the V&V effort shall be controlled in accordance with the Project Quality Assurance Plan (Reference 2.4.14) and section 10 of the SQAP.

7.5 Standards, Practices and Conventions

For Standards, Practices, and Conventions, Refer to section 5 of SQAP.

8 V&V Documentation Requirements

This section defines the purpose, format, and content of the test documents, the Hazard Analysis Documents, and the RTMs.

8.1 Test Documents

NED shall establish the following test documents.

(1) System Validation test procedure
The System Validation test procedure shall be established so that it includes the contents of the Test Plan, the Test-Design Specification, the Test-Case Specification, and the Test-Procedure defined in IEEE Std 829-1983 (Reference 2.3.2).

The System Validation test procedure shall be accordance with AS-300A103 (Reference 2.4.12).

(2) System Validation test report
The System Validation test report shall be established so that it includes the contents of Test Log, Test Incident Report, and Test Summary Report defined in IEEE Std 829-1983.

The System Validation test report shall be prepared in accordance with AS-300A103.

Note that IEEE Std 829-1983 requires the Test-Item Transmittal Report. However, since the transmittal of the test items or the test specimen is performed in accordance with another procedure of this project, the Test-Item Transmittal Report is not included in this plan.

NICSD shall establish the following test documents in accordance with IEEE Std 829-1983:
(1) Unit/Module Validation test procedures
(2) Unit/Module Validation test reports
(3) FPGA Validation test procedures
(4) FPGA Validation test reports

The NICSD VVP shall prescribe the purpose, format, and content of the test documents.

8.2 Hazard Analysis Documents

For Hazard Analysis, the initial PHA Report shall be prepared at the Concept Phase, and be updated from the Requirements Definition Phase through System Validation Testing Phase. SQAP (Reference 2.4.15) section 4.2.4 describes the reporting in detail.

8.3 RTM

As described in Section 5 of this plan, NED will create the Concept phase RTM, and then NICSD will maintain and update the RTM for the work in NICSD's scope.

NED shall develop the Concept phase RTM in accordance with procedure AS-200A130 (Reference 2.4.7). The content of the RTM shall consist of the requirements from the ERS and other applicable documents, presented in a matrix format.

NED and NICSD shall use the same general format in Exhibit for the RTM. If the RTM becomes too large to be filled in the format, the RTM may be divided into sub matrices, as long as the traceability between two subsequent phases must be clearly shown.

Exhibit RTM format

No.	Findings and Open Items	Project Planning and Concept Definition Phase	Requirements Definition Phase	Design Phase	Implementation and Integration Phase	Unit/Module Validation Testing Phase	System Validation Testing Phase

Note: The row width and the column height, and the size of the format are not restricted.

Appendix A Compliance with IEEE Std 1012-1998

Section	IEEE Std 1012-1998	NED V&V Plan	Compliance	Comments
1	Overview	-	-	*No specific requirement*
2	Normative reference	-	-	*No specific requirement*
3	Definitions, abbreviations	-	-	*No specific requirement*
4	V&V software integrity levels	-	-	*Section title*
4.1	Software integrity levels	-	-	*Section title*
	The V&V effort shall specify a software integrity scheme.	4.3	Comply	
	The mapping of the software integrity level scheme and the associated minimum V&V tasks shall be documented in the SVVP.	4.3	Comply	
	The basis for assigning software integrity levels to software components shall be documented in a V&V Task Report and V&V Final Report.	4.3	Comply	
	The integrity level assigned to reusable software shall be in accordance with the integrity level scheme adopted for the project, and the reusable software shall be evaluated for use in the context of its application.	4.6	Comply	
5	V&V processes	-	-	*Section title*
	The V&V effort shall comply with the task descriptions, inputs, and outputs as described in Table 1.	5	Comply	Section 5 of VVP covers the requirements described in Table 1.
	The V&V effort shall perform the minimum V&V tasks as specified in Table 2 for the assigned software integrity level.	5	Comply	Section 5 of VVP covers the requirements described in Table 2
	If the user of this standard has selected a different software integrity level scheme, then the mapping of that integrity level scheme to Table 2 shall define the minimum V&V tasks for each of the user's software integrity levels.	4.3	Comply	Secion 4.3 of VVP requires all the V&V activities defined for SIL 4 software.
	Some V&V activities and tasks include analysis, evaluations, and tests that may be performed by multiple organizations (e.g., software development, project management, quality assurance, V&V). ... The degree to which these analyses efforts are coordinated with other organizations shall be documented in the organizational responsibility section of the SVVP.	-	N/A for VVP	SQAP covers the requirement by describing the Hazard Analyses that performed by the Design engineers.
	The user of this standard shall document the V&V processes in the SVVP and shall define the information and facilities necessary to manage and perform these processes, activities, and tasks, and to coordinate those V&V processes with other related aspects of the project. The results of V&V activities and tasks shall be documented in task reports, activity summary reports, anomaly reports, V&V test documents, and the V&V Final Report.	5, 6	Comply	
5.1	Process: Management	-	-	*Section title*
5.1.1	The V&V effort shall perform, as appropriate for the selected software integrity level, the minimum V&V tasks for Management of V&V from the following list:	-	-	Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.
	1) Task: Software Verification and Validation Plan (SVVP) Generation	Table 5-1	Comply	
	2) Task: Baseline Change Assessment			
	3) Task: Management Review of V&V			
	4) Task: Management and Technical Review Support			
	5) Task: Interface With Organizational and Supporting Processes			

Section	IEEE Std 1012-1998	NED V&V Plan	Compliance	Comments
5.2	Process: Acquisition	-	N/A	Out of the project scope
5.3	Process: Supply	-	N/A	Out of the project scope
5.3.1	Activity: Planning V&V	-	-	*Section title*
5.4	Process: Development	-	-	*Section title*
5.4.1	Activity: Concept V&V The V&V effort shall perform, as appropriate for the selected software integrity level, the minimum V&V tasks for Concept V&V from the following list:	-	-	Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.
	1) Task: Concept Documentation Evaluation 2) Task: Criticality Analysis 3) Task: Hardware/Software/User Requirements Allocation Analysis	5.1.2	Comply	
	4) Task: Traceability Analysis	5.1.3	Comply	
	5) Task: Hazard Analysis	5.1.2	Comply	The PHA is performed by the design engineers.
	6) Task: Risk Analysis	5.1.4	Comply	
5.4.2	Activity: Requirements V&V The V&V effort shall perform, as appropriate for the selected software integrity level, the minimum V&V tasks for Requirements V&V from the following list:	-	-	Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.
	1) Task: Traceability Analysis	5.3.2	Comply	
	2) Task: Software Requirements Evaluation 3) Task: Interface Analysis	5.3.1	Comply	
	4) Task: Criticality Analysis	5.3.2	Comply	
	5) Task: System V&V Test Plan Generation and Verification	5.6.2	Comply	Module/Unit/System validation test procedures. In addition, the ERS describes testing.
	6) Task: Acceptance V&V Test Plan Generation and Verification	-	N/A	Out of the project scope
	7) Task: Configuration Management Assessment	5.1.2 5.7.4 5.10	Comply	NED/NICSD V&V team performs V&V activities on the MCL throughout the project life cycle.
	8) Task: Hazard Analysis	5.3.1	Comply	PHA shall be performed by the design engineers, and reviewed by V&V personnel.
	9) Task: Risk Analysis	5.3.3	Comply	VVR describe the project risk.
5.4.3	Activity: Design V&V The V&V effort shall perform, as appropriate for the selected software integrity level, the minimum V&V tasks for Design V&V from the following list:	5.4	-	Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.
	1) Task: Traceability Analysis	5.4.2	Comply	
	2) Task: Software Design Evaluation 3) Task: Interface Analysis	5.4.1, 5.4.2	Comply	
	4) Task: Criticality Analysis	5.4.2	Comply	
	5) Task: Component V&V Test Plan Generation and Verification	5.5.4	Comply	
	6) Task: Integration V&V Test Plan Generation and Verification	5.6.2	Comply	
	7) Task: V&V Test Design Generation and Verification	5.5.4	Comply	
	8) Task: Hazard Analysis	5.4.1	Comply	
	9) Task: Risk Analysis	5.4.3	Comply	
5.4.4	Activity: Implementation V&V The V&V effort shall perform, as appropriate for the selected software integrity level, the minimum V&V tasks for Implementation V&V from the following list:	-	-	Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.
	1) Task: Traceability Analysis	5.5.5, 5.5.1	Comply	
	2) Task: Source Code and Source Code Documentation Evaluation	5.5.1	Comply	

Section	IEEE Std 1012-1998	NED V&V Plan	Compliance	Comments
	3) Task: Interface Analysis	5.5.4	Comply	The interface in IEEE standard is considered to correspond to internal and external wiring connections in FPGA systems.
	4) Task: Criticality Analysis	5.5.1, 5.5.4	Comply	The V&V activities of the Implementation phase are planed so that they are commensurate with SIL 4 software.
	5) Task: V&V Test Case Generation and Verification 6) Task: V&V Test Procedure Generation and Verification	5.5.4	Comply	
	7) Task: Component V&V Test Execution and Verification	5.5.3	Comply	
	8) Task: Hazard Analysis	5.5.4	Comply	
	9) Task: Risk Analysis	5.5.7	Comply	
5.4.5	Activity: Test V&V	-	-	*Section title*
	For software integrity levels 3 and 4, the V&V effort shall generate its own V&V software and system test products (e.g., plans, designs, cases, procedures), execute and record its own tests, and verify those plans, designs, cases, procedures, and test results against software requirements.	5.5.3, 5.5.4 5.6.1, 5.6.2 5.7.1, 5.7.2	Comply	
	For software integrity levels 1 and 2, the V&V effort shall verify the development process test activities and products (e.g., test plans, designs, cases, procedures, and test execution results).	-	N/A	This VVP does not target level 1 and 2 software. Although test equipment software is SIL 2 software, its V&V is not included in this VVP.
	The V&V effort shall perform, as appropriate for the selected software integrity level, the minimum V&V tasks for Test V&V from the following list:	-	-	Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.
	1) Task: Traceability Analysis	5.6.3, 5.7.3	Comply	
	2) Task: Acceptance V&V Test Procedure Generation and Verification		N/A	Out of the project scope
	3) Task: Integration V&V Test Execution and Verification	5.6.1	Comply	
	4) Task: System V&V Test Execution and Verification	5.7.1	Comply	
	5) Task: Acceptance V&V Test Execution and Verification		N/A	Out of the project scope
	6) Task: Hazard Analysis	5.6.2, 5.7.2	Comply	
	7) Task: Risk Analysis	5.6.5	Comply	
5.4.6	Activity: Installation and Checkout V&V		N/A	Out of the project scope
5.5	Process: Operation		N/A	Out of the project scope
5.6	Process: Maintenance		N/A	Out of the project scope
6.	Software V&V reporting, administrative, and documentation requirements		-	*Section title*
6.1	V&V reporting requirements V&V reporting occurs throughout the software life cycle. The SVVP shall specify the content, format, and timing of all V&V reports. The V&V reports shall constitute the Software Verification and Validation Report (SVVR). The V&V reports shall consist of required V&V reports (i.e., V&V Task Reports, V&V Activity Summary Reports, V&V Anomaly Reports, and V&V Final Report). The V&V reports may also include optional reports. Reporting requirements are described in 7.6 of this standard.	6	Comply	
6.2	V&V administrative requirements The SVVP describes the V&V administrative requirements that support the V&V effort. These V&V administrative requirements shall consist of the following:	-	-	Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.
	1) Anomaly Resolution and Reporting	7.1	Comply	

Section	IEEE Std 1012-1998	NED V&V Plan	Compliance	Comments
	2) Task Iteration Policy	7.2	Comply	
	3) Deviation Policy	7.3	Comply	
	4) Control Procedures	7.4	Comply	
	5) Standards, Practices, and Conventions	7.5	Comply	
	V&V documentation requirements	8	Comply	
7.	SVVP outline The SVVP shall contain the content as described in 7.1 through 7.8 of this standard.	VVP section 1 through 8	Comply	
7.1	(SVVP Section 1) Purpose The SVVP shall describe the purpose, goals, and scope of the software V&V effort, including waivers from this standard. The software project for which the Plan is being written and the specific software processes and products covered by the software V&V effort shall be identified.	1	Comply	
7.2	(SVVP Section 2) Referenced documents The SVVP shall identify the compliance documents, documents referenced by the SVVP, and any supporting documents supplementing or implementing the SVVP.	2	Comply	
7.3	(SVVP Section 3) Definitions The SVVP shall define or reference all terms used in the SVVP, including the criteria for classifying an anomaly as a critical anomaly. All abbreviations and notations used in the SVVP shall be described.	3	Comply	
7.4	(SVVP Section 4) V&V overview The SVVP shall describe the organization, schedule, software integrity level scheme, resources, responsibilities, tools, techniques, and methods necessary to perform the software V&V.	4	Comply	
7.4.1	(SVVP Section 4.1) Organization The SVVP shall describe the organization of the V&V effort, including the degree of independence required. The SVVP shall describe the relationship of the V&V processes to other processes such as development, project management, quality assurance, and configuration management.	4.1	Comply	
	The SVVP shall describe the lines of communication within the V&V effort, the authority for resolving issues raised by V&V tasks, and the authority for approving V&V products.	4.1	Comply	
7.4.2	(SVVP Section 4.2) Master Schedule The SVVP shall describe the project life cycle and milestones. It shall summarize the schedule of V&V tasks and task results as feedback to the development, organizational, and supporting processes. V&V tasks shall be scheduled to be re-performed according to the task iteration policy.	4.2	Comply	

Section	IEEE Std 1012-1998	NED V&V Plan	Compliance	Comments
7.4.3	(SVVP Section 4.3) Software integrity level scheme The SVVP shall describe the agreed upon software integrity level scheme established for the system and the mapping of the selected scheme to the model used in this standard. The SVVP shall document the assignment of software integrity levels to individual components (e.g., requirements, detailed functions, software modules, subsystems, or other software partitions), where there are differing software integrity levels assigned within the program. For each SVVP update, the assignment of software integrity levels shall be reassessed to reflect changes that may occur in the integrity levels as a result of architecture selection, detailed design choices, code construction usage, or other development activities.	4.3	Comply	
7.4.4	(SVVP Section 4.4) Resources summary The SVVP shall summarize the V&V resources, including staffing, facilities, tools, finances, and special procedural requirements (e.g., security, access rights, and documentation control).	4.4.	Comply	
7.4.5	(SVVP Section 4.5) Responsibilities The SVVP shall identify an overview of the organizational element(s) and responsibilities for V&V tasks.	4.5	Comply	
7.4.6	(SVVP Section 4.6) Tools, techniques, and methods The SVVP shall describe documents, hardware and software V&V tools, techniques, methods, and operating and test environment to be used in the V&V process. Acquisition, training, support, and qualification information for each tool, technology, and method shall be included.	4.6	Comply	
	Tools that insert code into the software shall be verified and validated to the same rigor as the highest software integrity level of the software. Tools that do not insert code shall be verified and validated to assure that they meet their operational requirements. If partitioning of tool functions can be demonstrated, only those functions that are used in the V&V processes shall be verified to demonstrate that they perform correctly for their intended use.	-	Not Comply	In Regulatory Guide 1.168, the NRC staff states that this requirement is one of the exceptions in endorsing IEEE std 1012-1998. See Appendix B.
	The SVVP shall document the metrics to be used by V&V (see Annex E), and shall describe how these metrics support the V&V objectives.	4.6	Comply	
7.5	(SVVP Section 5) V&V processes The SVVP shall identify V&V activities and tasks to be performed for each of the V&V processes described in Clause 5 of this standard, and shall document those V&V activities and tasks. The SVVP shall contain an overview of the V&V activities and tasks for all software life cycle processes.	5	Comply	
7.5.1	(SVVP Sections 5.1 through 5.6) "Software life cycle" The SVVP shall include sections 5.1 through 5.6 for V&V activities and tasks as shown in SVVP Outline (boxed text). The SVVP shall address the following eight topics for each V&V activity:	-	-	Because this statement constitutes specific requirements with the list below, the compliance is determined for each item in the list.

Section	IEEE Std 1012-1998	NED V&V Plan	Compliance	Comments
	1) V&V Tasks. The SVVP shall identify the V&V tasks to be performed.	5	Comply	
	2) *Methods and Procedures.* The SVVP shall describe the methods and procedures for each task, including on-line access, and conditions for observation/evaluation of development processes. The SVVP shall define the criteria for evaluating the task results.	5.1 – 5.10	Comply	
	3) *Inputs.* The SVVP shall identify the required inputs for each V&V task. The SVVP shall specify the source and format of each input.	5, 5.1, 5.3 – 5.8	Comply	
	4) *Outputs.* The SVVP shall identify the required outputs from each V&V task. The SVVP shall specify the purpose, format, and recipients of each output.	5, 5.1, 5.3 - 5.8	Comply	
	The outputs of the Management of V&V and of the V&V tasks shall become inputs to subsequent processes and activities, as appropriate.	5, 5.1, 5.3 - 5.8	Comply	
	5) *Schedule.* The SVVP shall describe the schedule for the V&V tasks. The SVVP shall establish specific milestones for initiating and completing each task, for the receipt and criteria of each input, and for the delivery of each output.	4.2	Comply	
	6) *Resources.* The SVVP shall identify the resources for the performance of the V&V tasks. The SVVP shall specify resources by category (e.g., staffing, equipment, facilities, travel, and training.)	4.4	Comply	
	7) *Risks and Assumptions.* The SVVP shall identify the risks (e.g., schedule, resources, or technical approach) and assumptions associated with the V&V tasks. The SVVP shall provide recommendations to eliminate, reduce, or mitigate risks.	5.1, 5.3 - 5.8	Comply	The risks and assumptions will be included in the VVR, and reported to the project management.
	8) *Roles and Responsibilities.* The SVVP shall identify the organizational elements or individuals responsible for performing the V&V tasks.	5.1, 5.3 - 5.8	Comply	
7.6	(SVVP Section 6) V&V reporting requirements V&V reporting shall consist of Task Reports, V&V Activity Summary Reports, Anomaly Reports, and the V&V Final Report.	6	Comply	
7.7	(SVVP Section 7) V&V administrative requirements	7	-	*Section title*
7.7.1	(SVVP Section 7.1) Anomaly resolution and reporting The SVVP shall describe the method of reporting and resolving anomalies, including the criteria for reporting an anomaly, the anomaly report distribution list, and the authority and time lines for resolving anomalies. The section shall define the anomaly criticality levels.	7.1	Comply	
7.7.2	(SVVP Section 7.2) Task iteration policy The SVVP shall describe the criteria used to determine the extent to which a V&V task shall be repeated when its input is changed or task procedure is changed.	7.2	Comply	

Section	IEEE Std 1012-1998	NED V&V Plan	Compliance	Comments
7.7.3	(SVVP Section 7.3) Deviation policy The SVVP shall describe the procedures and criteria used to deviate from the Plan. The information required for deviations shall include task identification, rationale, and effect on software quality. The SVVP shall identify the authorities responsible for approving deviations.	7.3	Comply	
7.7.4	(SVVP Section 7.4) Control procedures The SVVP shall identify control procedures applied to the V&V effort. These procedures shall describe how software products and V&V results shall be configured, protected, and stored.	7.4	Comply	
	The SVVP shall describe how the V&V effort shall comply with existing security provisions and how the validity of V&V results shall be protected from unauthorized alterations.	4.5	Comply	
7.7.5	(SVVP Section 7.5) Standards, practices, and conventions The SVVP shall identify the standards, practices, and conventions that govern the performance of V&V tasks including internal organizational standards, practices, and policies.	7.5	Comply	
7.8	(SVVP Section 8) V&V documentation requirements The SVVP shall define the purpose, format, and content of the test documents.	8	Comply	

Appendix B Compliance with Regulatory Guide 1.168

Regulatory Guide 1.168 Rev.1 (Reference 2.2.1) endorses IEEE Std 1012-1998 with some exceptions. The following table describes the compliance of the VVP with the exceptions.

Reg. Guide 1.168 Regulatory Position	NED V&V Plan	Compliance	Comments
1. CRITICAL SOFTWARE Software used in nuclear power plant safety systems should be assigned integrity level 4 or equivalent, as demonstrated by a mapping between the applicant or licensee approach and integrity level 4 as defined in IEEE Std 1012-1998.	4.3	Comply	
2. SOFTWARE RELIABILITY Consistent with the staff's position on reliability measures for digital safety systems contained in other regulatory guides, the NRC staff's acceptance of quantitative reliability goals for computer-based safety systems is predicated on deterministic criteria for the computer system in its entirety (i.e., hardware, system software, firmware, application, and interconnections). 1.168-6	5	Comply	The NED VVP describes the V&V activities that shall be performed. The criterion for the reliability goal is whether the activities are appropriately accomplished or not.
3. INDEPENDENCE OF SOFTWARE VERIFICATION AND VALIDATION A method of performing independent software V&V is described in Revision 1 of Regulatory Guide 1.152.	4.1	Comply	
4. CONFORMANCE OF MATERIALS IEEE Std 1012-1998 provides guidance for retrospective V&V of software that was not verified under the standard. The use of this guidance for the acceptance of pre-existing safety system software not verified during development to the provisions of this regulatory guide or its equivalent is not endorsed. Revision 1 of Regulatory Guide 1.152 provides information on the acceptance of pre-existing software. Additional detailed information on acceptance processes is available in EPRI TR-106439, "Guideline on Evaluation and Acceptance of Commercial Grade Digital Equipment for Nuclear Safety Applications" (October 1996).4	-	N/A	No legacy software shall be used in the PRM system.
5. QUALITY ASSURANCE In addition to the provisions of IEEE Std 1012-1998 (in Clause 7.7.4) regarding control procedures, any V&V materials necessary for the verification of the effectiveness of the V&V programs or necessary to furnish evidence of activities affecting quality should be maintained as quality assurance records. The records necessary for the verification of changes must be maintained in accordance with Criterion XVII.	-	N/A for VVP	TOSHIBA NED QA program based on Appendix B shall be applied.
6. TOOLS FOR SOFTWARE DEVELOPMENT Tools used in the development of safety system software should be handled according to IEEE Std 7-4.3.2-1993,1 as endorsed by Revision 1 of Regulatory Guide 1.152. IEEE Std 7-4.3.2-1993 states that "V&V tasks of witnessing, reviewing, and testing are not required for software tools, provided the software that is produced using the tools is subject to V&V activities that will detect flaws introduced by the tools." If this cannot be demonstrated, the provisions of this regulatory guide are applicable.	5.5.2, 5.5.4, 5.8	Comply	Section 5.5.2, 5.5.4, and 5.8 of VVP address how to possible tool errors.
7. VERIFICATION AND VALIDATION TASKS Exception is taken to the "optional" status of some tasks on this list; they are considered by the NRC staff to be necessary components of acceptable methods for meeting the requirements of Appendices A and B to 10 CFR Part 50 as applied to software, regardless of whether they are performed by the V&V organization.	-	-	*Section title*

7.1 Audits Safety system software V&V organizations may employ audits, including functional audits, in-process audits, and physical audits of software. Although these audits are commonly considered to be the responsibility of the software quality assurance organization and the configuration management organization, they may be performed and relied upon by the V&V organization.	-	N/A for VVP	Because Audit shall be performed by PJ QA, this VVP does not refer to audit.
7.2 Regression Analysis and Testing Criterion III, "Design Control," requires that design changes be subject to design control measures commensurate with those applied to the original design. Regression analysis and testing following the implementation of software modifications is an element of the V&V of software changes. It is considered by the NRC staff to be part of the minimum set of software V&V activities for safety system software.	7.2	Comply	
7.3 Security Assessment A security breach of a digital system containing safety system software has the potential to prevent that software from fulfilling its safety function. Appendix A imposes functional and reliability requirements with respect to safety systems. According to 10 CFR 73.46, vital equipment (which includes safety system software) must be protected by physical barriers and access control. The NRC staff considers security assessment of safety system software to be part of the minimum set of software V&V activities for such software. 1.168-9	4.5	Comply	
7.4 Test Evaluation Test evaluation includes confirming the technical adequacy of test materials such as plans, designs, and results. These materials are evaluated for consistency with Criterion II, "Quality Assurance Program," in its requirement for controlled conditions, and with Criterion XI, "Test Control," in its requirement for the evaluation of test results.	5.5.4, 5.6.2, 5.7.2, 5.7.4	Comply	
7.5 Evaluation of User Documentation User documentation is important to the safe operation and proper maintenance of safety system software. The requirements of Criterion III, "Design Control," for correctly translating the design basis of safety system software into specifications, procedures, drawings, and instructions, apply to software documentation, including user documentation.	5.6.2	Comply	
8. OTHER CODES AND STANDARDS Various sections of IEEE Std 1012-1998 and IEEE Std 1028-1997 reference other industry codes and standards. These references to other standards should be treated individually. If a referenced standard has been incorporated separately into the NRC's regulations, licensees and applicants must comply with that standard as set forth in the regulation. If the referenced standard has been endorsed in a regulatory guide, the standard constitutes a method acceptable to the NRC staff for meeting a regulatory requirement as described in the regulatory guide. If a referenced standard has been neither incorporated into the NRC's regulations nor endorsed in a regulatory guide, licensees and applicants may consider and use the information in the referenced standard, if appropriately justified, consistent with current regulatory practice.	-	N/A	

Toshiba Project Document No.	Rev. No.
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Project	NRW-FPGA-Based I&C System Qualification Project
Contract No.	: ——

X	For Approval		For Information

Action		
A	X	Approved No Further Action
C		Approved with Comment Revised and Resubmit
D		Disapproved Revised and Resubmit
I		Accepted for Information Only ☐ Recommendation Included

Group	Electrical System Design & Engineering Dept.
Approved by	Reviewed by
M. Hamada 07-Jul-2016	T. Hayashi Jul. 6, 2016

Approval by buyer does not release seller of his obligation to furnish all goods and services in strict conformance with all of the terms of the Purchase Order.

TOSHIBA CORPORATION
NED

■Safety-Related
☐Non-Safety-Related
☐ASME CODE
☐Others ( )

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NRW-FPGA-Based I&C System Qualification Project

Software Verification &Validation Plan

Title: Nuclear Instrumentation & Control Systems Department Verification and Validation Plan for FPGA-based Safety-Related Systems

Customer Name	None
Project Name	NRW-FPGA-Based I&C System Qualification Project
Item Name	None
Item Number	A32
Job Number	9P04482
Applicable Plant	None

TOSHIBA NICSD verified this Document;
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8	See Cover Page	See Cover Page	See Cover Page	See Cover Page	See Cover Page

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1 Introduction

1.1 Purpose

The Nuclear Instrumentation & Control Systems Department (NICSD) Verification and Validation (V&V) plan (NICSD VVP) is prepared for Non-Rewritable (NRW) Field Programmable Gate Array (FPGA)-based safety-related Instrumentation and Control (I&C) systems based on the Nuclear Energy Systems and Services Division (NED) V&V plan (NED VVP) (Reference (47)) to define the NICSD V&V activities.

The system design is determined by the Instrumentation & Control Systems Design and Engineering Department (ICDD) of Nuclear Energy Systems and Services Division (NED), and ICDD procures the FPGA-based equipment from Toshiba Fuchu Complex Power Systems Segment (Fuchu-PS) NICSD. NICSD procures major FPGA-based components, including modules with FPGA logic from the Toshiba Fuchu-PS Power Platform Development Department (PPDD) using a commercial grade dedication process.

For V&V of the FPGA-based safety-related I&C systems, ICDD and NICSD organize independent V&V (IV&V) Teams. The ICDD and NICSD IV&V Teams work together.

The software lifecycle process, including V&V, is defined in the project document "NICSD Software Management Plan for FPGA-based Safety-Related Systems" (NICSD SMP) (Reference (48)). This NICSD VVP covers the Section 4 "Software Verification and Validation Program Plan" of the project document "Software Program Plan" (SPP) (Reference (45)). This NICSD VVP is prepared by the NICSD IV&V Team in accordance with the following reference documents:

- NED, FA10-3709-0001 "Nuclear Energy Systems and Services Division FPGA-based Safety-Related Systems Verification and Validation Plan " (Reference (47))
- NED AS-200A130 "Digital System Verification & Validation Procedure" (Reference (12)), and
- NICSD NQ-2013 "Preparation Guide for V&V Plan" (Reference (17))

1.2 Scope

This NICSD VVP applies to the V&V activities for the FPGA-based safety-related I&C systems, which Toshiba will supply to US Nuclear Power Plants.

Section 4 of the project document "Software Program Plan," (SPP) (Reference (45)) establishes requirements and provides guidance and expectations for the V&V activities. This NICSD VVP complies with Section 4 of the SPP for the NICSD portions of the V&V activities. Table A shows compliance to Section 4 of the SPP.

2 Definitions and Abbreviations

2.1 Definitions

Functional Element (FE): A Functional Element is a component of digital logic that is completely verified and validated through full pattern testing, i.e. tests that are performed for all possible input combinations. An FE is written in Very High Speed Integrated Circuit Hardware Description Language (VHDL). All VHDL source codes for the NRW-FPGA-based System solely consist of FEs and interconnect between FEs.

Module: A part of a unit. Each module consists of one or more printed circuit boards, on which the FPGAs and other circuitry are mounted, and a front panel.

Netlist: Description of logics created by the logic synthesis tool. A design engineer describes FPGA logic in the form of VHDL source codes and FEs. The logic synthesis tool converts the VHDL source code into forms of digital circuits and outputs the resulting circuit in the form of a netlist. The layout tool transforms the netlist into physical placement of interconnects on the FPGA, which are represented as an FPGA fuse-map.

Unit: A major component of FPGA-based equipment. A unit is a chassis that has front slots and back slots to mount modules. Each unit consists of several modules. There is a vertical middle plane between the front and back slots in each unit. This plane consists of two circuit boards. These circuit boards provide backplanes for the front and rear modules. Modules plug into the backplanes using connectors. Once a module is plugged into the appropriate connector, it exchanges data with other modules in the unit, connects to other units and any external field equipment, and is powered.

Validation: Validation is used to ensure that the final product satisfies the user requirements. Validation shall be performed on the final product, although validation may be necessary or performed prior to the final code being produced. See Section 4.2 of the SPP (Reference (45)).

Verification: Verification consists of reviews performed on the results of each development phase to ensure the phase was completed appropriately and correctly. See Section 4.2 of the SPP (Reference (45)).

2.2 Abbreviations

BRR	Baseline Review Report
CAR	Corrective Action Request
CDR	Critical Digital Review
CFR	Code of Federal Regulation
CM	Configuration Management
CG	Commercial Grade
COTS	Commercial-Off-The-Shelf
DCN	Design Change Notice
DVR	Design Verification Report
ECWD	Elementary Control Wiring Diagram
EDIF	Electronic Design Interchange Format

EDS	Equipment Design Specification
ES	Engineering Schedule
FE	Functional Element
FPGA	Field Programmable Gate Array (a programmable logic device)
Fuchu-PS	Toshiba Fuchu Complex Power Systems Segment
I&C	Instrumentation and Control
IBD	Interlock Block Diagram
ICDD	Instrumentation & Control Systems Design and Engineering Department
IDE	Integrated Development Environment
IED	Instrumentation Electrical Diagram
IEEE	Institute of Electrical and Electronics Engineers
IR	Independent Reviewer
IV&V	Independent Verification and Validation
MCL	Master Configuration List
NED	Nuclear Energy Systems and Services Division
NICSD	Nuclear Instrumentation & Control Systems Department
NISD	Nuclear Instrumentation Systems Development & Designing Group
NICS-QA	Quality Assurance Group for Nuclear Instrumentation & Control Systems
NNR	Nonconformance Notice Report
NQ	Nuclear Quality (standards for NICSD)
PC	Personal Computer
PCD	Project Control Document
PCDL	Project Control Document List
PDS	Previously Developed Software
PM	Project Manager
PPDD	Power Platform Development Department
PRM	Process Review Meeting
PRS	Problem Reporting Sheet
PSNE	Toshiba Corporation, Power Systems & Services Company, Nuclear Energy
QA	Quality Assurance
QAD	Quality Assurance Department
QC	Quality Control
RG	Regulatory Guide
RTIS	Reactor Trip and Isolation System
RTM	Requirements Traceability Matrix

SBPR	Software Build Procedure and Report
SSAR	Software Safety Analysis Report
SCAR	Fuchu Site Corrective Action Request
SCMP	Software Quality Configuration Management Plan
SCSI	Small Computer System Interface
SD	Software Development
SDD	Software Design Description
SDL	Software Development Lead
SDOE	Secure Development and Operational Environment
SIL	Software Integrity Level
SM	Senior Manager
SMP	Software Management Plan
SQA	Software Quality Assurance
SQAP	Software Quality Assurance Management Plan
SRS	Software Requirements Specification
SPP	Software Program Plan
SVTP	Software Validation Test Plan
SVTR	Software Validation Test Report
V&V	Verification and Validation
VDCL	Vendor generated Document Check List
VFS	Verification Follow Sheet
VHDL	Very High Speed Integrated Circuit Hardware Definition Language (A hardware description language that defines the FPGA circuit)
VNNR	Vendor Nonconformance Notice Report
VVP	Verification and Validation Plan
VVR	Verification and Validation Report

Table 3-1 of the NICSD SMP is provided for a better understanding of terminological difference between the SPP and NICSD SMP. This NICSD VVP also uses Table 3-1 of the NICSD SMP.

3 Reference Documents

3.1 Code of Federal Regulations

This NICSD VVP does not refer to the Code of Federal Regulations (CFR) directly. The Toshiba internal standards in Section 3.4 are based on the CFR.

3.2 Regulatory Guides and NRC Documents

(1) Regulatory Guide 1.168
"Verification, Validation, Reviews, and Audits for Digital Computer Software Used in Safety Systems of Nuclear Power Plants." Rev.1, 2004

(2) Regulatory Guide 1.152
"Criteria for Use of Computers in Safety Systems of Nuclear Power Plants," Rev.3, July 2011

Other regulatory guides may be referred to indirectly through the Toshiba internal standards in Section 3.4.

3.3 Industry Standards

(3) IEEE Std. 1012-1998
"IEEE Standard for Software Verification and Validation"

(4) IEEE Std. 1028-1997
"IEEE Standard for Software Reviews"

3.4 Toshiba Internal Standards (NED, NICSD)

(5) Toshiba Nuclear Energy Systems and Services Division AS-100A004
"Document Control Procedure"

(6) Toshiba Nuclear Energy Systems and Service Division AS-100A012
"Preparation Procedure for Engineering Communication Sheet"

(7) Toshiba Nuclear Energy Systems and Service Division AS-200A002
"Design Verification Procedure"

(8) Toshiba Nuclear Energy Systems and Services Division AS-200A010
"Control Procedure of vendor generated documents"

(9) Toshiba Nuclear Energy Systems and Service Division AS-200A017
"Design Planning Procedure"

(10) Toshiba Nuclear Energy Systems and Service Division AS-200A128
"Digital System Life Cycle Procedure"

(11) Toshiba Nuclear Energy Systems and Service Division AS-200A129
"Digital System Development Procedure"

(12) Toshiba Nuclear Energy Systems and Service Division AS-200A130
"Digital System Verification & Validation Procedure"

(13) Toshiba Nuclear Energy Systems and Service Division AS-200A131
"Digital System Configuration Management Procedure"

(14) Toshiba Nuclear Energy Systems and Service Division AS-300A008
"Nonconformance Control and Corrective Action Procedure"

(15) Toshiba Nuclear Energy Systems and Services Division AS-300A009
"Corrective Action Request Application Procedure"

(16) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2011
"Procedure for FPGA Test"

(17) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2013
"Preparation Guide for V&V Plan"

(18) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2014
"Preparation Guide for V&V Report"

(19) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2015
"Preparation Procedure for RTM & RTM Report"

(20) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2019
"Preparation Procedure for Test Specification"

(21) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2024
"Procedure for Document Control"

(22) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2030
"Procedural Standard for FPGA Products Development"

(23) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2031
"Procedural Standard for FPGA Device Development"

(24) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2032
"Procedural Standard for Functional Element Development"

(25) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2033
"Procedural Standard for FPGA Configuration Management"

(26) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2003
"Procedure for Control of Software Tools"

(27) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2036
"Procedure for Design Control"

(28) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2037
"Cyber Security Procedures of Safety Related Digital System"

(29) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3005
"Procedure for Evaluation of Suppliers"

(30) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3006
"Procedure for Control of Nonconforming Procurement Items and Services"

(31) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3009
"Corrective Action Request Application Procedure"

(32) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3015
"Test Control Procedure"

(33) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3016
"Software Test"

(34) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3019
"Procedure for Control of Nonconformance and Corrective Action"

(35) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3020 "Control Procedure of QA Records"

(36) Toshiba Nuclear Instrumentation & Control Systems Department NQ-4001 "Commercial Grade Dedication"

3.5 Toshiba Internal Standards (PPDD)

(37) Toshiba Power Platform Development Department E-67019 "PPDD Procedure for Operation for Problem Reporting Sheet"

(38) Toshiba Power Platform Development Department E-68016 "PPDD Procedural Standard for FPGA Products Development"

(39) Toshiba Power Platform Development Department E-68017 "PPDD Procedural Standard for FPGA Device Development"

(40) Toshiba Power Platform Development Department E-68018 "PPDD Procedural Standard for Functional Element Development"

(41) Toshiba Power Platform Development Department E-68019 "PPDD Procedural Standard for FPGA Configuration Management"

(42) Toshiba Power Platform Development Department E-68020 "PPDD Procedural Standard for Control of Software Tools for FPGA-based Systems"

(43) Toshiba Power Platform Development Department E-68027 "Standard for Preparation of the Test Specification"

Notice: Upon application of above NED, NICSD and other Toshiba internal standards, the latest version shall be used.

3.6 Project Documents

(44) NRW-FPGA-Based I&C System Qualification Project, FA10-0301-0001 "Project Specific Document Control Procedure," Rev. 0

(45) NRW-FPGA-Based I&C System Qualification Project, FA10-0501-0024 "Software Program Plan," Rev. 1

(46) NRW-FPGA-Based I&C System Qualification Project, FA32-3702-0005 "Nuclear Energy Systems and Services Division FPGA-based Safety-Related Systems Software Management Plan," Rev. 2

(47) NRW-FPGA-Based I&C System Qualification Project, FA32-3709-0001 "Nuclear Energy Systems and Services Division FPGA-based Safety-Related Systems Verification and Validation Plan," Rev. 3

(48) NRW-FPGA-Based I&C System Qualification Project, FA32-3702-1000 "Nuclear Instrument & Control Systems Department Software Management Plan for FPGA-based Safety-Related Systems," Rev. 2

(49) NRW-FPGA-Based I&C System Qualification Project, FA32-3701-1001
"Nuclear Instrument & Control Systems Department Software Quality Assurance Plan for FPGA-Based Safety-Related Systems," Rev. 1

(50) NRW-FPGA-Based I&C System Qualification Project, FA32-3708-1000
"Nuclear Instrument & Control Systems Department Software Configuration Management Plan for FPGA-Based Safety-Related Systems," Rev. 1

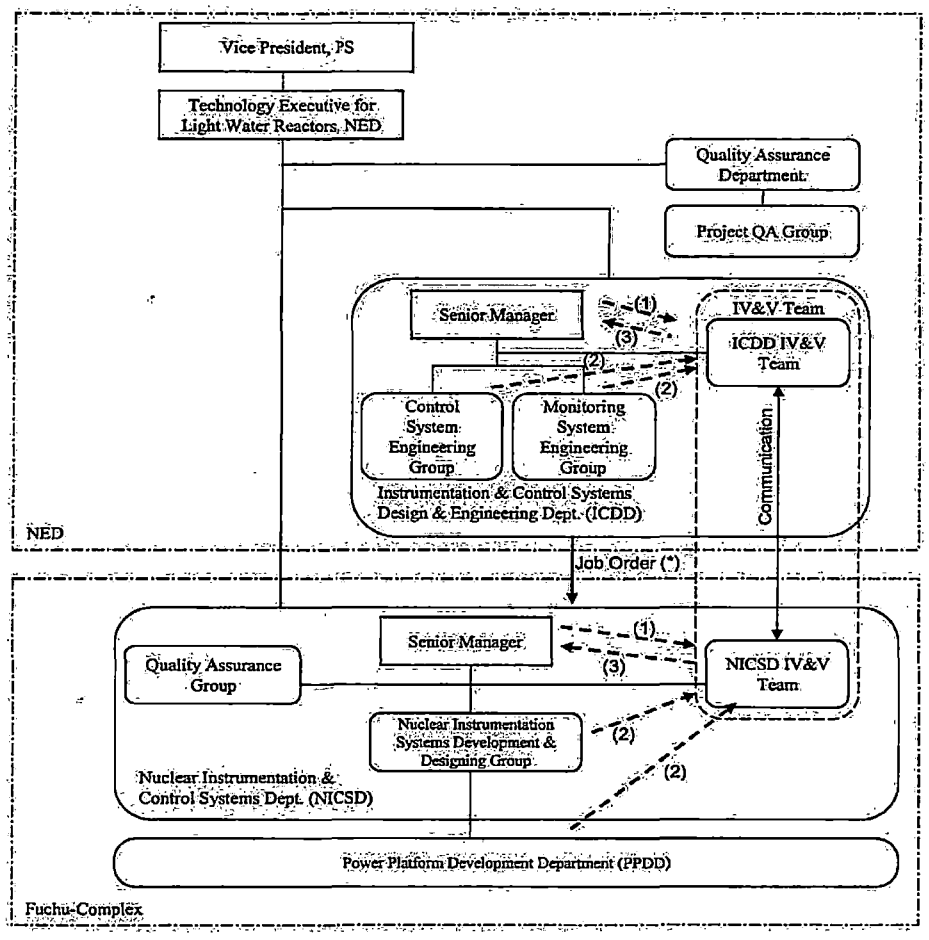
3.7 Toshiba Internal Guide (NICSD)

(51) Nuclear Instrument & Control Systems Department 8M8K0000
"Code Review Guide," Rev.0

4 Verification and Validation Overview

4.1 Organization

Figure 4-1 shows the Toshiba organizations for FPGA-based safety-related I&C systems design and development. Engineers from ICDD and NICSD organize Independent Verification and Validation (IV&V) Teams for the V&V of the FPGA logic. The engineers from ICDD and the engineers from NICSD in the IV&V Teams communicate with each other, and work together as one IV&V Team as needed for the quality of the products. In this plan, the word "ICDD IV&V Team" or "NICSD IV&V Team" is used when two IV&V Teams needs to be distinguished. Otherwise, the remark applies to the both IV&V Teams. The NICSD IV&V Team performs the NICSD V&V activities defined in this NICSD VVP. This structure provides the required independence between development activities and V&V activities.



*) A Job Order is issued from each group in ICDD to the Nuclear Instrumentation Systems Development & Designing Group.

(1) Oversight of IV&V team
(2) Submittal of Design Documents
(3) Report of V&V Results

Figure 4-1 Toshiba Organizations for FPGA-based FPGA Systems Design and Development

For the FPGA-based safety-related I&C systems, the Nuclear Instrumentation Systems Development & Designing Group (NISD) in NICSD is responsible for the design and development. The NICSD Software Development Team (NICSD SD Team) comprised of NICSD Software Development Lead (NICSD SDL) and NISD design engineers are responsible for software development (i.e. FPGA logic development).

4.2 Master Schedule

The NICSD IV&V activities and milestones are developed and controlled as described in the NICSD SMP (Reference (48))

4.3 Software Integrity Level Scheme

The software integrity level (SIL) scheme shall be determined based on Table A-1 of NED AS-200A129 (Reference (11)), which is substantially equivalent to Appendix B of IEEE Std. 1012 (Reference (3)).

For safety-related FPGA logic, the SIL shall be 4 in accordance with RG 1.168 (Reference (1)). All documents pertaining to safety-related FPGA design are labeled as "US Safety-Related" on the cover sheet, and are considered SIL 4 software documents. All software embedded in the FPGA-based Safety-Related I&C systems shall be developed, verified, and validated as SIL 4, safety-related software.

4.4 Resource Summary

The Senior Manager (SM) of NICSD as the NICSD Project Manager (NICSD PM) shall provide appropriate resources for the V&V activities defined in this NICSD VVP. For human resources, the following conditions shall be met.

All NICSD IV&V Team members shall:

- Be independent of the design activities in management, budget, and resource.
- Be technically qualified for the work performed.

The NICSD IV&V Team members shall be qualified as described in the Section 15.4 of the NICSD SMP (Reference (48)). The Section 15.4 of the NICSD SMP requires that the NICSD IV&V Lead shall determine necessary training related to the following skills, as applicable to the job functions being performed, and require the responsible manager to schedule project specific training as "Project Specific Indoctrination/Training Course."

- Code inspection
- Software tool to be used for V&V

The NICSD IV&V Team members shall be aware of and comply with the requirement for independence from the development organization.

This NICSD VVP includes some special procedural requirements to PPDD. NICSD shall put these requirements in the procurement specification to the PPDD.

4.5 Responsibilities

The SM of NICSD as the NICSD PM shall assign the NICSD IV&V Lead, who leads the V&V activities encompassing the NICSD engineering/design work in accordance with the NICSD SMP (Reference (48)). The NICSD IV&V Lead assigns the other IV&V Team

members of NICSD who were trained as described in Section 4.4 of this VVP.

The NICSD IV&V Lead is equivalent to the Software V&V Lead described in the SPP (Reference (45)). In addition to the responsibilities defined in the NICSD SMP, the NICSD IV&V Lead has responsibilities listed in Section 4.2.4 of the SPP, including review of Secure Development and Operational Environment (SDOE) implementation. SDOE is defined in the SPP and in Regulatory Guide 1.152 (Reference (2)).

The following positions, created as necessary during the project, are administratively assigned to the Software V&V Lead, as necessary. If these positions are not assigned, the Software V&V Lead shall be responsible for the activities listed below:

Software Test Lead –The Software Test Lead shall be responsible for defining the software and systems test plans, procedures, and cases. Each Software Test Lead shall be responsible for the overseeing the performance of testing and test engineers, working with the NICSD Software Development Lead (SDL) to resolve test anomalies, and setting boundaries and requirements for retest activities.

Baseline Review – The NICSD IV&V Team ensures that activities are properly performed and documented at each phase in the software life cycle. The NICSD IV&V Team is responsible for verifying all work products are completed, placed under configuration control, and records updated to reflect completion of a life cycle phase, reporting to the NICSD Quality Assurance Group. Work products to be subject to baseline review shall be defined in the Software Configuration Management Plan. The NICSD IV&V Team shall prepare a Baseline Review report at the result of baseline review. Section 4.6.3 explains Baseline Review.

NED AS-200A130 (Reference (12)) defines the responsibilities in the V&V activities of both ICDD and NICSD. NQ-2030 (Reference (22)) defines the responsibilities in the NICSD V&V activities of the NICSD engineering and design work.

The Preparer(s) of the NICSD VVP and V&V reports (VVR) shall:

- Be part of the NICSD IV&V Team.
- Not have contributed to the design.
- Be technically qualified for the work performed, and knowledgeable in the technologies and methods used in the design.

The NICSD IV&V Team performs independent reviews of the NICSD and PPDD design documents.

The NICSD IV&V Team may also oversee the work of NICSD and PPDD, to verify that they are working in compliance with applicable internal standards, and to evaluate that their work is technically acceptable for safety-related use.

The NICSD Software Quality Assurance (SQA) Team (NICSD SQA Team) will conduct oversight of the NICSD IV&V Team activities.

4.6 Tools, Techniques, and Methodologies

The NICSD IV&V Team will use several commercial software tools for the V&V activities of the FPGA-based safety-related I&C systems. The NICSD SMP (Reference (48)) describes software tools used for engineering.

4.6.1 Verification and Validation

The NICSD IV&V Team shall review the Requirements Traceability Matrix (RTM) and the Software Safety Analysis Reports (SSAR), Equipment Design Specification (EDS), System Test Procedures, System User's Manuals, Elementary Control Wiring Diagrams (ECWD), Unit Detail Design Specifications, Unit User's Manuals, Module Design Specifications, Module Test Procedures, FPGA Design Specifications, and FPGA Test Procedures. This review may be performed on either the printed or the electronic documents. Toshiba NUPDM will be used for distribution and archives of the documents. And a set of standard business software tool will be used for the review.

Document review is a method of verification to assure that the design output is correct and satisfactory by addressing that, the design inputs were correctly incorporated into the design, and the design output is reasonable compared to the design input. The review shall be performed in accordance with NED AS-200A002 (Reference (7)), AS-200A130 (Reference (12)), and NQ-2036 (Reference (27)). IEEE Std. 1012 (Reference (3)), and IEEE Std. 1028 (Reference (4)) provide guidance for the reviews.

Document review performed as technical review confirms whether:

a) The document conforms to its upstream requirements

b) The document adheres to regulations, standards, guidelines, plans, and procedures applicable to the project

c) Changes to the document are properly implemented and affect only those system areas identified by the change specification

For planning documents, implementation process documents, and design outputs including SSAR and VVR, document review shall be performed for completeness, consistency, correctness, and verifiability as applicable. Appendix A of the SPP "Terms and Definition" provides definitions for these words.

The review result shall be documented on the Design Verification Report (DVR), and when applicable the Verification Follow Sheet (VFS) shall be used for identification of comments and following up the comments to close.

4.6.2 Requirements Traceability Activities

Requirements Traceability Matrices (RTMs) shall be generated by the NICSD SD Team and PPDD design engineers and reviewed by the IV&V Team to ensure the software has completely, accurately, correctly, and consistently addressed the requirements. The RTM shall provide traceability, verification, and validation of requirements.

4.6.3 Baseline Reviews

The NICSD IV&V Team shall perform Baseline Reviews at the conclusion of each phase in the software life cycle to ensure that the required activities during that phase were completed. The Baseline Review shall confirm that planned products including design documents, test documents, VHDL source codes, netlists, fusemaps, test reports, RTMs, SSARs, and V&V Reports were prepared, that appropriate reviews were performed for these products, and that these products were documented and maintained under configuration management (CM).

The NICSD IV&V Team shall confirm the following:

- The NICSD design activities are performed, and the design outputs are prepared as

planned in the NICSD SMP.

- NICSD V&V activities are performed as planned in this NICSD VVP.
- The NICSD design output documents are controlled and listed on a Project Control Document List (PCDL) in accordance with NQ-2036 (Reference (27)).

  Documents which are issued or used for a specific plant (project) and specify technical and quality requirements or prescribe activities affecting quality, such as specification, instructions, procedures and drawings are categorized as Project Control Documents (PCDs). PCDL is the list of PCDs, including:

  (1) Contract name (or Project name)

  (2) Job Number

  (3) Project Document Number

  (4) Document Filing Number

  (5) Revision Number

  (6) Document Title.

All software life cycle activities for a given phase shall be completed prior to initiating a baseline review. Each anomaly or nonconformance found in baseline reviews shall be resolved through the software life cycle processes. Each of the baseline reviews shall confirm disposition of design, documentation, review, and any other nonconformance identified during the phase, or shall track any unresolved nonconformance through to resolution if the nonconformance cannot be resolved in that phase.

The NICSD IV&V Team shall document the result of a baseline review in a Baseline Review Report (BRR), and report it to the NICSD SQA Team for review and approve it as QA record. In accordance with Section 4.2.6.6 of the SPP (Reference (45)), the BRR shall:

- Describe the review scope,
- Identify the reviewers,
- Identify the persons contacted during the review,
- Document the outputs and versions reviewed,
- Contain a summary of the review results, and
- Describe recommendations and findings.

4.6.4 FPGA development Tool

The NICSD IV&V Team will use the following FPGA development tools for V&V activities.

1. Designer tool
2. Synplify® tool
3. Netlist Viewer tool
4. ModelSim® tool

These tools are commercial software tools, that PPDD uses for development of FPGA based modules. Section 8.1.2 of the NICSD SMP (Reference (48)) describes the tools as well as methods used to accept use of the tools for FPGA-based safety systems for nuclear power

plants.

In addition to the above tools, NICSD uses office productivity tools, database software, or editor tools. These software tools are SIL 1 software, and do not need special control procedure.

4.6.5 Test Equipment

NICSD shall control the software tools as described in the NICSD SMP.

The NICSD IV&V Team will review and approve the PPDD work products associated with FPGA review and test.

The NICSD IV&V Team shall document the result of a software tool in a V&V Report.

NICSD expect that PPDD uses the following test equipment for the module testing at the factory:

- Signal-generating equipment – Signal-generating equipment is used to generate test signal to modules.
- Signal-recording equipment – Signal-recording equipment is used to record response signals from the module.
- Test Personal Computer (PC) – One or more PCs are used to control the signal-generating equipment and the signal-recording equipment. The Test PC records the generated and response signals.

NICSD will use test equipment for the verification and validation activities for the units and the system. The test equipment is similar to that of PPDD. The NICSD IV&V Team will evaluate adequacy of these tools.

Test equipment software is not embedded in any FPGA-based safety-related systems.

4.6.6 Metrics

The NICSD IV&V Team should monitor and track the following metrics through the lifecycle phases described in Section 5 to evaluate the product quality.

- Number of changes applied for the design documents
- Number of open items carried to the next phase
- Number of open items closed in the current phase
- Number of Site Corrective Action Requests (SCARs)
- Number of Site Nonconformance Notice Reports (SNNRs)
- Number of problems found during V&V testing

4.7 Security

NICSD takes appropriate measures to ensure Secure Development and Operational Environment (SDOE) as addressed in the SPP. The requirements for the NICSD SDOE are mapped and described in the NQ-2037 (Reference (28)). The NICSD IV&V Team shall verify that the cyber security requirements described in NQ-2037 are correctly reflected in the software life cycles.

5 Verification and Validation Activities

Table B of this NICSD VVP describes V&V activities assigned to each Software Life Cycle Phases.

The following sub-sections describe the V&V activities for the NICSD scope.

5.1 Management

5.1.1 Management of V&V

Section 4.3.1 of the SPP (Reference (45)) describes management of the V&V Activities. The management of the V&V process is performed throughout the life cycle phase. Table 10 of the SPP defines the V&V management tasks, which are equivalent to the management tasks defined in IEEE Std. 1012 (Reference (3)). Table 5-1 shows the corresponding activities to the management tasks in this VVP.

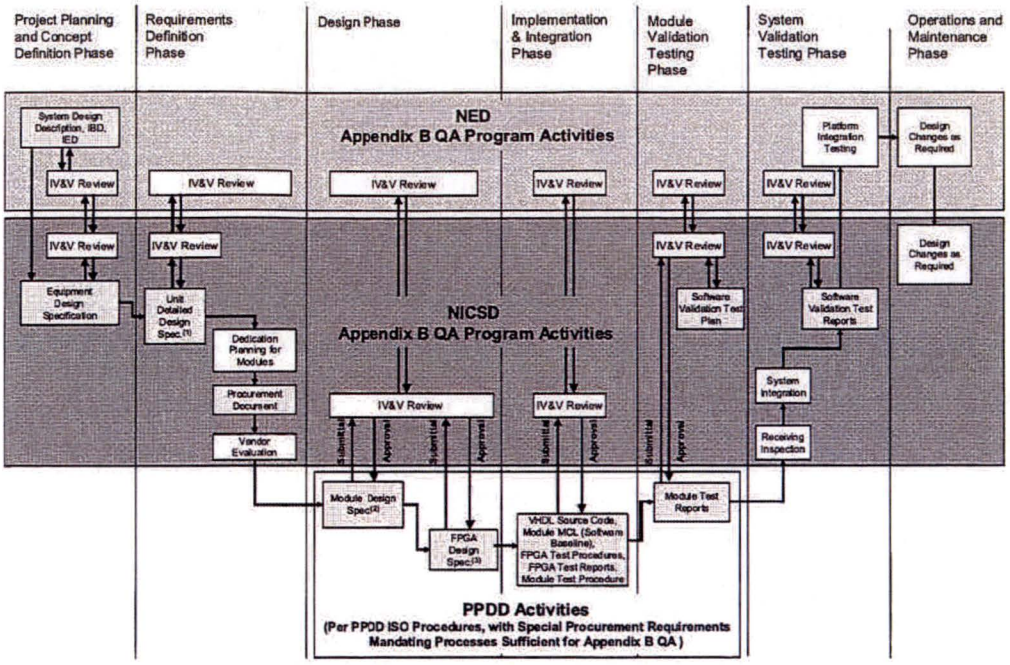
Table 5-1 V&V Management Activities

SPP Table 10 Tasks	Activity in this NICSD VVP
1) Software Verification and Validation Plan (SVVP) Update	Establishment of this NICSD VVP
2) Baseline Change Assessment	Activity Iteration Policy in Section 7.2 in this NICSD VVP covers the requirements of the Baseline Change Assessment
3) Management Review	The NICSD PM and NICSD SQA Team oversee the NICSD IV&V Team activities.
4) Management and Technical Review Support	A Process Review Meeting (PRM) is held in every phase to ensure that the required activities during that phase were completed. The NICSD IV&V Team shall attend the PRM for management and technical support.
5) Organizational and Supporting Processes Interface	The NICSD IV&V Team shall attend the PRM. The NICSD IV&V Team shall attend the project management meetings when the NICSD IV&V Lead considers it necessary. The NICSD SQA Team will oversee NICSD IV&V work when the NICSD SQA Lead determines that such oversights are needed.

5.1.2 V&V Phases

Section 13 of the NICSD SMP (Reference (48)) defines the software life cycle for the FPGA-based safety-related I&C systems. Figure 5-1 is the summary drawing illustrating the

major activities in the life cycle process for FPGA-based systems.



(1) Unit Detailed Design Spec. includes Software Requirements Specification.
(2), (3) Module Design Spec. and FPGA Design Spec. include Software Design Description.

Figure 5-1 Life Cycle Process for FPGA-based Systems

The NICSD IV&V Team activities shall be performed for the life cycle phases defined in the NICSD SMP (Reference (48)). This NICSD VVP includes the life cycle phases from the Project Planning and Concept Definition Phase through the System Validation Testing Phase. This NICSD VVP ends after the System Validation Testing, prior to shipment from Japan However, if any need for design change arises after finalizing the V&V activities, this NICSD VVP and the V&V activities shall be reactivated from the earliest phase affected by the change, and necessary activities shall be iterated. For design changes in the Operations and Maintenance phase, another VVP will be prepared.

5.1.3 Use of Previously Developed or Purchased Software

PPDD is a commercial supplier. The FPGA logic lifecycle is treated as the software lifecycle in the NICSD SMP (Reference (48)) and SPP (Reference (45)). The FPGA logic procured from PPDD is included in the FPGA and is commercial. The FPGA logic is treated as Previously Developed Software (PDS). The FPGA logic is comprised of combinations and connections of software elements called functional elements (FEs). The FEs are treated as Commercial-off-the Shelf (COTS) software. NICSD dedicates the FPGA logic implemented in FPGA under NICSD Commercial Grade Dedication (CGD) process defined in the NICSD SMP. NICSD shall evaluate the PPDD before ordering to PPDD through a CG Survey, Critical Digital Review (CDR), or both of them. The NICSD IV&V Team will review and oversee the PPDD in each step of works, and accept those works.

5.2 Project Planning and Concept Definition Phase

The activities in the Project Planning and Concept Definition Phase are performed by ICDD and NICSD. The activities of NICSD in the Project Planning and Concept Definition Phase are described in this section.

During this phase, NICSD generates the Equipment Design Specification (EDS) including the design basis and applicable regulations and industry practices in the design, and starts the master configuration list (MCL). The MCL started in this phase is updated throughout the software life cycle.

Table A of the NICSD SMP (Reference (48)) lists the outline of the output documents of the NICSD V&V activities.

5.2.1 Preparation of NICSD VVP

The NICSD IV&V Team shall prepare this NICSD VVP in accordance with NQ-2013 (Reference (17)), coordinating the plan with the ICDD VVP. The NICSD IV&V Lead shall review this NICSD VVP.
For the procedures to be used for the document review, see Section 4.6.1 in this NICSD VVP.

The NICSD IV&V Team delivers the NICSD VVP to the ICDD IV&V Team for review.

5.2.2 Preparation of Software Test Plan

The NICSD IV&V Team shall prepare a Software Test Plans as described in Section 9 of the SPP (Reference (45)). The NICSD IV&V Team uses the EDS as the base to prepare the Software Test Plan. The scope of tests covered by the Software Test Plan is as follows.

- FPGA Testing
- Module Validation Testing
- System Validation Testing

The Software Test Plan defines the scope, approach, resources, and schedule of the testing activities, and shall require generation of the following documents:

- Software Validation Test Plan (SVTP)
- Test Specification (including Test Design, Test Case)
- Test Procedure
- Test Report

5.2.3 Document Reviews

The NICSD IV&V Team shall perform independent reviews of the documents, which are listed in Table A of the NICSD SMP marked "DVR" in the "Other Outputs" column. For the procedures to be used for the document review, see Section 4.6.1 in this NICSD VVP.

The NICSD IV&V Team reviews the documents for the V&V activities in this phase referring to the methods and procedures described in Table 11 of the SPP. The Table B is provided for a better understanding of terminological difference between the SPP and NICSD VVP.

5.2.4 Project Planning and Concept Definition Phase RTM efforts

(1) Preparation of the RTM

The NICSD SD Team shall update the Project Planning and Concept Definition Phase RTM delivered by ICDD to maintain the traceability between the ICDD requirements and the EDS

in accordance with NQ-2015 (Reference (19))

The NICSD SD Team traces the upper level requirements in the NED documents to the EDS, and traces the EDS requirements back to the upper level requirements.

The RTM efforts ensure the following:

- The requirements are traced "forwards" from the upstream documents to the downstream documents.
- The downstream requirements are traced back to the upstream documents.

See Section 8.1 for preparation of RTM.

(2) Compilation of the Project Planning and Concept Definition Phase RTM report

The NICSD SD Team summarizes open items revealed by the RTM efforts. The NICSD SD Team must resolve these items to the satisfaction of the RTM preparer(s).

The NICSD IV&V Team shall review the RTM for work performed by NICSD.

The NICSD IV&V Team shall describe the result of RTM review in the V&V Report for this phase.

5.2.5 Security Review

The NICSD IV&V Team shall review that the cyber security requirements described in NQ-2037 (Reference (28)) and the SPP are correctly reflected in the software life cycles.

The NICSD IV&V Team shall perform independent review (IR) of the EDS and SSARs, and ensure that appropriate cyber security requirements complying with NQ-2037 and the SPP are included in the EDSs and SSARs. In addition, the NICSD IV&V Team shall confirm that an appropriate secure development environment is established. The result of Security Review shall be described in the V&V Report.

5.2.6 Project Planning and Concept Definition Phase V&V Reporting

The NICSD IV&V Team shall prepare the Project Planning and Concept Definition Phase V&V Report summarizing the V&V activities performed for this Project Planning and Concept Definition Phase. This report will be extended at the end of each phase to add the results of each phase report. At the end of the lifecycle, the final report will thus contain the results from all lifecycle phases.

The NICSD V&V Report shall include:

(1) References to the reviewed documents
(2) References to the Design Verification Reports (DVR)
(3) Reference to the Project Planning and Concept Definition Phase RTM (NICSD portion)
(4) Open items revealed in the RTM efforts
(5) Result of the Security Review
(6) Result of the SSAR review
(7) Metrics described in Section 4.6.6
(8) Any findings, recommendations, or suggestions to reduce any risks identified in the V&V activities

The NICSD IV&V Team delivers the NICSD V&V Report to the ICDD IV&V Team for review.

5.2.7 Baseline Review

To complete the Project Planning and Concept Definition Phase, the NICSD IV&V Team shall perform baseline reviews at the phase end as described in Section 4.6.3. The NICSD IV&V Team shall issue a Baseline Review Report (BRR) documenting the results of the Baseline Review and report to the NICSD SQA Team for review and approval as QA record.

5.3 Requirements Definition Phase

The development activities in the Requirements Definition Phase are performed by NICSD. In the Requirements Definition Phase, the NICSD SD Team develops a Unit Detailed Design Specification. This specification addresses software and hardware requirements accomplished by unit design, and provides necessary functional requirements for module design.

Table A of the NICSD SMP (Reference (48)) lists the outline of the output documents of the NICSD V&V activities.

5.3.1 Document Reviews

The NICSD IV&V Team shall perform independent reviews of the documents, which are listed in Table A of the NICSD SMP (Reference (48)), and marked "DVR" in the "Other Outputs" column. For the procedures to be used for the document review, see Section 4.6.1 in this NICSD VVP.

The NICSD IV&V Team reviews the documents for the V&V activities in this phase referring to the methods and procedures described in Table 12 of the SPP (Reference (45)). The Table B is provided for a better understanding of terminological difference between the SPP and NICSD VVP.

5.3.2 Requirements Definition Phase RTM efforts

(1) Preparation of Requirements Definition Phase RTM

The NICSD SD Team performs the Requirements Definition Phase RTM efforts.
The RTM efforts ensure the following:

- The requirements are traced "forwards" from the Project Planning and Concept Definition Phase to this phase design documents.
- The requirements are traced back from this phase to the Project Planning and Concept Definition Phase. That is, all requirements listed in this phase are covered by the Project Planning and Concept Definition Phase requirements, and no new requirements have been created in this phase.

In this Requirements Definition Phase, some requirements from the Project Planning and Concept Definition Phase are allocated to hardware. These hardware requirements are also traced. In addition, the RTM efforts must address interface requirements among units, and among modules.

(2) Compilation of the Requirements Definition Phase RTM report

The NICSD IV&V Team shall review the RTM.
The NICSD IV&V Team shall describe the result of RTM review in the V&V Report for this phase.

5.3.3 Security Review

The NICSD IV&V Team shall review that the cyber security requirements described in NQ-2037 (Reference (28)) and the SPP (Reference (45)) are correctly reflected in the software life cycles.

The NICSD IV&V Team shall perform independent review (IR) of the Unit Detailed Design Specifications and SSARs, and confirm that appropriate cyber security requirements complying with NQ-2037 and the SPP are included in the Unit Detailed Design Specifications. The result of Security Review shall be described in the V&V report.

5.3.4 Requirements Definition Phase V&V Reporting

The NICSD IV&V Team shall prepare the Requirements Definition Phase V&V Report summarizing the V&V activities performed for this Requirements Definition Phase.

The NICSD V&V Report shall include:

(1) Reference to the reviewed documents

(2) Reference to the Design Verification Reports (DVR)

(3) Reference to the Requirements Definition Phase RTM

(4) Open items revealed in the RTM efforts

(5) Results of the Security Review

(6) Results of the SSAR review

(7) Metrics described in Section 4.6.6

(8) Any findings, recommendations, or suggestions to reduce any risks identified in the V&V activities

The NICSD IV&V Team delivers the NICSD V&V Report to the ICDD IV&V Team for review.

5.3.5 Baseline Review

To complete the Requirements Definition Phase, the NICSD IV&V Team shall perform baseline reviews at the phase end as described in Section 4.6.3. The NICSD IV&V Team shall issue a BRR documenting the results of the Baseline Review and report to the NICSD SQA Team for review and approval as QA record.

5.4 Design Phase

NICSD procures the FPGA-based modules from PPDD. In the design phase, PPDD produces the Module Design Specifications and the FPGA Design Specifications, which define the FPGA logic design, in accordance with PPDD procedure E-68017 (Reference (39)). A special characteristic of the Toshiba FPGA-based I&C systems is that FPGA logic consists of the verified and well proven functional elements (FEs) and interconnects between FEs. All FE are generated by PPDD. The V&V activities for FEs are described separately in Section 5.8.

Table A of the NICSD SMP (Reference (48)) lists the outline of the output documents of these V&V activities.

5.4.1 Preparation of SVTP

The NICSD IV&V Team shall initiate preparation of a Software Validation Test Plan (SVTP) in accordance with this NICSD VVP and in Section 9 of the SPP (Reference (45)). The SVTP shall outline the methodology of how various tests will be used to validate that the integrated software meets the requirements stated in the EDS and the Unit Detailed Design Specification.

The SVTP can include a plan for Platform Factory Test (PFT), if necessary.

This activity shall be initiated in this phase to ensure completion prior to the System Validation Testing Phase.

5.4.2 Document Reviews

During this phase, the NICSD IV&V Team is involved in reviewing each PPDD work product. The NICSD IV&V Team ensures the quality and completeness of each work product and its readiness for CGD.

The NICSD IV&V Team shall perform independent reviews of the documents, which are listed in Table A of the NICSD SMP (Reference (48)), and marked "DVR" in the "Other Outputs" column. For the procedures to be used for the document review, see Section 4.6.1 in this NICSD VVP.

The NICSD IV&V Team reviews the documents for the V&V activities in this phase referring to the methods and procedures described in Table 13 of the SPP. The Table B is provided for a better understanding of terminological difference between the SPP and NICSD VVP.

The NICSD IV&V Team shall review design and test documents submitted by PPDD. PPDD use PPDD standard E-68017 (Reference (39)) that has equivalent requirements for FPGA design, coding and testing specified in NICSD Standard NQ-2031 (Reference (23)).

The NICSD IV&V Team shall confirm that the FPGA logic is designed adhering to the design rules given in the NICSD Standard NQ-2031, Appendix A, as well as confirming that guidance provided by the FPGA vendor, Microsemi Corporation, in Application Notes for the chosen FPGA integrated circuit is appropriately incorporated in the design. In particular, the FPGA logic consists of the verified and well proven FEs, and the interface to each FE is consistent with the FE specification. The NICSD IV&V Team shall review and approve the results of the PPDD review.

The NICSD IV&V Team shall check that the FE documents are appropriately maintained as described in Section 5.8.

The NICSD IV&V Team shall confirm that the requirements in PPDD Standard E-68017 are equivalent to the requirements in NICSD Standard NQ-2031 through the CG Survey report or CDR report, or other means.

5.4.3 Design Phase RTM efforts

(1) Preparation of Design Phase RTM

The PPDD design engineers prepare the RTM to maintain the traceability from the unit design to the module design and to the FPGA. The RTM efforts ensure the following:

- The requirements are traced "forwards" from the Requirements Definition Phase to this phase design documents. That is, all requirements in the unit design are allocated to modules mounted in the unit, and requirements in each module design are

allocated to FPGAs included in the module.

- The requirements are traced back from this phase to the Requirements Definition Phase. That is, all requirements listed in this phase are covered by the Requirements Definition Phase, and no new requirements have been created in this phase.
  Note: An FPGA design may include maintenance or test purpose circuits. Inclusion of these kinds of circuits must be described in the Module Design Specification as exceptions. The NICSD IV&V Team shall confirm that these circuits do not cause any adverse effects to the module functions.

(2) Compilation of the Design Phase RTM report

The NICSD IV&V Team shall review the RTM prepared by PPDD.

The NICSD SD Team shall update the RTM of the Requirements Definition Phase based on the RTM prepared by PPDD.

The NICSD IV&V Team shall describe the result of RTM review in the V&V Report for this phase.

5.4.4 Security Review

The NICSD IV&V Team shall verify that the cyber security requirements described in NQ-2037 (Reference (28)) and the SPP (Reference (45)) are correctly reflected in the software life cycles.

The NICSD IV&V Team shall perform independent review (IR) of the Module Design Specifications, FPGA Design Specifications and SSARs, and confirm that appropriate cyber security requirements complying with NQ-2037 and the SPP are included in the Module Design Specifications and FPGA Design Specifications. In addition, the NICSD IV&V Team shall confirm that an appropriate secure development environment is established in PPDD. The result of the Security Review shall be described in the V&V Report.

5.4.5 Design Phase V&V Reporting

The NICSD IV&V Team shall prepare the Design Phase V&V Report summarizing the V&V activities performed for this Design Phase.

The NICSD V&V Report shall include:

(1) Reference to the reviewed documents

(2) Reference to the Design Verification Reports (DVR)

(3) Reference to the results of the FE document and the software tool control checks, see Section 5.8.

(4) Reference to the Design Phase RTM

(5) Open items revealed in the RTM efforts

(6) Results of the Security Review

(7) Results of the SSAR review

(8) Metrics described in Section 4.6.6

(9) Any findings, recommendations, or suggestions to reduce any risks identified in the V&V activities

The NICSD IV&V Team delivers the NICSD V&V Report to the ICDD IV&V Team for review.

5.4.6 Baseline Review

To complete the Design Phase, the NICSD IV&V Team shall perform baseline reviews at the phase end as described in Section 4.6.3. The NICSD IV&V Team shall issue a BRR documenting the results of the Baseline Review and report to the NICSD SQA Team for review and approval as QA record.

5.5 Implementation and Integration Phase

In the Implementation and Integration Phase, the FPGAs are developed by PPDD in the following three steps:

Step 1 VHDL Source Coding:

The PPDD design engineers generate VHDL source code that implements the functional requirements written in the FPGA Design Specification in accordance with PPDD procedure E-68017 (Reference (39)). In generating the VHDL source code, the PPDD design engineers use editor tools. Since subsequent activities adequately verify and validate the VHDL source code, no V&V activities are necessary for the editor tools.

Step 2: FPGA Implementation

The PPDD design engineers convert the VHDL source code into netlists using the Synplify® tool, a logic synthesizer. Netlists of FEs used in the design are taken from the PPDD FE library, and integrated into a single netlist by the Designer tool supplied by Microsemi.

To detect errors in the netlists, which may be undetected by the software tools, and errors in the source code, the NICSD IV&V Team confirms logic diagrams from the netlist, and inspects the logic diagrams comparing with the VHDL source code. The logic diagrams are drawn by the Netlist Viewer tool, which is supplied by Microsemi, but is independent of the Synplify® tool.

After the inspection, the PPDD design engineers convert the netlists into a placed, routed netlist, called fuse map, and embeds the fuse map into a test purpose FPGA.

To minimize risks associated with timing, the PPDD design engineers perform timing analysis and simulation during their design process. This two-part process includes static timing analysis and dynamic timing simulation. Static timing analysis evaluates the setup and hold times on each path within the FPGA design. The Designer software tool evaluates the propagation delay to each element in the code in order to determine each timing path in the code. The result from this static analysis can be interpreted by the ModelSim® tool. The PPDD design engineers then use ModelSim® tool to validate the design with dynamic simulation, using accurate propagation delays.

Step 3: FPGA Testing

PPDD performs testing on the FPGAs as defined below. The NICSD IV&V Team reviews the FPGA Test Procedure prepared by PPDD.

This testing includes:

a) Simulation of the fuse map generated in Step 2, and

b) FPGA Testing using the test purpose FPGA produced in Step 2.

The PPDD design engineers perform FPGA Testing using the ModelSim® tool, and the PinPort device. The ModelSim® tool is not only used in simulation, but also in FPGA Testing using an FPGA chip that embeds target FPGA logic for testing. The ModelSim® tool generates inputs to the FPGAs according to the test vectors that are prepared prior to the FPGA Testing.

The PPDD engineers use ModelSim® tool to simulate the internal operation of the logic. The ModelSim® tool provide the PPDD engineer with the capability to watch individual signals within the FPGA and validate that timed FPGA logic works as the engineer intends. These tests verify that the FPGA timing constraints are satisfied, and that additional PPDD timing rules are satisfied. The NICSD IV&V Team shall review FPGA Test Reports describing the result of the FPGA Testing.

After the test is satisfactorily performed using both the simulation software tool and an implementation in an FPGA, the FPGA logic is considered qualified, and registered. Thus the baseline for the registered FPGA logic is established.

The qualified FPGA logic must be implemented in an FPGA integrated circuit prior to being soldered to a module printed circuit board.

All testing results are brought into the NICSD Appendix B program and placed under configuration management at the successful conclusion of testing and acceptance of that testing by NICSD.

Table A of the NICSD SMP (Reference (48)) lists the outline of the outputs of these V&V activities.

The NICSD IV&V Team should observe PPDD activities to verify that PPDD work in accordance with their procedures and NICSD's expectations. These observations could be coordinated with NICSD SQA Team. Results of the observation shall be documented in the V&V Report. If the NICSD IV&V Team finds any nonconformance in PPDD's activities, the NICSD IV&V Team shall issue a SCAR documenting the rejection of the PPDD work product.

5.5.1 VHDL Source Code Reviews

The NICSD IV&V Team shall review the source code to verify correctness, consistency, completeness, accuracy, and traceability to the design specifications in accordance with NQ-2031 (Reference (23)), Sections 13.4.3 and 14.5.1 of the NICSD SMP (Reference (48)), and Code Review Guide 8M8K0000 (Reference (51)). The results of these reviews must be documented using a Source Code Review Sheet. These verifications must include (at a minimum) review of the FPGA source code written in VHDL (or equivalent configuration information) to ensure that the source code matches what was specified in the FPGA Design Specification (Software Design Description). NICSD IV&V Lead shall organize a Code Review Team by assigning Code Review Lead and Code Reviewers. The reviewer may use software development tools such as a VHDL Simulator in addition to traditional techniques described in IEEE Std 1028 (Reference (4)).

PPDD shall provide necessary information for the source code reviews such as source codes,

report files of software tools (Synplify, Designer, and other tools), and software documents to the Code Review Team.

The Code Reviewers review the information with a Source Code Review Sheet specified in Code Review Guide 8M8K0000.

The major checkpoints are,

(1) Use of FE Design,

(2) Synchronous Design

(3) Interface review for compatibility between FPGA, specially for Input/Output Pin Setting,

(4) Warning of Software Tools,

(5) Equations, algorithms, and control logic,

(6) Constraint,

(7) Software operation within requirement constraints, and

(8) Conformance to Coding Guideline E-68017 (Reference (39)).

The results of these reviews must be documented in the Source Code Review Sheet by the Code Reviewer. Anomalies found during the review shall be documented in an Anomaly List. A Code Reviewer shall set up the Exit Meeting of Code Review Team with Code Designer in PPDD and observers. Code Review Team shall classify each anomaly as Major or Minor, and shall determine the disposition of each anomaly as "Use as is" or "Rework." Source Code Review Sheet shall include the classification, the disposition, and the determination whether the criteria of closing the disposition is satisfied.

5.5.2 Logic Synthesis and Layout

The PPDD design engineers convert the VHDL source code into a netlist using the Synplify® tool, and convert the netlist into a fuse map using a place and layout tool integrated in the Designer tool. The PPDD design engineers check the message files from the software tools to confirm that logic synthesis and layout are performed without errors, or problematic warnings. The NICSD IV&V Team verifies the result of the message checks and documents it in the V&V Report.

5.5.3 Signal Timing

The NICSD IV&V Team confirms that the PPDD design engineers meet the FPGA design rules. The NICSD IV&V Team shall verify the timing analysis performed to show that the timing margin described in NQ-2031 (Reference (23)) exists within this FPGA. The NICSD IV&V Team shall evaluate the result of the FPGA internal timing analysis, and document it in the V&V Report.

5.5.4 Netlist Inspection

The NICSD IV&V Team inspects the netlists by comparing the original VHDL files with the logic diagrams generated from the netlists by the Netlist Viewer tool, to verify the correctness of the conversion. In the comparison, the FE interfaces shall be checked, because the VHDL

source code implements logic using FEs.

The results of the netlist check shall be documented in the V&V Report.

5.5.5 Document Reviews

The NICSD IV&V Team shall perform independent reviews of the documents, which are listed in Table A of the NICSD SMP (Reference (48)), and marked "DVR" in the "Other Outputs" column. For the procedures to be used for the document review, see Section 4.6.1 in this NICSD VVP.

The NICSD IV&V Team reviews the documents for the V&V activities in this phase referring to the methods and procedures described in Table 14 of the SPP. The Table B is provided for a better understanding of terminological difference between the SPP and the NICSD VVP.

It should be noted that the NICSD IV&V team must confirm that the test cases for FPGA Testing achieve 100% toggle coverage (see NICSD Standard NQ-2011(Reference (16)) for a definition of toggle coverage) of the active FE connections, and the test cases are sufficient to ensure that the FPGA performs its intended functions.

5.5.6 FPGA Testing

PPDD prepares the FPGA Test Procedures in accordance with E-68016 (Reference (38)), including test cases, before the execution of the testing. The NICSD IV&V Team shall review the FPGA Test Procedures in accordance with NQ-2030 (Reference (22)).

FPGA Testing shall be performed in accordance with the FPGA Test Procedure approved by NICSD. The results of the FPGA Testing shall be documented in FPGA Test Reports. The NICSD IV&V Team shall evaluate the FPGA Test Reports.

Any test failures, any product or configuration nonconformances, or any errors in the test procedure itself shall be resolved as described in Section 7.1.

5.5.7 Software Tool Control Review

The NICSD IV&V Team shall review the PPDD control of the software tools used in their design and V&V activities as described in Section 8.1.2 of the NICSD SMP. The NICSD IV&V Team shall review PPDD's records for software tool control to ensure:

- PPDD uses correct versions of software tools for FPGA manufacturing.
- PPDD is controlling the software tools in accordance with procedures that NICSD has reviewed and approved.

5.5.8 Implementation and Integration Phase RTM efforts

(1) Preparation of Implementation and Integration Phase RTM

The PPDD design engineers perform the Implementation and Integration Phase RTM efforts. The RTM efforts ensure that the FPGA Test Procedures cover all logic requirements for FPGAs defined in the FPGA Design Specifications. Note that traceability between FPGA design to VHDL source code is verified in VHDL source code review, and is not included in the RTM efforts.

(2) Compilation of the Implementation and Integration Phase RTM Report

The NICSD IV&V Team shall review the RTM from PPDD.

The NICSD IV&V Team shall describe the result of RTM review in the V&V Report for this phase.

5.5.9 Security Review

The NICSD IV&V Team shall review that the cyber security requirements described in NQ-2037 (Reference (28)) and the SPP (Reference (45)) are correctly reflected in the software life cycles.

The NICSD IV&V Team shall perform an independent review (IR) of the FPGA Test Procedures, FPGA Test Reports. The NICSD IV&V Team shall also review that appropriate cyber security requirements complying with NQ-2037 and the SPP are included in the FPGA Test Procedures.
In addition, the NICSD IV&V Team shall confirm that appropriate security measures are taken in VHDL code generation, code conversion from source code to fuse map, and data storage.
The result of the Security Review shall be described in the V&V Report.

5.5.10 Implementation and Integration Phase V&V Reporting

The NICSD IV&V Team shall prepare the Implementation and Integration Phase V&V Report summarizing the V&V activities performed for this Implementation and Integration Phase. The combination of the Source Code Review Sheet and FPGA Test Report satisfies the requirements for Software Implementation Review Report described in Section 3.12.3.5 of the SPP (Reference (45)).

The NICSD V&V Report shall include:

(1) Reference to the reviewed documents

(2) Reference to the Design Verification Reports (DVR)

(3) Reference to the Source Code Review Sheet

(4) Reference to the software tools message file checks

(5) Reference to the netlist inspections

(6) Reference to the FPGA Test Reports

(7) Reference to the FPGA Control Sheets

(8) Reference to Purchase Specification to PPDD

(9) Reference to the Implementation and Integration Phase RTM

(10) Results of Software Tool Control Review

(11) Open items revealed in the RTM efforts

(12) Results of the Security Review

(13) Results of the SSAR review

(14) Metrics described in Section 4.6.6

(15) Any findings, recommendations, or suggestions to reduce any risks identified in the V&V activities

The NICSD V&V Report includes the Software Build Procedure and Report (SBPR) as defined in the SPP. The following documents are treated as SBPR.

- FPGA Control Sheet
  FPGA Control Sheet shall document the names of the VHDL source code files.

The NICSD IV&V Team delivers the NICSD V&V Report to the ICDD IV&V Team for review.

5.5.11 Baseline Review

To complete the Implementation and Integration Phase, the NICSD IV&V Team shall perform baseline review at the phase end as described in Section 4.6.3. The NICSD IV&V Team shall issue a BRR documenting the results of the Baseline Review and report to NICSD SQA Team for review and approval as QA record.

5.6 Module Validation Testing Phase

Once the module using verified FPGAs has been assembled, PPDD performs module functional testing in accordance with written test procedures. In the Module Validation Testing Phase, PPDD demonstrates that the modules perform all intended functions within the predetermined design, and that the modules do not perform unintended or undesirable functions. PPDD develops Module Test Procedures based on E-68016 (Reference (38)). These test procedures, including test plan, test cases, and acceptance criteria, are written by an engineer other than the engineer who designed the module to be tested.

The PPDD personnel perform module validation testing and generate a Module Test Report which includes a test log and a listing of any testing anomalies. PPDD will resolve test anomalies, by changing the test procedure or changing FPGA logic. If FPGA logic is changed, the V&V activities in Section 5.5 for the FPGA logic shall be iterated. These changes shall be recorded. The test is repeated in its entirety until the test passes successfully. After successful results are obtained, the test report shall be reviewed with change records (if any), approved, and placed under CM.

Table A of the NICSD SMP (Reference (48)) lists the outline of the outputs of these V&V activities.

In addition to the activities described in the following subsections, the NICSD IV&V Team should oversee PPDD activities to verify that PPDD work in accordance with their procedures and NICSD's expectations. Results of observation shall be documented in the V&V Report. If the NICSD IV&V Team finds any nonconformance in a PPDD's activity, the NICSD IV&V Team shall issue a SCAR in accordance with NQ-3019 (Reference (34)).

5.6.1 Document Reviews

The NICSD IV&V Team shall perform independent reviews of the documents, which are listed in Table A of the NICSD SMP (Reference (48)), and marked "DVR" in the "Other Outputs" column. For the procedures to be used for the document review, see Section 4.6.1 in this NICSD VVP.

The NICSD IV&V Team reviews the documents for the V&V activities in this phase referring to the methods and procedures described in Table 15 of the SPP (Reference (45)). The Table B is provided for a better understanding of terminological difference between the SPP and NICSD VVP.

5.6.2 Module Validation Testing

PPDD prepares Module Test Procedures in accordance with E-68016 (Reference (38)). PPDD personnel perform the module validation testing in accordance with the Module Test Procedures. PPDD prepares the Module Test Procedures before the execution of the testing. The NICSD IV&V Team shall review the Module Test Procedures in accordance with NQ-2030 (Reference (22)). If NICSD considers necessary, NICSD shall require additional testing to PPDD, in order to check that the module has satisfied the software requirements.

Any test failures, any product or configuration nonconformances, or any errors in the test procedure itself shall be resolved as described in Section 7.1.

5.6.3 Test Equipment Software Review

The NICSD IV&V Team shall review the PPDD control of the test equipment software, used in the Module Validation Testing. The NICSD IV&V Team shall review PPDD's records for test equipment software control to ensure:

- Test equipment software used for the project tests is prepared in accordance with procedures that the NICSD IV&V Team has reviewed and approved.
- PPDD is controlling the software tools in accordance with PPDD procedure E-68020 (Reference (42)).

5.6.4 Module Validation Testing Phase RTM efforts

(1) Preparation of Module Validation Testing Phase RTM

The PPDD design engineers perform the Module Validation Testing Phase RTM efforts. The RTM efforts ensure the module test procedures cover all logic requirements for the modules defined in the Module Design Specifications.

(2) Compilation of the Module Validation Testing Phase RTM Report

The NICSD IV&V Team shall review the RTM from PPDD.

The NICSD IV&V Team shall describe the result of RTM review in V&V Report for this phase.

5.6.5 Security Review

The NICSD IV&V Team shall review that the cyber security requirements described in NQ-2037 (Reference (28)) and the SPP (Reference (45)) are correctly reflected in the software life cycles.

The NICSD IV&V Team shall perform independent review (IR) of the Module Test Procedures and shall review that appropriate cyber security requirements complying with NQ-2037 and the SPP are included in the Module Test Procedures and the SSARs.

In addition, the NICSD IV&V Team shall confirm that appropriate security measures are taken in the following activities:

- Delivery of the fuse map
- Embedment of logic into FPGAs
- Storage of logic embedded FPGAs
- Module assembly

- Transportation and storage of modules

The result of Security Review shall be described in the V&V Report.

5.6.6 Module Validation Testing Phase V&V Reporting

The NICSD IV&V Team shall prepare the Module Validation Testing Phase V&V Report summarizing the V&V activities performed for this Module Validation Testing Phase.

The NICSD V&V Report shall include:

(1) Reference to the reviewed documents

(2) Reference to the Design Verification Reports (DVR)

(3) Reference to the Module Test Reports

(4) Reference to the Module Validation Testing Phase RTM

(5) Results of Test Equipment Software Review

(6) Open items revealed in the RTM efforts

(7) Results of the Security Review

(8) Results of the SSAR review

(9) Metrics described in Section 4.6.6

(10) Any findings, recommendations, or suggestions to reduce any risks identified in the V&V activities

The NICSD IV&V Team delivers the NICSD V&V Report to the ICDD IV&V Team for review.

5.6.7 Baseline Review

To complete the Module Validation Testing Phase, the NICSD IV&V Team shall perform baseline reviews at the phase end as described in Section 4.6.3. The NICSD IV&V Team shall issue a BRR documenting the results of the Baseline Review and report to NICSD SQA Team for review and approval as QA record.

5.7 System Validation Testing Phase

For the unit integration, a NICSD receiving inspector receives the modules to be installed in the units. After accepting the modules in the previous phase, NICSD assembles the module into the units. Then, NICSD assembles the system from the units. The NICSD test personnel shall perform the System Validation Testing in accordance with the SVTP. This test must demonstrate that the system performs all intended functions within the predetermined design, and that the system does not perform unintended or undesirable functions that were identified in the test scope.

The NICSD test personnel generate a test record, which includes a test log. Testing anomalies, if any, will be recorded in a NNR in accordance with NQ-3019 (Reference (34)). NICSD will resolve test anomalies, which may require changing the test procedure or changing FPGA logic. If FPGA logic is changed, the V&V activities in Section 5.5 and 5.6 for the FPGA logic shall be iterated. The test is repeated in its entirety until the test passes successfully. After successful results are obtained, the NICSD IV&V Team shall review the

test record with change records (if any). Then the test record will be approved, and placed under the SCMP (Reference (50)).

Table A of the NICSD SMP (Reference (48)) lists the outline of the outputs of these V&V activities.

The NICSD IV&V Team evaluates the results of the System Validation Testing to confirm that requirements identified in the EDS and Unit Detailed Design Specifications are satisfactorily covered, and issue a Software Validation Test Report (SVTR).

The NICSD IV&V Team may also observe NICSD activities to verify that NICSD work in accordance with applicable NICSD procedures. Results of observation shall be documented in the V&V Report.

5.7.1 Document Reviews

The NICSD IV&V Team shall perform independent reviews of the documents, which are listed in Table A of the NICSD SMP (Reference (48)), and marked "DVR" in the "Other Outputs" column. For the procedures to be used for the document review, see Section 4.6.1 in this NICSD VVP.

The NICSD IV&V Team reviews the documents for the V&V activities in this phase referring to the methods and procedures described in Table 15 and Table 16 of the SPP (Reference (45)). The Table B is provided for a better understanding of terminological difference between the SPP and NICSD VVP.

5.7.2 Unit Validation Testing

The NICSD test personnel shall perform the unit validation testing as a part of System Validation Testing in accordance with SVTP.

Any test failures, any product or configuration nonconformance, or any errors in the test procedure itself shall be resolved as described in Section 7.1.

The NICSD IV&V Team shall describe the result of Unit Validation Testing in the V&V Report for this phase.

5.7.3 System Validation Testing

The NICSD test personnel shall perform the System Validation Testing in accordance with SVTP.

Any test failures, any product or configuration nonconformance, or any errors in the test procedure itself shall be resolved as described in Section 7.1.

Successful completion of testing and document reviews will complete the requirements for commercial grade dedication. The NICSD IV&V Team shall review the completed commercial grade dedication package to confirm that all required activities are complete and that the evaluations are complete and correct. Completion of the NICSD IV&V Team review of the commercial grade dedication shall be the last technical activity to be completed.

The NICSD IV&V Team shall describe the result of System Validation Testing in V&V Report for this phase.

The NICSD IV&V Team shall prepare a Software Validation Test Report (SVTR). The Software Validation Test Report (SVTR) includes the result of Unit Validation Testing and System Validation Testing.

5.7.4 Test Equipment Software Review

The NICSD IV&V Team shall review the NICSD control of the test equipment software, used in the Unit and System Validation Testing. The NICSD IV&V Team shall review NICSD's records for test equipment software control to ensure that the test equipment software used for the tests is controlled in accordance with NQ-2003 (Reference (26)).

5.7.5 System Validation Testing Phase RTM efforts

(1) Preparation of System Validation Testing Phase RTM

NICSD design engineers perform the System Validation Testing Phase RTM efforts. The RTM efforts ensure the units and system validation test procedures cover all functional requirements defined in the Unit Detailed Design Specifications and the EDS.

(2) Compilation of the System Validation Testing Phase RTM Report

The NICSD IV&V Team shall review the RTM.
The NICSD IV&V Team shall describe the result of RTM review in the V&V Report.

5.7.6 Security Review

The NICSD IV&V Team shall review that the cyber security requirements described in NQ-2037 (Reference (28)) and the SPP (Reference (45)) are correctly reflected in the software life cycles.

The NICSD IV&V Team shall perform independent review (IR) of the test procedures, and SSARs. The NICSD IV&V Team shall also review that appropriate cyber security requirements complying with NQ-2037 and the SPP are included in the test procedures
In addition, the NICSD IV&V Team shall confirm that appropriate security measures are taken in storage of the units and the systems.
The result of Security Review shall be described in the V&V Report.

5.7.7 System Validation Testing Phase V&V Reporting

The NICSD IV&V Team shall prepare the System Validation Testing Phase V&V Report summarizing the V&V activities performed for this System Validation Testing Phase.

The NICSD V&V Report shall include:

(1) Reference to the reviewed documents, including hardware verification, see Section 5.9

(2) Reference to the Design Verification Reports (DVR)

(3) Reference to the units and system validation test report

(4) Reference to the System Validation Testing Phase RTM

(5) Results of the Test Equipment Software Review

(6) Results of the Security Review

(7) Completion of SSAR, which shall confirm that:
- All system safety requirements have been satisfied by the life cycle phases.
- No additional hazards have been introduced by the work done during the life cycle activity.

(8) Metrics described in Section 4.6.6

(9) Evaluation of the test results

(10) Conclusion of the V&V activities

The NICSD IV&V Team delivers the NICSD V&V Report to the ICDD IV&V Team for review.

5.7.8 Baseline Review

To complete the software development, the NICSD IV&V Team shall perform baseline reviews at the phase end as described in Section 4.6.3. ICDD and NICSD shall confirm the completion the V&V activities from the Project Planning and Concept Definition Phase through the System Validation Testing Phase to complete the software development. All open items shall be closed. The NICSD IV&V Team shall issue a BRR documenting the results of the Baseline Review and report to NICSD SQA Team for review and approval as QA record.

5.8 Functional Element V&V

FPGA logic is designed using FEs from the PPDD FE library. The control of these FEs is reviewed in the Design Phase by the NICSD IV&V Team. The IV&V Team shall review the following at a minimum:

- Documentation for the FEs including FE test reports — each FE shall be developed, verified, and validated in accordance with PPDD procedure E-68018 as described below.
- Control of FE library and software tools — FE library and software tools shall be controlled under an appropriate configuration management.

The following subsection provides details of the review.

These FE V&V activities can be omitted for the FE for which PPDD has already performed the same V&V activities, and NICSD or ICDD has performed the same review for another safety-related work.

To prepare an FE used in the FPGA-based system, PPDD shall follow the PPDD procedure E-68018 (Reference (40)) for design and testing, and shall get review and approval from NICSD, including the IV&V Team.

The outline of the procedure prescribed in E-68018 is as follows:

(1) FE Requirements Specification

The FE Requirements Specification is established to address at a minimum:

- FE functional requirements,
- Input/Output Signals, and
- Interface/Interaction with other FE.

The FE Requirements Specification must be verified by other engineers who do not contribute the FE Requirements Specification.

(2) FE Design

The PPDD design engineers establish the FE Specification and the other PPDD design engineers establish the FE Test Procedure. The FE Specification states how all of the

requirements specified in the FE Requirements Specification for this FE will be implemented, and should contain sufficient criteria to support functional testing of the FE.

The FE Test Procedure describes the process from producing the VHDL source code through the execution of FE testing using test FPGA chips.

The FE Specification and FE Test Procedure must be verified by other engineers who do not contribute to the FE Specification or FE Test Procedure.

An RTM is prepared to trace the design features in the FE Specification to the requirements shown in the FE Requirements Specification. The RTM must also be verified.

(3) FE Coding

The PPDD design engineers generate VHDL source code of FEs in accordance with the design rules shown in E-68017 (Reference (39)) Appendix A. The VHDL source code is converted into an FE EDIF File by the Synplify® tool. At this point, the PPDD design engineers perform functional testing of the FE to verify that the FE meets the requirements defined in the FE Specification using the ModelSim® tool.

The FE source code must be reviewed by independent engineers in PPDD who do not contribute to the FE coding.

(4) FE Testing

The PPDD design engineers map FE to FPGA, program FPGA, and perform an FE validation using hardware stimulation of the programmed FPGA.

The PPDD design engineers perform FE testing in accordance with an FE Test Procedure prepared prior to the testing and record the results in an FE Test Report. Another PPDD design engineer evaluates the FE Test Report and record the results of the evaluation.

(5) Final FE Acceptance/Release

The PPDD design engineers propose the registration of the FE in the FE library to the PPDD configuration manager. The PPDD configuration manager confirms that the FE Requirement Specification, FE Specification, FE Test Procedure, and FE Test Reports with a satisfactory result are established, and determines whether the FE is acceptable. When the FE is acceptable, the PPDD configuration manager releases the FE for use, by approving the registration of the FE in the FE library.

The duplicated complete package of electronic files for FEs library that is incorporated into FPGA design is also stored in NICSD controlled storage locker.

(6) Maintenance Phase

FE logic modifications are approved, documented, verified and validated, and controlled. Section 7.1.2 explains PPDD activities for problem reporting.

The verification process for the FE permits a more traceable process than for complete FPGA logic verification. Because of the simplicity of the FE, a shorter simulation is possible, with more thorough verification at this level.

5.8.1 Document Check

The NICSD IV&V Team shall check the following documents to ensure that PPDD procedure E-68018 (Reference (40)) is appropriately applied for FEs placed in the FE library:

- FE Requirements Specification
- FE Specification
- RTM between the FE Specification and the FE Requirements Specification
- FE Test Procedure
- RTM between the FE Specification and the FE Test Procedure
- FE Test Report

The NICSD IV&V Team shall check the documents for the following items:

- FE Specifications, FE Test Procedure and FE Test Reports should be established and checked against FE Requirements Specifications. FE Requirements Specifications should be established and checked against NQ-2032 (Reference (24)).
- The RTMs between documents have been appropriately prepared and reviewed.
- Full pattern tests have been performed for each FE
- The test results are acceptable

The results of the check shall be documented and included in the V&V Report at the Design Phase. See Section 5.4.5.

5.8.2 Check of FE Library Control and Software Tool Control

The NICSD IV&V Team shall check the following items at a minimum, to confirm that PPDD adequately controls the FE library:

- PPDD controls the FE library in accordance with PPDD procedure E-68019 (Reference (41)).
- PPDD controls the software tools in accordance with PPDD procedure E-68020 (Reference (42)). See Section 5.5.7 of this NICSD VVP.

The NICSD IV&V Team shall document the results of the check in the V&V Report at the Design Phase. See Section 5.4.5 of this NICSD VVP.

5.9 Hardware V&V

The NICSD IV&V Team or verifier in NICSD shall perform an independent review of the unit and module hardware design in accordance with NQ-2030 (Reference (22)). The NICSD IV&V Team or verifier in NICSD shall perform an independent review (IR) of ECWD. The results of the review shall be documented and reported as a part of the V&V Report.

6 V&V Reporting

6.1 V&V Report

The NICSD IV&V Team shall prepare the NICSD Verification and Validation Report (VVR), which documents the NICSD activities starting with the Project Planning and Concept Definition Phase and progressing through the System Validation Testing Phase. The NICSD VVR shall be prepared at the Project Planning and Concept Definition Phase, and shall be updated at the end of each life cycle phase. Section 5 describes the contents to be included in the NICSD VVR.

The NICSD IV&V Lead shall approve NICSD VVR.

6.2 Anomaly Reporting

Anomalies found after a version of the software was released or became a baseline, these anomalies shall be controlled in accordance with NQ-3019 (Reference (34)). Anomalies found before the above milestones, such anomalies shall be controlled in accordance with the applicable design control procedures. Normally, anomalies identified during design reviews are controlled per Verification Follow Sheet (VFS) and/or Comment List those referred by Design Verification Report in accordance with AS-200A002 (Reference (7)), and ones during source code reviews are controlled through Source Code Review Sheet and Anomaly List.

The NICSD IV&V Team shall perform independent reviews of documents, which are described in section 5.2.3, 5.3.1, 5.4.2, 5.5.5, 5.6.1, and 5.7.1. For document reviews, the NICSD IV&V Team shall use the Design Verification Report (DVR), which shall include a list of comments to be resolved. Resolution for the open items shall be tracked using a Verification Follow Sheet (VFS) and/or Comment List. The DVR shall be closed with evaluation that all identified issues have been resolved. Closed items at the phase and open items to the next phase shall be verified in each Baseline Review Report (BRR).

For source code reviews, the Source Code Review Sheet shall be used, which is described in section 5.5.1. The Code Review Team shall create an Anomaly List to track identified anomalies. The classification and disposition for each anomaly shall be documented in the Source Code Review Sheet. At the Exit Meetings, the resolution of anomalies in the Source Code Review Sheet shall be verified and the exit decision shall be determine if the Code Review result meet the exit criteria.

For individual FPGAs tests, the IV&V Team shall review the test procedures and test results. The IV&V Team shall use list of comments, and a DVR to record their review. Anomalies shall be tracked with a Verification Follow Sheet. Results shall be summarized in the BRR and resolution of anomalies shall be verified through the Baseline Review Meeting.

For FPGA tests, the IV&V Team shall review the test procedures and test results. The IV&V Team shall use list of comments, and a DVR to record their review. Anomalies shall be tracked with a Verification Follow Sheet. Results shall be summarized in the BRR and resolution of anomalies shall be verified through the Baseline Review Meeting.

Through completion of module testing, the IV&V Team shall review work performed by the design team. After module testing is complete, the IV&V Team shall be responsible for generation and performance of Software Validation Testing.

For Software Validation Testing of Individual Units and of Systems, an IV&V Team member shall generate a written Software Validation Test Plan (SVTP), which is described in section 5.4.1. The design team shall write System Test Specification, which shall be reviewed by the IV&V Team. A member of the Quality Control Group for Nuclear Instrumentation & Control Systems (NICS-QC) shall write Software Validation Test Procedures, and NICS-QC shall perform testing and shall generate Software Validation Test Records. IV&V Team shall issue Software Validation Test Reports based on the Software Validation Test Records. Test anomalies shall be reported to the Design and IV&V Team through the Site Corrective Action Request (SCAR) or Site Nonconformance Notice Report (SNNR) processes. Sections 6.2.1 and 6.2.2 explain the SNNR and SCAR processes and interactions with the Design and IV&V Teams.

6.2.1 Site Nonconformance Notice Report

If an anomaly is found in the FPGA-based Safety-Related I&C systems that will be shipped and used in US nuclear power plants, the anomaly is controlled in accordance with NQ-3019 (Reference (34)). In case that the anomaly is judged nonconforming parts, modules, units or systems (hardware) of which cause is generated by the NICSD, Site Nonconformance Notice Report (SNNR) is issued in accordance with NQ-3019 (Reference (34)). If the anomaly is a result from a design error, the IV&V Team shall send the nonconformance to the NISD group that shall then propose a Technical Justification and disposition. The IV&V Team shall review the Technical Justification and Disposition in the SNNR, and shall send acceptable SNNR responses to the Quality Control Group for Nuclear Instrumentation & Control Systems (NICS-QC) for acceptance of the proposed resolution. Modifications and testing shall be initiated and performed as required, potentially flowing back through many portions of the previous process. NQ-3019 describes the process for resolution of the nonconformance. The IV&V Team shall evaluate each open item and summarize the current status of each SNNR in the VVR. Results shall be summarized in the BRR and resolution of anomalies shall be verified through the Baseline Review Meeting.

Anomalies may be found during validation testing, or in a design used at equipment fabrication.

6.2.2 Site Corrective Action Request

A Corrective Action Request (CAR) is used to document a cause, corrective action to be taken, and to follow corrective action processes, when a condition adverse to quality is identified after the baseline has been established in PCDs. When a condition adverse to quality is found during IV&V activities, the NICSD IV&V team has a responsibility for preparation of SCAR in accordance with AS-300A009 (Reference (15)). And the Quality Assurance Group for Nuclear Instrumentation & Control Systems (NICS-QA) has a responsibility for issuance of SCAR. NICSD Standard NQ-3009 (Reference (15)) is applied. Note that if the anomaly has already been implemented in the product, the NICSD IV&V Team shall report the anomaly to NICS-QC to determine whether a SNNR is to be issued or not.

7 V&V Administrative Requirements

7.1 Anomaly Reporting and Resolution

7.1.1 Problems Found in NICSD Activities

If a problem is identified in the NICSD design or IV&V in any phase including Software Validation Testing, each problem shall be reported using the SNNR or SCAR processes, as described in Section 6.2.

NICSD test personnel perform the System Validation Testing. The test personnel shall document any test failures, any product or configuration nonconformance, or any errors in the test procedure as a nonconformance using the SNNR or SCAR processes. The nonconformance may be resolved by modifying design documentation, logic, test plans or test procedures as necessary. The NICSD IV&V team shall review the revised materials that incorporate the changes. NICSD documents the amount of retest required for these changes, and performs retests as needed to resolve all SNNRs and SCARs The NICSD IV&V team shall confirm that all SNNRs and SCARs are adequately resolved by the end of the System Validation Testing Phase.Problems Found in PPDD Activities

7.1.2 Problems Found in PPDD Activities

The PPDD engineers who perform FPGA or module testing shall document any test failures, any product or configuration nonconformance, or any errors in the test procedure using Problem Reporting Sheets (PRSs) as described in E-68016 (Reference (38)). The PRS may be resolved by modifying design documentation, logic, or test plans and procedures as necessary. The NICSD IV&V Team shall review the revised materials that incorporate the changes and the PRS to confirm that all anomalies are resolved adequately. PPDD document the amount of retest required for these changes, and performs retests as needed to resolve all PRSs. Retests shall go back to PPDD design team.

If PPDD finds any problem in the configuration items during FPGA Testing, or Module Validation Testing after shipment of any module containing the design to NICSD (e.g., when the nonconformance discovered in other PPDD projects is affected to this FPGA products.), PPDD issues a VNNR. NICSD shall control the VNNR in accordance with NQ-3006 (Reference (30)).

7.1.3 Problems Found in Other Vendors' Activities

If any problem is found in NICSD vendor's activities after the vendor's work products have been provided to NICSD or PPDD, the problem shall be considered a vendor nonconformance, and a VNNR is issued in accordance with NQ-3006 (Reference (30)).

7.1.4 Design Change Activities

Change control shall be implemented in accordance with the NICSD SCMP (Reference (50)).

When changes are needed in documents, Document Change Request (DCR) sheet can be used for notification in accordance with NQ-2024 (Reference (21)).

7.2 Activity Iteration Policy

If a design is changed, or a result of test or analysis is changed, the V&V activities that are affected by the change shall be iterated as follows:

- The NICSD IV&V Team shall perform an independent review, or evaluation of the affected documents.
- The extent of the condition shall be analyzed, and all affected work products for NED, NICSD, and PPDD identified and tracked for resolution, which may affect any or all of the design phases.
- The NICSD SD Team shall update the work products, RTM and SSAR to reflect the design change.
- The PPDD engineers shall update the work products and RTM to reflect the design change.
- The NICSD IV&V Team shall perform an independent review of the updated work products, RTM, and SSAR, including evaluation of regression testing requirements.
- Any required retesting activities shall be performed and reviewed by IV&V.
- The NICSD IV&V Team shall update the VVR for the updated work products.
- The NICSD IV&V Team shall prepare a V&V Report for the updated work products.

Note that a change of the RTM for one phase may affect another phase, and the effect can be propagated through the entire lifecycle. The NICSD SD Team shall follow the propagation, and the IV&V Team shall review the changes. The NICSD IV&V Team shall review the changes in the RTM.

7.3 Deviation Policy

If any deviations from this NICSD VVP are required, this NICSD VVP shall be updated using the same review and approval process by which this NICSD VVP was originally created.

The information required for deviations shall identify activities to be deviated, and shall include rationales and effects on software quality.

7.4 Control Procedures

The documents that resulted from the V&V activities shall be controlled in accordance with the NICSD SCMP (Reference (50))

7.5 Standards, Practices and Conventions

The Toshiba Internal Standards in Section 3.4, and project documents in Section 3.6 shall be applied to the V&V activities. The SPP (Reference (45)) is used for guidance. The IEEE standards in Section 3.3 are used as guidance, as endorsed by applicable USNRC regulatory guides.

The Toshiba Internal Standards in Section 3.5 shall be applied to PPDD's activities.

8 V&V Documentation Requirements

8.1 RTM

The RTM traces the base requirements through the life cycle phases, ensuring forward and backward traceability. The NICSD SD Team shall use NQ-2015 (Reference (19)) to prepare the RTM. Also, the PPDD design engineer shall use NQ-2015 required with the procurement specification by the NICSD SD Team to prepare the RTM.

8.2 Test Documents

(1) NICSD Test Documents

The NICSD IV&V Team prepares the test documents for unit validation testing and System Validation Testing, which contain test cases and acceptance criteria, in accordance with the Software Test Plan.

The following procedures are used when creating test documents.

- NQ-2019 (Reference (20))
- NQ-3016 (Reference (33))
- NQ-3015 (Reference (32))

(2) PPDD Test Documents

The PPDD design engineers prepare the FPGA Test Procedures and the Module Test Procedures in accordance with E-68027 (Reference (43)). The PPDD design engineers generate the FPGA Test Reports in accordance with E-68017 (Reference (39)). The PPDD test personnel generate the Module Test Reports in accordance with E-68016 (Reference (38)).

9 VVP Maintenance

The NICSD IV&V Team shall be responsible for the maintaining of this NICSD VVP. The NICSD VVP shall be maintained in accordance with Section 16 of the NICSD SMP (Reference (48)). The updated NICSD VVP shall be prepared, verified and approved in the same manner that the NICSD VVP was first established as a document in accordance with NICSD NQ-2024, "Procedure for Document Control" (Reference (21)). Also the issued NICSD VVP shall be retained as a QA record in accordance with NICSD NQ-3020, "Control Procedure of QA Records" (Reference (35)).

Table A, Compliance to SPP

Table A, Compliance to the SPP

No	SPP Section	Title	VVP Section(s)	Remark
1	4	Software Verification and Validation Program Plan (SVVPP)	N/A	Section Title
2	4.1	Introduction	N/A	No requirement
3	4.1.1	Purpose	1	
4	4.1.2	Scope	1	
5	4.1.3	[Deleted]	N/A	No requirement
6	4.1.4	Relationship of the SVVPP to Other SPP Sections	N/A	No requirement
7	4.2	Verification and Validation Overview	1	
8	4.2.1	Organization	4.1	
9	4.2.2	Schedule	4.2	
10	4.2.3	Resource Summary	4.4	
11	4.2.4	Roles and Responsibilities	4.5	
12	4.2.5	Qualifications	4.4, 4.5	
13	4.2.6	Tools, Techniques, and Methodologies	4.6	
14	4.3	Life Cycle Verification and Validation	5	
15	4.3.1	Management of V&V Activities	5.1	
16	4.3.2	Planning Phase V&V Activities	5.2	
17	4.3.3	Requirements Phase V & V Activities	5.3	
18	4.3.4	Design Phase V & V Activities	5.4	
19	4.3.5	Implementation Phase V & V Activities	5.5	
20	4.3.6	Testing and Integration Phase V & V Activities	5.5, 5.6, 5.7	
21	4.3.7	Installation Phase V & V Activities	5.7	SVT include PFT
22	4.3.8	Operation Phase V & V Activities	N/A	Out of scope
23	4.3.9	Maintenance Phase V & V Activities	N/A	Out of scope
24	4.3.10	Summary of V&V Activities	Table B	
25	4.3.11	Previously Developed or Purchased Software	5.1.3	
26	4.4	V & V Reporting and Administrative Requirements	N/A	Section Title
27	4.4.1	Reporting For Each System or Logical Group of Systems	5.11	
28	4.4.2	Anomaly Reporting and Resolution	6.3, 7.1	

Notice:

The definition of phase for the FPGA-based safety-related systems differs from that in the SPP (Reference (45)), see SMP (Reference (48)).

Table B, V&V Activities Assigned to Each Software Life Cycle Phase

Table B, V&V Activities Assigned to Each Software Life Cycle Phase

Life Cycle Process		Development					
SPP	This NICSD VVP	Project Planning and Concept Definition V&V	Requirements Definition V&V	Design V&V	Implementation and Integration V&V	Module Validation Testing V&V	System Validation Testing V&V
Software Classification		SR	SR	SR	SR	SR	SR
V&V Activities							
Management Review of V&V	Management Review of V&V	PM	PM	PM	PM	PM	PM
SVVP Generation	SVVP Generation	V&V					
Concept Documentation Evaluation	Project Planning and Concept Definition Phase DVR	V&V					
Program Plan Evaluation		V&V					
PFT Plan Generation	Software Test Plan Generation (PFT Plan is included in SVTP)	V&V					
PIT Plan Generation	N/A						
Planning Traceability Analysis	RTM Review	V&V					
Hazard Analysis	N/A (Safety Analysis)	SST	SST	SST	SST	SST	SST
Risk Analysis	N/A	PM	PM	PM	PM	PM	PM
Phase Report	Project Planning and Concept Definition Phase V&V Report	V&V	V&V	V&V	V&V	V&V	V&V
Baseline Reviews	Baseline Reviews	V&V	V&V	V&V	V&V	V&V	V&V
Requirements Traceability Matrix	RTM Review		V&V				
Software Requirements Evaluation	Requirements Definition Phase DVR		V&V				
Software Requirements Interface Analysis			V&V				
Configuration Management Assessment	N/A		DT				
Design Traceability Analysis	RTM Review			V&V			

Table B, V&V Activities Assigned to Each Software Life Cycle Phase

Life Cycle Process		Development					
SPP	This NICSD VVP	Project Planning and Concept Definition V&V	Requirements Definition V&V	Design V&V	Implementation and Integration V&V	Module Validation Testing V&V	System Validation Testing V&V
Software Design Evaluation	Design Phase DVR			V&V			
Software Design Interface Analysis				V&V			
Unit Test Plan Generation	System Validation Test Plan Generation			V&V(Test personnel)			
Integration Test Plan Generation				V&V(Test personnel)			
System Validation Test Plan Generation				V&V(Test personnel)			
SVT Test Case Generation				V&V(Test personnel)			
PFT Test Case Generation				V&V(Test personnel)			
PIT Test Case Generation	N/A						
Source Code Traceability Analysis	VHDL Source Code Review				V&V		
Source Code Evaluation					V&V		
Source Code Interface Analysis					V&V		
Unit and Integration Test Case Generation	Implementation and Integration Phase DVR				PPDD(prepare V&V(review)		
Unit, Integration, and SVT Test Procedure Generation					PPDD(prepare V&V(review)		
Operation and Maintenance Manual Review					V&V		
Unit and Integration Test Execution					STT		
Software Release Report	Implementation and Integration Phase and System Validation Phase DVR				V&V		V&V
Test Traceability Analysis	RTM Review					V&V	V&V

Table B, V&V Activities Assigned to Each Software Life Cycle Phase

Life Cycle Process		Development					
SPP	This NICSD VVP	Project Planning and Concept Definition V&V	Requirements Definition V&V	Design V&V	Implementation and Integration V&V	Module Validation Testing V&V	System Validation Testing V&V
PFT Procedure Generation	System Validation Test Procedure Generation					V&V(Test personnel)	V&V(Test personnel)
SVT Execution	SVT Execution (including PFT)					V&V(Test personnel)	V&V(Test personnel)
PFT Execution						V&V(Test personnel)	V&V(Test personnel)
PIT Execution	N/A						
Installation Configuration Audit	N/A						
Installation Checkout	N/A						
V&V Final Report Generation	Final V&V Report Generation						V&V
Evaluation Of New Constraints	N/A						
Operation Procedures Evaluation	N/A						
Proposed Change Assessment	N/A						
SVVP Revision	N/A						
Anomaly Evaluation	N/A						
Migration Assessment	N/A						
Retirement Assessment	N/A						
Task Iteration	N/A						
Regression Analysis	N/A						

SR = Safety related

empty cell = process is not applied

CCB=Change Control Board
CM=Configuration Management Lead
DT=Software Development Team

PM=Project Manager, may be two separate PM, one responsible for design/development and responsible for V&V
SSL=Software Safety Lead
SST=Software Safety Team

V&V=V&V Lead
SIT=System Installation Test Team
STT=Software Test Team

PSNN-2016-0382

■Safety-Related
□Non-Safety-Related
□ASME CODE
□Others ( )

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Project	NRW-FPGA-Based I&C System Qualification Project
Contract No.	---

X	For Approval		For Information

Action		
A	X	Approved No Further Action
C		Approved with Comment Revised and Resubmit
D		Disapproved Revised and Resubmit
I		Accepted for Information Only ☐ Recommendation Included

Group: Monitoring System Engineering Group	
Approved by	Reviewed by
N. Oda 06-Jul-2016	T. Miyazaki Jul 5, 2016

Approval by buyer does not release seller of his obligation to furnish all goods and services in strict conformance with all of the terms of the Purchase Order.

TOSHIBA CORPORATION NED

NRW-FPGA-Based I&C System Qualification Project

Software Quality Assurance Plan

Title: Nuclear Instrumentation & Control Systems Department Software Quality Assurance Plan for FPGA-based Safety-Related Systems

Customer Name	None
Project Name	NRW-FPGA-Based I&C System Qualification Project
Item Name	None
Item Number	A32
Job Number	9P04482
Applicable Plant	None

TOSHIBA NICSD verified this Document;

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3	See cover page	See cover page	See cover page	See cover page	See cover page

Table of Contents

1 Introduction

1.1. Purpose

This Nuclear Instrumentation & Control Systems Department (NICSD) Software Quality Assurance Plan (NICSD SQAP) describes the software quality assurance plan that NICSD utilizes to develop and procure the Field Programmable Gate Array (FPGA)-based safety-related Instrumentation and Control (I&C) systems for US nuclear power plant.

This NICSD SQAP defines an additional software Quality Assurance (QA) requirements that shall be applied to the systems and equipment. This NICSD SQAP complies with and supplements an existing Quality Assurance Program Description (QAPD) of Toshiba Corporation, Power Systems Company, Nuclear Energy (PSNE), AS standards of Nuclear Energy Systems & Services Division (NED), and NICSD NQ standards to implement all safety-related activities. The requirements provided herein augment the PSNE QAPD.

1.2. Background

This NICSD SQAP is developed for the FPGA-based safety-related I&C systems based on a description of Section 5 of the "Software Program Plan" (SPP) (Reference (8)), and in accordance with the NICSD Standard NQ-2038 "Preparation Procedure for Software Quality Assurance Plan" (Reference (42)).

NED procures the FPGA-based safety-related I&C equipment from NICSD in the Fuchu Complex. NICSD procures the FPGA-based modules from Power Platform Development Department (PPDD) as commercial grade items for the equipment. NICSD has a quality assurance program in accordance with 10 CFR 50 Appendix B requirements. PPDD has a quality assurance program in accordance with ISO-9001. The process for obtaining commercial grade items is described in Section 10 of the NICSD Standard NQ-2030 "Procedural Standard for FPGA Products Development" (Reference (34)). This NICSD SQAP describes the software quality assurance activities performed by NICSD, including the Commercial Grade Dedication (CGD) activities used to designate commercial grade items from PPDD for use in safety-related applications, and to determine compliance with the requirements of SPP.

As described in the "Nuclear Energy Systems and Services Division FPGA-based Safety-Related Systems Software Management Plan" (NED SMP) (Reference (9)), NED performs a limited part of the software life cycle of FPGA-based safety-related systems and, the NED SMP covers their activities including software quality assurance. Therefore this SQAP does not include NED's life cycle and their activities.

The NICSD SQAP sections are prepared to comply with the life cycle activities described in Section 13 of the "Nuclear Instrumentation & Control Systems Department Software Management Plan for FPGA-based safety-related I&C Systems" (NICSD SMP) (Reference (10)) and, using the IEEE Std 730 (Reference (2)) as a guide. Figure 13-1 of the NICSD SMP shows a simplified diagram of the process flow through the life cycle phases for the FPGA-based systems.

1.3. Scope

This NICSD SQAP shall be applied to the software quality assurance activities from the Project Planning and Concept Definition Phase through the Retirement Phase in the software life cycle for the FPGA-based safety-related I&C systems.

The "Software Program Plan" (SPP) (Reference (8)) establishes requirements and provides guidance and expectations for the design, development, implementation, safety analysis, review, testing, installation, and configuration management etc. This NICSD SQAP covers Section 5 "Software Quality Assurance Program Plan" (SQAPP) of the SPP.

Table A in Appendix B shows the compliance traceability matrix of this SQAP to the SPP.

The NICSD SQAP provides the following information:

- A description of the project software quality assurance planning measures to be used to demonstrate how the project requirements are met. NICSD's basic approach is described in this NICSD SQAP.
- A determination of the Software Integrity Level (SIL) for the types of software is covered by this SQAP. See IEEE Std.1012 (Reference (5)) for the SIL levels to be used for various types of software.

This NICSD SQAP addresses QA activities in the software life cycle defined in the NICSD SMP (Reference (10)). The following software are excluded from the requirements of this SQAP:

- Administrative software used for the purposes of ordering, scheduling, and project management.
- Commercial applications software for use in database management systems, word processing, and commercially purchased Computer Aided Design (CAD) systems not used for FPGA development (for example, Excel, Word, AutoCAD, and electrical schematic drawing tools).

2 Abbreviations

AS	Toshiba Nuclear Energy Systems and Services Division Work Standard
BRR	Baseline Review Report
CAD	Computer Aided Design
CDI	Commercial Dedication Instruction
CG	Commercial Grade
CGD	Commercial Grade Dedication
CGS	Commercial Grade Survey
COTS	Commercial Off-the-Shelf Software
DCR	Documents Change Request
DR	Design Review
DVR	Design Verification Report
EPC	Engineering, Procurement, and Construction
FE	Functional Element
FPGA	Field Programmable Gate Array
FTER	Final Technical Evaluation Report
Fuchu-PS	Fuchu Complex Power Systems Segment
GPM	Group Manager
I&C	Instrumentation and Control
IEEE	Institute of Electrical and Electronics Engineers
IR	Independent Reviewer
ISO	International Standardization Organization
IV&V	Independent Verification and Validation

IV&V Lead	Independent Verification and Validation Lead
NED	Nuclear Energy Systems & Services Division
NICSD	Nuclear Instrumentation & Control Systems Department
NICS-QA	Quality Assurance Group for Nuclear Instrumentation & Control Systems
NICS-QC	Quality Control Group for Nuclear Instrumentation & Control Systems
NISD	Nuclear Instrumentation Systems Development & Designing Group
NQ	Nuclear Quality
PDS	Previously Developed Software
PFT	Platform Factory Test
PM	Project Manager
PPDD	Power Platform Development Department
PRM	Process Review Meeting
PRS	Problem Reporting Sheet
PSNE	Power Systems Company, Nuclear Energy
PTER	Preliminary Technical Evaluation Report
QA	Quality Assurance
QAPD	Quality Assurance Program Description
QC	Quality Control
QVL	Qualified Vendor List
RG	Regulatory Guide
RTM	Requirements Traceability Matrix
SCAR	Site Corrective Action Request
SCL	Software Configuration Lead
SCMP	Software Configuration Management Plan
SD	Software Development
SD Team	Software Development Team
SDL	Software Development Lead
SDOE	Secure Development and Operational Environment
SIL	Software Integrity Level
SMP	Software Management Plan
SNNR	Site Nonconformance Notice Report
SPP	Software Program Plan
SQ	Software Quality
SQA	Software Quality Assurance
SQA Team	Software Quality Assurance Team
SQAL	Software Quality Assurance Lead
SQAP	Software Quality Assurance Plan
SQAPP	Software Quality Assurance Program Plan
SS	Software Safety
SS Team	Software Safety Team
SSAR	Software Safety Analysis Report
SSL	Software Safety Lead
SSP	Software Safety Plan
SVTP	Software Validation Test Plan
SVTR	Software Validation Test Report
SVVP	Software Verification and Validation Plan
USNRC	United States Nuclear Regulatory Commission
V&V	Verification and Validation
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VNNR	Vendor Nonconformance Notice Report
VVP	Verification and Validation Plan
VVR	Verification and Validation Report

3 Reference Documents

(1) USNRC, RG 1.169,
"Configuration Management Plans for Digital Computer Software Used in Safety Systems of Nuclear Power Plants" , Revision 0

(2) IEEE Std. 730-2002,
"IEEE Standard for Software Quality Assurance Plans"

(3) IEEE Std. 828-1990,
"IEEE Standard for Software Configuration Management Plans"

(4) IEEE Std. 829-1983,
"IEEE Standard for Software Test Documentation"

(5) IEEE Std. 1012-1998,
"IEEE Standard for Software Verification and Validation Plans"

(6) Not used

(7) Toshiba Project Document Number FA10-0301-0001,
"Project Specific Document Control Procedure", Rev.0,

(8) Toshiba Project Document Number FA10-0501-0024
"Software Program Plan" Rev.1,

(9) Toshiba Project Document Number FA32-3702-0005,
"Nuclear Energy Systems and Services Division FPGA-based Safety-Related Systems Software Management Plan" Rev.2,

(10) Toshiba Project Document Number FA32-3702-1000,
"Nuclear Instrumentation & Control Systems Department Software Management Plan for FPGA-based Safety-Related Systems" Rev.2,

(11) Toshiba Project Document Number FA32-3708-1000
"Nuclear Instrumentation & Control Systems Department Software Configuration Management Plan for FPGA-based Safety-Related Systems" Rev.1,

(12) Toshiba Project Document Number FA32-3709-1000,
"Nuclear Instrumentation & Control Systems Department Verification and Validation Plan for FPGA-based Safety-Related Systems" Rev.7,

(13) Toshiba Corporation Power Systems Company Nuclear Energy Regulations and Procedures 4810, "REPORTING PROCEDURE FOR DEFECTS AND NONCOMPLIANCE UNDER USNRC 10CFR21"

(14) Toshiba Nuclear Energy Systems and Service Division AS-200A002,
"Design Verification Procedure"

(15) Toshiba Nuclear Energy Systems and Service Division AS-200A128,
"Digital System Life Cycle Procedure"

(16) Toshiba Nuclear Energy Systems and Service Division AS-200A129,
"Digital System Development Procedure."

(17) Toshiba Nuclear Energy Systems and Service Division AS-200A130,
"Digital System Verification & Validation Procedure"

(18) Toshiba Nuclear Energy Systems and Service Division AS-200A131,
"Digital System Configuration Management Procedure"

(19) Toshiba Nuclear Energy Systems and Service Division AS-200A132,
"Digital System Safety and Hazards Analysis Procedure"

(20) Toshiba Nuclear Energy Systems and Service Division AS-300A005
"Preparation Procedure for Source Verification Report"
(21) Toshiba Nuclear Energy Systems and Service Division AS-300A009,
"Corrective Action Request Application Procedure"
(22) Toshiba Nuclear Instrumentation & Control Systems Department NQ-1002,
"Standard of Organization for Fuchu-PS Nuclear Quality Assurance"
(23) Toshiba Nuclear Instrumentation & Control Systems Department NQ-1003,
"Application of AS Standards"
(24) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2001,
"Process Review Meeting Convening Standard"
(25) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2003,
"Procedure for Control of Software Tools"
(26) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2004,
"Preparation Procedure for Equipment Design Specification"
(27) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2013,
"Preparation Guide for Verification and Validation Plan"
(28) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2014,
"Preparation Guide for V&V Report"
(29) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2015,
"Preparation Procedure for RTM and RTM Report"
(30) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2019,
"Preparation Procedure for Test Specification"
(31) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2024,
"Document Control Procedure"
(32) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2025,
"Preparation Procedure for Procurement Document for CG Items & Services"
(33) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2026,
"Control Procedure of supplier generated documents"
(34) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2030,
"Procedural Standard for FPGA Products Development"
(35) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2031,
"Procedural Standard for FPGA Device Development"
(36) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2032,
"Procedural Standard for Functional Element Development"
(37) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2033,
"Procedural Standard for FPGA Configuration Management"
(38) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2034,
"Procedural Standard for Control of Software Tools Used with FPGA Based Systems"
(39) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2035,
"Procedure for Design Change Control"
(40) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2036,
"Procedure for Design Control"
(41) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2037,
"Cyber Security Procedures of Safety Related Digital System"
(42) Toshiba Nuclear Instrumentation & Control Systems Department NQ-2038,
"Preparation Procedure for Software Quality Assurance Plan"
(43) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3005,
"Procedure for Evaluation of Suppliers"
(44) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3006,
"Procedure for Control of Nonconforming Procurement Items and Services"
(45) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3009,
"Corrective Action Request Application Procedure"

(46) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3015, "Test Control Procedure"
(47) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3016, "Software Test"
(48) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3019, "Procedure for Control of Nonconformance and Corrective Action"
(49) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3020, "Control Procedure of QA Records"
(50) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3022, "Internal Audit Procedure"
(51) Toshiba Nuclear Instrumentation & Control Systems Department NQ-3023, "Procedure for Purchase"
(52) Toshiba Nuclear Instrumentation & Control Systems Department NQ-4001, "Commercial Grade Dedication"
(53) Toshiba Fuchu Complex Power Systems D-81018, "Procedure for Control of Cyber Security"
(54) Toshiba Fuchu Complex Power Systems D-81030, "Standard for Document System"
(55) Toshiba Power Platform Development Department E-68007, "DR control procedure"
(56) Toshiba Power Platform Development Department E-68016, "PPDD Procedural Standard for FPGA Products Development"
(57) Toshiba Power Platform Development Department E-68017, "Procedural Standard for FPGA Device Development"
(58) Toshiba Power Platform Development Department E-68018, "Procedural Standard for Functional Element Development"
(59) Toshiba Power Platform Development Department E-68019, "Procedural Standard for Configuration Management"
(60) Toshiba Power Platform Development Department E-68027 "Test Specification Preparation Standard"

Notice: Upon application of above NED, NICSD, and other Toshiba internal standards, the latest version shall be used.

4 Management

This section describes the project's organization structure, roles, and responsibilities.

4.1. Organization

The organization's responsibility for development of the FPGA-based systems software design is described in Section 5.1 of the NICSD SMP (Reference (10)).

NICSD has two quality assurance groups. The NICS-QA group is responsible for ensuring process as Staff QA. The NICS-QC group is responsible for ensuring items as the line QA/QC group defined in the NICSD Standard NQ-1002 "Standard of Organization for Fuchu-PS Nuclear Quality Assurance" (Reference (22)). For software quality assurance activities, both of these groups work together as a Software QA (SQA) Team which is organizationally independent from the NICSD Software Development Lead (SDL) and Software Development (SD) Team. NICS-QA performs verification of the software design activities through an internal audit, Commercial Grade (CG) survey, and software surveillance of the NICSD Independent Verification and Validation (IV&V) Team. And NICS-QC performs more direct validation of items, such as oversight, witness, receiving inspection, test, and inspection. NICSD organizes an IV&V Team for the V&V of the

FPGA software. The NICSD IV&V Team ensures the software design activities independently from the NICSD SDL and SD Team. The organization and responsibility of the NICSD IV&V Team is described in the "Nuclear Instrumentation & Control Systems Department Verification and Validation Plan for FPGA-based Safety-Related Systems" (NICSD VVP) (Reference (12)).

4.2. Responsibilities

The NICSD Software QA Lead (SQAL) who is assigned by the NICSD Project Manager (PM) is responsible for conducting the activities described in the following subsections. The NICSD SQAL has an authority to assign the NICSD SQA Team members. The NICSD SQAL is responsible to provide QA trainings to NICSD personnel in the project. The NICSD SQAL shall be responsible for implementing this SQAP and, shall verify that a schedule and resources are adequate to ensure that required SQAPP of SPP (Reference (8)) and the NICSD SMP (Reference (10)) can be provided throughout the life cycle. The NICSD SQAL who is responsible for the personnel implementing this SQAP shall also verify that the processes defined in this SQAP are effective, adequate, suitable, and sufficient, by correcting and extending the SQAP as required to ensure that the SQAPP of SPP and NICSD SMP objectives are met. The NICS-QA Group Manager takes a role of the NICSD SQAL, unless the NICSD PM assigns someone else.

4.2.1. Responsibilities for FPGA-based Safety-Related I&C Systems Life Cycle

The software life cycle of the FPGA-based safety-related I&C systems is defined in Section 13 of NICSD SMP (Reference (10)). As described in the NICSD SMP, the software life cycle is implemented by NED, NICSD, and PPDD. And as mentioned in Section 1.2 of this SQAP, the portion of the software life cycle performed by NED is outside the scope of this SQAP. NICSD performs "Project Planning and Concept Definition Phase", "Requirements Definition Phase", "System Validation Testing Phase", and "Operations and Maintenance Phase". PPDD effort is during the "Design Phase", "Implementation and Integration Phase", and "Module Validation Testing Phase". Although PPDD effort is performed under the CGD process in NICSD, it is inspected by through safety activities of NICSD as discussed and dedicated through an approved CGD process. NICSD has a responsibility to review and approve the PPDD activities through CGD and IV&V activities throughout the course of PPDD's work.

The NICSD SQAL has a responsibility to ensure that the FPGA-based safety-related I&C systems life cycle is correctly and sufficiently performed.

The NICS-QA conducts internal audits of each organization inside NICSD in accordance with the NICSD Standard NQ-3022 "Internal Audit Procedure" (Reference (50)), at least once a year. When the subject of an audit includes FPGA-based safety-related I&C systems, the NICSD SQAL should be the audit leader, or at least, the audit team shall include the NICSD SQA Team member. The audit team shall verify adequacy of the activities performed under the software life cycle, by checking objective evidence using written checklists reviewed by the NICSD SQAL. The checklists shall be based on the requirements of the procedural software plans which are the NICSD SMP, the "Nuclear Instrumentation & Control Systems Department Software Configuration Management Plan for FPGA-based Safety-Related Systems" (NICSD SCMP) (Reference (11)), the NICSD VVP (Reference (12)), and this SQAP, to the life cycle phase and activity being audited. The NICSD SQA Team shall participate in Process Review Meeting (PRM) convened in accordance with the NICSD Standard NQ-2001 "Process Review Meeting Convening Standard" (Reference (24)) to oversee the adequate activities under the life cycle. In addition to participating in the PRMs, the NICSD SQAL will conduct a software surveillance of the NICSD IV&V Team activities at the end of each life cycle phase, to confirm the correctness and sufficiency of the verification activities performed by them. In the software surveillance, the NICSD SQA Team shall review the Design Verification Reports (DVRs) prepared by Verifier and/or Independent Reviewer (IR) in

accordance with the NED Standard AS-200A002 "Design Verification Procedure" (Reference (14)) and, Verification and Validation Reports (VVRs), and Baseline Review Reports (BRRs) prepared by the NICSD IV&V Team. And if necessary, The NICSD SQAL will conduct a direct surveillance for the NICSD IV&V Team to confirm that the IV&V and Baseline Review activities are performed appropriately in accordance with applicable procedures and plans.

The NICS-QA shall conduct a CG Survey of PPDD when required by a Commercial Dedication Instruction (CDI) in accordance with the NICSD Standard NQ-4001 "Commercial Grade Dedication" (Reference (52)). The NICSD SQAL should be the CG survey leader, or at least, the CG survey team shall include the NICSD SQA Team member In the CG Survey, the survey team shall verify capability of PPDD to control Critical Characteristics identified by the CDI. The documentation process of PPDD should be one of the Critical Characteristics for the digital items, and the CG Survey team shall verify it. This CG Survey could support the IV&V activities to verify documents prepared by PPDD in each life cycle phase, and the NICSD SQAL to confirm the results of the IV&V activities. The NICSD SQA Team shall participate in the Design Review (DR) Meeting(s) convened by the PPDD in accordance with the PPDD Standard E-68007 "DR control procedure" (Reference (55)) to oversee the PPDD work in each life cycle phase.

The NICS-QC shall be responsible to verify and validate that the products from PPDD are correctly manufactured and tested without discrepancies.

4.2.2. Responsibilities for Using FEs

As described in Section 11 of the NICSD SMP (Reference (10)), NICSD treats the FPGA logic as "Previously Developed Software (PDS)", and treats the Functional Elements (FEs), which constitute the FPGA logic, as "Commercial Off-the-Shelf Software (COTS)." Both of FPGA logic and FEs are developed by PPDD. NICSD procures the FPGA-based modules which include the FPGA logic comprised of FEs from PPDD. NICSD will not modify any FPGA logic and FEs of its own accord. The specific requirements for using FEs are described in Section 11.1 of this SQAP. The procedure for control of FEs developed by PPDD is documented in the PPDD Standard E-68018 "Procedural Standard for Functional Element Development" (Reference (58)).

The NICSD IV&V Team is responsible to ensure that all documentation including records and associated data regarding FEs, which demonstrates the traceability to products, are prepared and controlled in PPDD and they have no nonconformance.

The NICSD SQA Team is responsible to ensure the adequacy of FE controlled by PPDD in accordance with their procedures throughout the CG Survey and the oversight of PPDD.

The NICSD SQA Team is also responsible for overseeing the NICSD IV&V Team activities over PPDD as described in Section 4.2.1.

4.2.3. Responsibilities for Using Software Tools

The NICSD SDL is responsible to list all software tools for NICSD use in the NICSD SMP (Reference (10)).

The NICSD SDL controls software tools used for software development and implementation in accordance with the NICSD Standard NQ-2034 "Procedural Standard for Control of Software Tools Used with FPGA Based Systems" (Reference (38)). The NICSD PM or the NISD GPM and/or SDL verifies that all of used software tools are listed in the NICSD SMP.

The NICSD SDL is responsible to specify the software tools and their revisions to be used for manufacturing of FPGA modules for the FPGA-based safety-related I&C systems in a job order to PPDD.

The NICSD SQA Team shall be responsible to ensure that the CGD based procurement process is correctly conducted and the acceptance of the product is performed correctly.

4.2.4. Responsibilities for Test Equipment Software

The NICSD SDL is responsible for identifying and verifying the Test Equipment software used for special testing for commercial grade items, hardware acceptance testing, and factory acceptance testing. The NICSD IV&V Lead is responsible for identifying and verifying the Test Equipment software used for software testing including FPGA Testing, Module Validation Testing, and System Validation Testing. The NICSD SDL and NICSD IV&V Lead verify that testing documents specify the identification of Test Equipment software. The NICSD SDL and NICSD IV&V Lead is responsible to confirm that the specified Test Equipment software is used at each test. The NICSD IV&V Team shall also confirm the usage of the Test Equipment software at the FPGA testing and Module Validation Testing through oversight of PPDD test activity. The NICS-QC test personnel shall use the Test Equipment software as specified by the test documents. The NICSD SDL and NICSD IV&V Lead are responsible for reviewing the test reports.

The NICSD SQA Team shall be responsible to ensure that adequate control is in place and used for the Test Equipment software. The CG Survey team that assigned by the NICS-QA Group Manager shall verify an adequacy of the PPDD control process of Test Equipment software when it is identified as a Critical Characteristic of FPGA module. The NICS-QA Group Manager shall approve the CG Survey report when acceptable. The NICSD SQA Team shall also check the results of verification of the procurement documents and testing documents performed by the NICSD SD Team and NICSD IV&V Team.

If NICSD or PPDD uses any Test Equipment software, the following activities shall be performed:

- Defining the Test Equipment software functions required in the project
- Establishing the Test Equipment software acceptance criteria
- Establishing the procedure to use the Test Equipment software
- Training and recording for a personnel to use the Test Equipment software.

These activities shall be described in appropriate Test Documents.

For PPDD activities, NICSD has a responsibility to review and approve the PPDD activities through CG survey, and through V&V activities to be performed throughout the course of PPDD's work. The V&V activities are described in the NICSD VVP (Reference (12)). The V&V activities in general include oversight to PPDD activities, in-process monitoring and, document reviews, etc.

5 Documentation

This section identifies the documentation governing the development, verification and validation of the software. Table-A of the NICSD SMP (Reference (10)) describes an outline of the output document required for software life cycle activities. This section addresses the QA related documentation.

5.1. Software Plans

The NICSD SD Team and Software Safety (SS) Team prepare an NICSD SMP including Software Safety Plan (SSP), the NICSD Software Configuration Lead (SCL) prepares an NICSD SCMP, and

the NICSD IV&V Team prepares an NICSD VVP respectively. The NICS-QA shall verify that these software plans are prepared in accordance with applicable requirements in the SPP. Revisions to these software plans will be recommended in a verification conducted by the NICS-QA using the measure of corrective action requirement, and also the internal audit team will make such recommendation as necessary at the conclusion of each audit.
Revision of these software plans shall be in accordance with Section 16 of the NICSD SMP (Reference (10)).

5.2. Audits, Surveillances and Commercial Grade Surveys

The NICS-QA will conduct the Internal Audit for each organization in the NICSD once a year as defined in NQ-3022 (Reference (50)). In addition to the NICSD Internal Audit, the NICSD SQAL also conducts the NICSD software surveillance at the end of the every software life cycle defined in the NICSD SMP (Reference (10)).
The NICS-QA conducts evaluation of the performance and capability of the PPDD and qualifies the PPDD as a Commercial Grade Supplier. The qualification of the PPDD is effective for three years and is continued by triennial Commercial Grade Survey (CGS). And between the CGS, the qualification is verified by annual evaluations performed in the year other than the year of the CGS. Additionally, the NICSD can request the NICS-QA to conduct the CGS as needed.
The V&V activities in general include oversight, in-process monitoring, document reviews, etc. The NICSD QA Team reviews the documentation of the V&V activities performed by the NICSD IV&V Team in accordance with the NICSD VVP (Reference (12)).
If required by the NICSD SD Team, the source verification performed by the NICS-QC will be applied for witness of FPGA program writing into FPGA chips, and monitoring of the DR Meeting(s) held by the PPDD. These activities will be verified recurrently for each order by the NICSD.

5.3. Report Documentation

The NICS-QA and/or the NICSD SQA Team will prepare the following reports in every audit, software surveillance, and CG Survey and evaluation. The audit reports, surveillance reports, CG Survey reports, and relating Fuchu Site Corrective Action Requests (SCARs) prepared in accordance with the NED Standard AS-300A009 "Corrective Action Request Application Procedure" (Reference (21)), shall be submitted to the NICS-QA manager for review. NICSD Standard NQ-3009 (Reference (45)) is applied instead of AS-300A009 after September 1, 2012 when it became available. The Internal Audit Report, the Software Surveillance Report, and the CG survey report prepared in the life cycle phase shall be subject of baseline review of the life cycle phase as described in the "Nuclear Instrumentation & Control Systems Department Software Configuration Management Plan for FPGA-based Safety-Related Systems" (NICSD SCMP) (Reference (11)).

- NICSD Internal Audit Report
  The NICS-QA will issue the Internal Audit Reports in accordance with NQ-3022 (Reference (50)) when they completed the annual NICSD Internal Audit.
- Software Surveillance Reports
  These reports will be prepared for the software life cycle phases when implemented using the same format as the Internal Audit Report.
- CGS Reports for the PPDD
  The NICS-QA will issue the Commercial Grade Survey reports in accordance with the NICSD Standard NQ-3005 "Procedure for Evaluation of Suppliers" (Reference (43)) when they conducted the CGS.
- Source Verification Report for the PPDD
  The NICS-QC will issue the Source Verification Reports in accordance with the NED Standard AS-300A005 "Preparation Procedure for Source Verification Report" (Reference

(20)) when they conduct a source verification of performance and capability of the PPDD, such as a witness of FPGA program writing into FPGA chips, and a monitoring of the DR Meeting held by the PPDD.

6 Standards, Practices, Conventions, and Metrics

An overview of the NICSD QA Program is provided in the NICSD SMP Section 6.1 (Reference (10)).

This section describes the standards, practices, and conventions to be applied to the FPGA-based safety-related I&C Systems. It identifies general statistical techniques and metrics to be applied in the quality assurance process.

A compliance with these standards shall be monitored and assured through a review and audit process described in Section 7.

6.1. Documentation Standards

All documents developed by the NICSD shall comply with the requirements in the NICSD Standard NQ-2024 "Document Control Procedure" (Reference (31)).

6.2. Design Standards

All design work developed by the NICSD shall comply with the requirements described in the NICSD Standard NQ-2036 "Procedure for Design Control" (Reference (40)).

6.3. Coding Standards

The software development process shall provide guidance to ensure standardization, compatibility, and maintainability of resulting software products. The process shall provide a coding standard for each language as well as usage guidelines for each software tool.

- VHDL source coding of the PPDD should conform to the PPDD Standard E-68017 "Procedural Standard for FPGA Device Development" (Reference (57)).
- The NICSD design team evaluates in the Preliminarily Technical Evaluation Report (PTER) that the coding guidance in the PPDD is acceptable. The NICSD has its own coding guideline document, the NICSD Standard NQ-2031 "Procedural Standard for FPGA Device Development" (Reference (35)) that is used in the evaluation.

6.4. Testing Standards

The NICSD IV&V Team prepares a Software Validation Test Plan (SVTP) for the validation testing that may include a Platform Factory Test (PFT) of the FPGA-based systems, based on the NICSD VVP (Reference (12)). The NICSD IV&V Team also prepares the test documents for unit validation testing and System Validation Testing, which contain test cases and acceptance criteria, in accordance with the SVTP, the NICSD Standard NQ-2019 "Preparation Procedure for Test Specification" (Reference (30)), the NICSD Standard NQ-3015 "Test Control Procedure" (Reference(46)), the NICSD Standard NQ-3016 "Software Test" (Reference (47)) and the NICSD VVP (Reference (12)).

The procurement document for the PPDD describes the requirements for the testing which are conducted by the PPDD in the following software life cycle phases defined in the NICSD SMP (Reference (10)). Testing documents prepared by the PPDD are verified by the NICSD IV&V Team in accordance with the NICSD VVP.

- Implementation and Integration Phase
- Module Validation Testing Phase

Testing of FPGAs and modules developed by the PPDD in the above phases shall comply with the requirements described in the PPDD Standard E-68027 "Test Specification Preparation Standard" (Reference (60)) with special provisions to be specified in the Job Order by the NICSD.

Complying to the instruction through CDI by the NICSD SD Team, the NICS-QA shall conduct a CG Survey for the PPDD in order to evaluate a capability of the PPDD to implement FPGA Testing and Module Validation Testing adequately. In the CG Survey, the survey team shall verify procedures for testing, including E-68027, performance and documentation in accordance with these procedures. The successful CG Survey allows the NICSD to accept the test results by the PPDD.

The NICSD IV&V Team verifies and approves the testing documents prepared by the PPDD through the IV&V activities prior to implementation of the test, and evaluate the test result to accept as a result of the validation testing after completion of the test. The NICSD SQAL shall confirm an adequacy of the NICSD IV&V Team activities by checking a documentation of verification result.

6.5. Acceptance Criteria for the Functional Elements (FEs)

As described in Section 4.2.2 of this NICSD SQAP, the FPGA-based modules incorporating the FEs, which are treated as COTS, are procured by the NICSD from the PPDD through the CGD process. The NICS-QA verifies that the control process of the FE is acceptable to the NICSD for use in the FPGA-based modules by conducting the Commercial Grade Survey (CGS) of the PPDD per request from the SDL, prior to the acceptance of the FPGA-based modules from the PPDD.

In this CGS, the NICS-QA shall verify that the PPDD procedure for the FE development is equivalent to and complies with the NICSD Standard NQ-2032 "Procedural Standard for Functional Element Development" (Reference (36)). The CGS team will verify a documentation and configuration control status of the FEs in compliance with verified PPDD procedures. The NICSD IV&V Team shall verify that the FEs are properly implemented in the FPGA through their activities over the PPDD. The NICSD SQAL shall oversee an activities of the NICSD IV&V Team by checking their results.

6.6. Metrics

The NICSD SQAL shall be responsible for defining, implementing, collecting, analyzing, and overseeing metrics data for the FPGA-based modules.
The following metrics shall be maintained:

- The errors discovered during FPGA Testing and the Module Validation Testing by the PPDD shall be identified through the use of Problem Reporting Sheets (PRS) (see Section 7.1.2 of the NICSD VVP (Reference (12))) so that the number of errors discovered can be tracked for an error discovery metric reporting. The overall goal is to identify a decreasing number and severity of errors, as the testing progresses.
- The errors discovered during System Validation Testing and Unit Validation Testing conducted by the NICSD shall be identified through the use of Fuchu Site Nonconformance Notice Report (SNNR) (see Section 9.1) so that the number of errors discovered can be

tracked for the error discovery metric reporting. The overall goal is to identify a decreasing number and severity of errors as the testing progresses.

- Each PRS and SNNR shall be recorded with identification number and date in the log.
- In cases where the problem was caused by either the NICSD or the PPDD could not be readily determined, the NICSD has a responsibility to determine the responsible organization.

Metrics that are demonstrated to be of no value shall be abandoned, or if necessary, shall be replaced with metrics that have a value to ascertaining process compliance.

7 Software Reviews

The purpose of this section is to address the review requirements throughout the software life cycle. Reviews are designed to ensure that software documentation and processes comply with the procedures, established standards, and guidelines. Reviews are technical in nature and are designed to verify technical adequacy and completeness of the design and development of software. The NICSD IV&V Team is responsible for software review. Methodologies of performing reviews are described in the NED Standard AS-200A130 "Digital System Verification & Validation Procedure" (Reference (17)) and NQ-2030 (Reference (34)). In this section, activities of the NICSD SQA Team are described.

The NICSD IV&V Team activities are described in the NICSD VVP (Reference (12)).

7.1. NICSD Activity Review

The NICS-QA shall conduct the Internal Audit for each organization of the NICSD once a year or more frequently if required as defined in NQ-3022 (Reference (50)). As described in Section 6.2 of NQ-3022, audits shall be performed as deemed necessary by the NICS-QA manager.

In addition to the NICSD Internal Audit, the NICSD SQAL shall also conduct the NICSD software surveillance at the end of the every software life cycle defined in the NICSD SMP (Reference (10)). In the software surveillance, the NICSD SQA Team shall review the DVRs prepared by the NICSD IV&V Team. The DVRs are intended to be prepared by the NICSD Independent Reviewer as described in the Table-A in the NICSD SMP. This review shall be documented in the Software Surveillance Report, which shall be updated for each life cycle phase. Through this review of the NICSD IV&V activities including reviewing the NICSD Software Safety Analysis Reports (NICSD SSARs) prepared by the NICSD SS Team in accordance with Section 14 of the NICSD SMP, the NICSD SQA Team reviews the software safety analysis activities.

The NICSD SQA Team shall also review the Baseline Review Report (BRR) prepared by the NICSD IV&V Team. Through a review of the BRR, the NICSD SQA Team shall ensure inclusion of all applicable software modification requested by Documents Change Request (DCR) defined by NQ-2024 (Reference (31)), SNNR-I/II, and SCAR, in the baseline reviews.

And if necessary, the NICSD SQAL shall conduct a direct surveillance for the NICSD IV&V Team to confirm that the IV&V and Baseline Review activities are performed appropriately in accordance with applicable procedures and plans including the NICSD VVP (Reference (12)). For example, when the IV&V activity is suspected as not adequate, prior to determining that, the NICSD SQAL will confirm more detail through the direct surveillance. When direct surveillance is conducted, the following shall be addressed to confirm IV&V activities (reference SPP Table-10 through 18 for each phase as guidance).

- Monitor execution of the Software Verification and Validation Plan (SVVP) (i.e., the NICSD VVP) and analyze problems associated with its execution
- Report progress of the various V&V activities
- Ensure the software being produced fulfills requirements
- Evaluate testing results and check for completeness
- Monitor V&V outputs and determine when a task is complete
- Assess proposed changes to the software to identify affected requirements and any new hazards or risks as well as changing and re-performing V&V tasks as necessary to address the changes
- Determine the timing for changes or updates in the SVVP are required

7.2. PPDD Activity Review

The NICS-QA also conducts the Commercial Grade Survey (CGS) for Toshiba Fuchu Complex Power Systems Segment (Fuchu-PS), which includes the PPDD, to keep them as a Commercial Grade Supplier in the Qualified Vendor List (QVL) of NICSD in accordance with NQ-3005 (Reference (43)) at least every 3 years. The NICS-QA also conducts an annual evaluation of the Fuchu-PS including the PPDD to maintain the qualification of them in the NICSD QVL every year.

In addition, the NICSD SDL or the NICSD SQAL can request NICS-QA to conduct a CGS as necessary. Upon their request, the NICS-QA shall conduct an additional CG Survey to evaluate performance and capability of the PPDD as requested.
Depending on the purpose of these CG Surveys, the NICSD key personnel including the NICSD SDL, SSL, SCL, and IV&V Lead will concurrently participate in carry out their responsibility for the PPDD.

8 Test

As mentioned previously, the NICS-QA conducts an internal audit for the NICS-QC to verify compliance with an applicable aspect of the QA program and to determine its effectiveness. The NICS-QC has a responsibility to perform testing in accordance with NQ-3015 (Reference(46)), so that the audit team evaluates the testing activities by the NICS-QC during an internal audit.

The NICSD SQAL will conduct the following activities regarding the software testing by reviewing the DVRs and V&V Report (VVR) prepared by the NICSD IV&V Team at the end of each life cycle phase which includes testing activities.

The NICSD SQAL also conducts a review of such testing activities through the Baseline Review Report prepared by the NICSD IV&V Team, if the specific testing activities are not addressed in the DVRs.

8.1. NICSD Activity Review for Testing

The NICSD SQA Team shall review the DVR for the following item prepared by the NICSD IV&V Team as a part of the software surveillance at the end of the software phases indicated in the double parenthesis below.

- Software Validation Test Plan (NICSD SVTP)
  ((Module Validation Testing Phase))

8.2. PPDD Activity Review for Testing

The NICS-QA shall review the testing activity of PPDD through the Commercial Grade Surveys (CGSs) as described in Section 4.2 and 7.2 in this NICSD SQAP.

The NICSD SQA Team also reviews the DVRs prepared by the NICSD IV&V Team for the following items which are the scope of responsibility of the PPDD under the procurement from the NICSD in accordance with the CGD process.

- FPGA Test Procedure (Implementation and Integration Phase)
- FPGA Test Report (Implementation and Integration Phase)
- Module Test Procedure (Module Validation Testing Phase)

When a source surveillance, monitoring, witness, or Hold Point is required by the procurement documents to the PPDD in accordance with the NICSD Standard NQ-2025 "Preparation Procedure for Procurement Document for CG Items & Services" (Reference (32)), an inspector of the NICS-QC performs these activities to verify the PPDD activities. The PPDD is requested to prepare and submit the schedule of these activities to the NICS-QC.

9 Nonconformance Control and Corrective Action

Any anomalies and deviations found in work product after its release for review, test, or other use by someone other than the author, during any phase of the software life cycle shall be formally documented. The purpose of a formal procedure for nonconformance control and corrective action is to ensure that all errors and failures are promptly acted upon and in a uniform manner encompassing all project software. V&V activities are the primary vehicle to uncover problems, while the NICSD SCMP (Reference (11)) shall ensure that actions taken to correct problems by changing design artifacts are consistent and traceable. Any problems found during V&V activities including the RTM efforts shall be reported in the V&V reports. Likewise, any problems found during the Baseline Reviews shall be reported in the Baseline Review Reports.

Through the NICSD SQA Team involvement in the review of DVRs, VVRs, and BRRs, the NICSD SQA Team has the authority to issue the SCAR as necessary in the same measures as an audit issue. Once the SCAR regarding the software Quality Assurance is issued, the NICSD SQAL will have a responsibility to ensure that the corrective action is firmly implemented.

Processing of anomalies and corrective actions shall include evaluation of any metrics indicated in Section 6.6, to determine if the anomaly or corrective action is indicative of a single event, or of a developing adverse trend.

The design change caused by corrective action shall be controlled in accordance with Section 5.2.6 "Change Control" of the NICSD SCMP.

9.1. Nonconformance Control and Corrective Action Process for NICSD Activities

Any problems identified through the NICSD IV&V activities and/or the NICSD SQA activities shall be reported in the following manner:

- As for the issues regarding an item of itself, the issue shall be reported and resolved with the Fuchu Site Nonconformance Notice Report (SNNR-I) in accordance with the NICSD

Standard NQ-3019 "Procedure for Control of Nonconformance and Corrective Action" (Reference (48)).

- As for the issues regarding a process, the issue shall be reported and resolved with the Fuchu Site Corrective Action Request (SCAR) in accordance with the NED Standard AS-300A009 (Reference (21)) with application identified by the NICSD standard NQ-1003 "Application of AS Standards" (Reference (23)), or the Fuchu Site Nonconformance Notice Report (SNNR-II) in accordance with the NICSD Standard NQ-3019. NICSD Standard NQ-3009 (Reference (45)) is applied instead of AS-300A009 after September 1, 2012.

In cases where it is not obvious to determine which organization caused the problem, i.e., which procedure shall be applied, the NICSD SQAL has a responsibility to make a final decision on a responsible organization.

Both in SNNR and SCAR, any safety critical anomalies discovered post-release or after a completion of CGD shall be evaluated to determine if notification under Part 21 is required and perform appropriate notifications in accordance with the PSNE Regulations & Procedures 4810 "REPORTING PROCEDURE FOR DEFECTS AND NONCOMPLIANCE UNDER USNRC 10CFR21" (Reference (13)).

9.2. Nonconformance Control and Corrective Action for PPDD Activities

If the PPDD finds any problem of the configuration items during FPGA Testing and Module Validation Testing, the problems shall be reported using a Vendor Nonconformance Notice Report (VNNR) in accordance with the NICSD Standard NQ-3006 "Procedure for Control of Nonconforming Procurement Items and Services" (Reference (44)). The requirement to use the VNNR process is transmitted to the PPDD by the NICSD procurement documents. The NICS-QC Manager, who is appointed as a person to receive VNNR by NQ-3006, shall notify the NICSD SQAL that a VNNR has been received from the PPDD.

10 Tools, Techniques and Methodologies

Tools, Techniques and Methodologies are described in Section 8.1 of the NICSD SMP (Reference (10)).

11 Vendor Control

The NICSD shall perform the procurement of FPGA-based modules in accordance with the CGD procedure described in Section 6.2 of the NICSD SMP (Reference (10)). Personnel implementing this SQAP shall verify correct implementation of these activities.

11.1. Previously Developed Software (PDS) and Commercial-off-the-Shelf (COTS)

As a part of the vendor control, this section provides the software QA functions for control of Previously Developed Software (PDS) and Commercial-off-the-Shelf (COTS) in the FPGA-based safety-related systems.

As defined in Section 11 of the NICSD SMP (Reference (10)), the NICSD treats the FPGA logic as PDS, and treats the Functional Elements (FEs), which constitute the FPGA logic, as COTS. NICSD procures the FPGA modules from the PPDD through the commercial grade dedication process. The PPDD shall develop the software for the FPGAs using the verified and adequately proven FEs in accordance with the requirements defined in the procurement documents from the

NICSD. This procurement documents shall be developed by the NICSD in accordance with NQ-2025 (Reference (32)).

The FEs and FPGA logic are categorized as Software Integrity Level (SIL) 4 software, because the FEs are incorporated into the FPGA logic to be used for an actual safety-related product. SIL is defined by IEEE Std. 1012 (Reference (5)).

The NICSD SQA activities for control of the FEs by the PPDD shall verify the followings:

- The FEs shall be the software library for the products qualified by the PPDD through the quality assurance program in accordance with ISO-9001.
- The PPDD shall train, educate, and qualify a personnel who involved in the development of FEs.
- The PPDD shall develop the software life cycle approach for FEs.
- The PPDD shall develop the software requirements documents for FEs.
- The PPDD shall provide adequate traceability of the FEs as well as the requirements throughout the life cycle, and perform the functional testing of the FEs.
- The PPDD shall demonstrate that the FEs meet the requirements through the functional testing.
- The PPDD shall document the results of the functional testing of the FEs.
- The PPDD shall store FEs using a sufficiently dependable method.
- The PPDD shall track the operating history of FEs which applied in FPGAs.
- The PPDD shall control and dispose problems to ensure they do not affect the safety function of any application, when applicable.
- The PPDD shall have a measure to report the problem to the NICSD in a timely manner.

The PPDD activities are verified or monitored by the NICSD SQA Team via the CG survey, source verification, and/or by the NICSD IV&V Team per the NICSD VVP (Reference (12)).

11.2. Software Tool Vendors

Software tool vendors shall be controlled in accordance with the NICSD Standard NQ-3023 "Procedure for Purchase" (Reference (51)). NQ-3006 (Reference (44)) defines the requirements to the vendors when the vendor finds the discrepancies in the delivered product.
The error notification from the software tool review results for the development of FPGA logic shall be controlled in accordance with NQ-2034 (Reference (38)).

The NICSD SQAL shall ensure that the NICSD SDL applies all pertinent information provided by the vendors in the form of reports on tools, integrated circuits, and application notes.

12 Records Collection, Maintenance and Retention

Records collection, maintenance and retention shall be in accordance with the 10 CFR 50 Appendix B Quality Assurance program, as described in the NICSD Standard NQ-3020 "Control Procedure of QA Records" (Reference (49)).

Requirements for records collection, maintenance, and retention by the NICSD for the FPGA-based safety-related I&C Systems shall comply with the requirements described in NQ-3020 (Reference (49)) with special provisions to be specified in the Job Order Sheet by the NED.

13 Software Training

All NICSD personnel who are involved in the activities for safety-related products including the software development shall be trained on the QA program course, the applicable AS standards, and the NQ standards identified by NQ-1003 (Reference (23)) and, shall be registered in the personnel list for the safety-related works, prior to start work on the specific project. Also, the personnel who are involved in the software Quality Assurance activities for the project shall be trained on this NICSD SQAP either by classroom training or self-study. The NICSD SQAL has a responsibility for this training. The software QA personnel shall be competent in the appropriate technical and quality activities required in the design, development, review, test, and modification of software products. The software training plan is described in Section 15 of the NICSD SMP (Reference (10))

14 Risk Management

If the NICSD SQAL finds QA related potential risks through the NICSD SQA activities, those potential risks shall be reported to the NICSD SDL, IV&V Lead, and Software Safety Lead so that all reported personnel shall evaluate reported potential risk. If the NICSD SQAL identifies the potential risk is a risk to the project through the evaluation of and the discussion with all members, the risk shall be reported to the NICSD PM, and the NICSD PM shall assign a responsible personnel for the risk mitigation plan. The mitigation plan shall be reviewed and approved by the NICSD PM. Once the mitigation plan is put in place, the status risk shall be monitored in the periodic NICSD Management Meetings.

15 Cyber Security

The NICSD (including SQA) and the PPDD shall implement Secure Development and Operational Environment (SDOE) requirements in accordance with the NICSD Standard NQ-2037 "Cyber Security Procedures of Safety Related Digital System" (Reference (41)).
The NICSD SQAL shall verify compliance with the requirements of the SDOE and Toshiba cyber security procedures and practices throughout every aspect of the NICSD SQA activities for the project.

16 SQAP Maintenance

As defined in Table-A of the NICSD SMP (Reference (10)), the NICSD SQA Team is responsible for preparing the NICSD SQAP, the NICSD SQAL is responsible for reviewing it, and the NICSD PM is responsible for approval. The QA personnel of the NICS-QA Group shall be responsible to maintain this SQAP. The NICSD SQAP shall be maintained in accordance with Section 16 of the NICSD SMP. The updated SQAP shall be prepared, verified and approved in the same manner as the SQAP was first established as a document in accordance with NQ-2024 (Reference (31)). Also issued NICSD SQAP shall be retained as a QA record in accordance with NQ-3020 (Reference (49)).

17 Life Cycle Task Iteration Process

The life cycle task iteration process is described in Section 13.9 of the NICSD SMP (Reference (10)).

18 Deviations

18.1. Deviation Policy

The deviation policy is described in Section 17.1 of the NICSD SMP (Reference (10)).

18.2. Deviation from NICSD SQAP

None

Appendix A: Compliance Traceability Matrix of Section 5 of Software Program Plan.

(Note: This appendix is just for reference and not a part of this document.)

Table A Compliance Traceability Matrix of Section 5 of Software Program Plan

Section in the SPP	Section in this SQAP
5.1 Introduction	1.Introduction
5.1.1 Purpose	1.1 Purpose
5.1.2 Scope	1.3 Scope
5.1.3 [Deleted]	-
5.1.4 Relationship of the SQAPP to Other SPP Sections	-
5.2 Reference Documents	3 Reference Documents
5.3 Management	4 Management
5.3.1 Organization	4.1 Organization
5.3.2 Tasks	4.2 Responsibilities
5.3.3 Roles and Responsibilities	4.2 Responsibilities
5.4 Documentation	5 Documentation, 7.1 NICSD Activity review
5.5 Standards, Practices, Conventions, and Metrics	6 Standards, Practices, Conventions, and Metrics
5.6 Reviews and Audits	7 Software Reviews
5.6.1 Reviews	7 Software Reviews
5.6.1.1 Baseline Reviews	7.1 NICSD Activity Review
5.6.1.2 Technical Reviews	7.1 NICSD Activity Review
5.6.1.3 Managerial Review	4.2 Responsibilities
5.6.2 Audits and Inspection	7.1 NICSD Activity Review
5.6.2.1 Functional Audit	4.2 Responsibilities, 7.1 NICSD Activity Review
5.6.2.2 Physical Audit	4.2 Responsibilities, 5.2 Audits, Surveillances and Commercial Grade Surveys, 7.1 NICSD Activity Review
5.6.2.3 In-Process Audit and Inspections	4.2 Responsibilities, 5.3 Reports Documentation, 7.1 NICSD Activity review
5.7 Test	8 Test
5.8 Anomaly Reporting and Corrective Actions	9 Nonconformance Control and Corrective Action
5.8.1 Anomaly Reporting	9 Nonconformance Control and Corrective Action
5.8.2 Corrective Action	9 Nonconformance Control and Corrective Action
5.9 Software Modification Process	7.1 NICSD Activity Review
5.10 Tools, Techniques, and Methodologies	10 Tools, Techniques and Methodologies
5.11 Code Control	-
5.12 Media Control	-
5.13 EPC Team Member, EPC Subcontractor, and Vendor Control	1.2 Background, 11 Vendor Control
5.14 Previously Developed or Purchased (COTS) Software	11.1 Previously Developed Software (PDS) and Commercial-off-the-Shelf (COTS)
5.15 Records Collection, Maintenance, and Retention	16 SQAP Maintenance
5.16 Training	13 Software Training
5.17 Risk Management	14 Risk Management