ASR 1000 Roadmap

May 2012

ASR 1000 in SP and Enterprise networks

- ASR 1000 is a feature-rich service edge router that can be deployed in both Service Provider and Enterprise networks in the following applications
- Enterprise
  - Secure WAN Aggregation including IPSec VPN – DMVPN, GETVPN
  - Private WAN
  - Internet Gateway – FW/NAT
  - Data Center Interconnect (DCI)
  - Voice services (CUBE(ENT))
  - Over the Top Virtualization (OTV)
- Service Provider
  - Managed CPE
  - Broadband Aggregation LAC/PTA/LNS
  - Voice services (CUBE (SP))
  - Hosted Security Services (FW/NAT, IPSec)
  - Provider Edge (L3VPN, L2VPN)
  - Virtual Private LAN Services (VPLS)

Topics Covered

- Introduction
- Hardware Components
- System Architecture and High Availability
- Software Architecture, Software Packaging

Where the ASR 1000 Fits

Performance and Scalability

MANAGED SERVICES CPE Routers

Managed L2/L3 VPNS
Integrated Security
Application Recognition

ISR Series

7200 Series

ASR 1000

- 2.5-360G per System
- Broadband
- Route Reflector
- Distributed PE
- Hosted Firewall
- IP Sec
- SBC/VoIP

7600 Series

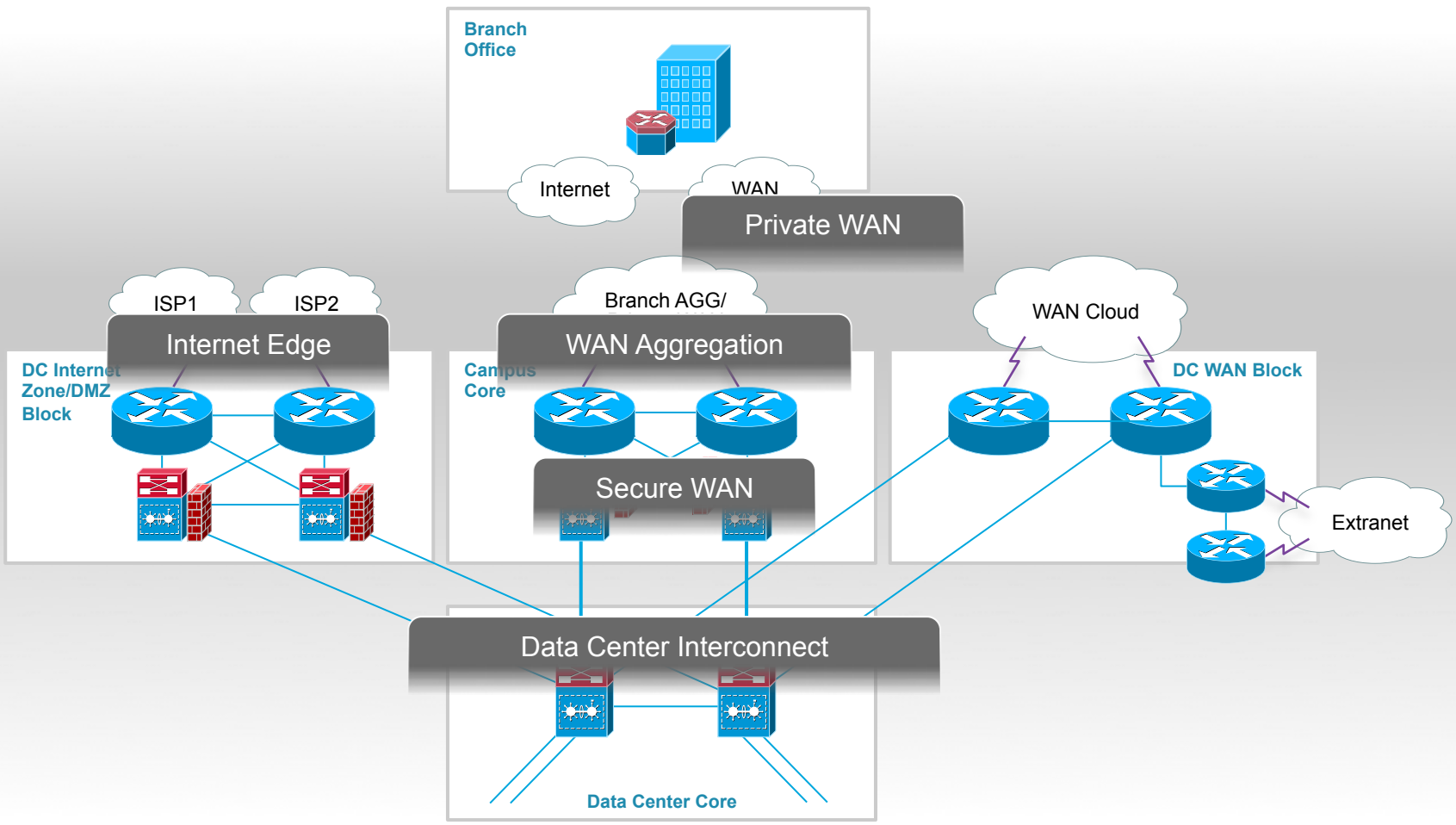
- Up to 2 Tbps per system
- Carrier Ethernet
- IP RAN
- Mobile Gateways
- SBC/VoIP
- Broadband
- Vidmon

ASR 9000

- Up to 48 Tbps per system
- Carrier Ethernet
- IP RAN
- L2/L3 VPNs
- Vidmon
- BNG

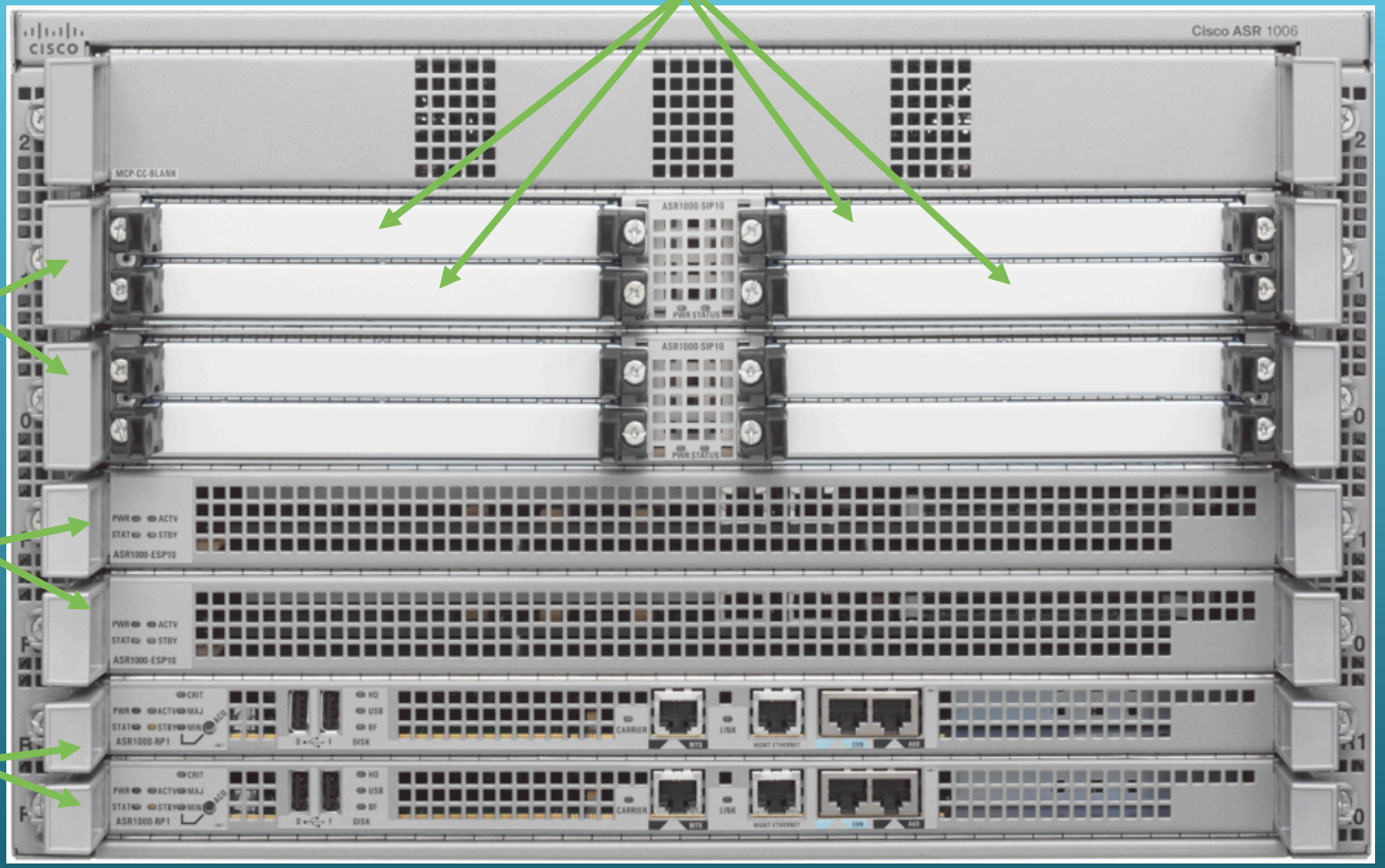
SERVICE PROVIDER EDGE Routers

ASR 1000: Enterprise Applications



Hardware Components

Chassis Options: ASR1006



Rack Mounts and Cable Management not shown

ASR 1000 Series Chassis

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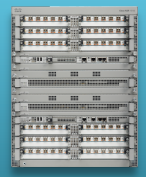
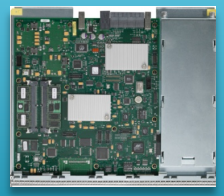
	ASR 1001	ASR 1002	ASR 1002-X Target IOS XE 3.7.1S (Sept. 2012)	ASR 1004	ASR 1006	ASR 1013
						
SPA Slots	1-slot	3-slot	3-slot	8-slot	12-slot	24-slot
RP Slots	Integrated	Integrated	Integrated	1	2	2
ESP Slots	Integrated	1	Integrated	1	2	2
SIP Slots	Integrated	Integrated	Integrated	2	3	6
IOS Redundancy	Software	Software	Software	Software	Hardware	Hardware
Built-In GE	4	4	6	N/A	N/A	N/A
Height	1.75” (1RU)	3.5” (2RU)	3.5” (2RU)	7” (4RU)	10.5” (6RU)	22.7” (13RU)
Bandwidth	2.5 to 5 Gbps	5 to 10 Gbps	5 to 36 Gbps	10 to 40 Gbps	10 to 100 Gbps	40-100+ Gbps
Maximum Output Power	400W	470W	470W	765W	1275W	3200W
Airflow	Front to back	Front to back	Front to back	Front to back	Front to back	Front to back
Integrated I/O Daughtercard	1					

Route Processors (RP)

	ASR1001	ASR1002-X	RP1	RP2
				
CPU	Dual-Core 2.2GHz Processor	Quad-Core 2.13GHz Processor	General Purpose CPU Based on 1.5GHz Processor	Dual-Core Processor, 2.66GHz
Memory	4GB default (4x1GB) 8GB(4x2GB) 16GB maximum (4x4GB)	4GB default 8GB 16GB	2GB default (2x1GB) 4GB maximum (2x2GB) RP1 with 4GB built in ASR 1002	8GB default (4x2GB) 16GB maximum (4x4GB)
Built-In eUSB Bootflash	8GB	8GB	1GB (8GB on ASR 1002)	2GB
Storage	External USB	160GB HDD (optional) & External USB	40GB HDD and External USB	80GB HDD and External USB
Cisco IOS XE Operating System	64 bit	64 bit	32 bit	64 bit
Chassis Support	Integrated in ASR1001 chassis	Integrated in ASR1002-X chassis	ASR1002 (integrated), ASR1004, and ASR1006	ASR1004, ASR1006, and ASR1013

ESP100

Roadmap for Increased Performance and Scale

Target IOS XE 3.7.1S (Sept. 2012)

ESP-100G

Total Bandwidth	• 100 Gbps
Performance	• Up to 32 Mpps
QuantumFlow Processors **- Resource Memory** **- TCAM** **- Packet Buffer**	• 2 • 4 GB • 1 x 80 Mb • 1 GB
Control CPU **- Frequency** **- Memory**	• Dual-core CPU • 1.73 GHz • 16 GB
Broadband **QoS** **IPSec Bandwidth (1400 B)** **FW/NAT**	• Up to 64 K sessions • Up to 232 K queues • 30 Gbps • 6 M sessions
Chassis **Route Processor**	• ASR 1006, ASR 1013 • RP2 + Future

Embedded Services Processors (ESP)

Based on Quantum Flow Processor (QFP)

	ESP-2.5G	ESP-5G	ESP-10G	ESP-20G	ESP-40G	ESP-100G
System Bandwidth	2.5Gbps	5Gbps	10Gbps	20Gbps	40Gbps	100Gbps
Performance	3Mpps	8Mpps	17Mpps	24Mpps	24Mpps	32Mpps
# of Processors	10	20	40	40	40	128
Clock Rate	900 MHz	900 MHz	900 MHz	1.2 GHz	1.2 GHz	1.5 GHz
Crypto Engine BW (1400 bytes)	1Gbps	1.8Gbps	4.4Gbps	8.5Gbps	11Gbps	25Gbps
QFP Resource Memory	256MB	256MB	512MB	1GB	1GB	4GB
Packet Buffer	64MB	64MB	128MB	256MB	256MB	1GB
Control CPU	800 MHz	800 MHz	800 MHz	1.2 GHz	1.8 GHz	Dual core 1.73 GHz
Control Memory	1GB	1GB	2GB	4GB	8GB	16GB
TCAM	5Mb	5Mb	10Mb	40Mb	40Mb	80Mb
Chassis Support	ASR1001 (Integrated)	ASR1001 (integrated), ASR 1002	ASR1002, 1004, 1006	ASR1004, 1006	ASR1004,1006, 1013	ASR1006, 1013

ASR 1000—SIP (SPA Interface Processors)

	ASR-1000-SIP10	ASR-1000-SIP40
Bandwidth	10G	40G
Ingress Buffering	128MB	128MB
Egress Buffering	8MB	8MB
ESI Frequency	3.125GHz	6.25GHz or 3.125GHz
Bandwidth per ESI Link	11Gbps	23Gbps
ESI Links Used	1	1 or 2
Total Bandwidth	11Gbps	23Gbps/46Gbps

ASR 1000 SPA Support

SPAs Currently Supported on Other Cisco Platforms
Will Also be Supported on the ASR 1000

Ethernet
FE
GE
10GE

ATM
OC3
OC12

Serial
12 in 1

Clear Channel
T3/E3

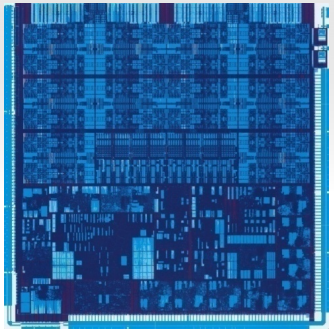
POS
OC3
OC12
OC48

Channelized
T1/E1
T3
STM1, STM4

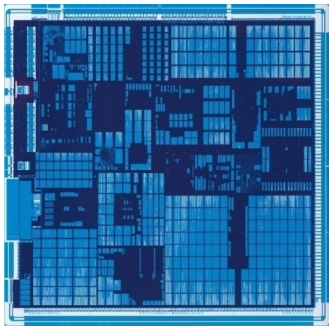
ASR 1000 Series Innovations
Cisco QuantumFlow Processor

- Five year design
- Massively parallel, 64 multi-threaded cores
- QFP Architecture designed to scale to >100Gbit/sec
- 256 processes available to handle traffic
- High-priority traffic is prioritised
- Packet replication capabilities for Lawful Intercept
- Full visibility of entire L2 frame
- Latency: tens of microseconds with features enabled
- Interfaces on-chip for external cryptographic engine
- First generation QFP is capable of 40 Gbps
- Second generation QFP is capable of 60 Gbps

	Cisco QFP	Sun Ultrasparc T2	Intel Core 2 Mobile U7600
Total number processes (cores x threads)	**256**	64	2
Power per process	**0.26W**	1.01W	5W
Scalable traffic management	**116k Queues**	None	None

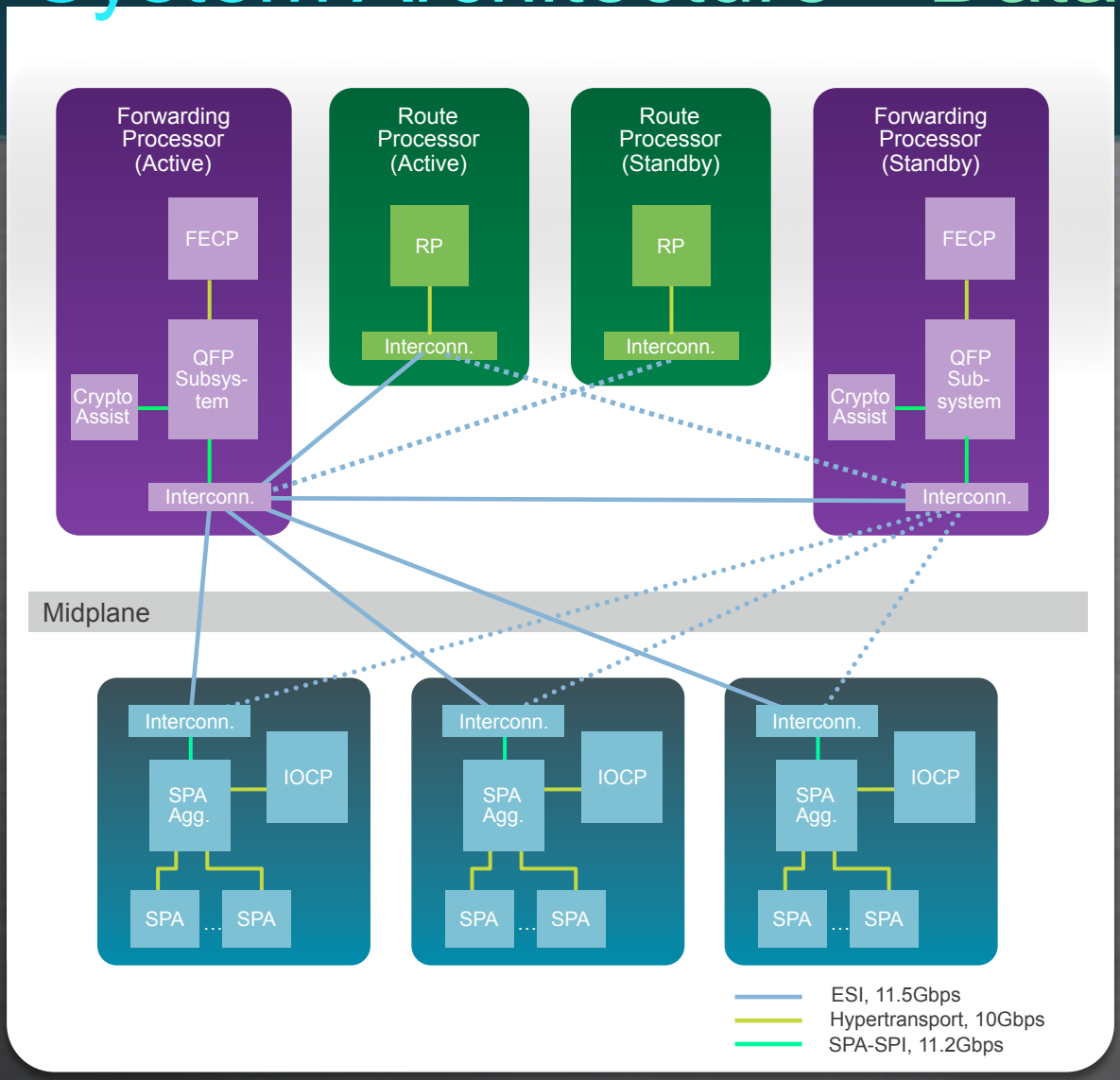


Cisco QFP



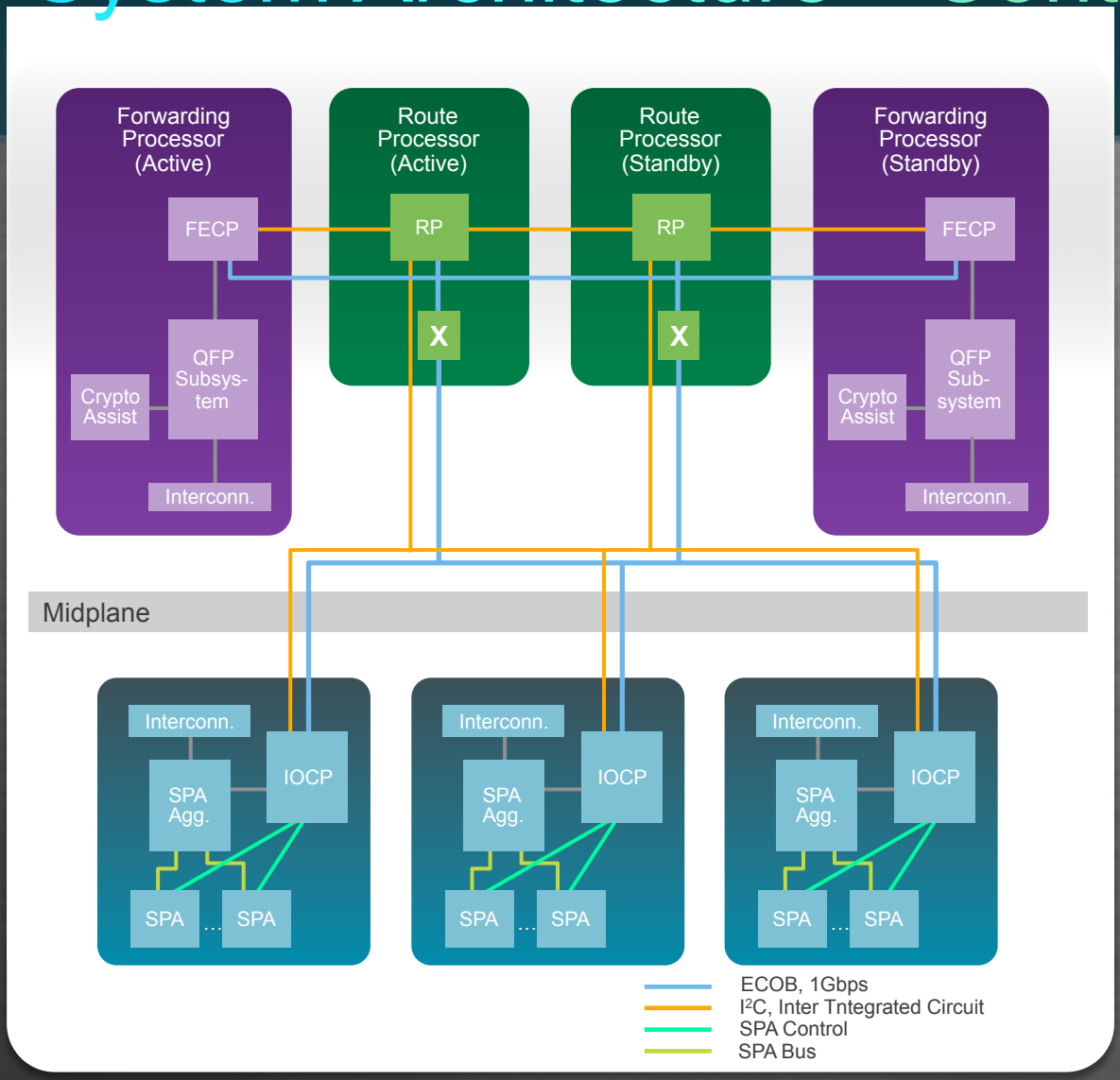
Cisco QFP Traffic Manager

System Architecture—Dataplane



- All data forwarding is through ESP
- Exception: Punt path for Legacy protocols—handled by the RP
- Interconnect ASIC in each of the functional elements provides the backplane connection through ESI links
- ESI (Enhanced Serdes Interconnect) links are used for Data forwarding
- SPA-SPI links connect to the backplane through the SPA-Agg ASIC

System Architecture—Control Plane



Ethernet Out-of-Band Channel (EOBC)

- Run between **all** components
- Indication if cards are installed and ready
- Watchdog timers
- State information exchange for L2 or L3 Protocols

I²C

- Monitor health of hardware components
- Control resets
- Communicate active/standby, real time presence and ready indicators
- Control the other RP (reset, power-down, interrupt, report power supply status, signal ESP active/standby)
- EEPROM access

SPA control links

- Run between IOCP and SPAs
- Detect SPA OIR
- Reset SPAs (via I2C)
- Power-control SPAs (via I2C)
- Read EEPROMs

ASR 1000 System Oversubscription

- Total bandwidth of the system is determined by the following factors
  - The type of forwarding engine—ESP-10G or ESP-20G
  - The type of SPA Interface Processor
- SPA Interface Processors in the system share the ESP bandwidth, regardless of the type of the SIP—2XSIP in 4RU chassis and 3XSIP in 6RU chassis
  - ESP-10G—10G bandwidth shared among all SPA Interface Processors
  - ESP-20G—20G bandwidth shared among all SPA Interface Processors
- The SIP bandwidth is the bandwidth of the link between one SPA Interface Processor and the ESP
  - SIP-10G—10G link between SIP and ESP

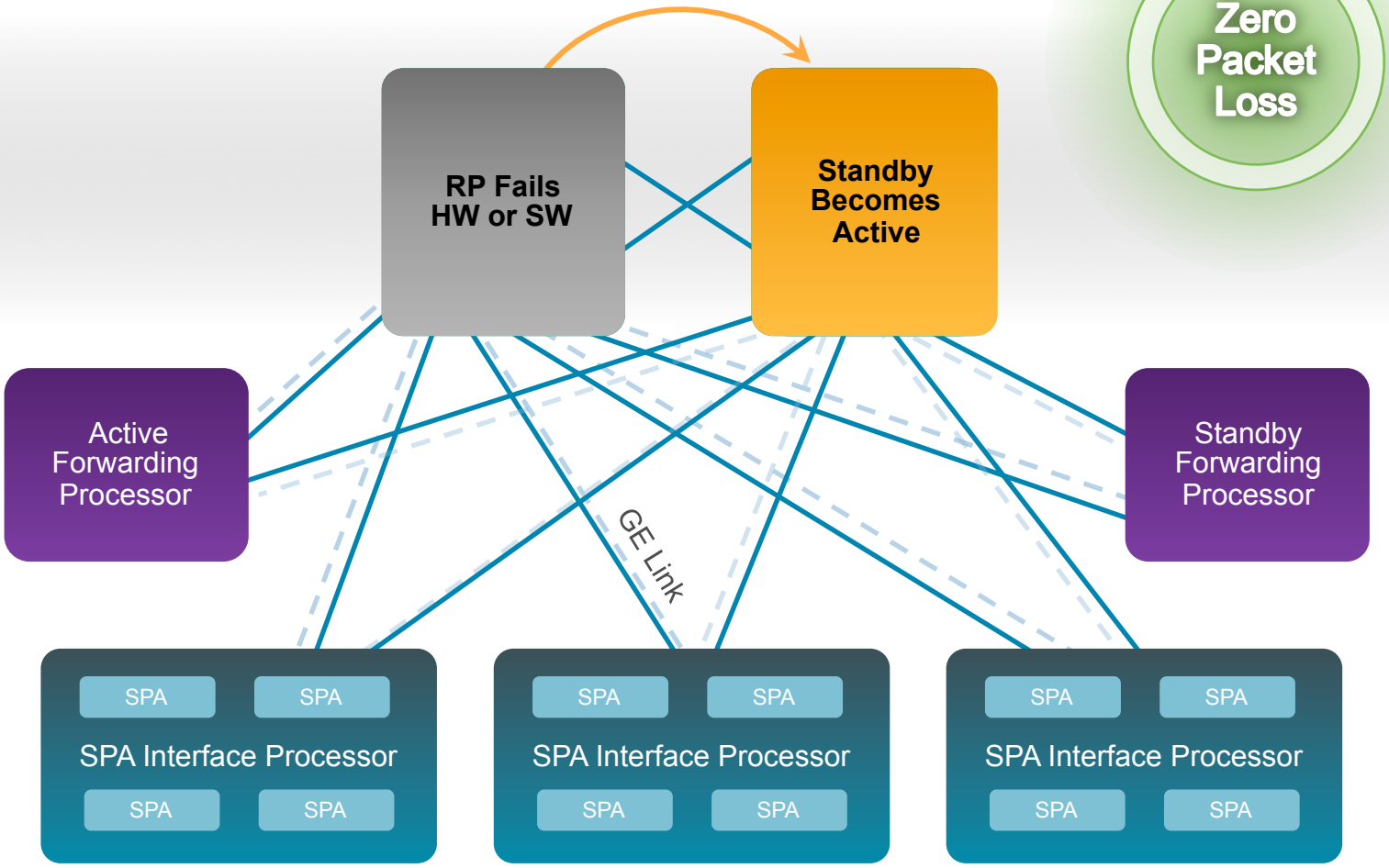
Chassis Version	ESP Version	SIP Version	SIP Slots	Max. Bandwidth per IP Slot (Gbps)	SPA to SIP Oversubscription	Bandwidth on ESP (Gbps)	ESP (System Bandwidth) Oversubscription	System (Chassis) Oversubscription
ASR 1001	ESP2.5	n.a.	n.a.	n.a.	2:1	2.5	5.6:1	5.6:1
ASR 1001/ ASR1002	ESP5	n.a.	n.a.	n.a.	4:1	5	6.8:1	6.8:1
	ESP10	n.a.	n.a.	n.a.	4:1	10	3.4:1	3.4:1
ASR 1002-X	ESP40	SIP40	n.a.	n.a.	9:10	36	1:1	9:10
ASR 1004	ESP10	SIP10	2	10	4:1	10	2:1	8:1
	ESP20	SIP10	2	10	4:1	20	1:1	4:1
	ESP40	SIP10	2	10	4:1	40	1:2	4:1

(Table continued on next slide)

ASR 1000 HA Highlights

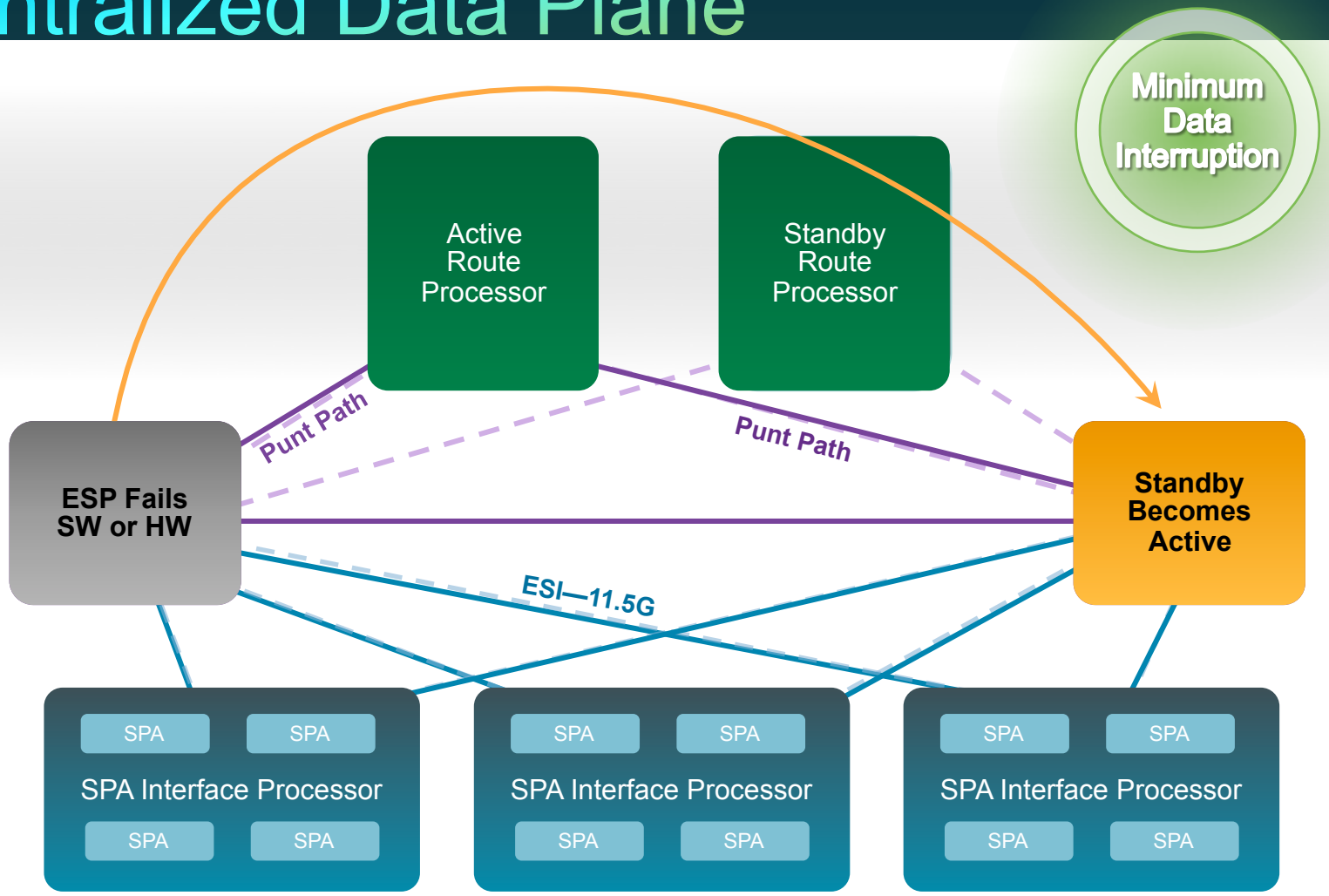
- ASR 1000 leverages Cisco IOS HA infrastructure—NSF/SSO, ISSU
- 1+1 redundancy option for RP and ESP
  - Active and standby
  - No load balancing
- RPs are separate from ESPs
  - Switchover of ESP does not result in switchover of RP
  - Switchover of RP/IOS does not result in switchover of ESP
- Single RP may be configured with dual IOS for SW redundancy (single RP only)
- No redundancy for SIP or other I/O cards
  - SPA plugs into a single SIP
- Protection against SPA or SIP failure is via APS or Y-cable redundancy feature (Future: requires SPA support)

System Architecture: Distributed Control Plane



Separate and Independent Internal Communication Link for Control Plane (GE)

System Architecture: Centralized Data Plane

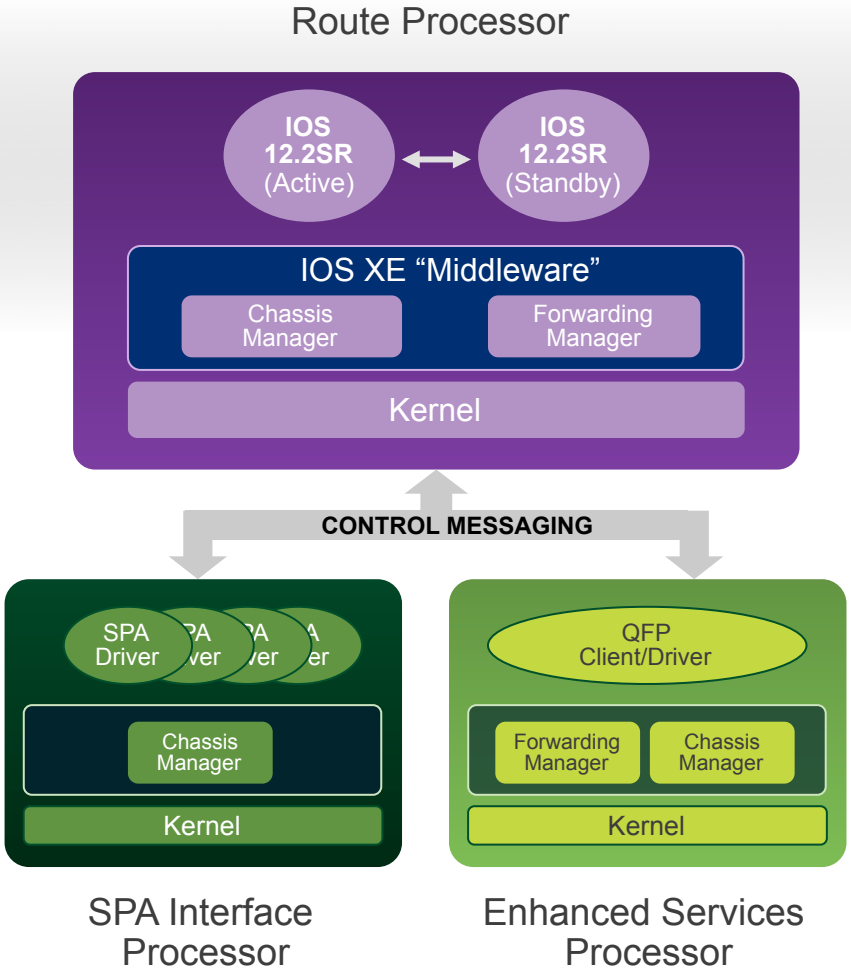


All Packets Processed by QFP for Forwarding
Separate and Independent links for Data Plane communication (ESI 11.5G)

Software Architecture and Packages

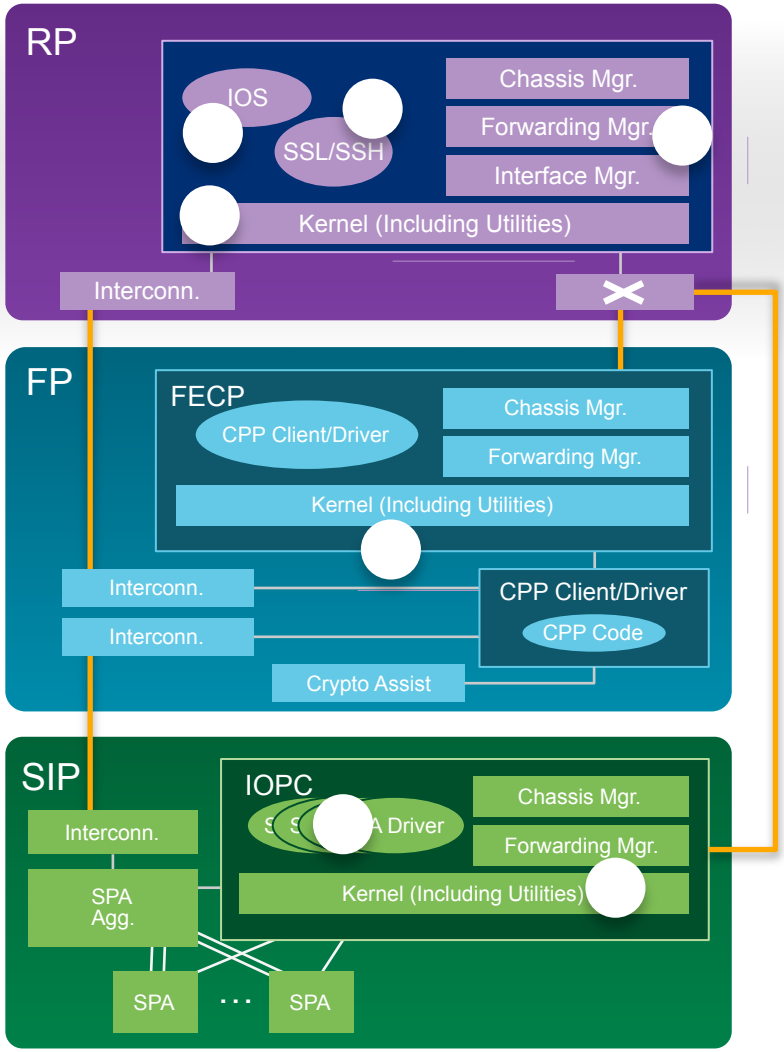
Software Architecture: IOS XE

- IOS XE = IOS + IOS XE Middleware + Platform Software
- Operational Consistency—same look and feel as IOS Router
- IOS runs as its own Linux process for control plane (Routing, SNMP, CLI, etc.); 32bit and 64bit options
- Linux kernel with multiple processes running in protected memory for:
  - Fault containment
  - Restartability
  - ISSU of individual SW packages
- ASR 1000 HA innovations
  - Zero-packet-loss RP Failover (ASR1006)
  - <50ms ESP Failover
  - “Software Redundancy” (ASR1001/2/4)



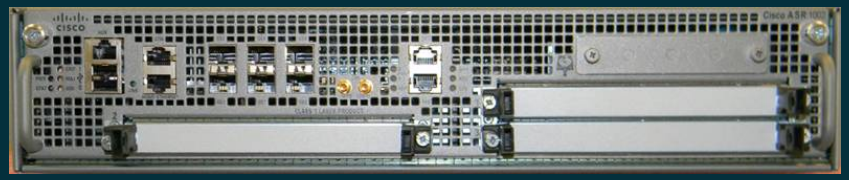
Software Sub-Packages

1. **RPBase:** RP OS
   Why?: Upgrading of the OS will require reload to the RP and expect minimal changes
2. **RPIOS:** IOS
   Why?: Facilitates Software Redundancy feature
3. **RPAccess (K9 and non-K9):** Software required for router access; two versions will be available. One that contains open SSH and SSL and one without
   Why?: To facilitate software packaging for export-restricted countries
4. **RPControl :** Control Plane processes that interface between IOS and the rest of the platform
   Why?: IOS XE Middleware
5. **ESPBase:** ESP OS + Control processes + QFP client/ driver/ucode:
   Why?: Any software upgrade of the ESP requires reload of the ESP
6. **SIPBase:** SIP OS + Control processes
   Why?: OS upgrade requires reload of the SIP
7. **SIPSPA:** SPA drivers and FPD (SPA FPGA image)
   Why?: Facilitates SPA driver upgrade of specific SPA slots



Roadmap

ASR1002-X Overview



Target IOS XE 3.7.1S (Sep 2012)

Chassis & HW	• 2RU form factor • Integrated RP, ESP & SIP • Redundant AC/DC PSU, same as ASR1002
System BW	• 5G, 10G, 20G, 36G, via software upgrade
Performance	• Up to 30 Mpps
Crypto BW	• 4G
Control Plane	• Quad-core @ 2.13GHz processor
Data Plane	• Integrated ESP with SW selectable BW from 5G to 36G
I/O	• 3 SPA bays + 6 built-inGE ports (Copper/Fiber SFP, SyncE capable) • Console / MGMT Ethernet / Aux • Management Ethernet • External USB storage • Optional HDD (160GB)
FW/NAT	• 36G FW/NAT, 2 M sessions
Network Timing	• Stratum 3/G.813 Clocking, BITS timing, GPS, SyncE, 1588
Image Security	• Secure boot • Code Signing (FIPS-140-3)

Customer Benefits

- Compact (2RU) WAN aggregation routing solution with embedded instant-on services
- Versatile Routing Solution …
  - WAN Aggregation including secure WAN
  - Internet Gateway with Performance Routing and Firewall
  - Managed Services Solution with highly integrated services
  - High-end branch office solution
  - Highly scalable Route Reflector
  - MSE, BRAS with up to 64K sessions

- **Performance** - Almost 4 times the performance of ASR1002
- **Pay-As-You-Grow**: Easy performance upgrade via software activated license (to10/20/36G)

- **Investment protection** - Same SPAs used across other ASR 1000 chassis and Cisco platforms
- Feature Licenses Monitoring for RTU licenses
  - For technology licenses (IPB,AIS,AES)
  - For honor-based feature licenses
- Same operational IOS “look & feel” as rest of ASR 1000 family

ESP100

Roadmap for Increased Performance and Scale

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ESP100

Total Bandwidth	• 100 Gbps
Performance	• Up to 32 Mpps
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Control CPU **- Frequency** **- Memory**	• Dual-core CPU • 1.73 GHz • 16 GB
Broadband **QoS** **IPSec Bandwidth (1400 B)** **FW/NAT**	• Up to 64 K sessions • Up to 232 K queues • 30 Gbps • 6 M sessions
Chassis **Route Processor**	• ASR 1006, ASR 1013 • RP2 + Future

Target FCS: July 2012

IOS XE 3.7S – Hardware & Routing

Routing
- uRPF with ACL feature
- BGP C-Route overlay signaling
- MLFR for IPv6
- RR for BGP auto-discovery of mVPN4 and mVPN6
- IPv6 GRE tunnel protection
- IPv6 export for Netflow
- IPSLA QFP timestamp

QOS
- GRE/VTI QoS: add new classes to 2nd level policy

Chassis
- ASR1002-X (Kingpin)*

**Available only in 3.7.1S – Sep'2012*

ESP
- ESP100*

** Available only in 3.7.1S – Sep'2012*

Target FCS: July 2012

IOS XE 3.7S – Services

Security
- Dual stack DMVPN over v4 transport
- NSA Suite B Control Plane (ECDH-ECDSA)
- Dual Stack FlexVPN over v4, v6 transport
- AAA Accounting for IKEv2
- ASR1k IPSec Debuggability Enhancement
- VRF aware CRL checking with LDAP
- VASI interface support in v6 ZBFW
- GGSN Pooling
- Resource Management support in v6 ZBFW
- SYN Cookie for v6 ZBFW
- DDoS support in v6 ZBFW
- FTP66 ALG support (FTP66/64)
- H.323 vTCP with HA Support

AVC
- NBAR2 ESP100 support
- FNF- IPFIX support
- PfR integration with NBAR2
- NBAR2 extracted fields (URL, User-Agent, Referrer)
- Multi-stage classification
- Protocol pack support

CUBE-SP
- H.248 Border Access Controller support
- IMS: Support for Rf interface
- H323v TCP with HA support

CUBE-ENT
- REFER pass-through and consumption
- Supplementary services for SRTP-RTP interworking
- Bandwidth based CAC
- Inclusion of authorization header in initial REGISTER request
- Populating route header based on proxy server, IP address and port
- Midcall codec renegotiate with RE-INVITe
- Multiple destination pattern support on voice dial-peer
- SIP registration pass through

Thank you.