Arm Cortex-M7 Processor Datasheet

Datasheet

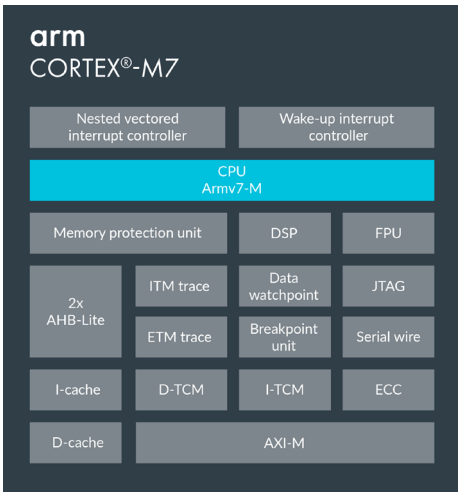

Figure 1: Block diagram of the Cortex-M7 processor

Overview

The Arm Cortex-M7 processor is the highest-performing processor in the Cortex-M family that enables the design of sophisticated MCUs and SoCs. The Cortex-M7 offers industry-leading scalar performance of 5.01 CoreMarks/MHz, while maintaining the excellent responsiveness and ease-of-use of the Armv7-M architecture. With built-in instruction and data caches and tightly coupled memories (TCMs) this superscalar processor never has to slow down even in the most demanding processing applications at the endpoint.

Features

Feature	Description
Architecture	Armv7E-M
ISA support	Thumb/Thumb2
Pipeline	6-stage superscalar and branch prediction
DSP extension	Single-cycle 16/32-bit MAC
	Single-cycle dual 16-bit MAC
	8/16-bit SIMD arithmetic
	Hardware divide
FPU	Optional single and double-precision FPU (choices of none, single-precision only, and single and double-precision)
	IEEE 754 compliant
Interconnect	64-bit AMBA4 AXI, 32-bit AHB peripheral (AHBP) port
	32-bit AHB slave (AHBS) port for external master (such as DMA controller) to access Tightly-Coupled Memories
	APB interface for CoreSight debug components
Instruction cache	0 to 64 KB, 2-way associative with optional error correction code (ECC)
Data cache	0 to 64 KB, 4-way associative with optional ECC
Instruction TCM	0 to 16 MB with optional ECC interface
Data TCM	0 to 16 MB with optional ECC interface
Memory protection	Optional Memory Protection Unit (MPU) with 8 or 16 regions with sub regions and background regions
Bit manipulation	Integrated Bit-Field Processing Instructions
Interrupts	Non-maskable Interrupt (NMI) + 1 to 240 physical interrupts

Interrupt priority levels	8 to 256 priority levels
Wake-up interrupt controller	Optional
Sleep modes	Integrated WFI and WFE Instructions and Sleep-On Exit capability
	Sleep and deep sleep signals
	Optional retention mode with Arm Power Management Kit
Debug	Optional JTAG and serial wire debug ports. Up to 8 breakpoints and 4 watchpoints
Trace	Optional Embedded Trace Macrocell (ETM), Micro Trace Buffer (MTB), Data Watchpoint and Trace (DWT), and Instrumentation Trace (ITM) Optional full data trace with ETM
Dual Core Lock-Step support (DCLS)	Yes, DCLS configuration

About the Processor

The Cortex-M7 is a high-performance processor with almost double the performance of the older Cortex-M4. It features a 6-stage superscalar pipeline with branch prediction and an optional FPU capable of single-precision and optionally double-precision operations. The instruction and data buses have been enlarged to 64-bit wide over the previous 32-bit buses.

The interfaces that the processor supports include:

- 64-bit AXI4 interface
- 32-bit AHB master interface
- 32-bit AHB slave interface
- 64-bit instruction TCM interface
- 2x32-bit data TCM interfaces

The processor has optional:

- Up to 64kB instruction cache
- Up to 64kB data cache
- MPUs which you can configure to protect regions of memory
- Double-precision and single-precision FPU
- Support for ETM

The processor is highly configurable and is intended for a wide range of high-performance, deeply embedded applications that require fast interrupt response features.

Block Diagram

Cortex-M7 processor components

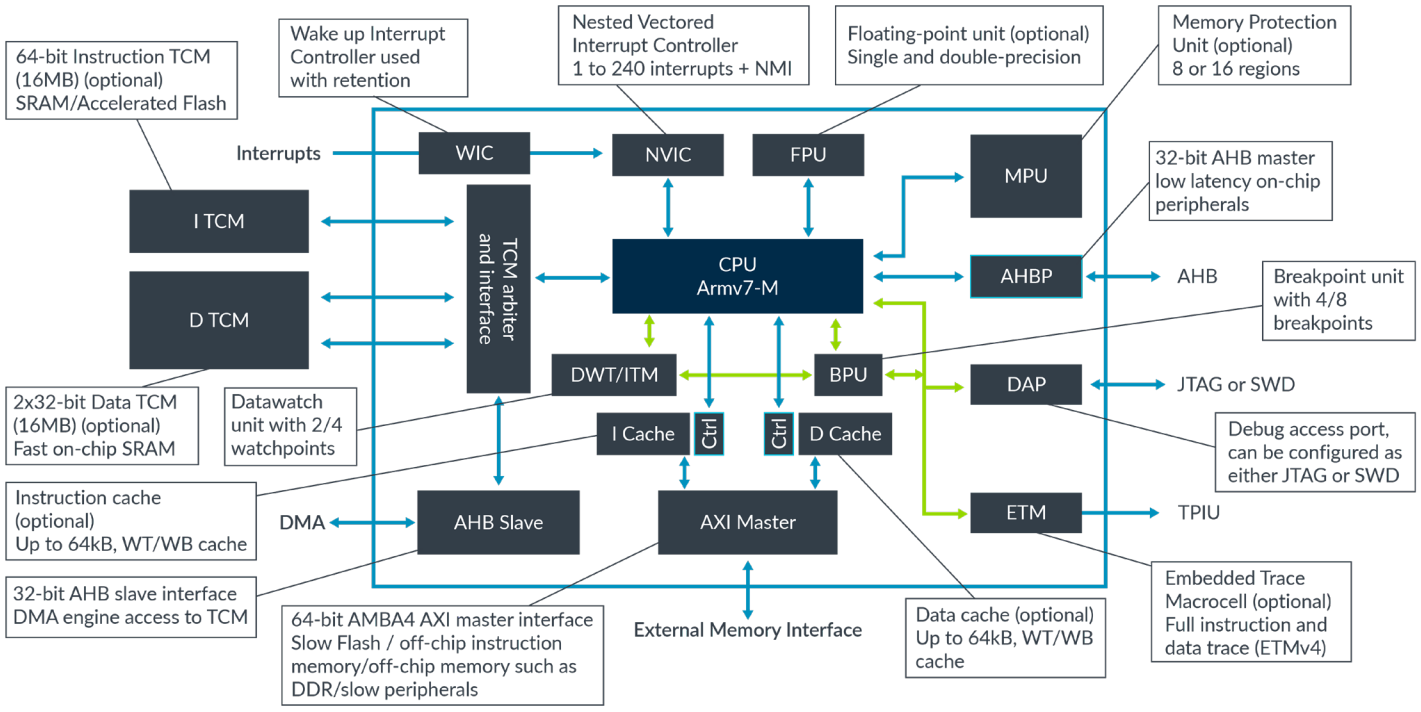

Figure 2: Cortex-M7 processor components

Cortex-M7 Processor Components

Data Processing Unit

The Data Processing Unit (DPU) provides:

- Parallelized integer register file with six read ports and four write ports for large-scale dual-issue
- Extensive forwarding logic to minimise interlocks
- Two Arithmetic Logic Units (ALUs), with one ALU capable of executing SIMD operations
- Single MAC pipeline capable of 32x32-bit + 64-bit → 64-bit with two cycle result latency and one MAC per cycle throughput
- Single divider unit with support for operand-dependent early termination

Prefetch Unit

The Prefetch Unit (PFU) provides:

- 64-bit instruction fetch bandwidth
- Four 64-bit prefetch queue to decouple instruction prefetch from DPU pipeline operation
- A Branch Target Address Cache (BTAC) for single-cycle turn-around of branch predictor state and target address

- A static branch predictor when no BTAC is specified
- Forwarding of flags for early resolution of direct branches in the decoder and first execution stages of the processor pipeline

Load Store Unit

The Load Store Unit (LSU) provides:

- Dual 32-bit load channels to TCM, data cache, and AXI master (AXIM) interface for 64-bit load bandwidth and dual 32-bit load capability
- Single 32-bit load channel to the AHB interface. Single 64-bit store channel
- Store buffering to increase store throughput and minimize RAM contention with data and instruction reads
- Separate store buffering for TCM, AHBP and AXIM for quality of service (QoS) and interface-specific optimizations

Floating-point Unit

The optional FPU provides:

- Lazy floating-point context save. Automated stacking of floating-point state is delayed until the ISR attempts to execute a floating-point instruction. This reduces the latency to enter the ISR and removes floating-point context save for ISRs that do not use floating-point
- Instructions for single-precision (C programming language float type) data-processing operations
- Optional instructions for double-precision (C double type) data-processing operations
- Combined multiply and accumulate instructions for increased precision (Fused MAC)
- Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square root
- Hardware support for denormals and all IEEE Standard 754-2008 rounding modes
- 32 x 32-bit single-precision registers or 16 x 64-bit double-precision registers

Nested Vectored Interrupt Controller

The NVIC is closely integrated with the core to achieve low-latency interrupt processing. Features include:

- External interrupts, configurable from 1 to 240. This is configured at implementation
- Configurable levels of interrupt priority from 8 to 256. Configured at implementation
- Dynamic reprioritization of interrupts
- Priority grouping. This enables selection of pre-empting interrupt levels and non-pre-empting interrupt levels
- Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts

Wake-up Interrupt Controller

The optional Wake-up Interrupt Controller (WIC) provides ultra-low power sleep mode support.

Memory System

The optional memory system includes:

- A Bus Interface Unit (BIU) with a configurable AMBA 4 AXI interface that can support a high-performance L2 memory system
- An extended AHB-Lite interface to support low-latency system peripherals
- A Tightly Coupled Interface Unit (TCU) with TCM interfaces that can support external
- ECC logic and an AHBS interface for system access to TCMs
- Instruction and data caches and controllers with optional ECC
- A Memory Built-in Self-Test (MBIST) interface. The interface supports MBIST operation while the processor is running

Memory Protection Unit

The optional MPU has configurable attributes for memory protection. It includes up to 16 memory regions and sub region disable (SRD), enabling efficient use of memory regions. It also has the ability to enable a background region that implements the default memory map attributes.

Cortex-M7 Processor and PPB ROM tables

The two ROM tables enable a debugger to identify and connect to CoreSight debug components.

Cross Trigger Interface Unit

The optional Cross Trigger Interface Unit (CTI) enables the debug logic and ETM to interact with each other and with other CoreSight components.

ETM

The optional Embedded Trace Macrocell provides instruction-only or instruction and data trace capabilities when configured. See the Arm CoreSight ETM-M7 Technical Reference Manual for more information.

Debug and Trace Components

- Configurable Breakpoint unit (FPB) for implementing breakpoints
- Configurable DWT unit for implementing watchpoints, data tracing, and system profiling
- Optional ITM for support of printf() style debugging, using instrumentation trace Interfaces suitable for:
  - Passing on-chip data to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode
  - Debugger access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even when reset is asserted

Interfaces

The processor contains the following external interfaces:

- AHBP interface
- AHBS interface
- AHBD interface
- External Private Peripheral Bus
- ATB interfaces
- TCM interface
- Cross Trigger interface
- MBIST interface
- AXIM interface

AHBP Interface

The AHBP interface provides access suitable for low latency system peripherals. It provides support for unaligned memory accesses, write buffer for buffering of write data, and exclusive access transfers for multiprocessor systems.

AHBS Interface

The AHBS interface enables system access to TCMs.

AHBD Interface

The AHB-Lite Debug (AHBD) interface provides debug access to the Cortex-M7 processor and the complete memory map.

External Private Peripheral Bus

The APB External PPB (EPPB) enables access to CoreSight-compatible debug and trace components, in the system connected to the processor.

ATB Interfaces

The ATB interface output traces information used for debugging. The ATB interface is compatible with the CoreSight architecture. See the Arm CoreSight™ Architecture Specification (v2.0) for more information.

TCM Interface

The processor can have up to two TCM memory instances, Instruction TCM (ITCM) and Data TCM (DTCM), each with a double word data width. Access to ITCM is through the ITCM 64-bit wide interface. Access to DTCM is through the 32-bit D0TCM interface and the 32-bit wide D1TCM interface. The DTCM accesses are split so that lower words always access D0TCM and upper words always access D1TCM. The size of both TCM instances is configurable, 4KB-16MB in powers of 2.

Cross Trigger Interface

The processor includes an optional Cross Trigger Interface Unit which includes an interface suitable for connection to external CoreSight components using a Cross Trigger Matrix.

MBIST Interface

The MBIST Interface is used for testing the RAMs during production test. The Cortex-M7 processor also allows the RAMs to be tested using the MBIST interface during normal execution. This is known as online MBIST.

AXIM Interface

The AXIM interface provides high-performance access to an external memory system. The AXIM interface supports use of the Arm CoreLink L2C-310 Level 2 Cache Controller. L2C-310 exclusive cache configuration is not supported.

Cortex-M7 Processor Pipeline

- 6-stage, in order, superscalar pipeline
- Integer pipe:
  - Dual shifters, dual ALUs, one MAC-capable
- Float pipe:
  - FP instructions can be dual issued with integer instructions
  - BTAC and branch predictor boost performance

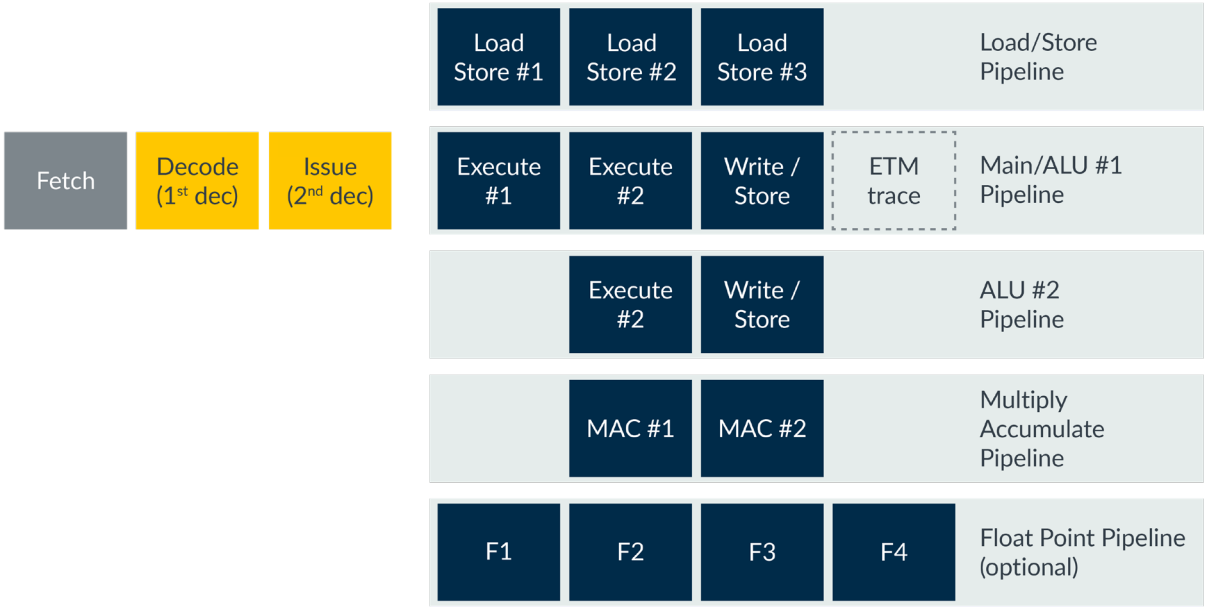

Figure 3: Cortex-M7 processor pipeline

Processor Configuration Options

The Cortex-M7 processor has configurable options that you can set during the implementation and integration stages to match your functional requirements.

Feature	Options
Floating-point	No floating-point
	Single-precision floating-point only
	Single-precision and double-precision floating-point
Instruction TCM	No instruction TCM
	4KB-16MB (powers of 2)
Data TCM	No data TCM
	4KB-16MB (powers of 2) The Data TCM is split equally into two TCMs, D0TCM, and D1TCM
Instruction cache	No instruction cache controller
	Instruction cache controller is included
Data cache	Area optimized AXIM interface, no data cache
	Performance optimized AXIM interface, data cache included
Instruction cache size	4KB, 8KB, 16KB, 32KB, 64KB
Data cache size	4KB, 8KB, 16KB, 32KB, 64KB
AHB peripheral size	64KB, 128KB, 256KB, 512MB
ECC support on caches	No ECC on instruction cache or data cache
	ECC on all implemented caches
Protected memory regions	0 region, 8 regions, 16 regions
Interrupts	1-240 interrupts
Number bits of interrupt priority	Between 3 and 8 bits of interrupt priority, 8 and 256 levels of priority
Debug watchpoints and breakpoints	Reduced set. 2 data watchpoints comparators and 4 breakpoint comparators
	Full set. 4 data watchpoints comparators and 8 breakpoint comparators
ITM and DWT trace functionality	No ITM or DWT trace
	Complete ITM and DWT trace
ETM	No ETM support
	ETM instruction trace only
	ETM instruction and data trace
Dual-redundant processor	No dual-redundant processor
	Dual-redundant processor included
Reset all registers	Only required registers that must be initialized are reset in the RTL
	All registers are reset in the RTL excluding those in the ETM, if included
	All registers are reset in the RTL including those in the ETM, if included
Cross Trigger Interface (CTI)	No CTI
	CTI included
WIC	No WIC
	WIC included

Instruction Set

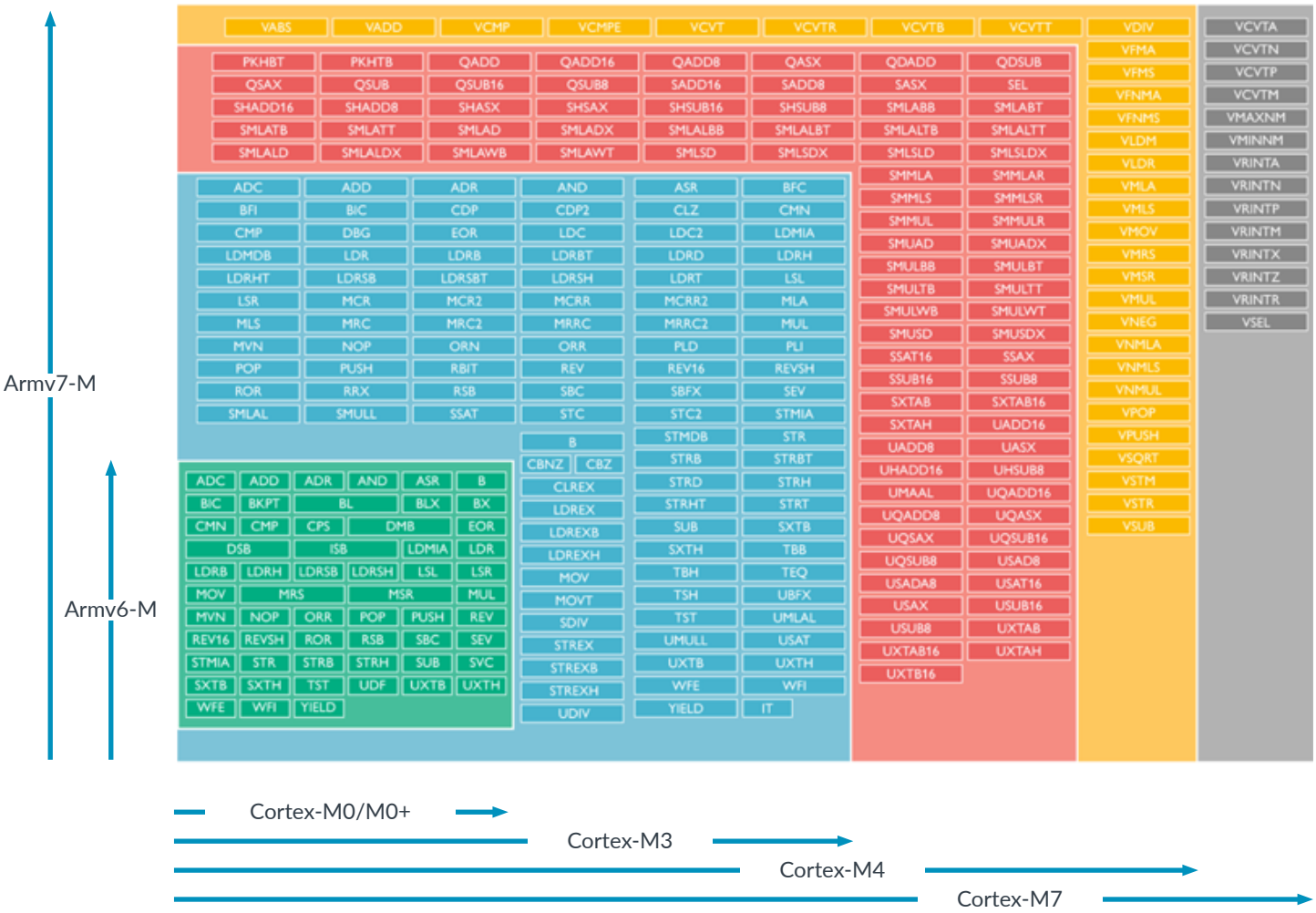

Figure 4: Instruction set

Power, Performance and Area

DMIPS	CoreMark/MHz
2.14	5.01

Configuration	40LP RVT, 9 track, C50, Typical, 1.1V, -40°C		28HT SVT, 9 track, C30, Typical, 0.9V 85°C		16FFC SVT, C16/C24. Typical, 0.72V 85°C	
	Area mm^2	Power µW/MHz	Area mm^2	Power µW/MHz	Area mm^2	Power µW/MHz
Minimum cacheless configuration @100MHz	0.105	58.5	0.052	31.8	0.028	18.5
Typical configuration (32 I/D cache, ECC @100Mhz	0.213 (core) 0.261 (memory)	72.2 (core) 46 (memory)	0.108 (core) 0.127 (memory)	41.4 (core) 15.8 (memory)	0.055 (core) 0.092 (memory)	26 (core) 16 (memory)

Max Freq	40LP ULVT, 12 track, C40, typical 0.99V, -40°C	28HPM LVT, C30, 12 track, typical 0.9v, 85°C	16FFC ULVT, C20, 7 track, typical 0.72V, 85°C
Typical configuration (32KB I/D cache, ECC)	400 MHz	1.1 GHz	1.4GHz

Additional Technical documents

1. Cortex-M7 Technical Reference Manual - TRM

2. Cortex-M7 Integration and Implementation Manual – available as part of the Bill of Materials

3. Armv7-M Architecture Reference Manual - Arm

4. CoreSight ETM-M7 Technical Reference Manual - ETM

Glossary of Terms

AHB	Advanced High-Performance Bus
AHBD	AHB-Lite Debug
AHBP	AHB-Lite Peripheral
AHBS	AHB-Lite slave
ALU	Arithmetic logic units
APB	Advanced Peripheral Bus
ATB	Advanced Trace Bus
AXI	Advanced Extensible Interface
BIC	Bus Interface Unit
BTAC	Branch Target Address Cache
CTI	Cross Trigger Interface Unit
DCLS	Dual Core Lock-step
DMA	Direct Memory Access
DMIPS	Dhrystone Million Instructions per Second
DPU	Data Processing Unit
DSP	Digital Signal Processing
DTCM	Data Tightly Coupled Memory
DWT	Data Watchpoint and Trace
ECC	Error Correction Code
EPPB	External Private Peripheral Bus
ETM	Instruction TraceEmbedded Trace Macrocell
FPU	Floating-point Unit
IEEE	Institute of Electrical and Electronics Engineers
ITCM	Instruction Tightly Coupled Memory
ITM	Instrumentation Trace
JTAG	Joint Test Action Group
LSU	Load Store Unit
MAC	Multiply Accumulate
MBIST	Memory Built-in Self-Test
MHz	Megahertz
MPU	Memory Protection Unit
MTB	Micro Trace Buffer
NMI	Non-maskable Interrupt
NVIC	Nested Vectored Interrupt Controller

PFU	Prefetch Unit
PPB	Private Peripheral Bus
QoS	Quality of Service
ROM	Read Only Memory
RTL	Register Transfer Level
SIMD	Single Instruction, Multiple Data
SRAM	Static RAM
SRD	Sub Region Disable
SWD	SingkleSingle Wire Debug
SWO	Single Wire Output
TCM	Tightly Coupled Memory
TCU	Tightly Coupled Interface Unit
TPA	Trace Port Analyzer
TPIU	Trace Port Interface Unit
WFE	Wait for interrupt
WFI	Wait for event
WIC	Wake-up Interrupt Controller
WT/WB	Write Through/Write Back

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