**Vol. 10(35), Jan. 2020, PP. 4518-4527**

Contents list available at IJMEC

International Journal of Mechatronics, Electrical and Computer Technology (IJMEC)

Journal Homepage: www.aeuso.org

PISSN: 2411-6173 - EISSN: 2305-0543

# A New10-bit SAR ADC with Energy-Efficient Switching in 0.35µm Process

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***Abstract***

This paper presents a novel method based on the reducing switches and capacitors at the output voltage DAC ($V_{dac}$) node, by selecting and applying the resistor string taps with the new technique on the SAR ADC's structure, as well. Simply, in the proposed technique, by decreasing the switches and capacitors of the $V_{dac}$ node, it is capable to achieve a low settling time and low power consumption of 10-bit SAR ADC compared to the conventional similar methods and works, as well. Therefore, it is noteworthy that, by utilizing the proposed method to achieve a 10-bit accuracy, it is required just 63 switches instead of 1024 switches at the $V_{dac}$ node, noticeably. The total power consumption of the proposed 10-bit SAR ADC is 9.66mW at power supply of 3.3 volts. The ADC shows a Signal-to-Noise-Distortion Ratio (SNDR) of 56.29 dB and an Effective Number of Bits (ENOBs) of 9.03bits at 2MS/s, respectively. Simulation results of the proposed SAR ADC are simulated using the HSPICE BSIM3 model of a standard 0.35µm CMOS process at power supply of 3.3 volts.

***Keywords:*** *Analog-to-digital converter (ADC), comparator, digital-to-analog converter (DAC), Successive Approximation Register (SAR)*

## I. INTRODUCTION

Analog-to-digital converters (ADCs) convert analog measures to digital language, which are characteristic of most phenomena in the actual world, used in computing, processing, data transmission, and control systems, as well [1-8]. Due to the high importance of ADC in circuits, there are many ways in which analog-to-digital conversion can be done. Some of the well-known architectures can be categorized as follows: counter type ADC, Flash ADC, pipeline, delta-sigma, Dual slope ADC and SAR ADC [1, 2, 8-10]. High resolution, high speed, and power efficient ADCs are used in many fields, including digital sampling oscilloscopes, biomedical acquisition, wireless communications, sensor applicable areas, and radio astronomy [1, 5, 7, 9-11]. Among various mentioned architectures, successive approximation register (SAR) ADC is more applicable ADC due to the benefits described below: It is the one widely used for accurate and medium speed conversion of Analog signals as well as low power consumption applications [1, 10, 12, 13]. It has simple structure and medium to high resolution and also high power efficiency due to the minimal



***Article History:***
**Received Date: Apr. 14, 2019**
**Accepted Date: Jun. 12, 2019**
**Available Online: Jan. 01, 2020**

use of analog building blocks, such as an open-loop comparator [4, 9, 14]. In principle, SAR ADC can be designed with no static power consumption. Most side elements are passive and digital. Meanwhile, the major portion of the SAR ADC construction is digital in nature and the analog part contains switched capacitor circuits and dynamic comparators. These circuits have zero steady-state current consumption which helps to design a SAR ADC with very low power budget [3, 9, 12, 14]. One of the conventional ways to increase the accuracy of ADCs is using arrays of capacitors. It is notable that the size of the capacitance has an exponential growth with the improvement of accuracy. Therefore, despite its advantage, it will have problems such as increased chip area and capacitor mismatches that lead to resolution limitation for SAR ADCs [3, 5, 9, 11, 14]. In order to improve the performance of an ADC, its components must be examined and improved individually. Since, the accuracy of ADC is mainly depending on the precision of DAC matching component and comparator's ability to resolve small change difference between input and output of DAC. In the other case, the speed of ADC is directly depending on the settling time of both DAC, comparators, the speed of SAR ADC and so on [1, 3, 9, 10, 12, 14, 15].

In this paper, a novel method for selecting resistor string taps of the SAR ADC's structure is presented. Reliably, in the proposed technique, by reducing $V_{dac}$ node capacitor, it is capable to achieve a low power consumption of 10-bit SAR ADC compared to the conventional similar works, as well. The main advantages of this method are reducing the capacitor of resistor string DAC's output node and settling time of the $V_{dac}$ clearly.

This paper is organized as follows: In section II, the proposed SAR ADC structure is discussed. Simulation results of the ADC is presented in section III. and finally, section IV concludes the paper.

## SAR ADC STRUCTURE

The SAR ADC usually consists of a sample and hold stage, a comparator, a DAC and a successive approximation register, and it mainly implements a binary search algorithm [1-3, 9, 10, 12, 14].

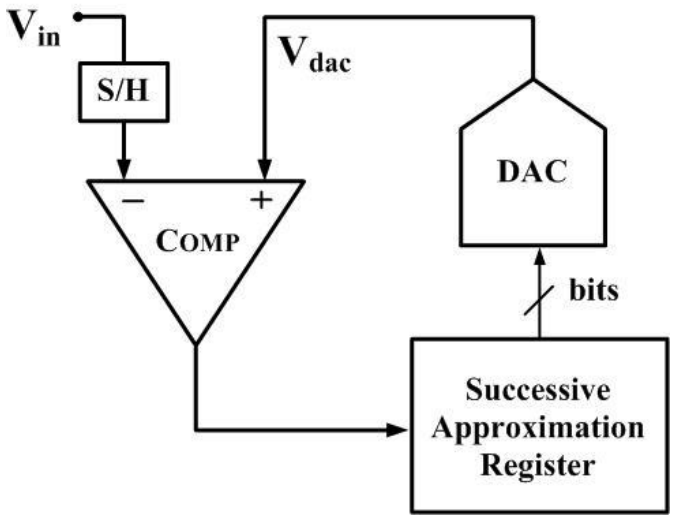



**Fig. 1.** A block diagram of SAR ADC

### *A. Proposed structure*

In this paper, a new technique for selecting taps of resistor string DAC in the SAR ADC is presented to decrease number of the switches and reduce the $V_{dac}$ node capacitor for better settling of $V_{dac}$ voltage signal. Block diagram of the proposed SAR ADC structure is shown in Fig. 2. In the algorithm of the proposed structure, the operation of extracting digital bits is performed in two steps. For the better explanation, suppose that, the n-bit extraction is desired; in Step 1, firstly extraction of the MSB (n/2)-bit is done, now, the extracted bits from Step1 requires (n/2) timing signals, to select the correct region for the Step2. Finally, in Step2, LSB (n/2)-bit is extracted as similarly. So by utilizing this technique, number of the switches connected to the $V_{dac}$ node is decreased from $2^n$ to $(2^{(n/2)} -1) + 2^{(n/2)}$, reliably.

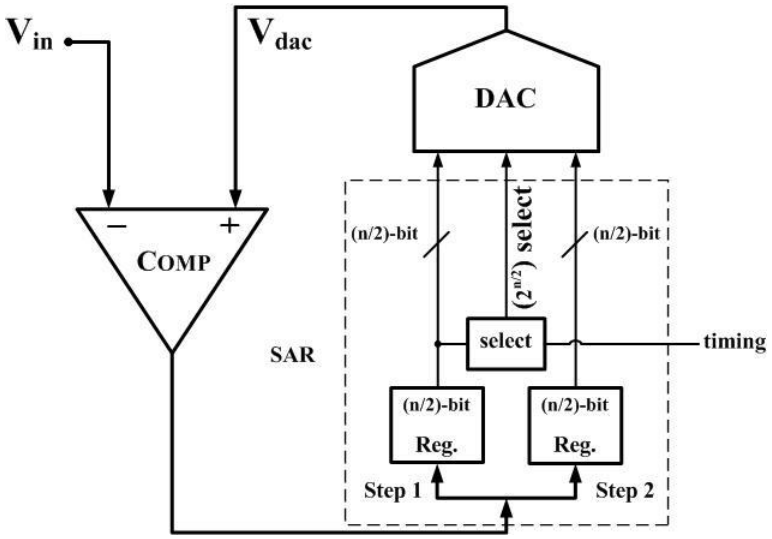
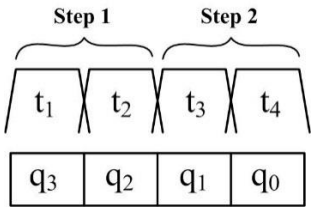


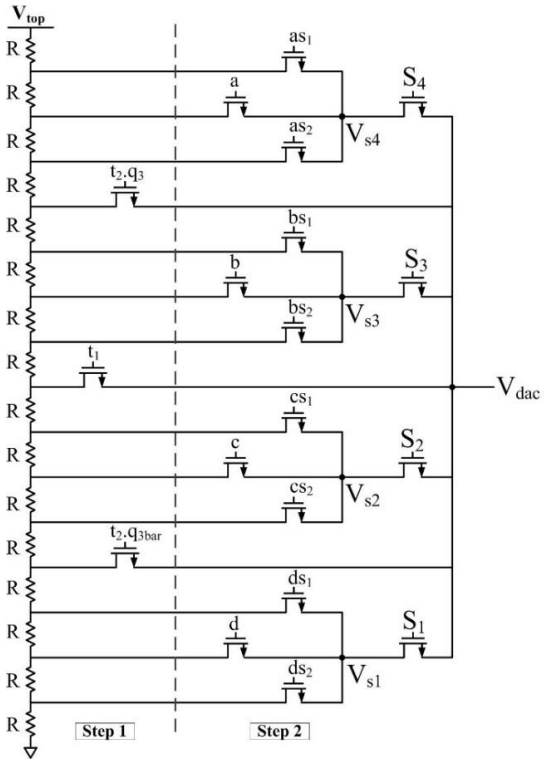

**Fig. 2.** A block diagram of Proposed SAR ADC Structure

### *B. Proposed DAC structure*

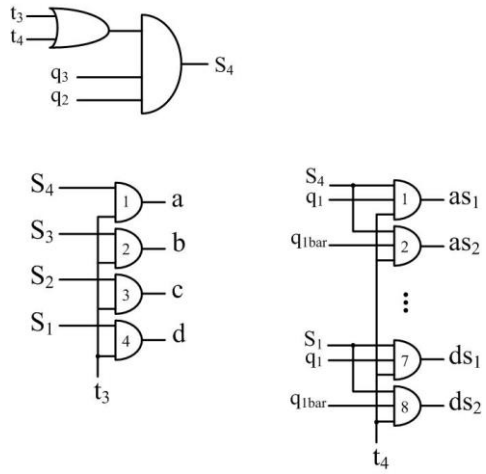
For better explanation of the proposed idea, by considering n=4 as an example, which is shown Fig. 3. Meanwhile, Fig. 3.(a) and Fig. 3.(b) show timing diagram and a four bits resistor string DAC structure, respectively. To show that circumstance of the reducing $V_{dac}$ node switches and capacitors, also, Fig. 3.(c) illustrates the gate level circuits for generating controlling signals in order to select resistor string DAC taps as well. Clearly, the structure's performance is examined as follows. In step1, two MSB bits are extracted. By these two extracted bits along with the t3 and t4 timings, 4-select signals are extracted to select each of the four regions that the switch of each region is connected to each of $Vs_{1\text{-}4}$ nodes, also each of these $Vs_{1\text{-}4}$ nodes is connected via a switch to $V_{dac}$ node. Therefore, in this case, there will be 7 switches, instead of 15 switches, in $V_{dac}$ node, as well. Consequently, by decreasing number of the switches of this node, capacitor of this node will be decreased, so the settling time of $V_{dac}$ node is decreased, too.




(a)




(b)



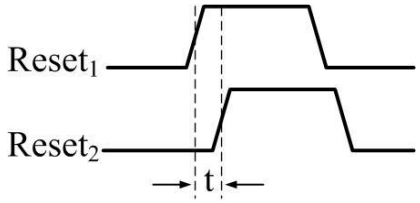

(c)

**Fig. 3.** (a) Timing diagram. (b) Proposed DAC structure for 4-bit. (c) Gate level circuits

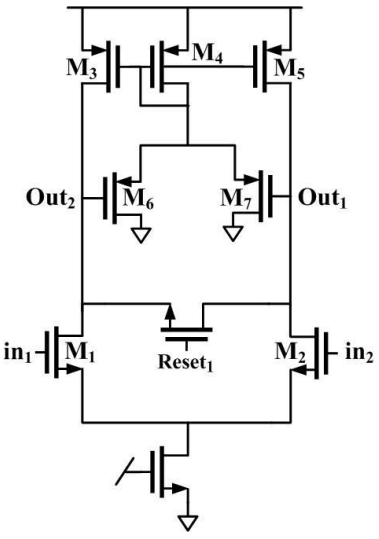
Finally, the main purpose of this paper is to extract 10-bit accuracy, so in step 1, 5-bit MSB is extracted. By using this 5-bit MSB and 5 timings ($t_{6\text{-}10}$), extraction of 32 select signals is performed to select 32 regions that each of the regions has a value of 5-bit. As explained in the above example, each of the regions is connected to one of the $Vs_{1\text{-}32}$ nodes, which are connected to the $V_{dac}$ node by 32 switches. Therefore, by using this method, to achieve 10-bit accuracy, instead of 1024 switches in the $V_{dac}$ node, 63 switches are required, which causes a reduction in the $V_{dac}$ output node capacitor, and as a result, the DAC output signal, at the $V_{dac}$ node, is better settled, as well.

### *C. Comparator*

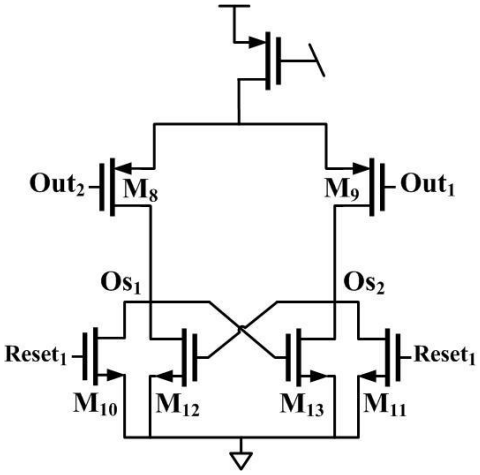
The comparator used in the proposed structure has 3 stages as shown in Fig. 4. The first stage in Fig. 4.(b), is pre-amplifier and has two outputs, $out_1$ and $out_2$, that are given to the inputs of the first latch stage in Fig. 4.(c), and the outputs of the first latch stage, $Os_1$ and $Os_2$, are given to the inputs of the 2nd Latch stage Fig. 4.(d) and final outputs, $O_1$ and $O_2$, are produced at this stage. In order to identify and amplify of the output signal, which is shown in Fig. 4.(a), the $reset_2$ signal used for resetting the third stage is applied with a slight delay compared to the $reset_1$ signal which used to reset the first and second classes.



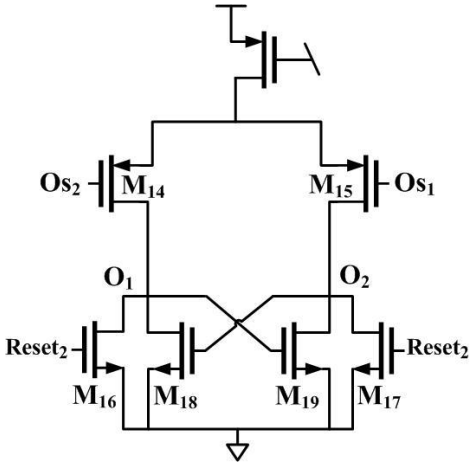

(a)




(b)




(c)




(d)

**Fig**. 4. (a) Reset timings. (b) Pre-Amplifier. (c) 1st Latch stage. (d) 2nd Latch stage[16]

## SIMULATION RESULTS

The simulation results of the proposed 10-bit SAR ADC is presented in this section. The behavioral input signal, digital codes, Sample and Hold (S/H) and DAC voltage signals are indicated in Fig. 5, clearly. The output FFT spectrum of the ADC by considering the different value for the Number of Point (NP) parameter such as 64, 128, 256, 512 are shown in Fig. 6, Fig. 7, Fig. 8 and Fig. 9, respectively. As simulation results prove that, the Signal to Noise Ratio ( SNR) and Effective Number of Bits (ENOB) are almost near to 56 dB and 9-bit in all the Figs, respectively.The performance of the proposed 10-bit SAR ADC is presented in Table I, also comparison table is given in Table II. The proposed paper, has been designed and simulated in 350nm CMOS process BSIM3 model of HSPICE with the power supply of 3.3 volts.

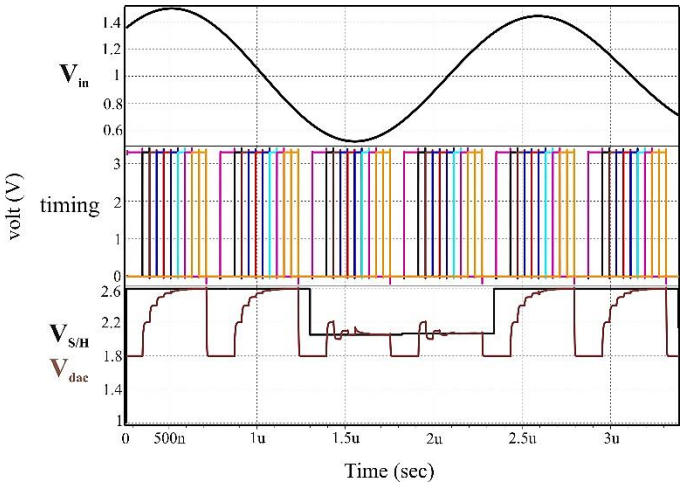



**Fig. 5.** The input voltage signal,digital codes, and the voltage signals of S/H and DAC

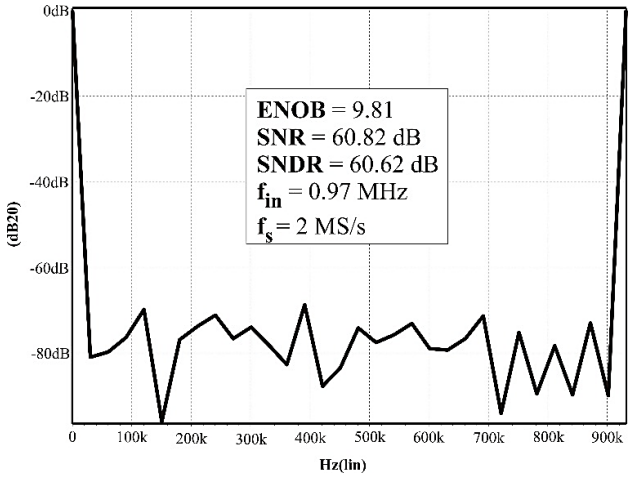



**Fig. 6**. The output FFT spectrum of the proposed ADC in nyquist input with considrenig the value of the number of NP= 64

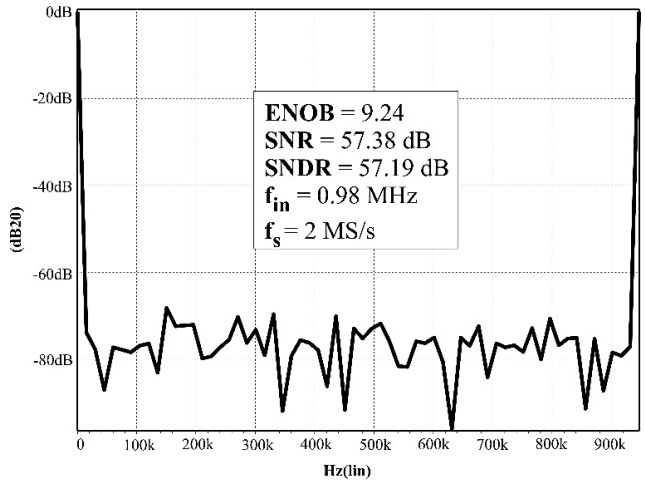



**Fig. 7.** The output FFT spectrum of the proposed ADC in nyquist input with considrenig the value of the number of NP= 128

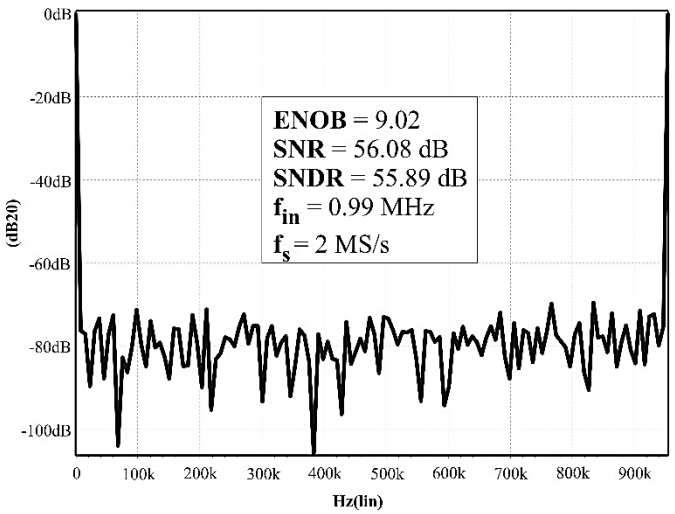



**Fig. 8.** The output FFT spectrum of the proposed ADC in nyquist input with considrenig the value of the number of NP= 256

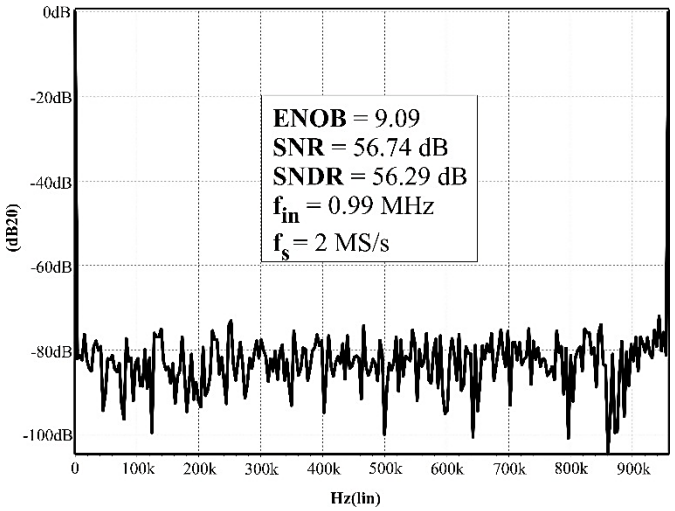



**Fig. 9.** The output FFT spectrum of the proposed ADC in nyquist input with considrenig the value of the number of NP= 512

## IV. CONCLUSION

This paper presents a novel method based on the reducing switches and capacitors at the output voltage DAC ($V_{dac}$) node, by selecting and applying the resistor string taps with the new technique on the SAR ADC's structure, as well. Simply, in the proposed technique, by decreasing the switches and capacitors of the $V_{dac}$ node, it is capable to achieve a low settling time and low power consumption of 10-bit SAR ADC compared to the conventional similar methods and works, as well. Therefore, it is noteworthy that, by utilizing the proposed method to achieve a 10-bit accuracy, it is required just 63 switches instead of 1024 switches at the $V_{dac}$ node, noticeably. The total power consumption of the proposed 10-bit SAR ADC is 9.66mW at power supply of 3.3 volts. The ADC shows a Signal-to-Noise-Distortion Ratio (SNDR) of 56.29 dB and an Effective Number of Bits (ENOBs) of 9.03bits at 2MS/s, respectively. Simulation results of the proposed SAR ADC are simulated using the HSPICE BSIM3 model of a standard 0.35µm CMOS process at power supply of 3.3 volts.

**TABLE** I. PERFORMANCE OF THE PROPOSED SAR ADC

| Specifications | Value |
|---|---|
| **Technology (nm)** | 350 |
| **Resolution (bits)** | 10 |
| **Sampling Rate(MS/s)** | 2 |
| **Supply Voltage(V)** | 3.3 |
| **Power Consumption(mW)** | 9.66 |
| **SNR(dB)** | 56.74 |
| **SNDR(dB)** | 56.29 |
| **ENOB(bits)** | 9.09 |

**TABLE** II. COMPARISON TABLE

| Specifications (Unit) | [7] | [8] | [13] 7-bit SAR | This work |
|---|---|---|---|---|
| **Technology (nm)** | 180 | 45 | 180 | 350 |
| **Resolution (bits)** | 12 | 9 | 7 | 10 |
| **Sampling Rate (MS/s)** | 0.1 | 100 | 2.78 | 2 |
| **Supply Voltage (V)** | 3.3 | 1 | 1.8 | 3.3 |
| **Power Consumption(mW)** | 2.04 | 6.1 | 4 | 9.66 |
| **SNR (dB)** | - | - | - | 56.74 |
| **SNDR (dB)** | 62.13 | - | 39.8 | 56.29 |
| **ENOB(bits)** | - | - | 6.22 | 9.09 |

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