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FINAL REPORT

FOR

BREADBOARD LINEAR ARRAY SCAN IMAGER PROGRAM

(Contract NAS 5-21806)

25 April 1975

For

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Goddard Space Flight Center
Greenbelt, Maryland

By

WESTINGHOUSE DEFENSE AND ELECTRONIC SYSTEMS CENTER
Systems Development Division
Baltimore, Maryland

75-0298A

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PREFACE

This document is the Final Report for Contract NAS 5-21806, entitled Breadboard Linear Array Imager Program. The report describes the objectives, approach, implementation, and test results of the program.

The objective of the program is to evaluate the performance of large scale integration (LSI) photodiode arrays in a linear array scan imaging system breadboard for application to multispectral remote sensing of the Earth's resources.

The Final Report is submitted in compliance with Deliverable Item 5a, Final Report of NASA Goddard Space Flight Center, Contract NAS 5-21806. The final report was prepared in accordance with GSFC specification S-250-P-1C, March 1972, entitled "Contractor-Prepared Monthly, Periodic, and Final Reports."

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LIST OF ILLUSTRATIONS

LIST OF ACRONYMS

CMOS	Complementary Metal Oxide Semiconductor
ERTS	Earth Resources Technology Satellite
HPBW	Half Power Band Width
IFOV	Instantaneous Field-of-View
LSB	Least Significant Bit
LSI	Large Scale Integration
MHP	Multichip Hybrid Package
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOST	Metal Oxide Semiconductor Technology
MTF	Modulation Transfer Function
NEI	Noise Equivalent Irradiance
OPD	Optical Path Difference
RMS	Root-Mean-Square
RSS	Root-Sum-Square
SNR	Signal-to-Noise Ratio
TTL	Transistor-Transistor Logic

1728 DETECTOR PHOTODIODE LINEAR ARRAY

ANALOG PROCESSOR-MULTI-HYBRID PACKAGE (MHP) ELECTRONICS

DATA RECORDER

IMAGE

OPTICAL BENCH

GENERAL PURPOSE COMPUTER

IMAGE RECORDER
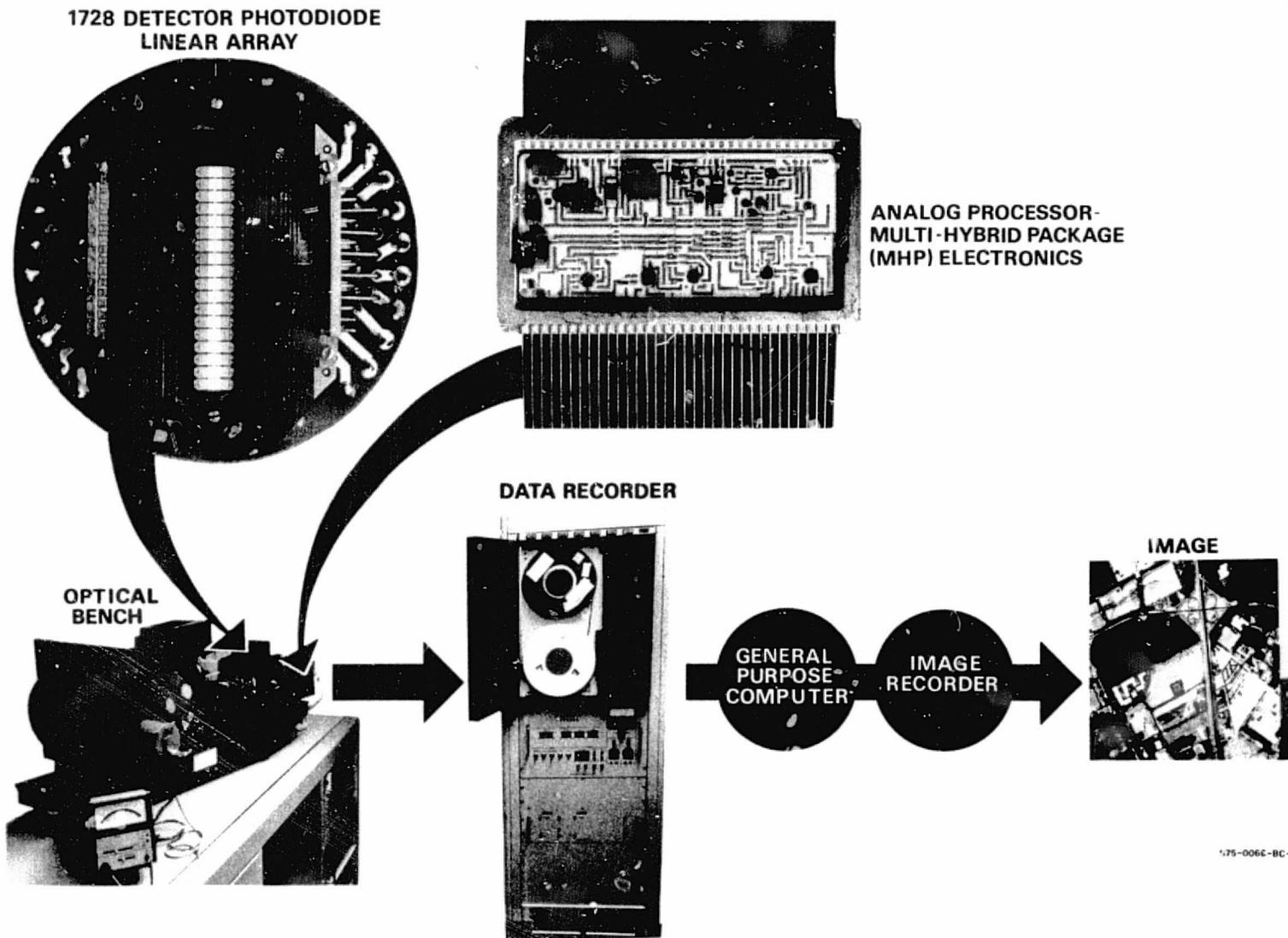
Frontispiece. Breadboard Linear Array Imager Program

1. BACKGROUND

In the evolutionary development of earth observation sensors, demands on improving reliability and resolution are ever present. The use of a long array of photodetectors in the image plane of a geocentric stabilized space-borne telescope used in the "pushbroom" scanning mode offers the opportunity to achieve both higher reliability and finer resolution. Improved reliability is achieved by the elimination of complex mechanical scanning mechanisms using point detectors, and finer resolution is achieved by increasing the number of detectors in the image plane per picture width.

The advent of large scale integration (LSI) CMOS (Complementary Metal Oxide Semiconductor) technology has allowed the inclusion of detector sampling and commutation circuitry on the same chip[1] as the silicon diode photodetectors. Heretofore, the use of conventional interconnection techniques made it impossible to connect the large quantity of photodetectors to subsequent signal processing circuitry. Thus, the application of pushbroom scanning using long arrays[1] of photodetectors has become a viable technique for future flight sensors.

The Breadboard Linear Array Scan Imager program was begun to exploit this emerging technology. The goal of the program is to demonstrate through experimentation and testing that the technology is feasible for use in future high resolution multispectral imaging sensors for earth and ocean survey applications.

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[1] The term chip used in this report is the component containing 96 photodetectors and associated electronic circuitry (see figure 1). An array is a contiguous line of chips.

1.1 INTRODUCTION

Solid-state linear array photodetector technology is being put to use to develop electronically-scanned multispectral imaging systems. Experience has shown that assembling discrete photodetectors into a long array produces a complex maze of wiring to access each detector element. Thus, a monolithic approach has been developed which results in a single substrate with many detectors interconnected within the chip. The detector outputs are multiplexed onto a few output lines minimizing the physical wiring required. A shift register provides time multiplexing of detectors and is within the chip to reduce the number of physical connections. The chip used on this program has 96 photodetectors and on-chip signal processing provides spatial sequential output time sharing on four common output lines. The chip requires less than two dozen external wires to be attached. Each chip is capable of being physically butted to provide a continuous line of photodetectors of thousands of resolution elements per line. Multiple chip sharing of the data output lines is possible by serially connecting the shift registers of butted chips, thus reducing external processing requirements to a minimum. The use of this approach allows the development of solid-state imaging systems with thousands of resolution elements requiring no mechanical scanning.

To investigate the characteristics and capabilities of fabricating solid-state arrays, NASA/GSFC issued contract NAS 5-21806, entitled Breadboard Linear Array Imager Using LSI Solid-State Technology, in July 1972. The governing technical specification and statement of work is included in NASA-GSFC document S-731-P-128, Specification for a Breadboard Linear Array Imager Using LSI Solid-State Technology, dated January 1972.

The original contract includes the design, fabrication, and test of a 576-detector element array. In late 1973, a contract change order was received to design, fabricate, and test an 18-chip (1728 detector) linear array which has been completed. In accordance with contract requirements, a test plan document was prepared and used as the test criteria for performance evaluation. The final system test program on the 6-chip array was completed in

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June, 1973. A similar test program was completed on an 18-chip array in February, 1974.

In June of 1974, a second contract change order was received to design, fabricate, and test multichip hybrid package (MHP) analog processing circuits and to perform a study to determine improved techniques for mechanically aligning linear photodiode detectors in long arrays. The goal of the MHP analog processor development was to provide a design which would more closely achieve detector-limited noise performance. The work performed on the multichip hybrid package analog processing circuits is discussed in paragraph 2.4.2.2. The array fabrication improvement study is included in paragraph 2.6.

1.2 SUMMARY OF RESULTS

The results of the Breadboard Linear Array Scan Program Imager Program have conclusively shown that photodiode linear arrays can be applied to multispectral remote sensing of earth resources. A summary table including the performance objective and the actual performance achieved on the program is shown in table 1, Summary of Results. The table also includes a reference to the paragraph number or appendix that discusses the source of the performance data.

TABLE 1

SUMMARY OF RESULTS

Performance Objective or Functional Evaluation (Spec S-731-P-128 par No.)	Performance/Evaluation Obtained
Noise (par. 3.1)	System level NEI (equivalent to 0.4 to 0.8 μm band) $\cong 1.4 \mu J/m^2$ (see par. 2.5.1.1)
Spectral Response (par. 3.1)	Typical silicon photodiode response (see par. 2.5.1.6)
Dynamic Range (par. 3.1)	Greater than 600:1; (see par. 2.5.1.4)
Calibration Problems (par. 3.1)	Image streaking due to thermal drift in array temperature (see par. 2.5.2.5)
Image Artifacts (par. 3.1)	Artifacts due to geometrical and electrical characteristics (see par. 2.5.2)
Cross Talk Between Detectors (par. 3.1)	Not detectable (see par. 2.5.1.5)
Reliability (par. 3.1)	Detectors meet Mil-883 level B; see Appendixes C and D for failure analyses
Temporal Characteristics	No apparent long-term (six-months) temporal problems, although a precise assessment of performance was not possible in laboratory environment (see appendix G)
Obtain Imagery	Extensive image production and evaluation was obtained (see par. 2.5.1.7)
Determine Array Fabrication Problems	Primary fabrication problem was found to be chip handling and intricacy of alignment (see par. 2.4.7.2). Corrective techniques discussed in par. 2.4.3.2 and par. 2.6
Performance Goals (par. 4.1)	
● 500 elements (later changed to 1728)	Three arrays were fabricated (two each 576 and one each 1728 detectors/array) (see par. 2.4.3.1)
● Four Spectral Bands (par. 4.2)	Spectral bands were: (1) 0.50 – 0.58 μm (2) 0.62 – 0.68 μm (3) 0.73 – 0.81 μm, and (4) 0.8 – 1.1 μm. See par. 2.4.1.3
● Radiance Conditions (par. 4.3)	Various radiance conditions used. (see par. 2.4.1.2)
● SNR_1 Goal 22 (par. 4.4)	For 0.5 – 0.6 μm band, system SNR of 40 was achieved for low radiance, low spatial frequency target (see par. 2.5.1.1)
● SNR_2 Goal 2 (par. 4.4)	For 0.5 – 0.6 μm band, system SNR of 4 was achieved for low contrast, high spatial frequency (see par. 2.5.1.1)
MTF Along Scan and Across Scan	The detector geometry was chosen to provide equal MTF along and across track. (see figure 9)
Radiometric Accuracy, 5 percent of High Radiance, (par 4.6)	HP 8330A radiometer calibration shows absolute uncertainty of better than 5 percent (see Appendix I)
Detector Geometric Linearity of 1 percent (par. 4.7)	Array chips positioned to within less than 1 percent of array length (see par 2.6.2)
Chip Alignment	Chip alignment of 1/4 resolution element was achieved (see par. 2.6.2)
NEI (Noise Equivalent Irradiance) of Detector to be Less Than 1.2 $\mu J/m^2$	The mean detector noise is less than 1.2 $\mu J/m^2$ (see par. 2.5.1.1)
Linearity Within 2 percent of Best Fit Line (par. 5.6)	Linearity measurements and detector data indicate a 2 sigma variation of less than 3 percent of full signal from a best fit line (see par. 2.5.1.2)
Detector Requirements: (par. 5.7)	
○ < 5 percent Element-to-Element Variation After Processing	For the signal quantization interval (approx. 30 to 50 intervals full scale signal) and 2 calibration levels and irradiance used this exceeds limit (peak error of 6 percent)
● No Dead Elements	Chip manufacturing data provided on 30 chips used on this program indicated only one bad element for all chips.
● End Elements to have Response of > 60 percent Mean Full Scale	Most of the chips used for this program had an end element response better than 60 percent of the mean response; however, limited availability of chips made this parameter an impractical selection criteria.

75-0298-TB-65-1

2. TECHNICAL REPORT

2.1 PROGRAM OBJECTIVE

The objectives of the program as stated in the Technical Specification are:

- To evaluate the performance of LSI photodiode arrays in a linear array scan imaging system. Emphasis will be placed on determining noise characteristics, calibration problems, spectral response, dynamic range, image artifacts, crosstalk between contiguous detectors, reliability, and temporal performance.

- To evaluate total system performance, especially for conditions simulating ERTS scenes.

- To provide high quality images from the camera system.

- To determine fabrication problems associated with making long arrays from many short arrays.

2.2 PERFORMANCE OBJECTIVES

The Technical Specification contains a listing of system performance objectives which are summarized below:

- Minimum of 500 detectors per array (this was later changed to 1728 detectors)

- Four passbands of interest are 0.5-0.6 μm, 0.6-0.7 μm, 0.7-0.8 μm and 0.8-1.1 μm.

- The system is to be evaluated with nominal ERTS scene conditions as follows:

Passband (μm)	Scene Radiance (W/cm^2 - sr)	
	High	Low
0.5-0.6	2.48×10^{-3}	1.20×10^{-4}
0.6-0.7	2.00×10^{-3}	2.00×10^{-4}
0.7-0.8	1.76×10^{-3}	2.80×10^{-4}
0.8-1.1	4.60×10^{-3}	6.7×10^{-4}

- After signal processing, the system is to have a signal-to-noise ratio in excess of 22 for the low radiance conditions (0.5-0.6 μm) with a high contrast, low spatial frequency target.

- For the low radiance conditions of the 0.5-0.6 μm passband and a target contrast ratio of 2 to 1, the system is to have a SNR greater than 2 at the limiting spatial frequency.

- The modulation transfer function (MTF) (at the limiting spatial frequency) in the along-scan and across-scan direction is to be approximately equal.

- After signal processing, relative radiometric measurements are to be accurate to 5 percent of the high radiance test conditions.

- The linear dimension geometric accuracy of the detector arrays is to be maintained to one percent.

- The system is to operate at room temperature.

- The bilinear staggered self-scanned LSI detector is to have a rectangular diode aperture with a cross-track to along-track dimensional ratio of 1.3:1 with an effective sample distance of 15.24 μm. The mean value of noise equivalent signal (NEI) is to be 1.2 μJ/m² for a spectral interval of 0.4 μm to 0.8 μm for a 6000K source.

- The diode array is to have a dynamic range (in terms of input radiant energy from NEI) of 600:1.

- The detector response linearity defined as percent error from the best straight line fit to the mean response curve for the full range is not to exceed two percent.

- Objectives in detector variation are: (1) after processing, the element-to-element variation for a given video output bus on a chip shall be less than or equal to ±5 percent of the full scale response, (2) there are to be no dead elements, and (3) after processing, the end element response is to be at least 60 percent of the mean full scale response.

2.3 PHOTODETECTOR ARRAY CHIP

The photodetector chip used on the breadboard linear array program is an array of 96 photodiodes on 0.6-mil centers with the associated electronics necessary to form an array of light detectors for image scanning (see figure 1). The scene image is formed by periodically sampling each photodiode in the line array. The on-chip electronics furnishes the first level of preamplification and the multiplexing necessary to periodically sample each sensor

57.6 MILS
(≈1.46 mm)

210 MILS (≈5.33 mm)

BONDING
PADS

SHIFT
REGISTER

AND GATES

AMPLIFIERS
AND
RESET SWITCHES

DIODE ARRAY

AMPLIFIERS
AND
RESET SWITCHES

AND GATES

SHIFT
REGISTER

BONDING
PADS

22 μm   7.5 μm

15 μm   75 μm   15 μm

75-0298-PB-6
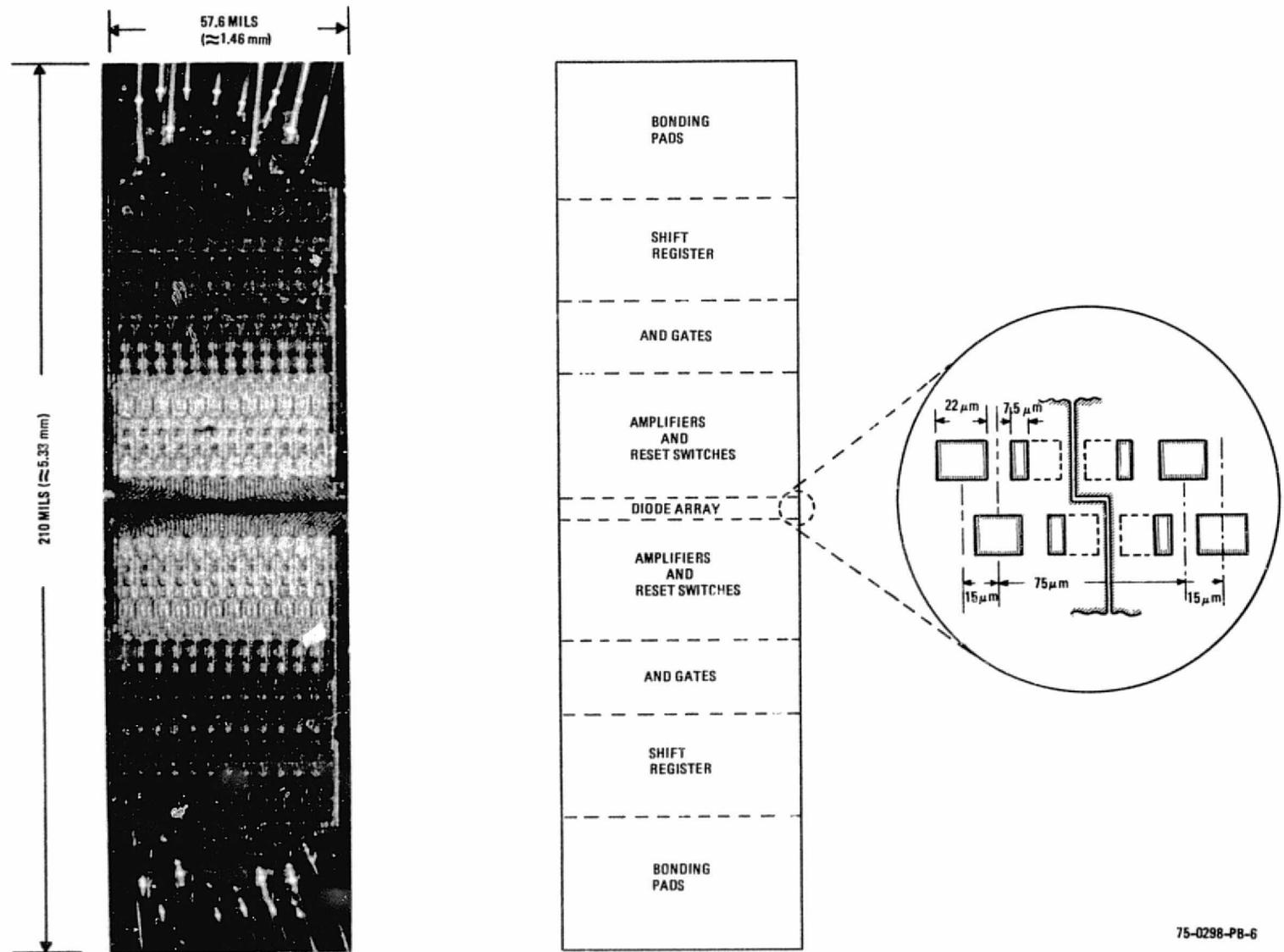
Figure 1.   96-Photodiode Detector Chip Showing Associated
Electronics and Geometry

and commutate the sensor outputs onto one of four output buses. The chips are fabricated using the complementary metal-oxide insulated-gate semiconductor transistor technology (MOST) which is compatible with the diode fabrication.

A schematic diagram of the chip is shown in figure 2. To perform the functions necessary of the array, a sensor, amplifier, and address and control circuitry are associated with each diode position in the line array. The photodiode, operating in the integration mode, and a reset switch form the sensor whose output is taken from the node between the two devices. The output of the sensor is connected to the gate of a single MOST whose drain current is the measured variable commutated to the output line. The address circuitry consists of a shift register stage and an AND gate to control the reset switch.

The schematic diagram of the detector and the amplifier is shown in figure 3 where Q_1 is the reset switch, Q_2 is the amplifier, Q_3 is the amplifier commutating switch, and the external amplifier is the output current detector.

The photodiode detector is operated in the integration mode. Initial conditions for the integration mode are established when the photodiode is reverse biased by switching Q_1 on. When Q_1 is switched off, the photodiode remains reverse biased because of the charge stored on the input capacitance of the amplifier, the parasitic capacitance of the interconnects and the reset switch, and the capacitance of the diode itself. The rate with which this voltage will decay toward zero is proportional to the leakage of the diode, the parasitic leakage of the node, and the light proportional reverse current of the photodiode. After a period t, Q_1 is again turned on and the capacitance is recharged. This mode of operation ensures that the diode is detecting during the entire period between reset pulses and offers an efficiency proportional to the ratio of the integration period to the total period from reset pulse to reset pulse. The measure of irradiance may be the peak recharge current,

8
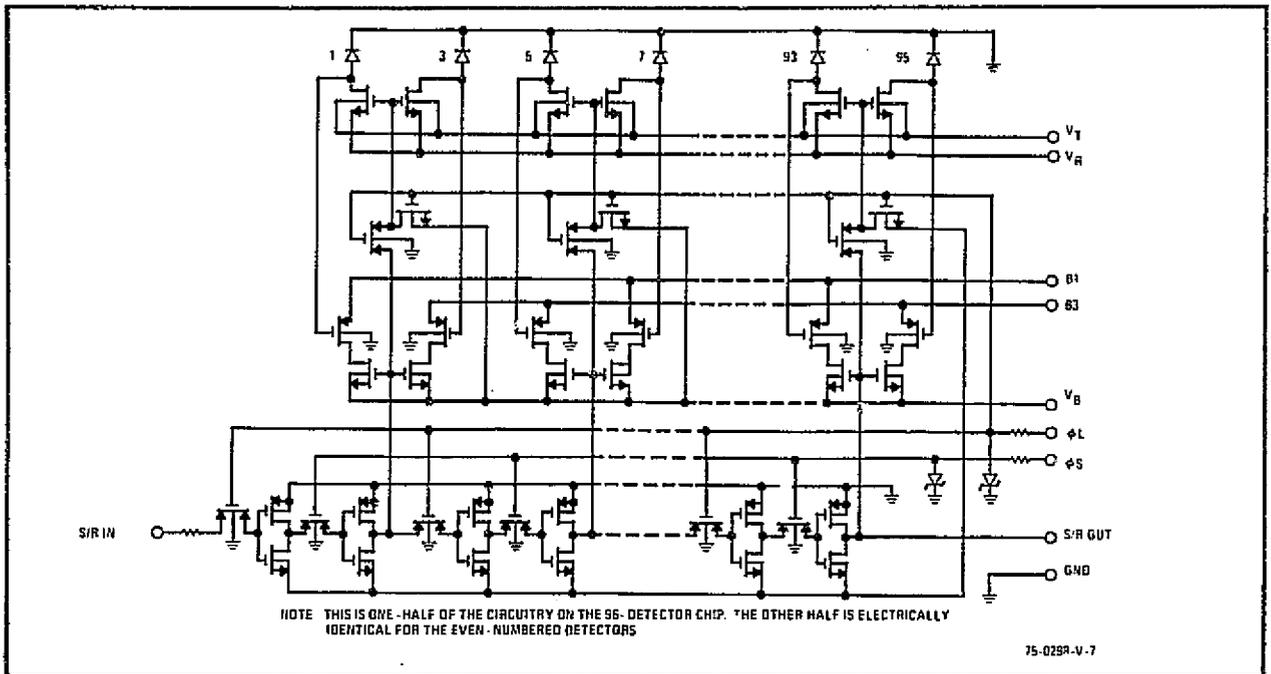
Figure 2. Schematic Diagram of 96-Detector Chip
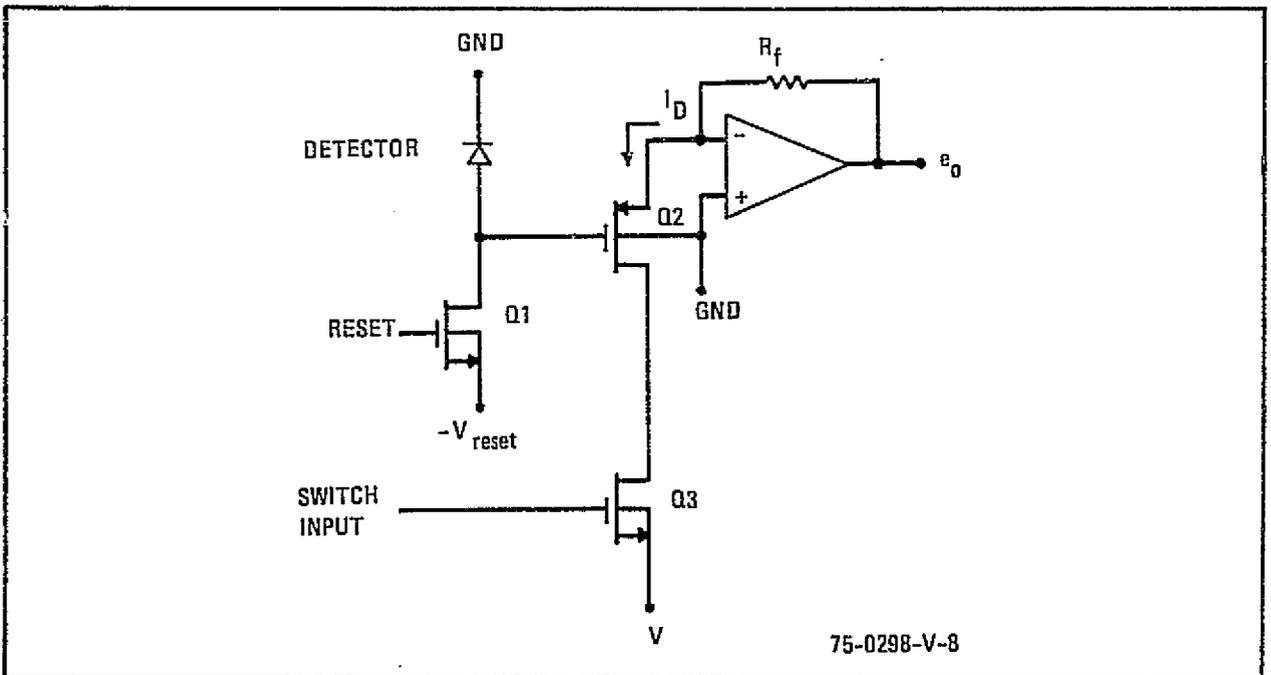
Figure 3. Schematic of Photodiode Detector and Amplifier

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the total replaced charge, or the voltage across the diode prior to reset. This last approach is used on the 96-detector chip.

The detector amplifier is the single p-channel MOST, Q_2, shown in figure 3. The voltage between its gate and the output bus is the integrated signal which in turn determines the source current flowing through R_f (the measured variable). The series n-channel MOST, Q_3, between the supply and the amplifier enable this current to flow through the amplifier when addressed by a 1 during the sample period and inhibits the current when addressed with a 0 between samples.

Figure 3 shows that the output bus is connected to the summing point of an operational amplifier which is referenced to ground. The output bus is thus a virtual ground with an impedance of R_f/A_v. This being the case, many amplifiers may be multiplexed onto this line without channel interaction. Thus, a substantial reduction in the number of output leads is made possible. The scene energy is converted into small analog signals and thus is available for further processing.

2.4 PROGRAM IMPLEMENTATION

The principal objective of the subject program is to evaluate the performance of large scale integration (LSI) photodiode arrays in a linear array scan imaging breadboard. To perform this evaluation required the construction of a test tool capable of performing appropriate quantitative tests. The integrated test tool and evaluation program consists of the breadboard imager, computer software programs for image data processing, and display software. An overall block diagram of the entire process of image generation, detection, signal processing, data processing, and display is shown in figure 4.

This program required the design and fabrication of a test bench, the design and fabrication of detector arrays, the preparation of computer software programs, and the conduct of a test and evaluation program.

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BREADBOARD LINEAR ARRAY OPTICAL TEST BENCH

INTEGRATING HEMISPHERE LIGHT SOURCE

λ → FILTER → λ → RADIO-METER

λ → FILTER → λ → SCENE & TRANS-LATOR → λ → OPTICS → λ → DETECTOR ARRAY → ANALOG PROCESSOR → A/D CONVERTER → DATA RECORDER

TIMING & CONTROL

UNIVAC 1110 COMPUTER

DISPLAY

```
         ┌──────────┐   ┌──────────┐
         │ DETERMINE│   │  PRINT   │
         │   RMS    │──▶│   RMS    │
         │  NOISE   │   │  NOISE   │
         └──────────┘   └──────────┘
```

```
┌──────────┐  ┌──────────┐  ┌───────────┐
│ DEVELOP  │  │  STORE   │  │ IDENTIFY  │
│ 2-POINT  │─▶│   CAL    │─▶│ INOPERA-  │
│CALIBRA-  │  │          │  │  TIVE     │
│  TION    │  │          │  │ DETECTORS │
└──────────┘  └──────────┘  └───────────┘
```

```
┌──────────┐ ┌────────┐ ┌────────┐ ┌──────────┐ ┌──────────┐ ┌──────────┐
│  INPUT   │ │ STORE  │ │ REMOVE │ │NORMALIZE │ │ CORRECT  │ │ RECORD   │
│ DATA &   │▶│ IMAGE  │▶│ DARK   │▶│  GAIN    │▶│ INOPERA- │▶│ IMAGE    │
│ REMOVE   │ │        │ │ OFFSET │ │          │ │  TIVE    │ │ TAPE     │
│ STAGGER  │ │        │ │        │ │          │ │ ELEMENTS │ │          │
└──────────┘ └────────┘ └────────┘ └──────────┘ └──────────┘ └──────────┘
```

```
┌──────────────┐
│ NASA - GSFC  │
│  GROUND      │
│ RECORDING    │
│ & PLAYBACK   │
│  SYSTEM      │
└──────────────┘
```

```
┌──────────────┐
│  OPTRONICS   │
│ PHOTOWRITE   │
│ FACSIMILE    │
│  RECORDER    │
└──────────────┘
```

75 0298-V-9

Figure 4. Overall Block Diagram of Integrated Breadboard Linear
Array Scan Imager, Data Processing and Display

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The following sections of this report describe the details of program implementation. The report includes an evaluation of test results.

2.4.1 Test Bench

The test setup for the Breadboard Linear Array Program consists of the array, optics, and scene simulator mounted on an optical bench. Analog processing circuitry is situated close to the array and the analog-to-digital conversion and digital processing and timing are remotely located. A separate console contains the digital data tape recorder and its associated processing circuitry. The composite test bench and data recording system are shown in figure 5. The optical bench is shown in figure 6.

The test setup allows testing of a six-chip (576 element) array and an 18-chip (1728 element) array. Since every effort was made to minimize the processor changes to meet these two operating conditions, only a few changes were made to accommodate these conditions and are noted in the technical discussion.

2.4.1.1 Scene Simulation

The simulated scene is a 2-inch by 2-inch transparency mounted on a positioning table to form a moving target scene simulator. The table is moved across-scan (along-track motion) and scene motion is provided by a 0.1-inch lead ball screw driven by a precision stepping motor. The motor drive is synchronous with the array scan, allowing at least one full integration period to occur while the scene is stopped. It is this line of data which is processed. Each step is a fraction of a resolution element. Because of a magnification difference required for the 576-detector and 1728-detector arrays, different motor steps are required per resolution element motion of the scene. Positional accuracy is better than 2.5 percent of a resolution element per scan line and 15 percent maximum per scene due to a nonaccumulative 5 percent of motor step contributed by the motor and a 0.0005 in/ft for the lead screw. These accuracies prevent scene distortions due to the scene simulator but use standard quality components.

13
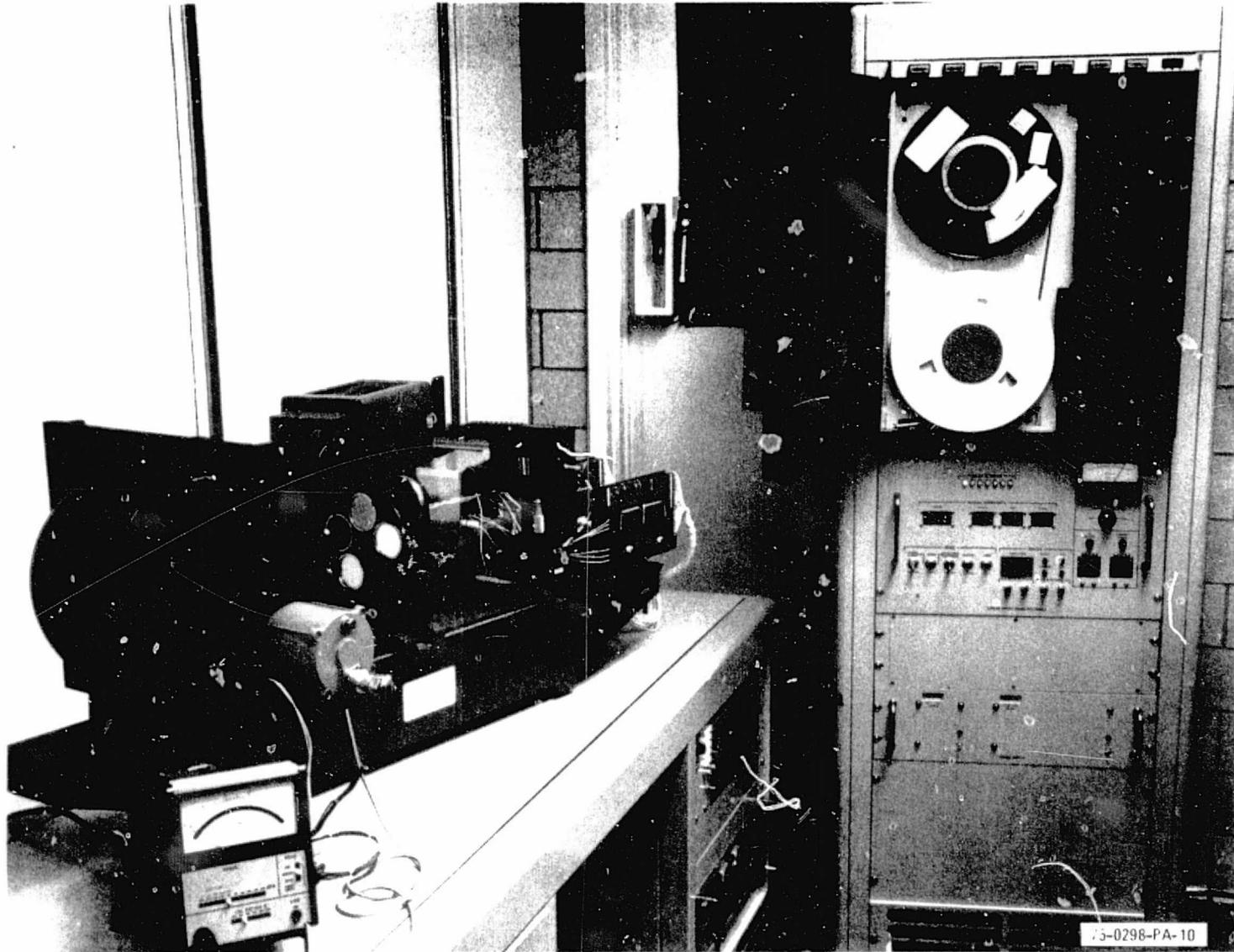
Figure 5. Test Bench and Data Recording System
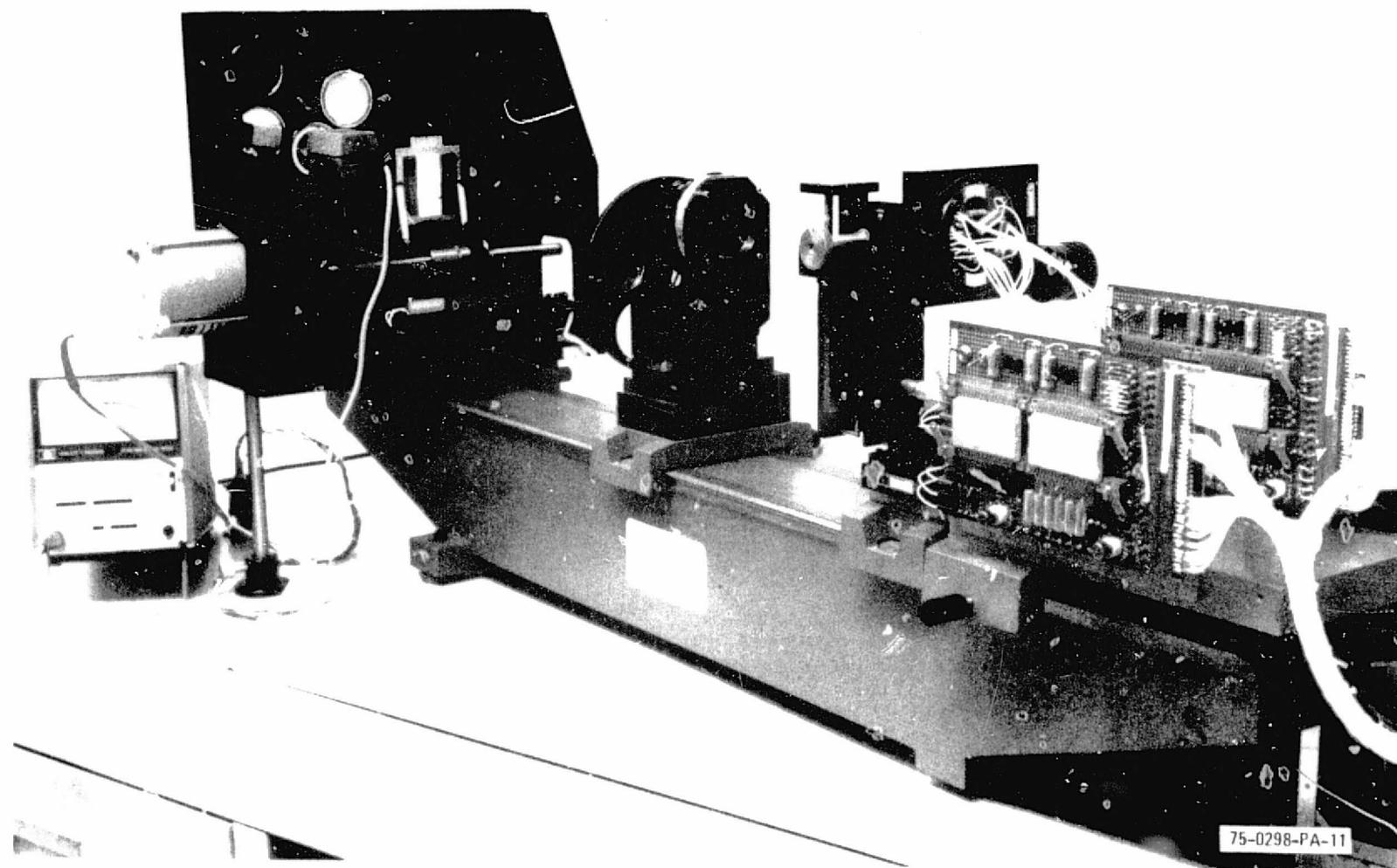
Figure 6.   Optical Bench Showing Light Source, Scene Translator, Filter Wheels,
Linear Detector Array and Mount, and Analog Processing Electronics

2.4.1.2 Radiant Source

The radiant source is a 10-inch diameter hemisphere with a high reflectance white interior. A 150 watt dc tungsten (3300K) bulb is located at the radius center and two apertures are cut in the flat surface cover. These apertures are: (1) a slit to back-irradiate the scene transparency, and (2) a circle to allow direct radiance measurement. The aperture areas are approximately equal, thereby minimizing the radiance measurement error. A Hewlett-Packard Radiant Flux Meter and Detector (Model 8330A/8334A) with an Infrasil window and thermopile detector are used for radiance monitoring. Levels are controlled by adjusting the dc lamp power supply. This source with the radiometer provides the capability for the specified radiance levels and the 5 percent of the full-scale measurement range. See Appendix I for the radiometer calibration results.

2.4.1.3 Spectral Separation

Spectral separation is achieved with thin film filters. Three bandpass filters centered at 0.55, 0.65, and 0.75 microns with 0.08-micron width are used. A long pass filter with a short wavelength cutoff at 0.8 micron provides the near IR band. The filters have a peak transmission greater than 60 percent. Characteristics of the filters are shown in figure 7. Although these "off the shelf" filters did not meet the 70 percent peak transmission of the original specification, they were chosen with NASA concurrence as fullfilling the intent of the program.

2.4.1.4 Detector Array Mount

The detector array is mounted in a micropositioning mount (see figure 8). It is adjustable along each axis and can be rotated about the optical axis and about the axis orthogonal to both the array and optical axis. This allows enough freedom to align the array relative to the scene and to finely adjust the focus. Either the 576- or 1728-detector array can be used in the micropositioner. This capability was required to overcome the coarse focus capability of commercial optics.
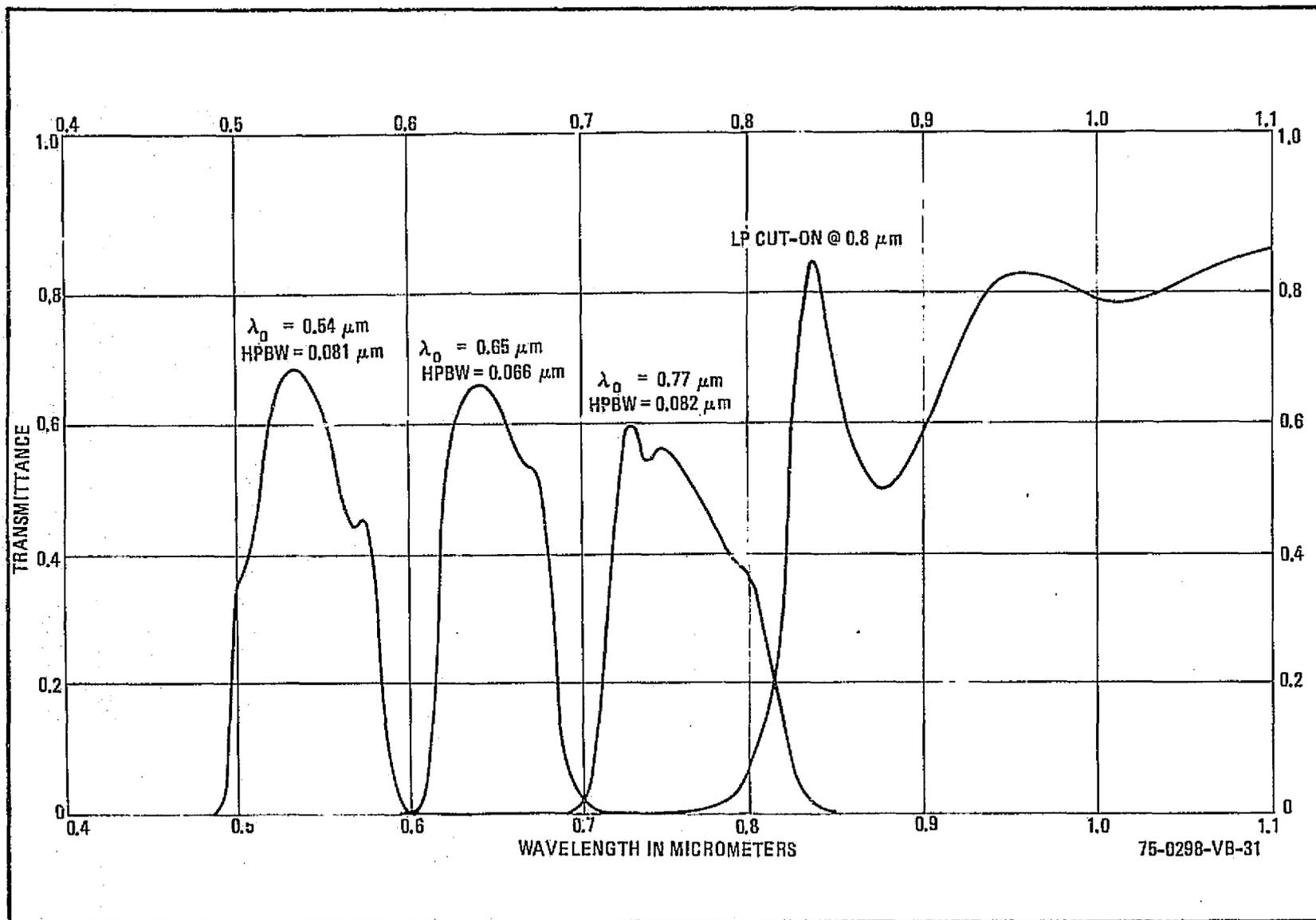
Figure 7. Filter Characteristics
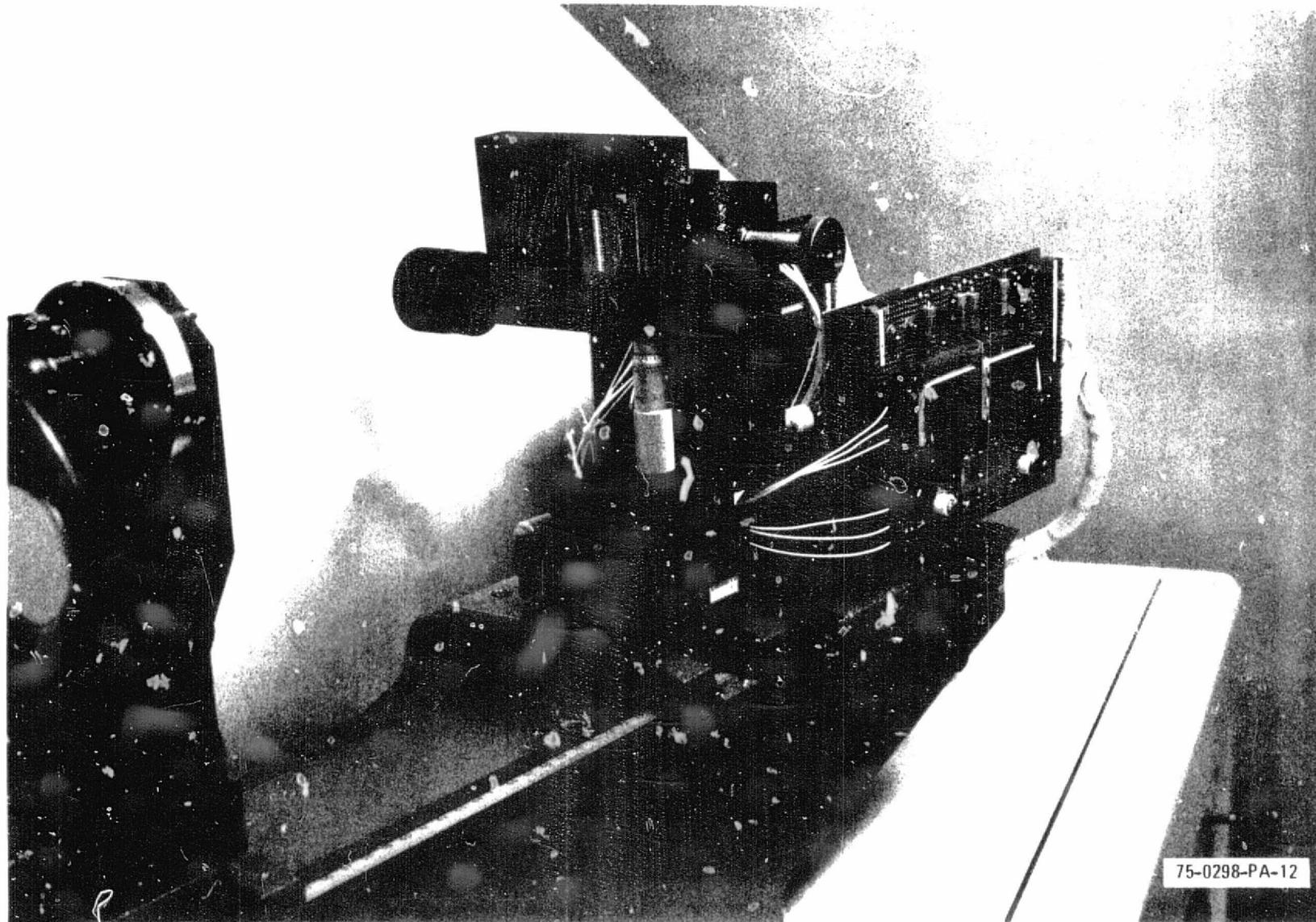
Figure 8. Detector Array in Micropositioning Mount

75-0298-PA-12

2.4.1.5 Optics

High quality commercial photographic lenses are used for the optical system. A 55 mm, f/3.5 lens optimized at 610 mm (2 feet) is used for the 576-detector array. The 1728-detector array uses a Nikon 150 mm, f/5.6 El-Nikkor enlarger lens. Optical distances and magnification were arranged to allow an integral number of motor steps per IFOV. For the 576-detector array, the object to image distance is 434 mm with a magnification of 0.172. The 1728-detector array has an object to image distance of 642 mm and a magnification of 0.600.

A squarewave MTF measurement was made using the 150 mm lens set at f/8. The measurement was made using the breadboard's spectral filters. The optical distances were made equivalent to the breadboard with a silicon detector used in the image plane to measure the response. The results of these squarewave MTF measurements for the 150 mm lens are shown in figures 9 through 12.

CALCULATED λ/4 OPD ABERRATION

MEASURED RESPONSE (EQUALS CALCULATED FOR≈3 λ/8 OPD)

CALCULATED λ/2 OPD ABERRATION

75-0298-VA-13
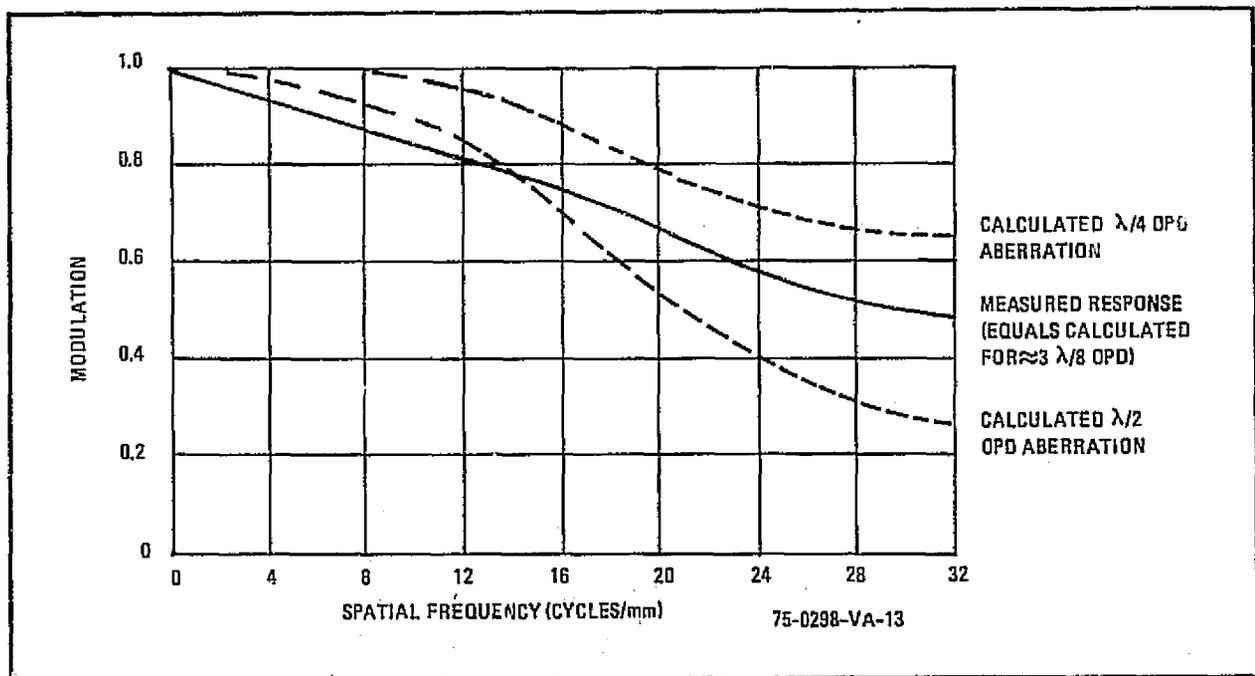
Figure 9. Lens MTF (Squarewave Response) for λ = 0.55 μm
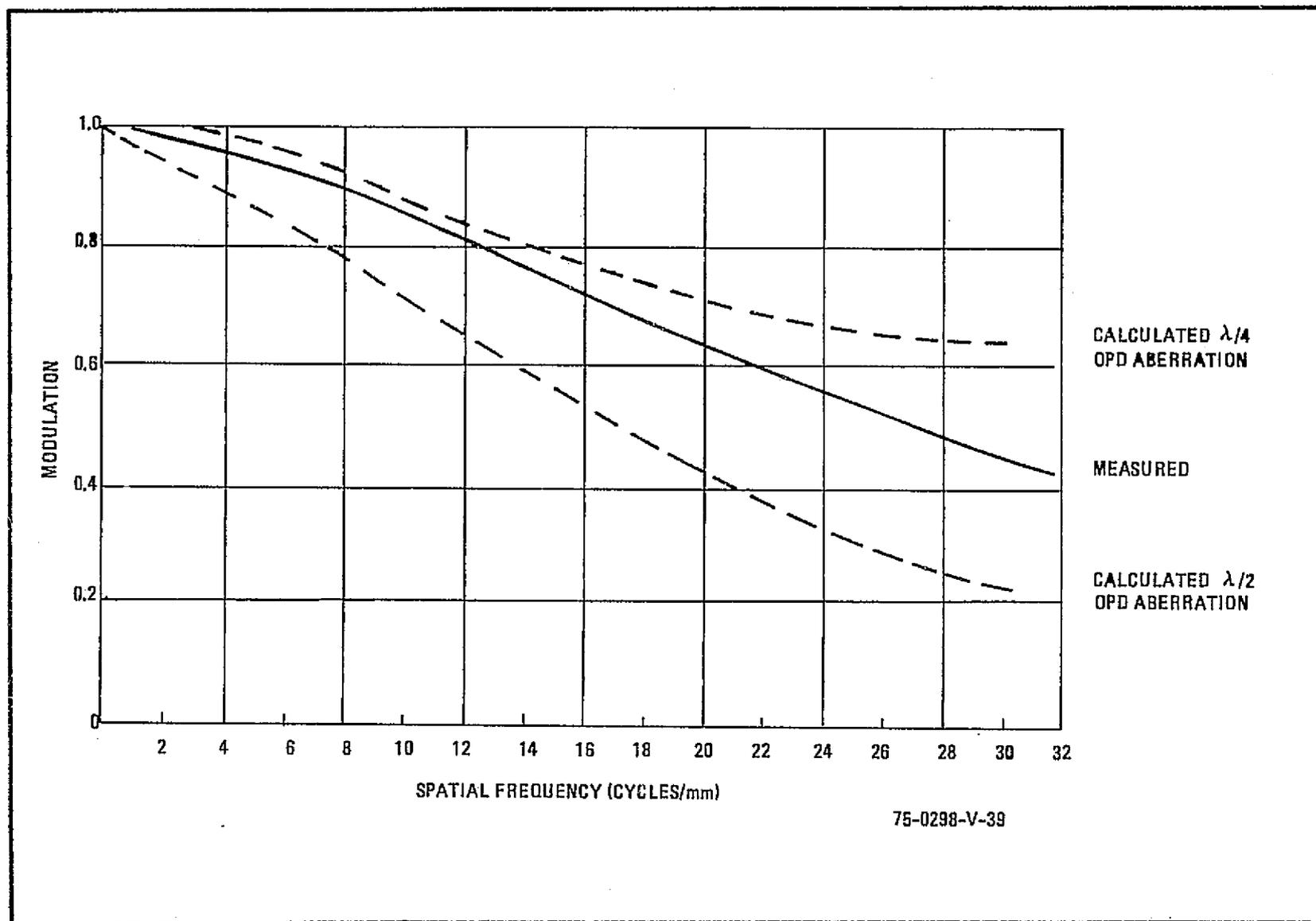
Figure 10. Lens MTF Squarewave Response 0.65 μm = λ
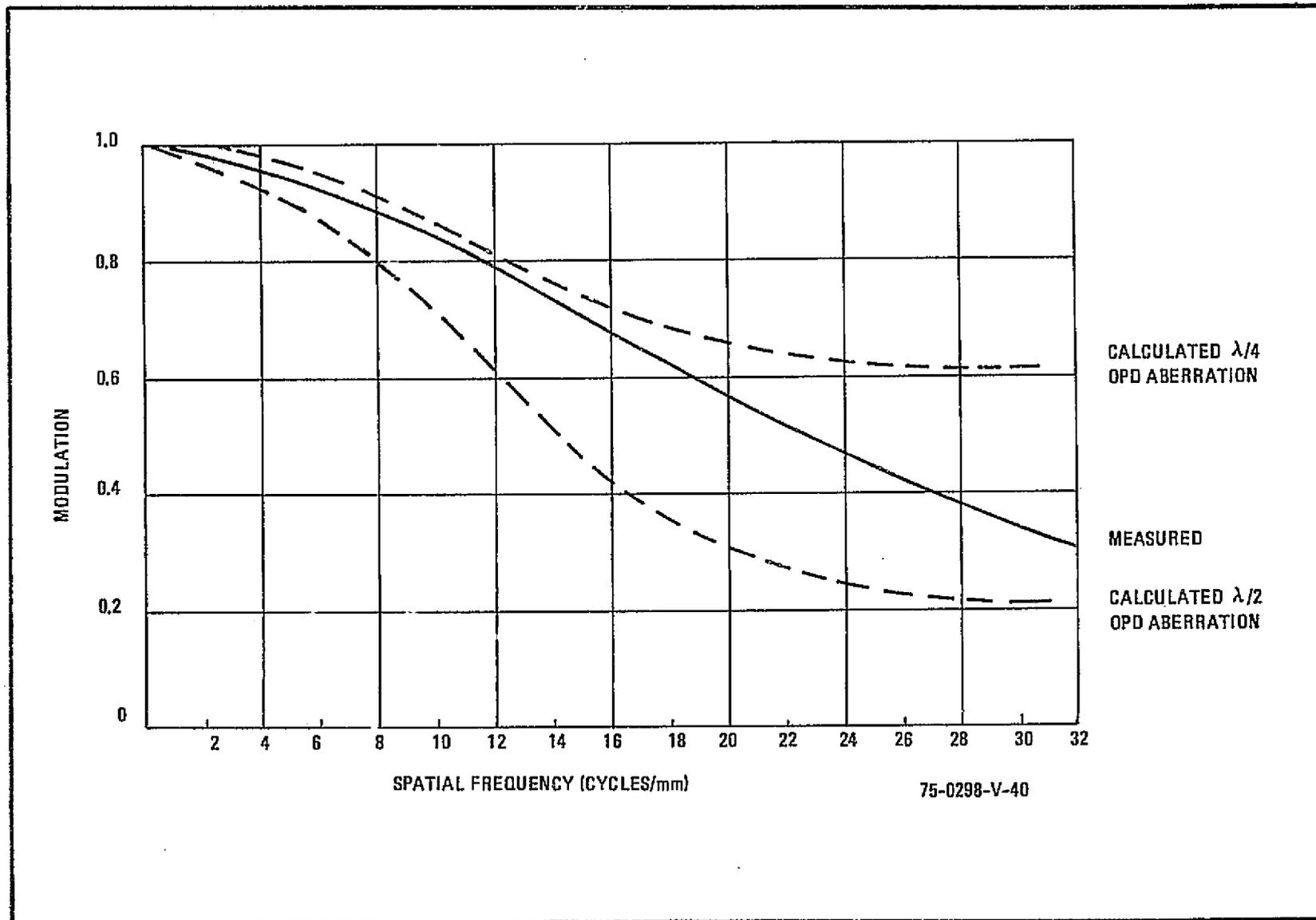
Figure 11.   Lens MTF Squarewave Response 0. 75 μm = λ

CALCULATED λ/4
OPD ABERRATION

CALCULATED (λ/2 OPD
ABERRATION)
MEASURED

SPATIAL FREQUENCY (CYCLES/mm)

75-0298-V-41
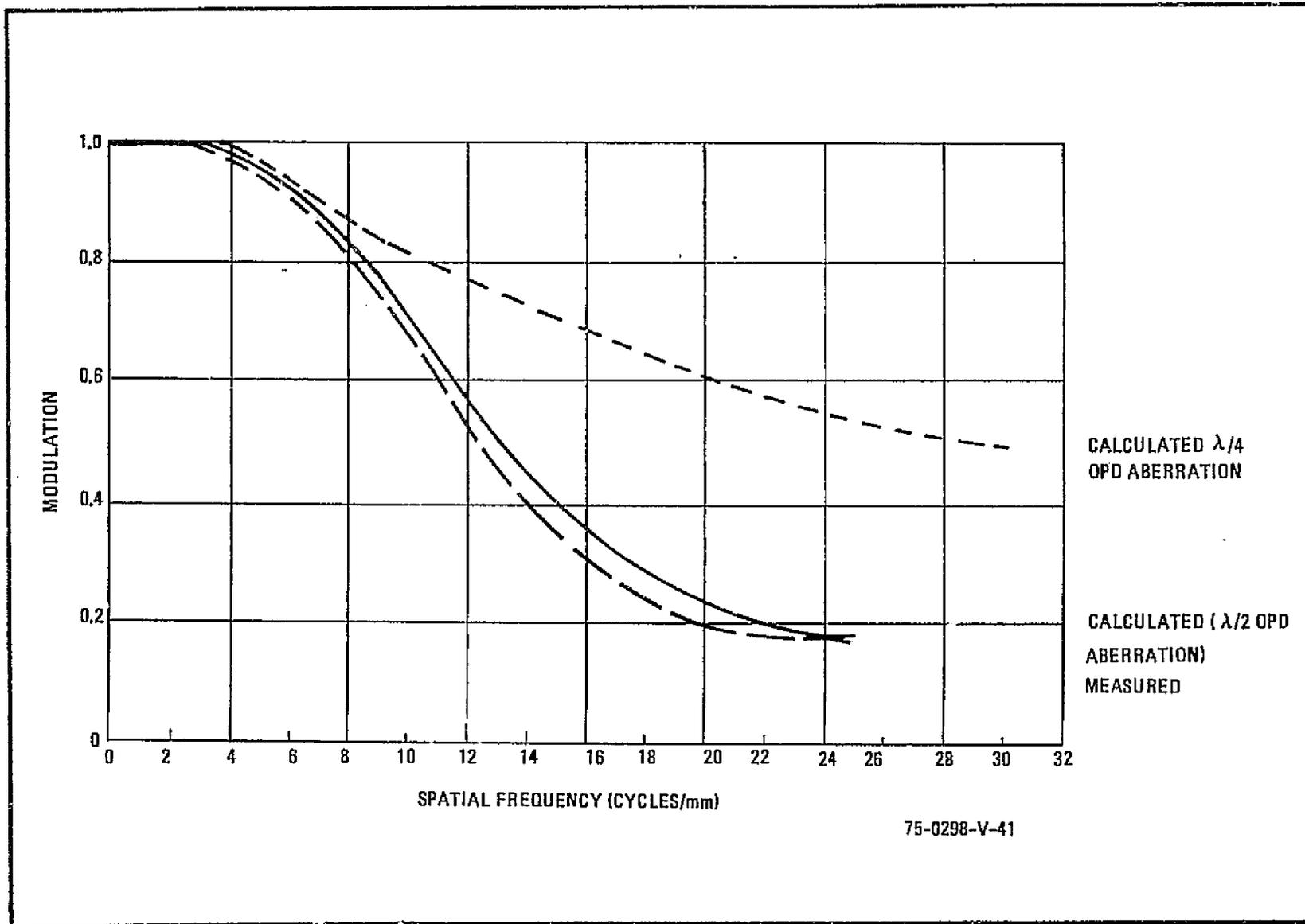
Figure 12.   Lens MTF Squarewave Response 1 μm = λ

These figures include the calculated squarewave response for $\lambda/4$ and $\lambda/2$ OPD (optical path difference) third order spherical aberation.[2] An f/number of 12.8 is used for the calculation. The f/12.8 is the effective f-number calculated for the image distance of the breadboard.

The photographic lenses used in the breadboard although of high commercial quality were not diffraction limited, therefore contributed to a reduction of system MTF. The lenses, however, were of sufficient quality to produce high quality imagery, a primary program objective.

2.4.2 Electronic Processing and Timing

The following sections describe the analog processing and timing circuits required to process the photodiode video data. It is important to note that the analog processor demonstrated an ability to meet program requirements. The timing circuits performed all functions satisfactorily and were flexible enough to permit the operation of two different size arrays (576 elements and 1728 elements).

2.4.2.1 Analog Signal Processing

The analog processor accepts the detector array output, derives the video signal, amplifies the signal, then stores it for A/D conversion. Figure 13 is a simplified schematic of the circuit configuration. Early in the program, discrete, hardwired components were used in the analog processor. A later phase modified the processor to a multichip hybrid package (MHP). The conversion from the discrete component analog processor to the multichip hybrid package is discussed in paragraph 2.4.2.2.

There are several constraints on the performance of the first analog processor amplifier. This amplifier must provide as much gain as possible to minimize the latter stage gain, but not exceed its dynamic range with detector chip bias current differences. The frequency response (and slew rate) must be wide enough to allow sufficient video sample time and small error even after

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[2] Smith, Warren J., Modern Optical Engineering, McGraw-Hill Book Company, page 322.
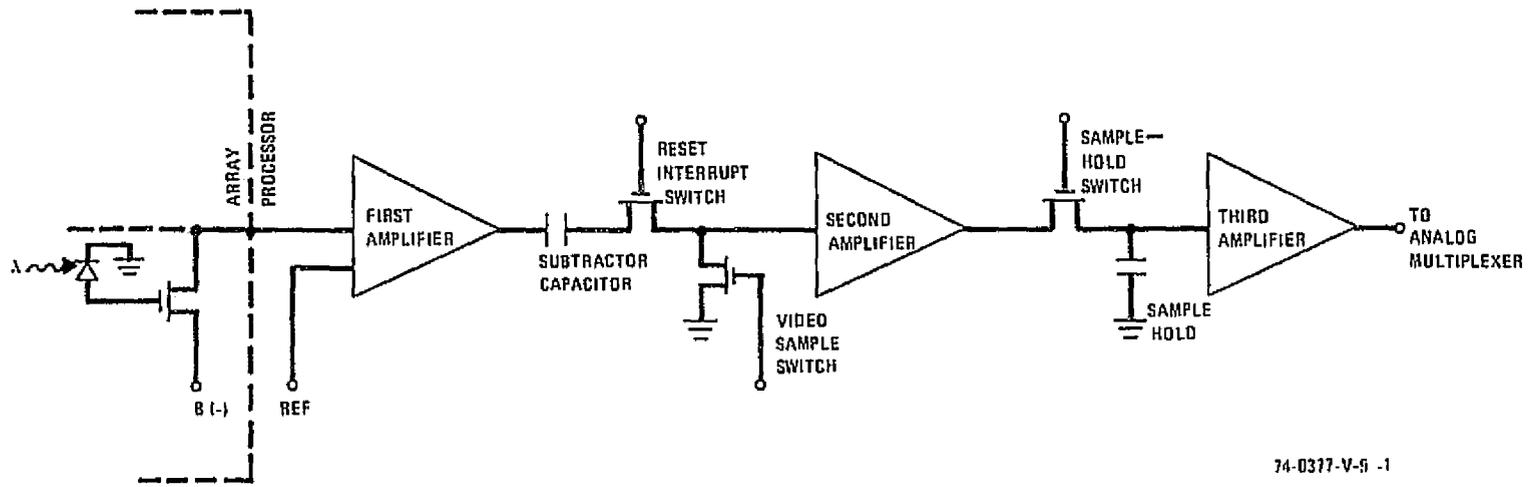
Figure 13.   Simplified Signal Processing Schematic

chip transitions, but preferably narrow enough to keep the noise bandwidth low and therefore, a low noise amplifier is required. In the breadboard, a Westinghouse type WA 1006 operational amplifier is used. Since the WA 1006 must operate on low power supply voltages, such as +5 and -2, the available dynamic range is limited. The bias current variations in the group of chips used in the array was in the range of 300 to 400 μA. With a 4-volt maximum output range, the feedback resistor was limited to $10k\Omega$. An input resistor was selected to provide the nominal bias current for each of the four buses. This typical resistor was $2k\Omega$. The amplifier bandwidth is approximately 800 kHz and voltage gain is 5, giving a Johnson noise at the amplifier output of approximately 25 μV rms. A measurement of a typical amplifier output indicated that a factor of 3 increase in noise is likely due to the amplifier. This gives a total processor-only noise of 75 μV rms at the first amplifier output. The gain from the first amplifier output to the analog channel output is 210. Additions to noise beyond the first amplifier are considered negligible since the first stage noise gain is greater than five. The RSS (root-sum-square) for noise contribution at the second stage (assuming a noise equal to the first stage input) increases the total noise by 2 percent. The impedance of the second stage is lower than the input and thus contributes even less noise.

A computer processed noise run (see Appendix B) using the MHP amplifiers indicated that the average noise is 0.566 counts (see table 2). This is equivalent to 100 μV at the first amplifier output or an NEI of 0.39 μjoule/m^2 in the 0.5 to 0.6-μm spectral band. Three buses (A, B, D) show 0.32 μjoule/m^2 noise and one bus (C) indicates a 0.48 μjoule/m^2 equivalent noise. The analog-to-digital quantization uncertainty is 0.2 μjoules/m^2 (see table 3) in the 0.5 to 0.6 μm band. The quantization uncertainty[3] is the quantization interval/$\sqrt{12}$.

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[3] Schwartz, M., "Information Transmission Modulation and Noise," McGraw-Hill, page 329.

TABLE 2

144 RMS NOISE SAMPLES FOR EACH OF FOUR MHP ANALOG PROCESSORS

MHP NO.

1	2	3	4	3	4	1	2	1	2	3	4	3	4	1	2
.37	.69	.25	.42	.42	.45	.45	.71	.51	.77	.50	.50	.46	.50	.49	.79
.50	.74	.75	.50	.48	.49	.49	.77	.50	.73	.51	.51	.46	.49	.49	.73
.50	.75	.50	.50	.46	.50	.49	.74	.50	.73	.50	.50	.48	.50	.50	.74
.50	.71	.50	.50	.48	.48	.50	.69	.50	.76	.50	.50	.47	.51	.50	.77
.49	.75	.51	.50	.48	.49	.50	.69	.51	.75	.50	.50	.47	.49	.49	.72
.48	.74	.51	.50	.50	.44	.50	.75	.50	.75	.50	.50	.48	.50	.49	.73
.50	.64	.50	.50	.47	.51	.51	.71	.51	.75	.50	.50	.48	.50	.51	.72
.48	.70	.50	.49	.47	.50	.49	.77	.49	.73	.50	.50	.47	.50	.49	.74
.49	.73	.50	.50	.47	.49	.52	.70	.50	.72	.50	.49	.47	.49	.50	.78
.48	.71	.50	.50	.46	.49	.50	.78	.49	.75	.51	.52	.48	.50	.50	.74
.50	.68	.50	.50	.47	.50	.51	.71	.49	.71	.50	.50	.47	.50	.49	.70
.49	.74	.51	.50	.49	.50	.49	.71	.50	.76	.50	.50	.47	.50	.51	.74
.48	.73	.50	.50	.47	.50	.50	.67	.49	.81	.50	.50	.48	.51	.50	.77
.49	.68	.50	.50	.48	.50	.51	.74	.49	.72	.50	.50	.47	.49	.50	.68
.46	.70	.50	.50	.48	.50	.50	.70	.48	.72	.50	.50	.48	.50	.51	.76
.49	.73	.50	.50	.48	.50	.50	.75	.49	.69	.51	.49	.47	.50	.51	.75
.48	.69	.77	.51	.47	.50	.50	.75	.48	.72	.50	.50	.48	.50	.50	.72
.49	.77	.52	.50	.47	.50	.52	.63	.49	.69	.50	.50	.47	.50	.50	.73
.48	.72	.51	.50	.47	.50	.50	.79	.49	.69	.50	.50	.47	.50	.51	.75
.40	.73	.50	.50	.48	.50	.50	.74	.49	.71	.52	.51	.46	.50	.52	.71
.50	.74	.53	.50	.47	.50	.51	.73	.48	.78	.50	.50	.47	.50	.50	.72
.53	.67	.51	.50	.48	.50	.52	.69	.48	.68	.50	.50	.51	.49	.51	.73
.47	.70	.50	.50	.48	.50	.50	.66	.52	.72	.51	.51	.47	.50	.52	.72
.49	.79	.50	.50	.50	.49	.50	.73	.49	.71	.54	.60	.49	.50	.50	.76
.44	.72	.50	.50	.47	.50	.50	.97	.48	.70	.50	.50	.49	.50	.50	.68
.51	.77	.53	.50	.48	.50	.51	.72	.52	.72	.51	.50	.47	.50	.52	.75
.48	.69	.50	.50	.50	.51	.49	.72	.49	.74	.50	.86	.49	.51	.52	.72
.50	.75	.51	.50	.48	.50	.54	.71	.50	.70	.50	.50	.52	.50	.50	.72
.49	.75	.51	.86	.48	.52	.49	.76	.52	.78	.50	.50	.48	.50	.51	.76
.49	.74	.50	.50	.48	.50	.49	.71	.49	.77	.53	.50	.45	.49	.50	.70
.49	.73	.51	.51	.50	.50	.52	.69	.48	.77	.50	.50	.49	.49	.50	.75
.49	.72	.54	.49	.44	.50	.50	.78	.51	.76	.50	.50	.48	.49	.55	.79
.48	.76	.50	.50	.50	.51	.50	.71	.49	.73	.50	.50	.47	.50	.50	.71
.49	.72	.51	.50	.46	.50	.53	.75	.49	.66	.51	.49	.48	.50	.50	.72
.49	.74	.50	.50	.46	.50	.61	.73	.52	.73	.50	.50	.47	.50	.49	.71
.50	.70	.50	.50	.49	.50	.50	.71	.49	.72	.50	.83	.48	.50	.50	.70

	AVERAGE RMS NOISE IN $\mu J/M^2$		MHP NO. 1
	0.35		1
	0.50		2
	0.35		3
	0.36		4

THIS IS THE COMPUTER PRINTOUT (SEE APPENDIX B) OF THE MHP ANALOG PROCESSOR RMS NOISE. FOR THIS CALCULATION, THE SYSTEM GAIN FROM SOURCE TO OUTPUT IS 1.3 COUNTS/ $\mu J/m^2$. THE AVERAGE OF THE RMS VALUES FOR THE MHP ANALOG PROCESSOR IS $0.39 \mu J/m^2$ FOR A LENS TRANSMISSION OF 90 PERCENT IN THE 0.5-0.6 μm BAND. THIS MEASUREMENT WAS MADE WITH A RESISTOR TO SIMULATE THE ARRAY IMPEDANCE.

75-0298-T-1-1

TABLE 3

ANALOG-TO-DIGITAL RMS QUANTIZATION ERROR

```
PICTURE NO.     1
DET NOISE HI  GAIN        MAX INPUT =  24.50
QUANTIZING ERROR
```

.86	.33	.21	.21	.20	.19	.27	.19	.25	.17	.20	.19	.19	.17	.28	.16
.25	.16	.19	.18	.19	.17	.27	.16	.25	.16	.19	.17	.18	.16	.26	.16
.24	.15	.18	.17	.17	.16	.25	.15	.23	.15	.18	.17	.17	.16	.25	.16
.23	.15	.18	.17	.17	.16	.24	.16	.23	.15	.19	.17	.17	.16	.25	.16
.23	.15	.18	.17	.17	.16	.25	.16	.23	.15	.18	.17	.17	.16	.24	.15
.22	.15	.18	.17	.16	.16	.23	.16	.22	.15	.19	.17	.18	.16	.39	.21
.00	.22	20.33	.19	.00	.18	.20	.16	.24	.17	.00	.19	.72	.20	.12	.18
.14	.16	.19	.17	.20	.19	.25	.17	.18	.18	.19	.19	.18	.17	.21	.16
.25	.16	.19	.18	.18	.18	.25	.16	.23	.17	.18	.18	.17	.18	.25	.16
.15	.17	.41	.19	.18	.19	.30	.16	.24	.18	.20	.17	.00	.19	.18	.17
.26	.18	.23	.19	.20	.20	.29	.17	.25	.18	.19	.19	.17	.18	.25	.17
.24	.18	.20	.20	.17	.19	.27	.17	.24	.16	.20	.19	.17	.19	.40	.22
.00	.00	.00	.22	.19	.20	.24	.20	.24	.16	.18	.19	.21	.19	.26	.18
.25	.17	.20	.19	.18	.19	.28	.17	.25	.18	.20	.20	.19	.19	.28	.17
.25	.18	.20	.19	.20	.19	.16	.28	.18	.31	.19	.19	.19	.20	.29	.18
.24	.18	.20	.20	.20	.19	.28	.18	.25	.18	.20	.20	.20	.20	.28	.18
.25	.18	.21	.21	.16	.18	.28	.17	.25	.17	.20	.20	.20	.19	.27	.18
.25	.17	.19	.20	.18	.19	.27	.18	.24	.22	.20	.19	.18	.19	.39	.23
.00	.23	.17	.17	.18	.16	.19	.15	.23	.16	.18	.18	.17	.18	.27	.17
.25	.17	.18	.17	.17	.17	.26	.16	.25	.16	.18	.16	.17	.17	.25	.16
.25	.16	.18	.16	.16	.17	.26	.16	.26	.16	.18	.17	.16	.17	.26	.16
.26	.17	.19	.17	.15	.18	.27	.17	.25	.17	.19	.17	.16	.18	.27	.17
.26	.17	.18	.17	.17	.18	.26	.16	.26	.17	.19	.17	.19	.19	.27	.17
1.05	.28	.18	.21	.17	.18	.22	.18	.28	.16	.16	.17	.15	.15	.45	.00
.27	.15	.16	.16	.15	.15	.24	.15	.26	.15	.15	.16	.15	.15	.26	.16
.26	.14	.15	.15	.15	.14	.24	.15	.26	.14	.15	.16	.15	.15	.23	.15
.25	.14	.15	.15	.14	.15	.24	.15	.26	.15	.14	.17	.14	.15	.23	.16
.25	.15	.15	.16	.14	.16	.23	.16	.24	.15	.14	.16	.14	.15	.22	.16
.00	.00	.25	.33	.20	.18	.23	.20	.22	.17	.19	.19	.20	.00	.28	.19
.27	.20	.21	.21	.23	.21	.30	.19	.29	.19	.21	.20	.19	.19	.27	.18
.26	.18	.20	.20	.20	.20	.26	.19	.25	.18	.19	.19	.20	5.26	.30	.12
.32	.11	.22	.15	.17	.11	.00	.16	.23	.20	.20	.19	.19	.22	.24	.19
.26	.21	.19	.22	.20	.22	.26	.19	.25	.20	.20	.21	.19	.20	.25	.20
.23	.19	.19	.20	.17	.19	.22	.18	.25	.18	.18	.20	.17	.23	.33	.00

THIS IS THE COMPUTER PRINTOUT OF THE RMS QUANTIZING ERROR DUE TO ANALOG-TO-DIGITAL
CONVERSION. THE NUMBERS IN THE TABLE ARE DETERMINED BY DIVIDING THE MEASURED QUANTI-
ZATION INTERVAL BY $\sqrt{12}$. IN THIS PRINTOUT, THE QUANTIZATION ERROR TABULATED IS IN $\mu J/m^2$.
IN CALCULATING THE AVERAGE OF THE RMS ERROR, INOPERATIVE DETECTORS ARE EXCLUDED.
THE AVERAGE OF THE RMS NOISE VALUES FOR ANALOG-TO-DIGITAL CONVERSION IS $0.2\,\mu J/m^2$.

75-0298-T-2-1

The array output is a current which includes the video information and a large bias level (see figure 14). The image information is the amplitude difference between the pre-reset (video) and post-reset (reference) current. This difference current is 20 μA or less, assuming a peak irradiance of 0.5 W/m^2 and a 1.5-msec integration period. The bias current is 1 mA or less and varies from chip to chip. Without chip selection, the chip-to-chip bias variation could be several orders of magnitude greater than the video signal level.

The first amplifier provides a dual function of current to voltage conversion and removal of the average bias level.

The pre- and post-reset differencing to extract the video is performed by a "keyed-clamp" circuit. A capacitor is charged to the pre-reset level by clamping one side to ground at the pre-reset time interval. At all other times, the clamp is opened. The clamp circuit output is the instantaneous first amplifier output less the stored value on the capacitor.

A series switch is included in this same area to open circuit the system during the reset period to prevent amplifier saturation. The combination series and clamp switches provide the charging impedance for the subtraction capacitor. It should be noted that this bandwidth essentially matches that of the first amplifier (800 kHz).

Selection of the time constant for the keyed clamp circuit involves the tradeoff of noise and offset. The circuit must have the speed to remove an offset that is much greater than the signal, but slow enough so as not to store noise pulses. The bias current changes between chips is nominally 10 times the 0.55-μm band, low level, full scale signal. In order to keep the coupled offset during chip to chip transitions below 1 percent of the full scale, a time constant of less than 1/7 of the pre-reset gate width is required. A factor of 1/10 was used, giving a coupling of 0.05 percent (0.5 to 1 percent of the signal full scale).

28
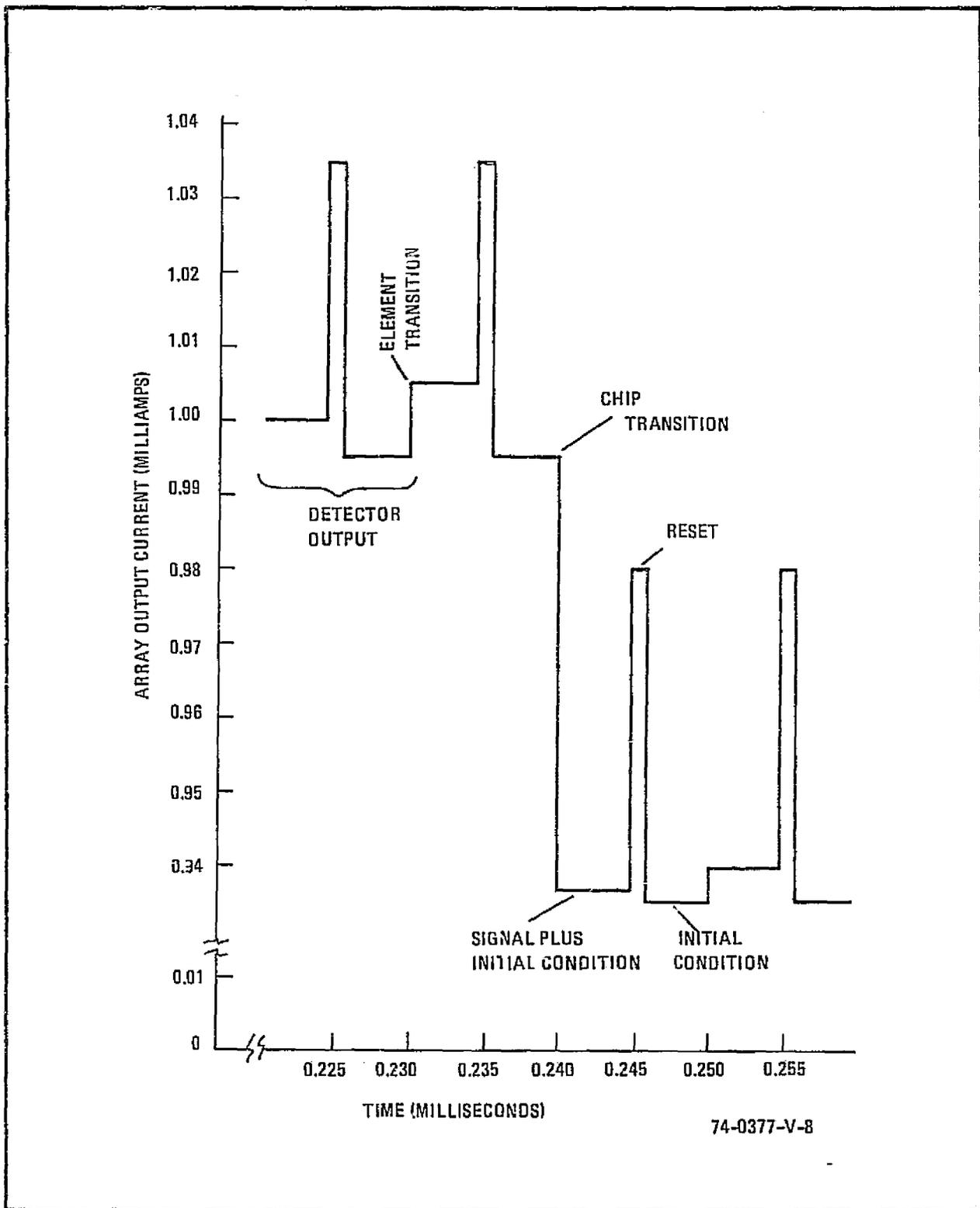
Figure 14.   Array Signal Current (Waveform Representation)

The second amplifier provides gain and a buffer between the keyed clamp subtractor capacitor and the sample-hold circuit and has a gain of 21 switchable to a gain of 3. There is no external bandwidth limiting added to this amplifier. It is desirable to have the amplifier recover from degraded elements or high offsets as rapidly as possible. The internal amplifier response gives a closed loop bandwidth near 800 kH'.

The sample-hold circuit samples the second amplifier output during the post-reset video period and holds it until the next element is sampled. A time constant to sample time ratio of 1/5 is used to keep signal cross-coupling below 1 percent.

The final amplifier provides a buffer and line driver. A National Semiconductor LH0003 is used with a gain of 10. This provides the 10-volt capability required for the A/D converters and causes a droop less than 1/2 an LSB (least significant bit) over the 10-μsec holding period.

A 4-μsec per conversion A/D converter is used for each channel. At the end of each element conversion, the data is stored in an 8-bit holding register. The data is multiplexed and sent to the recording encoder on eight lines in the correct pixel sequence. A clock signal is sent with each data word.

2.4.2.2 Analog Processor Conversion to Multichip Hybrid Package (MHP)

A change order to the contract provided for the conversion of the analog process electrical schematic (see figure 15) into a microminiature module. The MHP was expected to give more nearly detector-limited performance. The design procedure is shown below. The 1" x 2" package was chosen because it meets both the requirements of small size and ease in manufacture. The layout takes into consideration the output lines and the minimization of interconnection lead lengths between amplifier stages and the use of power line bypassing in several places to ensure decoupling.

| Electrical Design | → | Perform Hybrid Layout | → | Manufacture Substrate | → | Perform Hybrid Assembly | → | Electrical Test |
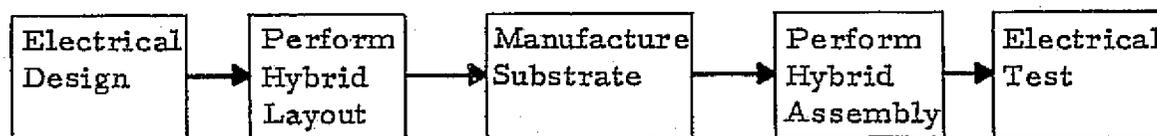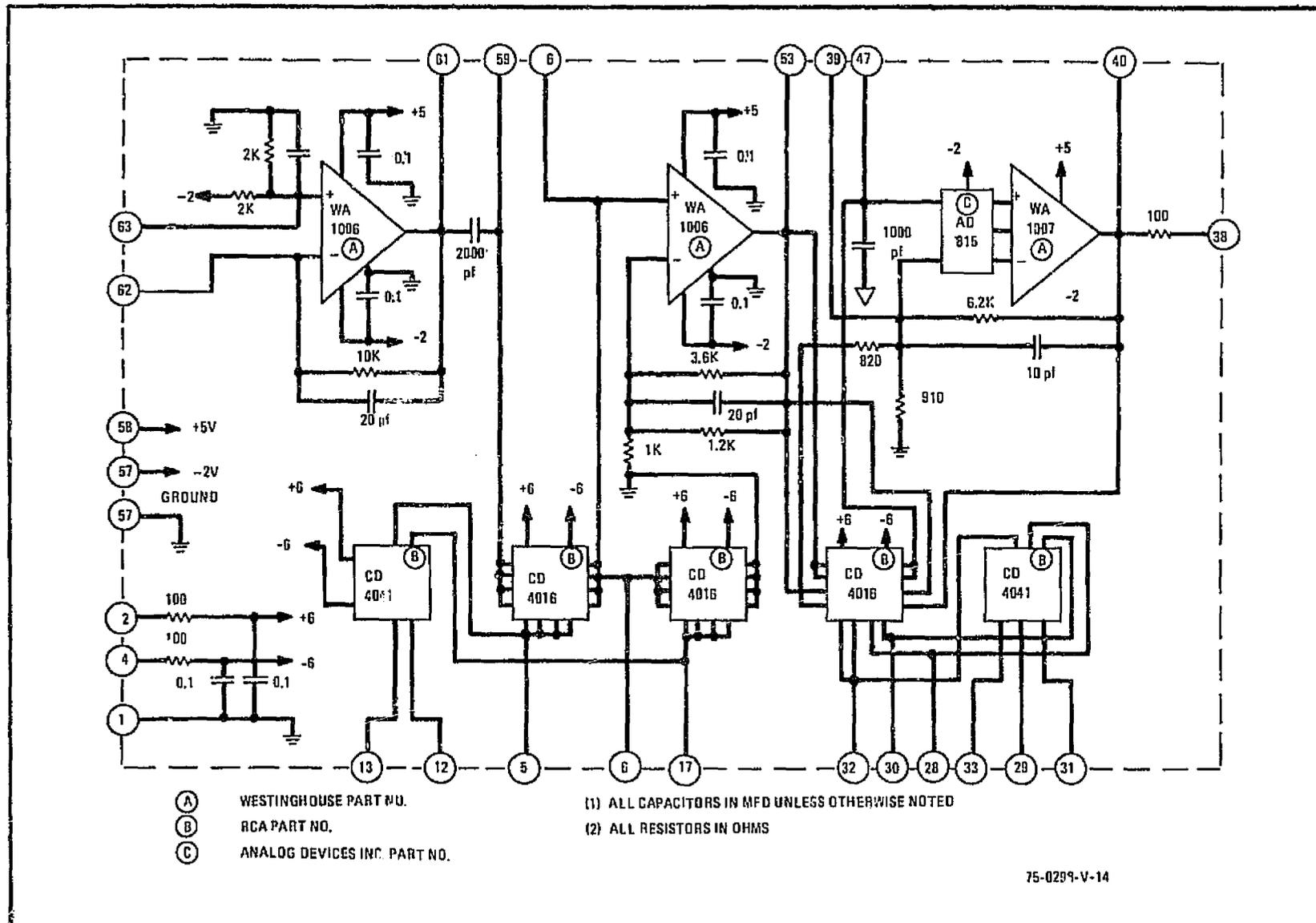
Figure 15. Analog Processor MHP Schematic

The layout is in three layers. The first layer is the main conductor layer where 85 percent of all necessary interconnections are made. The second layer is a dielectric which provides insulation between conductor layers as well as providing an insulation over which a wirebond passes. The third layer is the second conductor layer; this layer serves to interconnect the lines on the first conductor layer.

The layout, after it was checked for accuracy, was next converted into artwork necessary for the manufacture of the substrate. Each layer was screened, then fired onto the substrate and visually examined. After the third layer was screened and fired, the substrate was again visually examined and electrically checked, thus assuring a quality substrate. The amplifier substrate consists of two thick film-deposited conductive layers with one dielectric layer and is inspected. The components which already have been visually examined are mounted in their respective places using nonconductive adhesives. After curing, the components are wirebonded using gold thermocompression ball bonding techniques. This assures a reliable connection between component and conductor.

The finished analog processor is shown in figure 16.

2.4.2.3 Timing and Control

All timing and control functions, except for recorder encoding and control, are provided by the main timing circuitry. Figure 17 is the system timing diagram. A 3.6-MHz clock is divided to provide the 400-kHz data rate clock. A preset counter counts to 576 (96 times 6) at the 400-kHz rate to provide an end-of-line signal to enable synchronizing at the line scanning rate. A shift register provides 0.28-μsec, the basic timing interval over a 10-μsec period. All analog gates, A/D control, holding register load, and array clocks are determined by decoding the proper interval from the shift register.

The maximum rate at which the digital data tape recorder can accept data is significantly less than the detector array can produce. Therefore, the record rate is designed to accept only one of sixteen scan lines. The scan

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75-0298-PA-15
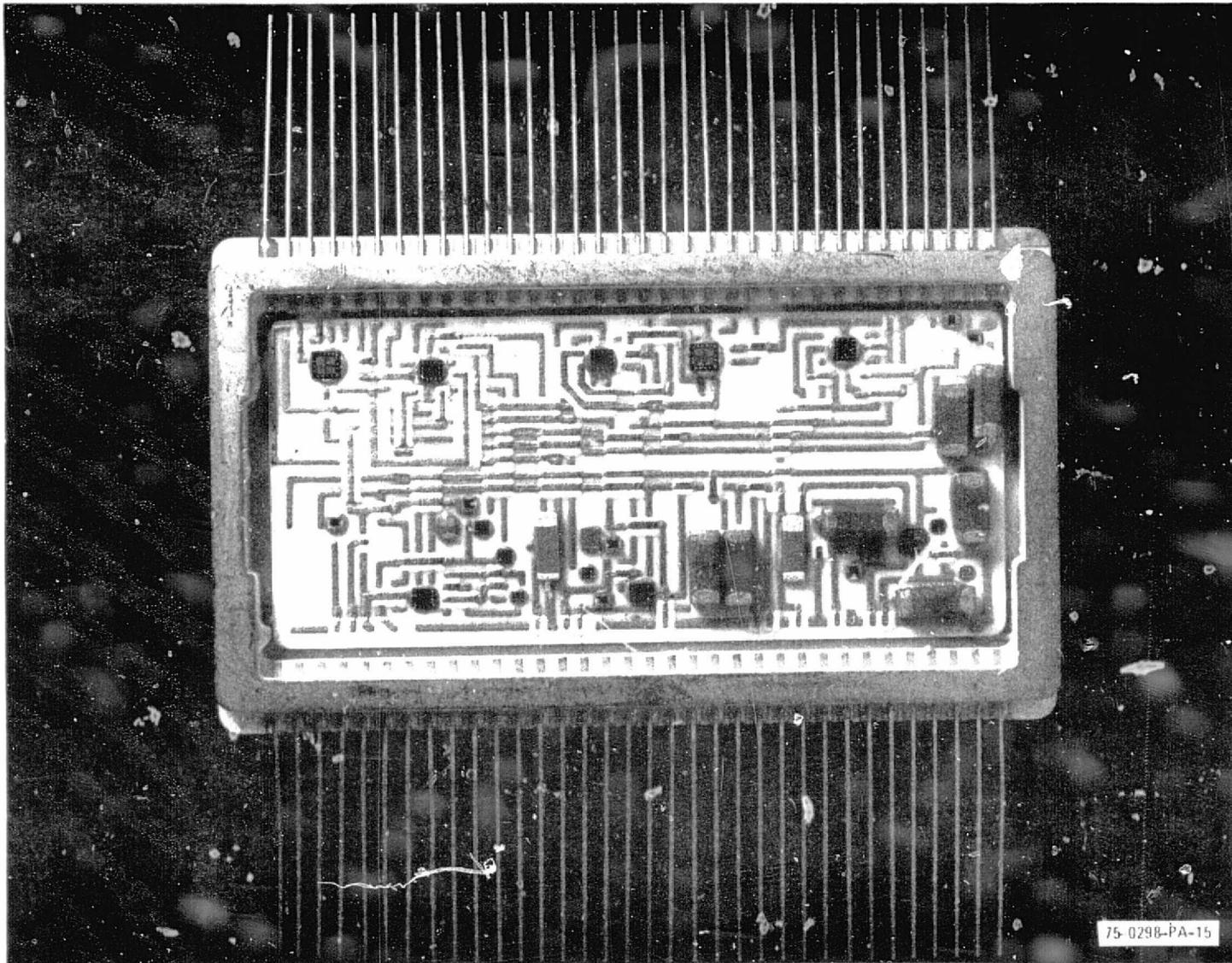
Figure 16.   Analog Processor MHP

Figure 17. System Timing Diagram

SHIFT REGISTER IN

SET UP/RESET CLOCK

SHIFT CLOCK

VIDEO SAMPLE SWITCH

RESET INTERRUPT SWITCH

SAMPLE—HOLD SWITCH

A/D CONVERSION

DIGITAL DATA STROBE

VIDEO SIGNAL

BUS   A   B   C   D   A   B   D

1.0μsec

1.44 msec
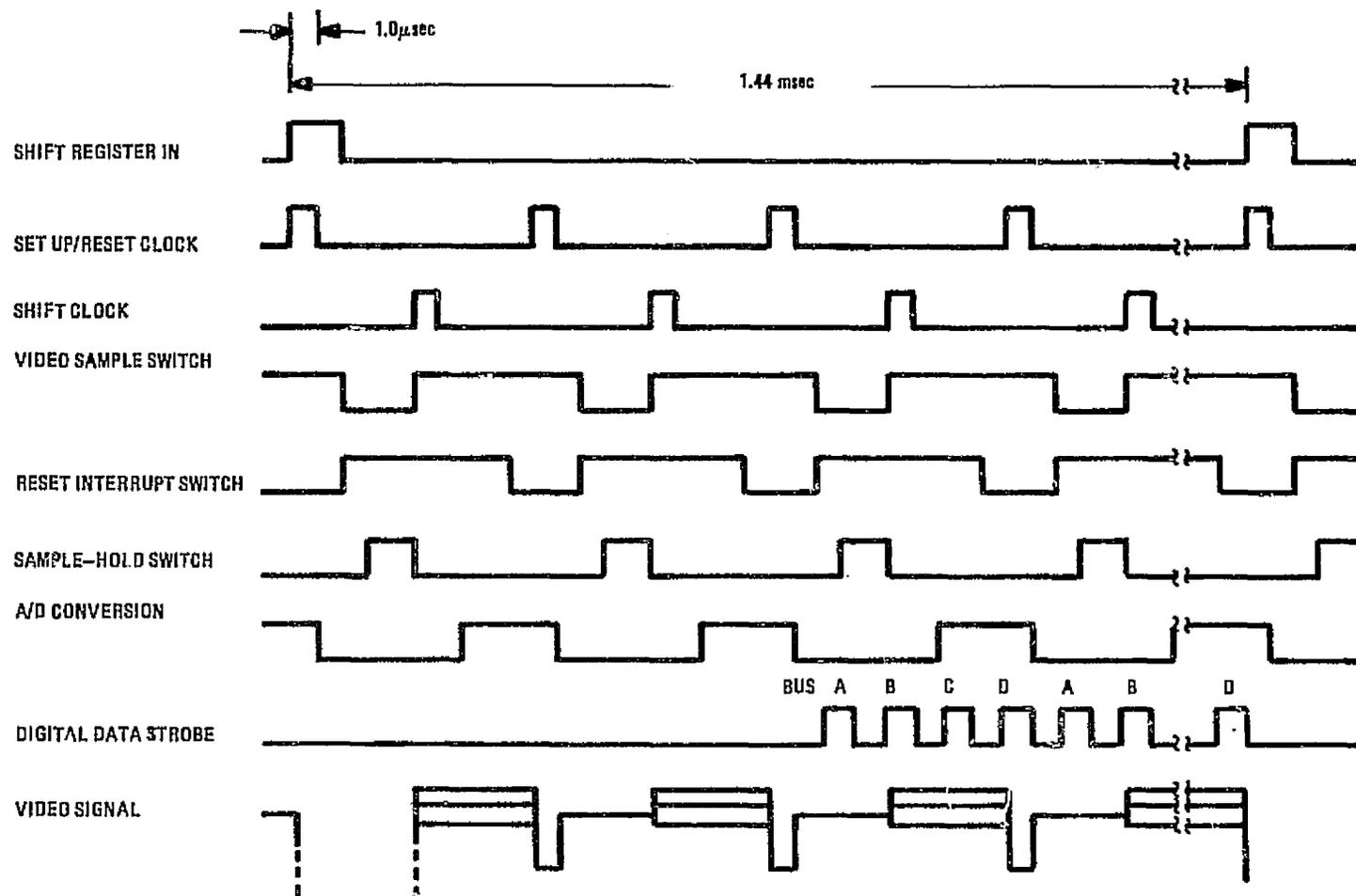
NOTES: 1) SIGNALS ARE LOGICAL REPRESENTATIONS OF FUNCTION SUCH THAT: HIGH LEVEL IS SWITCH ON OR SHORTED, LOW LEVEL
IS SWITCH OFF OR OPEN CIRCUIT.
2) VIDEO IS SHOWN FOR RELATIVE TIMING REFERENCE

75-0298-V-16

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line that is recorded represents one contiguous IFOV of the scene. During the interval between recorded data lines, the scene is translated and stopped prior to recording. The timing and logic is arranged to provide the correct number of motor steps (2 motor steps for the 18-chip array and 7 for the 6-chip array) to accommodate the different field-of-views required for the 6-chip and 18-chip arrays.

The clock signals used to control the timing of the analog processor and array use open collector TTL to increase the voltage limits. This 12V signal is ac-coupled for the negative voltage biased array and the bipolar analog gates. A CMOS CD4041 driver interfaces between the TTL and array inputs. CMOS CD4041 drivers also interface with the CD4016 analog switches in the processor.

2.4.3 Detector Array Design and Fabrication

A major objective of the breadboard program was to determine the feasibility of fabricating long detector arrays for possible use on future earth observation sensors. This section discusses the fabrication of detector arrays and both achievements and problem areas are identified.

2.4.3.1 Fabrication Techniques

An early program decision was to select a design which would allow replacement of individual chips. This was of particular importance with the limited number of chips available. During the program, several chips were successfully replaced.

The selected approach shown in figure 18 uses the "chip carrier" concept and the use of multi-level substrate interconnections. Each detector is cemented to a precisely machined chip carrier. The carriers are assembled on a baseplate with each aligned such that the chips form a contiguous line of detector elements. An appendage on the carriers extends beyond the chip edges, on alternating sides, providing a surface with up to twice the chip width for baseplate mounting. Figure 19 shows the assembled 6-chip array with this carrier arrangement. It is well to remember that one chip contains 96 detectors; therefore, six chips is equal to 576 detectors.

Substrate Assy

Base

Chip Assys

Interconnection Board

Housing

Sensor Assembly

Interconnection Layer

Dielectric

Buss Layer

Dielectric

Gold Shield

Sapphire Substrate

Substrate Assembly

Base

Chip Epoxy Bond

Chip Carrier

Chip Assembly

74-0484-VC-30
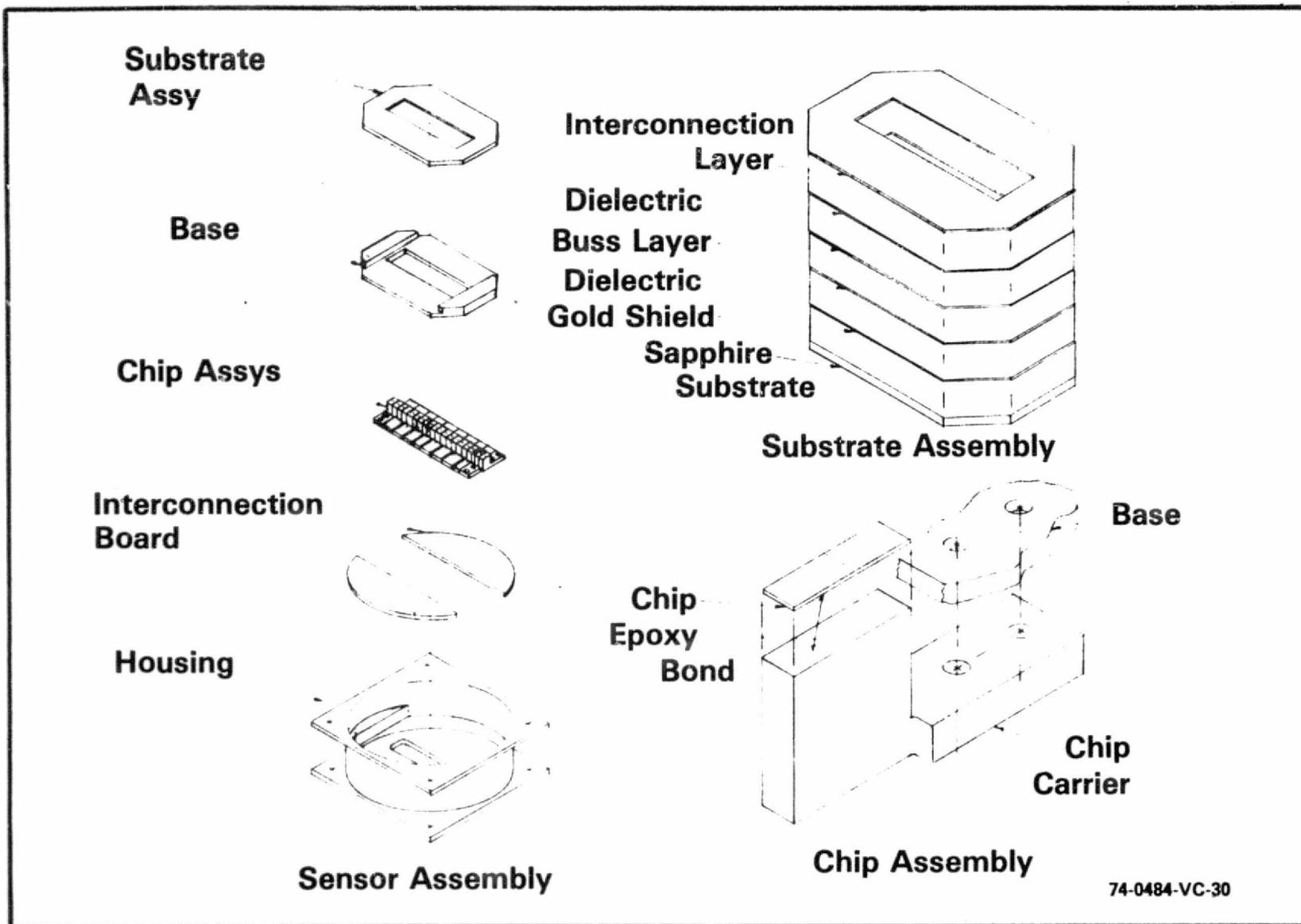
Figure 18. Chip Carrier and Array Assembly Technique

75-0298-PA-17
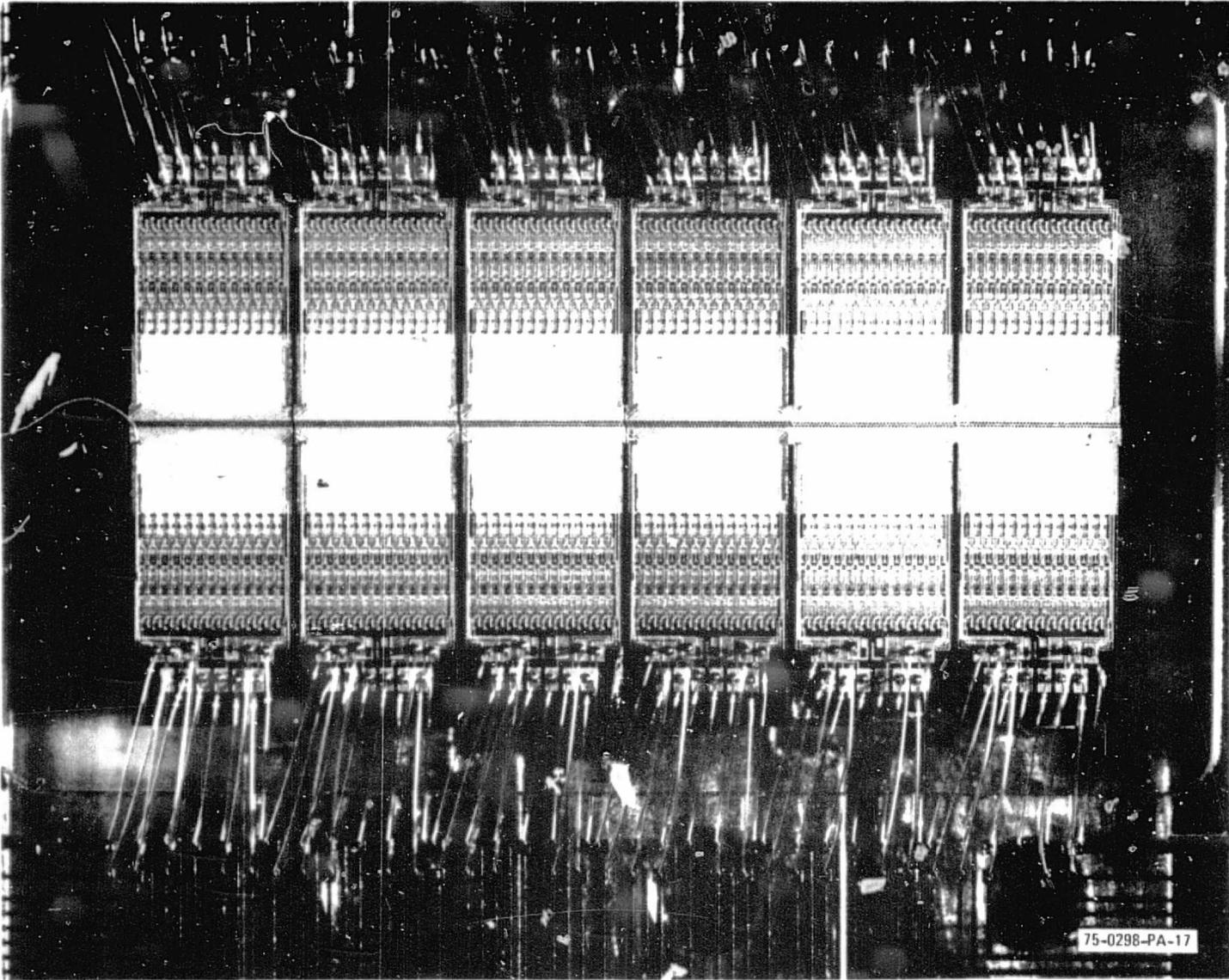
Figure 19. 6-Chip Array (576 Detectors)

The chips are cemented to the carriers with an epoxy cement double-sided film. The film cement eliminated possible metering problems associated with liquids. This also eased the handling and prevented seepage onto the chip surface. Curing is performed at 150°C and a jig is used to align the chip on the carrier during the cement curing period.

The chip alignment was performed by manipulating the baseplate mounted carriers while viewing the detector elements through a microscope. A custom fixture was used to elevate the array during alignment to allow access to the screws on the bottom surface. The chip carrier mounting screws could, therefore, be tightened while observing the chip alignment to detect movement of the carrier. A measuring stage was used with the microscope providing a means of measuring the final alignment accuracy. Using this measuring capability, all chips were assembled relative to a datum to prevent error accumulation. It is important to note that with this technique errors in the along scan direction are not accumulated. However, positional error can occur from one chip to an immediate neighbor chip. A measurement made on the 18-chip array indicated a maximum error of 0.15 mil (3.8 μm) between adjacent chips.

With the use of a measuring microscope, an imaginary reference line (best fit) was developed which minimized the maximum detector lateral excursion from the reference line. For the 6-chip array, the maximum lateral excursion was 0.2 mil (5.1 μm) and for the 18-chip array, the maximum lateral excursion was 0.3 mil (7.5 μm).

The errors in detector lateral excursion in the across-scan direction and positional error between adjacent chips in the along-scan direction are within the specification requirement of 1 percent of the array linear dimension.

For interconnecting the chips electrically, a substrate of synthetic sapphire was used on which gold conductor patterns had been deposited. This also provided the connection to the array package interface leads. All interconnect wires within the array package were gold and ultrasonically bonded. Rework of the gold-to-gold bonds was made many times with

excellent results. The gold-aluminum (chip pads) bonds were reworked, but the number of times an aluminum pad could be used with a good bond was less than three.

The array package was assembled in a standard 1 inch by 1 inch micro-electronic package. This package was attached to an adapter ring for assembly into the micropositioner. A filter board was connected to the rear surface of the adapter ring and wires run through the adapter and filter for connecting the array to the signal processing and power supplies.

Photographs of the 576 detector (6-chip), the 1728 detector (18-chip) and the fully assembled 18-chip array are shown in figures 19, 20, and 21. From an observation of the photographs, it is readily seen that a major objective of the breadboard program was achieved. Thus it is fully demonstrated that the fabrication of long arrays is totally feasible. Achieving this objective was not devoid of problem areas, however. Some of the problem areas encountered during the array fabrication phase are discussed in the following paragraphs.

2.4.3.2 Fabrication Problem Areas

Throughout the fabrication and test phases, both accomplishments were made and problem areas became apparent. Those problems which could readily be resolved were improved with the later 18-chip array fabrication. This section discusses the problem areas and possible solutions.

Many of the early chip failures were similar, occurring after several hours of operation. One of these damaged chips was sent to NASA-GSFC for failure analysis (see Appendix C, Failure Report SN-2979). The conclusion was that the chip had a probable electrical overstress although some manufacturing scrapes could have been contributing factors.

Later in the program, there was a long period during which no failures occurred until some electrical modifications were performed. The coincidence of electrical circuit modifications and the occurrence of array failure may have been due to the use of an ungrounded soldering iron. The extremely

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75-0298-PA-18
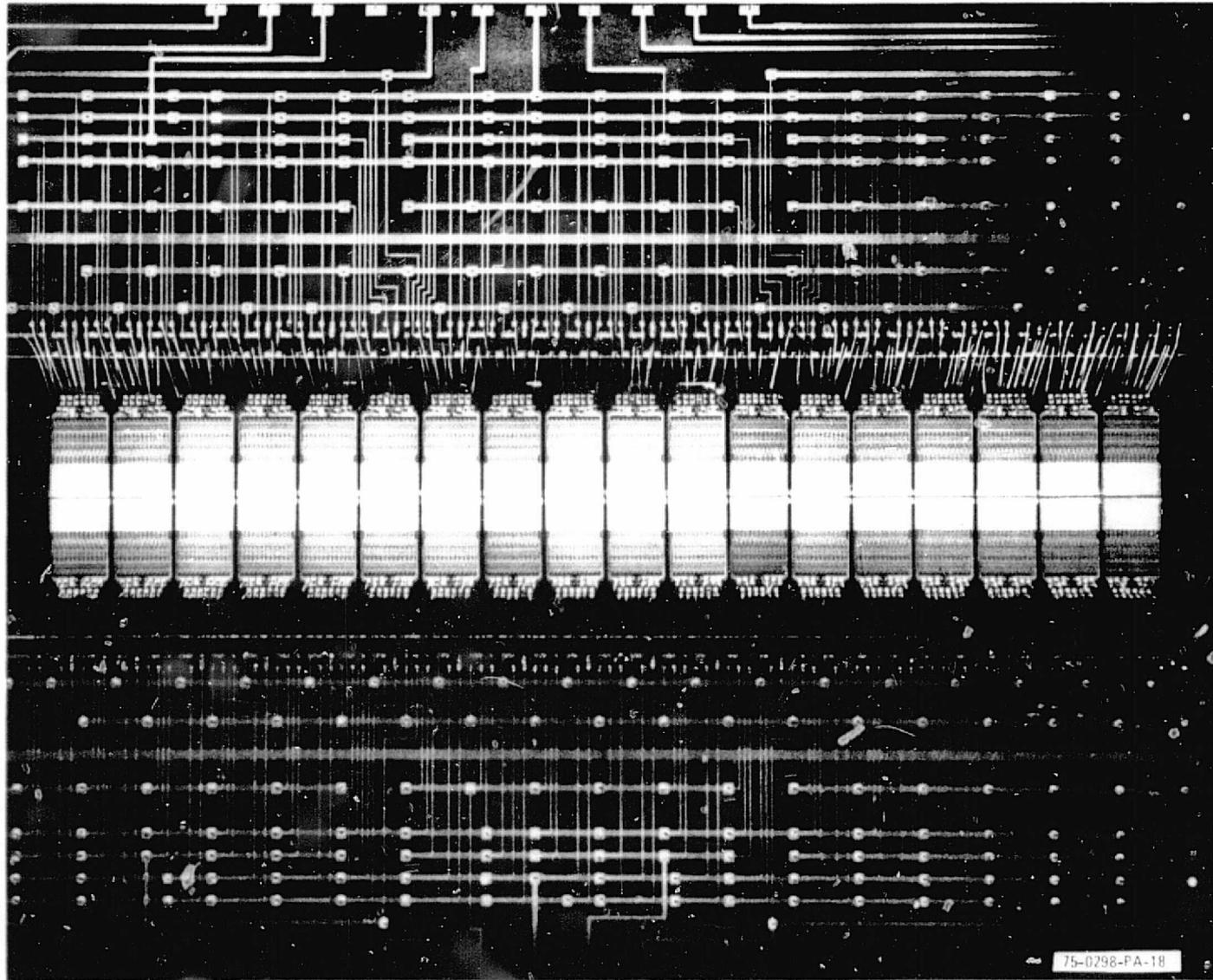
Figure 20.   18-Chip Array (1728 Detectors)
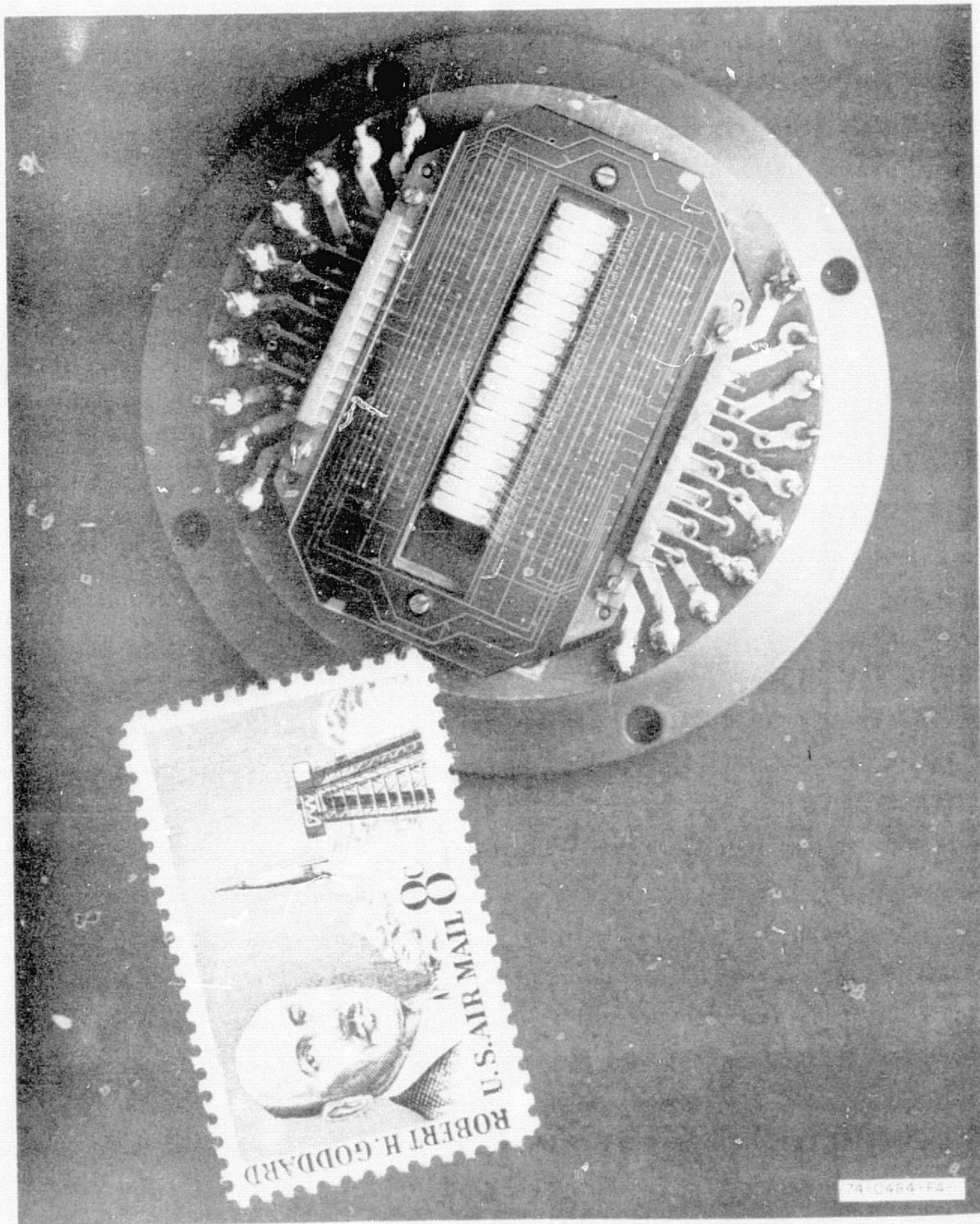
Figure 21. Fully Assembled 1728-Detector Focal Plane Array

high in pedance of the MOSFET devices make them very susceptible to static charge damage. For the 18-chip assembly, special care was used to do all wiring with a grounded soldering iron thus preventing failure due to static charge effects. Also, the power lines are decoupled with large capacitors, zener diodes, and resistors to remove the possibility of power line transient damage to the array. The data buses were decoupled by the first amplifier resistances and the MOSFET gates are protected on the chips with zener diodes. No failure occurred during an operating period of many months with the 18-chip array, indicating that the electrical induced problems were resolved.

Probably the most critical problem area is the chip sensitivity to handling. The chip is very brittle, making the chips very susceptible to nicks and cracks from pressure or edge contact. Pressure on the front surface can cause breakdown of the thin dielectric between conductors. These are the most probable causes of the majority of chip failures seen during the array fabrication. Many of the visible damage problems are caused during the array assembly and alignment. The cause of problems during this phase is the awkwardness of handling the small chips while performing the required assembly procedure. Particularly during alignment and tightening, it is necessary to manipulate the chips which are now mounted to their carriers while viewing the procedure through a microscope. The microscope objective depth of field is so limited that it allows only one surface to be visible. Beyond the focal plane, small spurs or debris on the chip edges can come in contact with an adjacent chip causing a piece to be broken off. It must be remembered that the chip-to-chip nominal spacing between edges is 7.6 μm (0.3 mil). In addition, the staggered geometry has interlocking edges which also interfere with the alignment (see figure 22). As the chip carrier screws are tightened, these edges can be overlapped (confused by the out-of-focus condition) and the chip broken or cracked.

The 6-chip array carriers were mounted to the top surface of the base-plate, with the sapphire substrate sandwiching the chip carriers between it

42
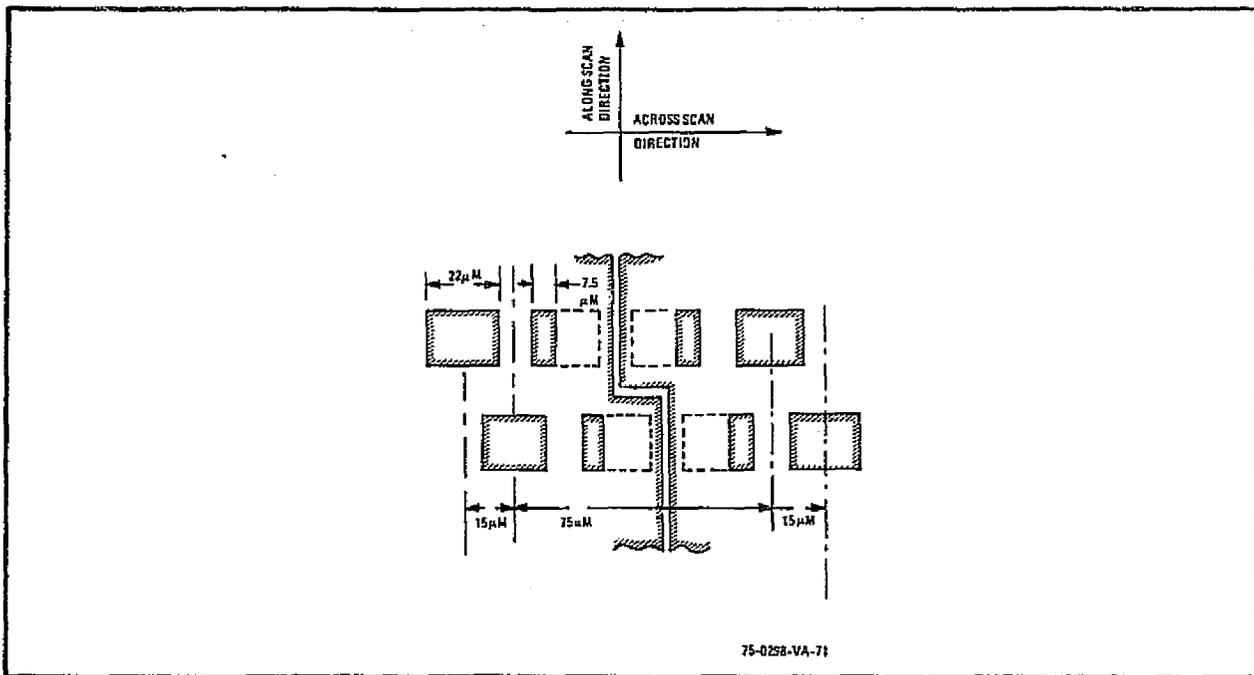
Figure 22. Bilinear Design (Detector and Edge Element Geometry)

and the baseplate. This technique provided the chip replaceability but re-quired removal of all chip wirebonds for a single chip change. Because of the gold-to-aluminum bonds on the chips, a maximum of three reworks were possible, but each rework had a good possibility of completely destroying a good chip bonding pad so that it also had to be replaced. This was an ob-vious limitation to the fabrication technique requiring improvement.

A modification to the mounting technique was incorporated into the 18-chip array. The chip carriers were modified to allow mounting to the bottom of the baseplate. This technique allows removal of individual chips without disturbing other chips of the array. Several chips were replaced in this array showing the great advantage of this technique.

A more subtle problem, because of the lack of visible damage, is the dielectric breakthrough. This can be caused by any front surface contact with even relatively small amounts of pressure. Most of the 18-chip failures, not attributed to nicks and cracks during the assembly phase, have been traced to front surface contact (see the Failure Analysis Report in Appendix D).

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A basic requirement of the breadboard program is to develop a totally contiguous array of photodetectors, i.e., no gaps between end-element detectors. The use of bilinear staggered detector geometry shown in figure 22 meets this requirement. But, as was stated in a previous paragraph, the physical interlocking of the chip edges is an extremely tedious, but feasible, mechanical assembly operation.

2.4.4 Computer Processing

The photodiode linear array detectors exhibit differences in signal offset and gain. Data from the program has shown that on a per bus basis, a majority ($\approx$ 80 percent) of the elements vary from each other by less than 15 percent of full scale. There is a finite number of elements with much larger offsets. Dynamic range and gain variations are relatively closely matched for all working elements. From this, it is seen that radiometric correction is the prime driving function in computer processing.

These characteristics (signal offset and gain) obscure the real information content of the raw data and therefore require removal prior to data evaluation. With the discrete element configuration, the linear array is ideally suited for computer processing of its data. The computer, therefore, was an important tool used during the breadboard linear array test phase.

The computer has two primary functions in this program: reordering of the staggered geometry and normalizing the data. During the data manipulation, other capabilities of the computer were also used for image cosmetics and data analysis. Although the listing (Appendix E) is lengthy, the actual function is not complex as can be seen in the simplified flow diagram of figure 23. The following paragraphs provide a more informative description of the computer functions.

Initially the data tape was formatted for 6-chip data. Rather than modify the hardware, when the 18-chip array was fabricated, the same 6-chip format was used. To process the data from the 18-chip array, three runs were made with each of three 6-chip segments. The software was modified to read

44
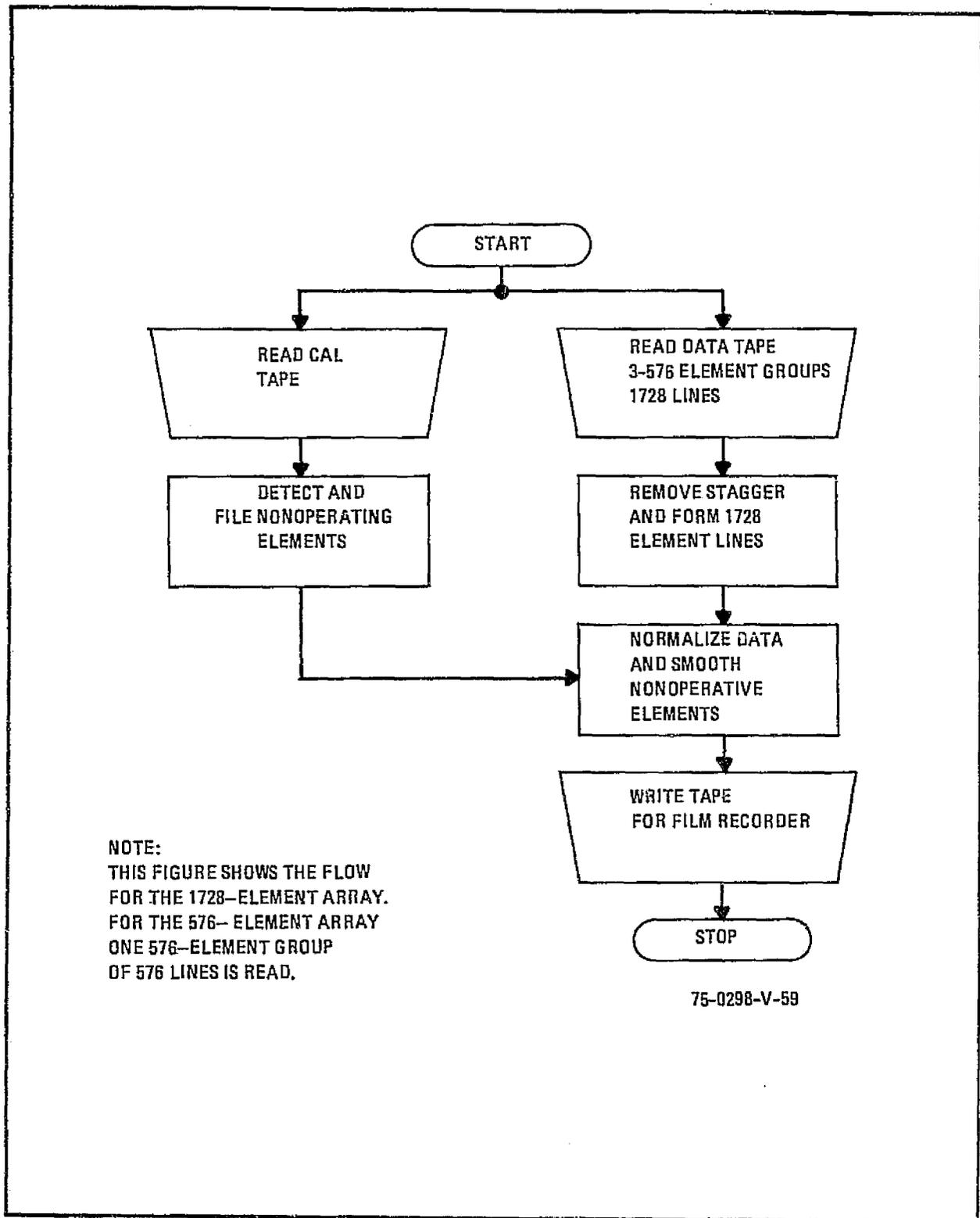
Figure 23.   Simplified Flow Diagram

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1728 lines of 576 elements each and then repeat the 6-chip process for each segment. The simple tape (calibration and scene data) format for the 6-chip array was changed to a two tape (one for calibration and one for scene data) format to handle the increased data requirement of the 18-chip array. The Appendix E program listing and the flow chart is for the 18-chip format.

The first information entered into the computer is the calibration data. These are array outputs for each element at five predetermined radiance levels. Five hundred seventy-six (576) samples are run for each element at each level. The computer averages these samples and stores the results for use in normalizing the picture data. While reading the tape data, the computer also smooths inoperative elements by averaging between the two adjacent elements to compensate for the missing data.

The next step is for the computer to read and store the image data. During the reading of this data, the inoperative elements are also removed by adjacent element averaging. Two 576 element data lines are read into the computer per tape access. The even numbered elements are stored for one tape access interval and then placed into the storage array with the data from the odd numbered elements read during the next interval forming a 576 element line. This removes the two pixel displacement (across scan) inherent in the staggered photodiode array. The elemental data values are compared to the calibration data and, by interpolation between the nearest higher and lower calibration values, normalized to a range of 0 to 255. One thousand, seven hundred twenty eight (1,728) lines of normalized data from each 6-chip section are accumulated in a drum storage area until the scene data from all three sections have been read.

The final step of a scene data process is to retrieve the data from the drum, taking a line from each 6-chip section, to form a single 1728 element data line. Values equivalent to each of the five calibration levels are added to the data lines (one level for each of 376 lines). This data is recorded on a magnetic tape for playback on a film recorder.

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Another benefit obtained from the computer usage was the obtaining of noise calculations. The same scene software was used except the scene processing was removed and an rms routine inserted. The rms deviation from the average level was calculated using 557 samples. This rms value was normalized to the 0 to 255 range for easy comparison to the signal levels. An rms value was then printed for each of the 1728 elements.

The computer was also used to obtain a comparison of temperature data. This was a simple plotting routine using the peripheral plotter. Room temperature and 0°C plots were made of the dark level for the 6-chip array. The effects of temperature become readily apparent with the plotted data as shown in Appendix F.

2.5 TEST PROGRAM

A comprehensive test program was performed on the Breadboard Linear Array Imager. Prior to performing the test program, a test plan, entitled Test Plan for Breadboard Linear Array Imager, Specification No. 21806-1, was prepared. This plan enumerated performance parameters to be evaluated.

2.5.1 Test Results

Test results are discussed in the following paragraphs. Each significant test parameter as identified in the test plan and technical specification is discussed as an individual performance item.

2.5.1.1 Noise

The noise contributors to the breadboard imaging system are from the detector, analog processor, and quantization. The detector noise was from 1.0 to 1.3 $\mu J/m^2$ based on measured manufacturing data in a 0.4 to 0.8-μm bandwidth with a 6000K source. A detector noise (NEI) distribution histogram of a typical 96-element chip is shown in figure 24. The MHP analog processor noise was measured at 0.39 $\mu J/m^2$ and the quantization noise was calculated to be 0.2 $\mu J/m^2$.

The breadboard system radiance band used for the noise measurements is centered at 0.54 μm with an 0.082-μm width with a source of approximately 3000 K. Although the measured manufacturing detector noise spectral

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MEAN NEI = 1.23 $\mu J/m^2$
STD. DEVIATION = 0.51 $\mu J/m^2$
MEAN IRRADIANCE = 40.7 mW/m^2
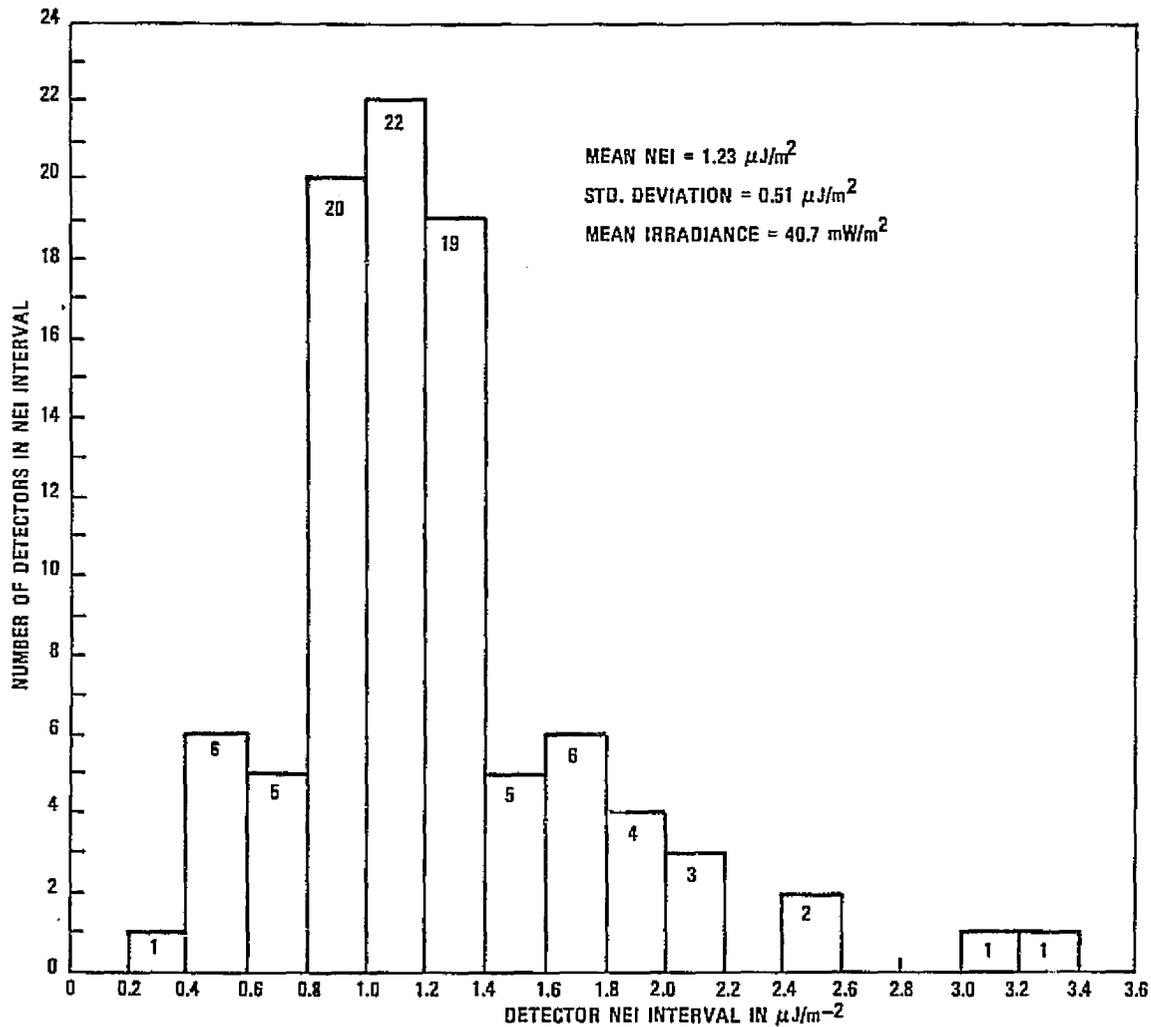
75-0298-VA-66

Figure 24.   Detector NEI Histogram For A Typical 96-Element Chip

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bandwidth is not the same as that of the breadboard, the product of the average detector response and integrated irradiance produces an error of less than 5 percent between the two measurements.

For tests on the breadboard, the two measurements (wide band and 0.5 - 0.6 μm narrow band) are considered to be equivalent. Taking the rms noise of each component of the system, detector, processor, and quantization noise, a total noise is calculated to be between 1.1 and 1.4 $\mu J/m^2$. A typical calculation of system noise (RSS) is:

$$\text{System noise} = \sqrt{(\text{detector noise})^2 + (\text{analog processor noise})^2 + (\text{quantization noise})^2}$$

where

- detector noise $= 1.3 \ \mu J/m^2$
- analog processor noise $= 0.39 \ \mu J/m^2$
- quantization noise $= 0.2 \ \mu J/m^2$

and,

$$\text{System noise} = \sqrt{(1.3)^2 + (0.39)^2 + (0.2)^2}$$
$$\cong 1.4 \ \mu J/m^{-2}$$

The noise measurement on the 6-chip array yielded a noise of 1.9 $\mu J/m^2$ (see table 4). To improve this condition, a processor change was made to correct a cross-coupling problem. The 18-chip array noise was then obtained yielding the maximum expected 1.4 $\mu J/m^2$ (see table 5).

The use of the MHP analog processor was expected to result in lower system noise. As seen above, the analog processor contributes less than 10 percent of the total system noise. For example, a 50 percent reduction in the MHP noise results in a reduction of 3 percent in system noise. The replacement of several detector chips in the 18-chip array coupled with the uncertainty in making precision analog measurements have obscured the effects of lower MHP noise. Therefore, the quantitative performance of the MHP has not been established. Actually, the test results of table 6 showed an

TABLE 4

RMS NOISE FOR 576 DETECTOR ARRAY WITH DISCRETE-COMPONENT ANALOG PROCESSORS

4.66	6.72	3.95	4.57	3.06	4.26	4.40	3.98	5.24	5.52	4.07	6.31	3.22	5.03	4.95	3.87
4.98	4.47	3.88	5.18	3.03	4.16	4.55	3.92	5.32	4.55	4.46	4.55	-11.38	3.77	4.57	3.74
4.74	4.23	3.70	3.95	3.30	3.89	4.74	3.78	4.89	4.00	3.51	4.21	3.03	3.32	4.33	4.06
4.79	4.88	3.07	4.23	3.95	4.19	4.87	4.70	5.33	6.05	3.70	5.87	3.41	5.19	5.51	4.09
5.15	6.16	3.54	6.03	3.23	4.93	5.00	3.72	5.33	6.00	3.34	5.83	3.26	4.51	4.55	4.14
5.15	6.05	3.48	6.07	3.17	5.51	5.14	4.26	2.79	5.49	4.03	5.63	4.56	5.47	6.45	5.33
-21.30	5.81	-11.38	4.33	5.14	4.24	4.39	4.29	5.61	4.37	4.27	4.96	4.27	5.74	4.78	4.27
4.53	4.21	3.80	4.75	3.99	4.17	4.85	4.35	4.63	4.10	3.69	5.03	3.93	4.42	4.26	4.20
4.53	3.88	3.44	4.49	4.04	4.85	4.82	4.61	4.83	3.99	3.48	4.80	3.72	4.61	4.54	4.05
4.52	4.17	3.75	5.18	3.54	4.78	4.62	4.39	4.98	4.20	3.51	4.86	3.70	4.78	4.71	4.11
5.00	4.40	3.91	5.13	4.19	5.03	4.52	4.47	4.91	4.41	3.99	5.04	10.90	4.94	4.61	4.34
4.43	3.88	3.94	3.95	3.94	5.21	4.76	4.03	5.06	4.40	4.30	5.44	3.87	5.52	7.50	6.15
6.11	5.81	4.37	5.29	4.22	4.47	5.09	4.81	5.37	4.31	4.08	4.57	4.22	4.62	5.03	4.62
5.57	4.36	4.16	4.97	4.92	4.68	5.58	4.73	5.04	4.42	4.16	5.09	5.02	5.31	5.17	4.84
5.34	4.56	4.32	5.29	3.91	4.68	4.67	4.25	4.89	4.18	4.11	4.44	4.10	4.71	4.67	3.97
5.15	4.34	4.08	4.83	4.03	4.76	5.01	4.21	5.17	4.26	4.34	4.94	4.27	4.61	5.08	4.38
4.98	4.20	4.27	4.27	4.21	4.33	4.96	4.43	5.05	4.28	4.28	4.79	4.40	4.58	4.91	4.43
4.92	4.47	4.18	4.42	3.91	4.50	4.75	4.65	5.19	4.34	4.31	5.49	4.38	6.19	7.48	-255.23
5.75	5.46	3.43	3.76	2.93	3.74	4.43	3.79	4.15	3.50	3.47	4.00	3.12	3.88	4.41	3.77
4.65	4.73	3.66	4.63	2.96	4.17	4.33	3.80	4.48	5.21	3.80	4.55	2.99	3.83	4.49	3.66
4.27	5.07	3.21	4.44	2.76	3.52	4.32	3.44	4.25	4.15	3.34	4.14	2.75	3.47	4.10	3.52
4.06	3.61	3.33	3.34	2.77	3.43	4.11	3.66	4.47	4.52	3.35	4.19	2.98	4.50	4.59	3.53
4.59	5.22	3.24	5.00	3.10	4.10	4.62	3.93	4.93	6.18	3.32	5.72	3.04	4.64	4.80	3.79
4.31	3.95	3.54	4.58	3.00	4.06	4.91	3.83	5.04	13.24	3.49	-9.28	4.62	-9.28	6.82	-6.87
4.54	4.10	3.20	1.57	3.05	3.44	4.18	4.26	4.86	3.72	3.83	3.89	3.61	5.54	5.52	4.58
4.88	4.25	3.54	5.27	3.19	4.94	4.37	4.70	5.06	3.94	3.64	5.37	3.01	3.88	4.26	3.69
4.25	3.67	3.65	3.94	3.03	3.40	4.15	3.49	4.33	3.77	3.46	3.98	3.00	3.53	4.15	3.42
4.41	4.19	3.38	4.12	3.01	3.45	4.21	3.55	4.65	4.10	3.64	4.43	3.21	3.56	4.30	3.57
4.81	4.07	3.78	4.09	3.32	3.94	4.67	3.47	4.49	3.82	3.42	4.20	3.14	3.55	4.49	3.58
4.74	3.98	3.95	4.15	3.00	3.57	4.04	3.51	4.93	3.93	3.88	4.51	3.49	3.66	6.33	4.56
6.05	5.75	2.78	3.70	2.96	4.23	4.06	6.11	4.43	6.36	3.25	4.96	2.70	3.83	4.42	3.51
4.45	3.70	2.78	3.70	2.88	3.65	4.29	3.30	4.30	3.50	2.56	3.49	2.89	3.28	3.99	3.27
4.27	3.50	2.67	3.51	2.98	4.20	5.00	3.45	4.39	4.04	2.51	3.60	2.63	4.82	5.53	3.63
4.47	4.79	2.96	4.03	2.87	3.83	4.45	3.67	4.31	3.70	3.17	4.14	2.77	3.71	4.25	3.61
4.42	3.81	2.92	3.90	2.85	3.37	4.05	3.27	4.53	3.43	2.80	3.80	3.04	3.41	4.31	3.33
4.39	3.63	2.91	3.59	2.84	3.60	4.37	3.40	4.57	3.74	4.24	5.15	6.84	10.37	22.26	31.20

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THIS IS THE COMPUTER PRINTOUT OF RMS NOISE (0.5-0.6 μm BAND) FOR 576 DETECTORS IN THE 6-CHIP ARRAY USING DISCRETE-COMPONENT ANALOG PROCESSORS. THE NOISE IN THE TABLE IS IN DIGITAL COUNTS WHERE ONE COUNT IS .45 $\mu J/m^2$. THE AVERAGE OF THE RMS NOISE VALUES IS 1.9 $\mu J/m^2$ WHICH INCLUDES 90 PERCENT LENS TRANSMISSION EFFICIENCY. INOPERATIVE DETECTORS ARE EXCLUDED.

75-0298-T-3

TABLE 5

RMS NOISE FOR THE 1728 DETECTOR ARRAY WITH DISCRETE COMPONENT ANALOG PROCESSORS

9.02	8.65	5.21	5.36	4.90	5.99	5.42	4.77	5.52	5.69	5.23	4.99	5.88	6.55	5.88	6.08
6.07	5.36	5.39	4.72	5.46	6.57	5.71	6.47	5.32	5.27	4.99	4.67	5.44	6.01	5.33	6.42
5.31	4.92	4.88	4.71	4.87	5.43	4.95	5.53	5.45	5.29	5.03	4.74	5.03	5.39	4.90	5.06
5.14	5.40	5.25	4.63	4.85	5.54	4.57	4.76	5.72	5.05	5.30	4.58	5.07	5.60	5.25	5.38
5.67	5.10	5.23	4.60	6.83	6.46	4.86	6.44	5.39	5.15	5.06	4.45	4.71	5.55	4.89	5.22
5.12	4.92	4.81	4.25	5.20	5.16	4.74	5.16	4.97	4.85	4.97	4.69	7.01	6.76	4.63	5.27
-17.09		7.18	-513.06	5.68	-82.19		6.17	-485.91	4.95	4.93	4.95	4.37	5.35	5.75	5.93	5.17	5.33
5.37	4.93	5.18	4.93	5.90	5.73	4.97	5.09	-10.95	5.04	5.33	4.81	5.66	5.57	5.00	4.88
4.83	4.93	5.47	4.94	22.04	5.59	4.44	4.45	5.42	4.85	5.46	4.91	4.57	5.53	4.45	4.32
5.02	-8.33	5.12	4.39	5.55	6.22	4.91	4.30	5.29	4.96	5.19	4.97	5.22	5.79	5.12	4.73
4.96	5.01	5.06	4.49	5.38	6.03	4.51	4.88	4.83	5.18	5.24	4.83	5.53	5.95	5.02	4.87
5.16	5.16	5.46	5.34	5.02	5.84	4.63	4.93	4.97	5.08	5.08	4.75	7.42	8.00	5.05	4.65
-.66	.00	-67.05	5.21	5.05	6.39	4.64	4.81	5.21	5.33	4.95	4.69	5.06	6.32	4.96	6.26
5.22	5.49	5.11	4.83	5.29	6.03	5.10	6.08	5.44	5.60	5.29	4.71	5.02	5.88	5.02	5.65
5.48	5.46	5.12	5.03	5.29	6.47	5.01	6.37	5.31	5.02	4.86	4.84	5.31	6.91	4.93	6.72
5.38	5.28	5.13	4.95	5.54	6.06	5.35	6.11	5.52	3.40	4.98	4.58	5.52	6.43	4.93	4.96
5.00	5.37	5.10	5.34	5.26	5.89	4.87	5.49	5.47	5.56	4.74	4.66	5.50	5.97	5.00	5.53
5.24	5.41	4.96	4.69	5.08	5.78	5.00	5.85	5.31	7.34	5.02	4.98	6.01	7.72	4.88	5.69
-9.38	7.82	4.70	5.08	5.51	6.15	5.88	5.33	5.94	5.51	5.48	5.76	5.66	6.63	5.96	5.92
5.64	5.68	5.60	5.67	6.07	6.57	5.42	6.30	5.96	5.49	5.46	5.31	5.32	6.46	5.82	5.83
5.42	5.45	5.19	5.27	6.29	6.54	5.60	6.03	5.58	5.56	5.30	5.07	5.83	6.81	6.01	6.18
5.96	5.41	5.98	5.48	5.78	6.65	5.74	6.45	5.58	5.48	5.34	5.17	6.19	6.63	5.82	6.32
5.82	5.54	5.76	5.51	5.57	6.20	5.40	5.62	5.73	5.69	5.39	4.91	5.78	6.68	5.65	5.91
5.80	5.20	5.25	4.78	5.00	6.67	5.72	5.95	5.57	5.25	5.66	5.11	7.83	.00	5.89	5.61

THIS IS THE COMPUTER PRINTOUT OF RMS NOISE (0.5–0.6 μmBAND) FOR 1728 DETECTORS IN THE 18–CHIP ARRAY USING DISCRETE–COMPONENT ANALOG PROCESSORS. THE NOISE IN THE TABLE IS IN DIGITAL COUNTS WHERE ONE COUNT IS $0.28\mu J/m^2$. THE AVERAGE OF THE RMS NOISE VALUES IS $1.4\,\mu J/m^2$ WHICH INCLUDES 90 PERCENT LENS TRANSMISSION. INOPERATIVE DETECTORS ARE EXCLUDED.

75-0298-T-4

TABLE 6

RMS NOISE FOR THE 1728 DETECTOR ARRAY WITH MHP ANALOG PROCESSORS

THIS IS THE COMPUTER PRINTOUT OF RMS NOISE (0.5–0.6 μmBAND) FOR 1728 DETECTORS IN THE 18–CHIP ARRAY USING MHP ANALOG PROCESSORS. THE NOISE IN THE TABLE IS IN μJ/m^2. THE AVERAGE OF THE RMS NOISE USING THE MHP ANALOG PROCESSOR IS 1.5μJ/m^2. INOPERATIVE DETECTORS ARE EXCLUDED.

75-0298-T-5

increase of $0.1\ \mu J/m^2$ up to $1.5\ \mu J/m^2$. It is concluded that this increase is not due to the MHP but to the use of replacement detectors with higher NEI.

Figure 25 is a histogram showing the system NEI distribution of approximately 576 detectors. The noise is plotted in terms of $\mu J/m^2$ in the 0.5 to $0.6\ \mu$m band.

In summary, noise equivalent irradiance (NEI) of $1.4\ \mu J/m^2$ has been achieved. With this NEI, signal-to-noise in excess of 200 is obtained from typical ERTS scenes, i. e., scene radiance of $10\ W/m^2$ - sr in the 0.5 - $0.6\ \mu$m band with an f/4. 7 optical system.

At the specified radiance of $1.2\ W/m^2$ - sr (0.5 - 0.6 μm band), and with the f/4. 7 lens setting and an NEI of $1.4\ \mu J/m^2$, a SNR in excess of 40 is achieved. The SNR of 40 significantly exceeds the program goal of 22.

For the specified condition using a target with a radiance ratio of 2:1 at the limiting frequency and an NEI of $1.4\ \mu J/m^2$, the low contrast SNR is calculated to be 4. This exceeds the program goal of 2 for the same conditions.

2.5.1.2 Linearity

Linearity measurements were made by making three independent runs with different irradiance levels. The upper level of each lower range was adjusted to be close to the low-level of the adjacent higher range and one amplifier gain change was made. Irradiance attenuation was produced by adjusting the aperture within a range and using the detector and radiometer between ranges. Since discontinuities are unlikely, errors between ranges were removed to make a smooth transition. The high radiance level outputs were increased by 7 to account for the gain change. Noise was removed by averaging 500 samples of each element. The full dynamic range covered is nominally 700:1.

The data indicated that the vast majority of the elements fall within 2 percent (full scale) of a best fit straight line. Only a few elements deviated from a straight line by not more than 3 percent.

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MEAN SYSTEM NEI = 1.49 μJ/m^2

NUMBER OF DETECTORS PER 0.1 μJ/m^2 INTERVAL

SYSTEM NEI IN μJ/m^2

75-0298-VA-67
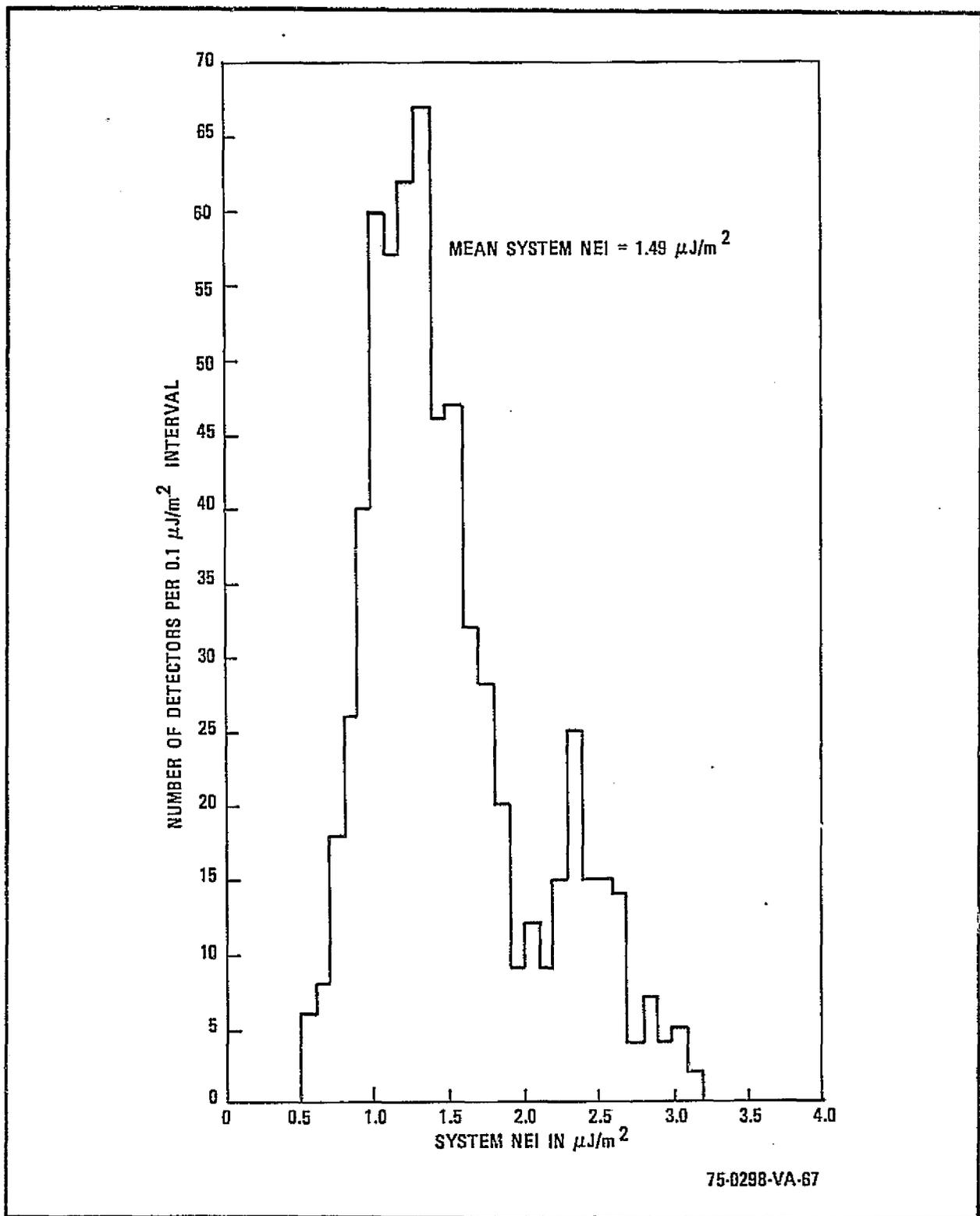
Figure 25.   System NEI Histogram for 576 Detectors

54

Chip manufacturing data (see Appendix H) indicates that a 2 to 3 percent deviation from a straight line can be expected. With careful design, the signal processing electronics will not add further nonlinearity.

2.5.1.3 Modulation Transfer Function (MTF)

The system modulation transfer function (MTF) for the breadboard system consists of the lens MTF, detector window function, image motion, temporal response of electronics, phase of image, and a Fourier coefficient factor for the squarewave targets used in the measurements. For the breadboard, a stationary scene is used and, therefore, image motion is not a factor. The electrical bandwidth (800 kHz) of signal processing electronics is very much greater than the array output frequency for a target period equal or less than the pixel spacing (0.6 mil), and therefore there is no temporal component. Phasing has also been removed by adjusting for maximum and minimum outputs. The detector window MTF component is rectangular, having a sine $(X)/X$ transfer function. The argument X is π times (detector window dimension) times (target spatial frequency). The lens factor was taken from Smith[2] with aberration indicated from the lens measured data.

The specification requires that the system MTF in the along-scan and across-scan direction to be approximately equal. Tests were performed to determine the extent to which this requirement was met. The experimental MTF in the across-scan and along-scan directions for the 6-chip and 18-chip arrays are shown in figures 26 and 27. It is seen from the figures that the MTF's are nearly the same. The effect of optics MTF can be clearly seen by observing the ideal detector response curve.

It is concluded from this experimental data that the specification of equal MTF in the along-scan and across-scan directions has been met.

[2] Smith, Warren J. page 322.
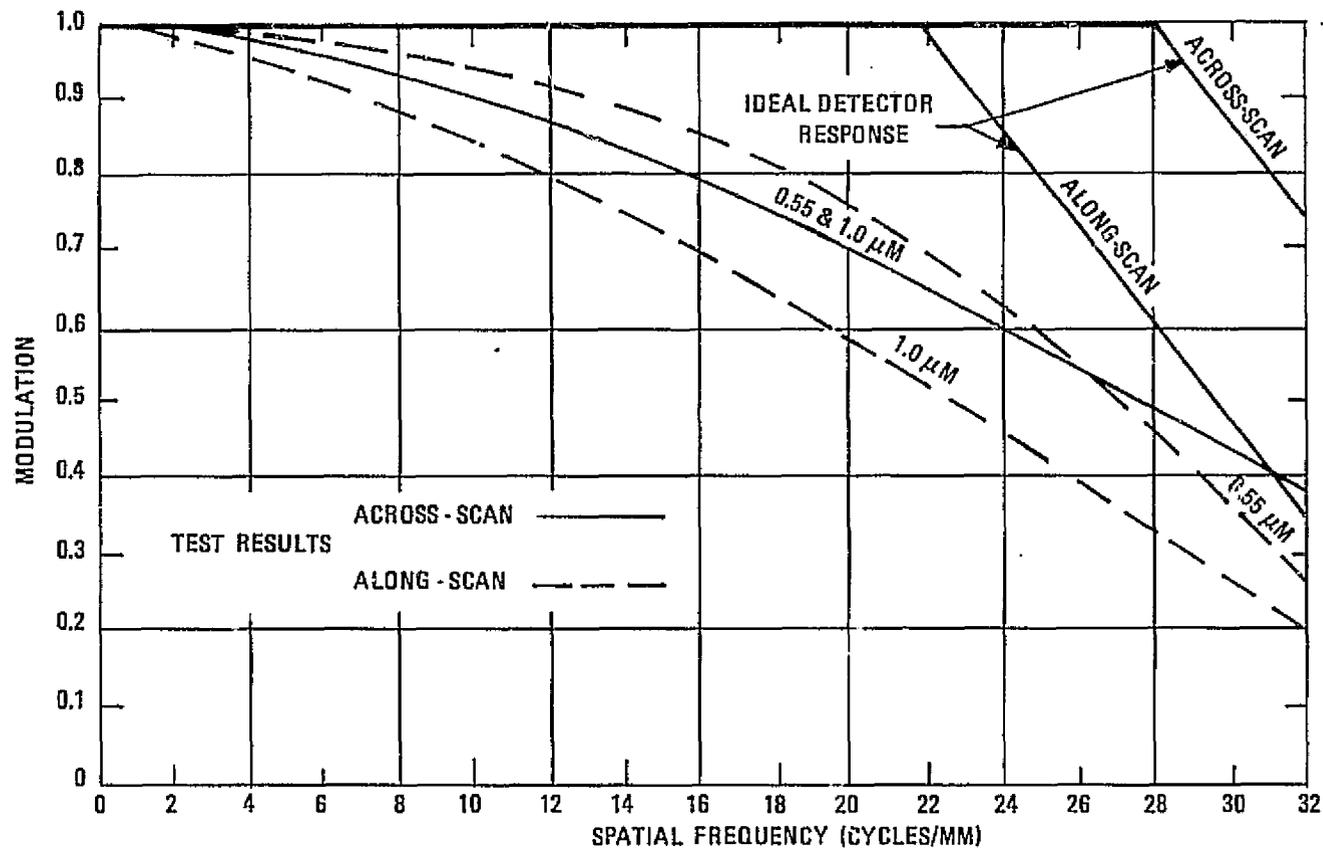
Figure 26. Squarewave MTF With Optics For 6-Chip Array
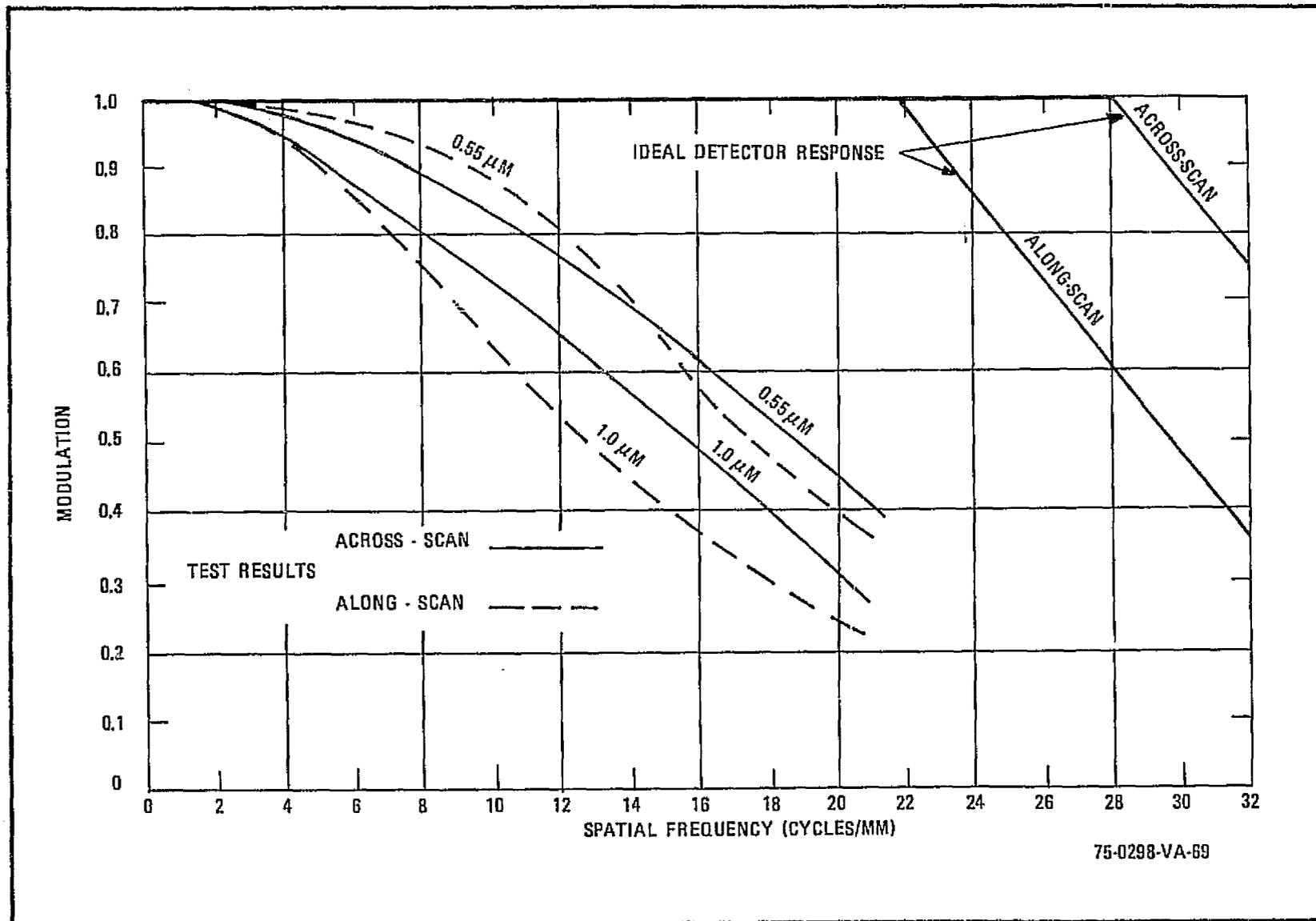
Figure 27. Squarewave MTF With Optics For 18-Chip Array

75-0298-VA-69

2.5.1.4 Dynamic Range

A performance goal of the breadboard is to demonstrate that the detector array is to have a dynamic range (in terms of input radiant energy relative to NEI) in excess of 600-to-1. Test results indicate that this goal was achieved.

Measurements of dynamic range were complicated by different bandwidths of the HP 8330 radiometer and detector, and the finite maximum energy output of the light source. For these conditions, a special procedure was developed to obtain dynamic range. The dynamic range of the detectors is measured by a procedure starting at low radiance and increasing to saturation. The procedure is to set the reference radiance to 0.7 to 0.8 μm with the use of bandpass spectral filter. This level is measured with an HP 8330 radiometer and the voltage level of a detector element output is also measured. For this test, the source clear aperture is more than 2 orders of magnitude greater than the detector element FOV. The spectral filter is then removed and the irradiance at the detector reduced with neutral density filters and the lens aperture until the original detector voltage is obtained. By removing the neutral density filters and changing the aperture settings the radiant energy to the detector is increased until saturation (no voltage change) is observed at the detector output. The neutral density and aperture changes required to achieve saturation provide a scale factor to be applied to the original radiometer reading.

2.5.1.5 Cross-Talk

Observation of the 6-chip MTF data reveals that cross-talk between adjacent detectors is not a significant factor in system performance. If crosstalk were present, it would be most predominant in the long wavelength (0.8- to 1.1-μm) band due to increased photon penetration at the high wavelength. Tests show the measured data higher, by 14 percent, along-scan, and 40 percent, across-scan, than the calculated value. A further examination of the measurement uncertainties involved show that the lens spectral

characteristics can cause a 25 percent variation in MTF (ΔMTF between $\lambda = 0.8$ and $1.0\,\mu$m). A 10 percent uncertainty in detector aperture dimension produces an 18 percent uncertainty in MTF. System noise is also a contributor by making high spatial frequency MTF measurements less precise. From the measured results and the known uncertainties, it can be seen that the 1 percent or less expected cross-talk is not detectable in the breadboard system.

2.5.1.6 Spectral Response

Spectral response data for the chips used in the 1728 detector (18-chip) array is shown in figure 28. The figure shows the mean spectral response of 96 detectors on one chip of the array and also the range of mean response for all of the chips. From the figure it is seen that the useful band extends from $0.4\,\mu$m to greater than $1.0\,\mu$m and the spread of mean responses is minimal. At wavelengths less than $0.8\,\mu$m, the peak-to-peak deviation is 6 percent, and at wavelengths greater than $0.8\,\mu$m, the peak-to-peak deviation is less than 12 percent. It is important to note that these spectral variations are removed in subsequent image processing operations.

2.5.1.7 Temperature

Although temperature testing was not a specific part of the initial program, the knowledge gained during the program indicated that temperature was a critical parameter for future array usage. In order to better understand the thermal effects on the data, a simple temperature test was run.

The array was mounted in a temperature chamber with the processor outside. A light source was placed in the chamber and all ports sealed. Two reference scans were made at 20°C, a dark level and a light level, to obtain a mid-range output. The lamp voltage was measured to allow later repetition of the same light level. The array was again operated at 0°C at both the dark and same light level as set by the lamp voltage. A third dark level was run at 10°C. Each of the runs consisted of 576 samples with the samples averaged to reduce the noise uncertainty. Appendix F includes the listing of the average data for each element.

RESPONSE IN PERCENT FULL SCALE

MEAN RESPONSE FOR CHIP NO. 3

RANGE OF MEAN RESPONSE FOR 18 CHIPS

WAVELENGTH IN MICROMETERS

75-0298-V-29
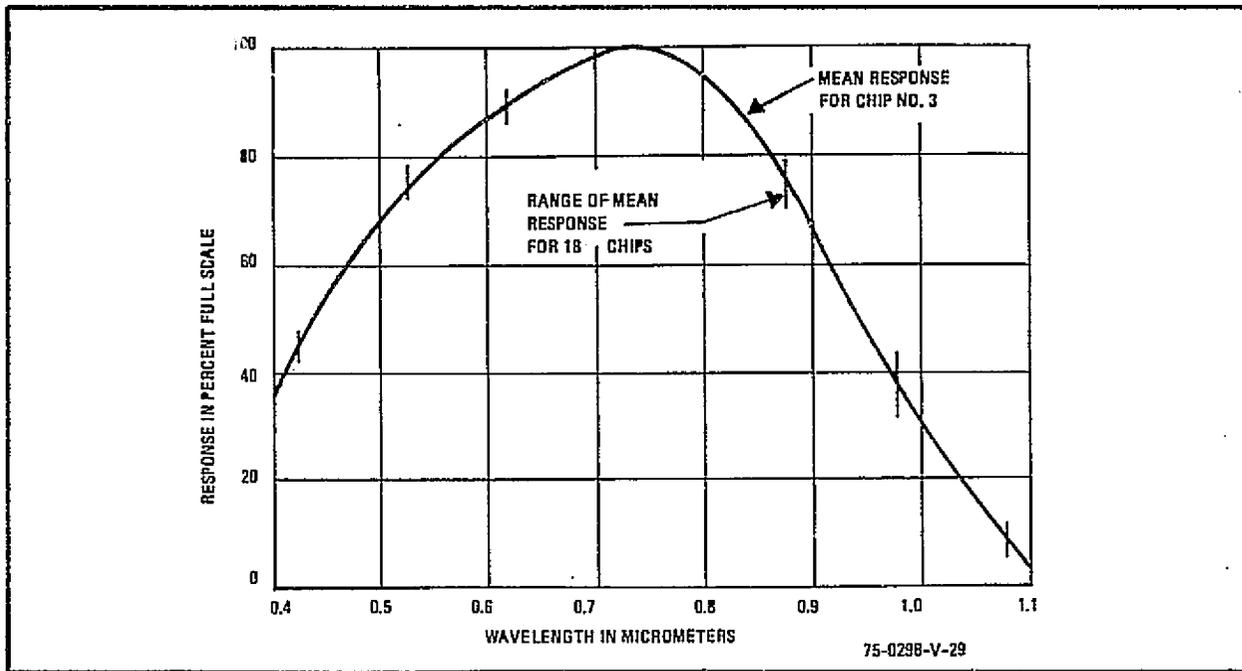
Figure 28. Spectral Response

The average dark level of the data reduces significantly at 0°C. But, of more interest, it was determined that the element to element offsets reduced by a nominal factor of 4 between 20°C and 0°C. This effect reduces the dynamic range required of a system since the offset is a significant portion of the typical signal level. It also reduces the temperature sensitivity of a system by making changes in offset a small fraction of a scene level. A composite plot of the dark level at 0°C and 20°C is given in Appendix F.

Although the temperature test did not provide a rigorous proof of gain variation factors, it did show that the effect is small. A total change of less than 10 percent was indicated over the 20°C temperature range.

2.5.1.8 Inoperative Elements

A goal of this program was to use detectors with no dead elements. With the 30 chips made available for the program, this goal has been nearly met with only one chip of the 576 element array having a dead element and none of the 1728 element array chips having dead elements prior to alignment.

60

Although the results of the program have shown the feasibility of producing linear array imaging systems, a perfect array was not achieved during the program. The 576 element array was fabricated with 1.2 percent inoperative elements and a 1728 element array with 5.5 percent was fabricated. These failures are attributed to handling and static discharge and a promising means of avoiding the problem in future systems is addressed in the fabrication improvement study discussed in paragraph 2.6.

2.5.2 Image Evaluation

The previous sections have presented the quantitative results of the breadboard linear array test program. This section presents the more subjective results of image evaluation.

2.5.2.1 Gray Scale Reproduction

An important requirement for a remote sensing system is its ability to faithfully reproduce scene gray levels. The results of scanning a nonstandard gray scale image show that the linear array technology is capable of meeting that requirement.

The plot of figure 29 shows the results of scanning a multi-level gray scale. Full scale irradiance at the detector (including a 90 percent lens efficiency) is 450 $\mu J/m^2$ providing a typical mission scene range. At 100 percent film transmission, the array output in counts would be 255. The plotted data shows an excellent relative linearity of within 1 percent of full scale for a best fit straight line. It also shows that the array output faithfully reproduces the gray levels within 3.7 percent absolute. Figure 30 is a film reproduction of the gray scale image from the array. The film fidelity is shown by the gray scale at the right, showing maximum irradiance, dark, and three factors of 2 steps.

2.5.2.2 576-Detector Array Imagery

Figure 31 shows four scenes made from the 576-detector array. The IFOV is 0.23 mrad with an irradiance of 0.03 mW/cm^2 in the 0.5 to 0.6 μm band.

61
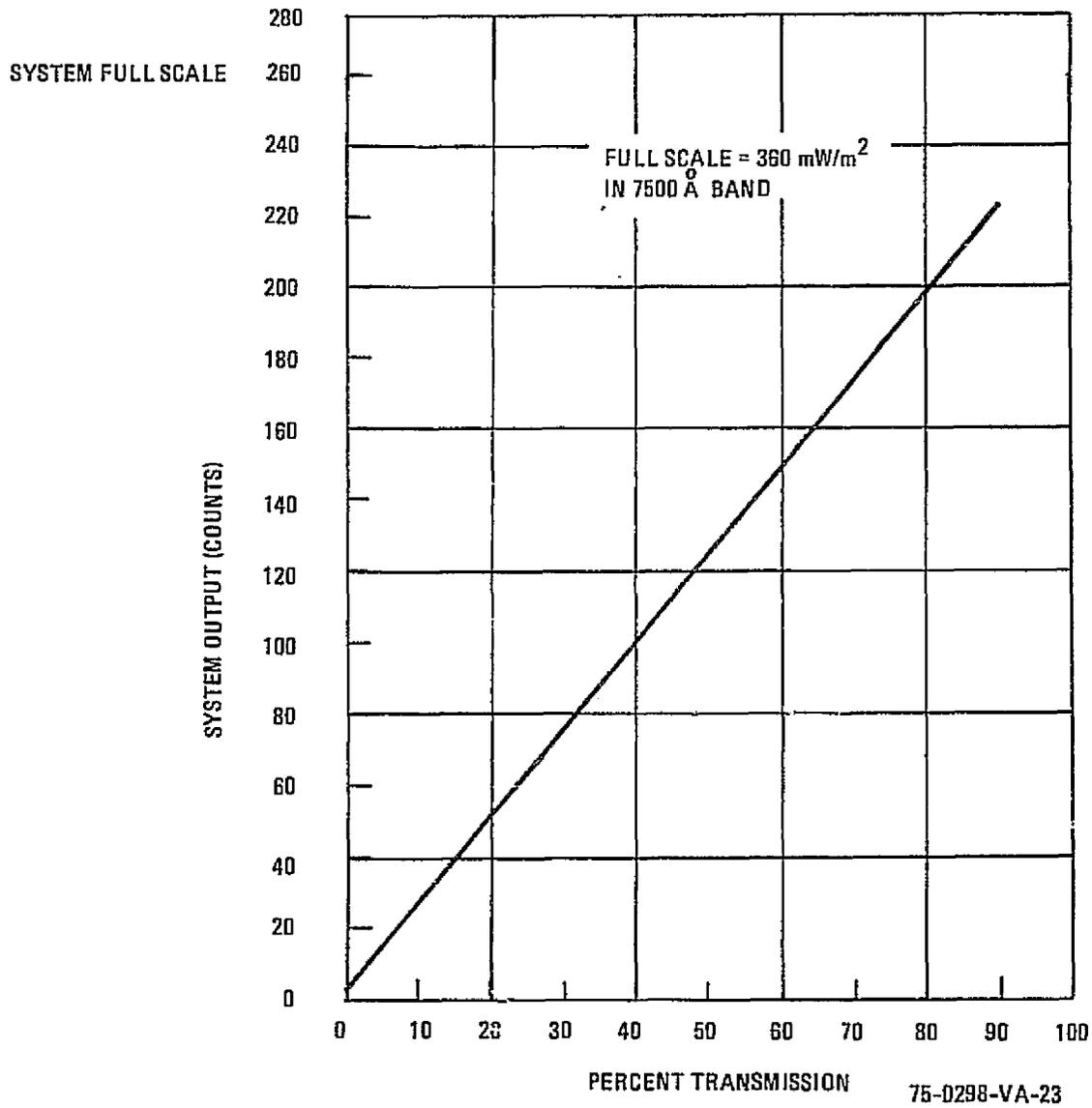
Figure 29. System Output as a Function of Gray Scale Transmission

62
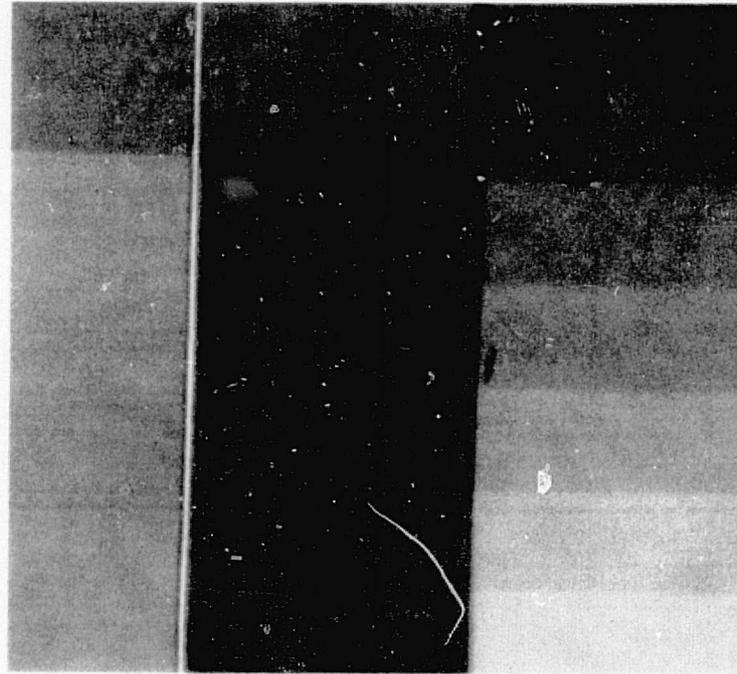
75-0298-PA-70

Figure 30. Gray Scale Image

63
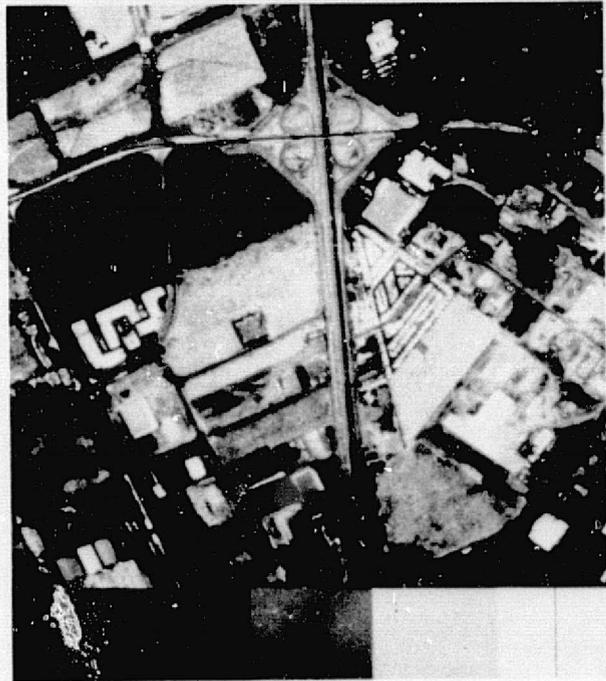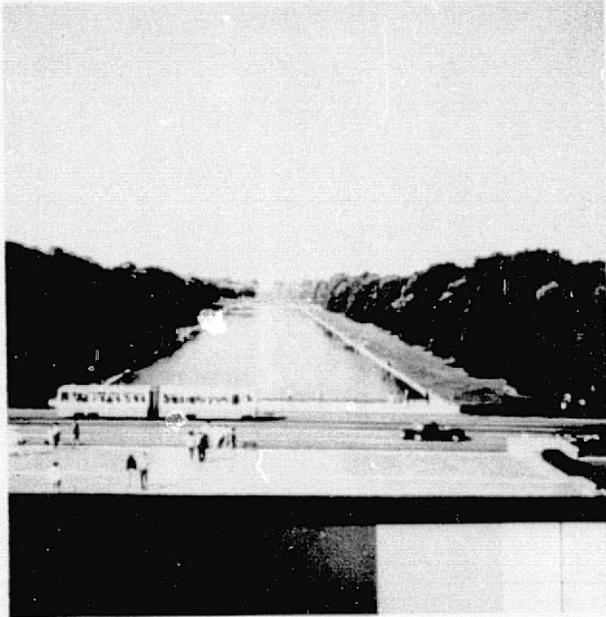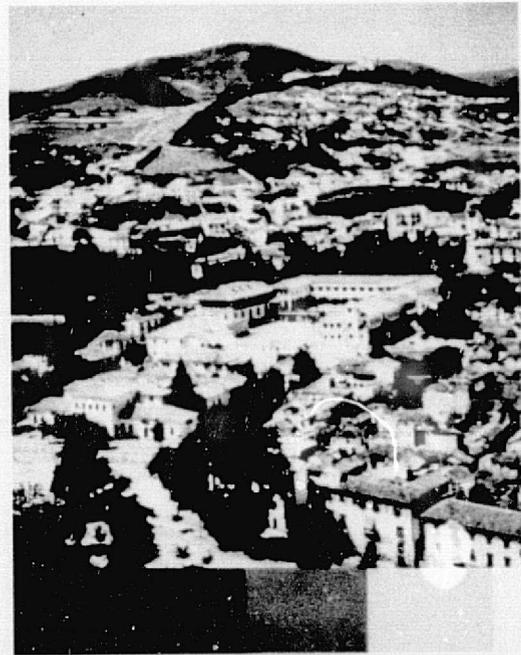
Figure 31. 576-Detector Array Imagery

2.5.2.3 1728-Detector Imagery

Figure 32 is a 1728-detector image produced from the breadboard from an aerial transparency provided by the U.S. Geological Survey. The figure is a contact print made from the exposed film produced from an Optronics P-1500 Photowrite display system. The facsimile recorder has a LED source which is optically focused and modulated to form an image with 64 gray levels and a square illumination spot size of 50 μm.

The image of figure 32 was produced from the 1728-detector, self-scanned photodetector linear array placed in the focal plane of the breadboard. The detector-to-detector spacing is 0.6 mil (15.6 μm) which results in an array length of 1.0368 inch. The scene radiance was 3.0 mW/cm^2-sr in the 0.7- to 0.8-μm spectral band. Using the breadboard lens at a focal length of 240 mm results in an effective focal ratio of f/12.8. The angular resolution under these conditions is 62 microradians.

75-0298-PA-25

Figure 32. 1728-Detector Image

Irradiance at the detectors for this image is 210 $\mu J/m^2$ and for an experimental noise equivalent irradiance (NEI) of 1.4 $\mu J/m^2$, a system signal-to-noise ratio of 150 was obtained.

2.5.2.4 Image Artifacts

One of the objectives of the breadboard program is to evaluate the performance of photodiode linear arrays in the context of image artifacts. Figure 33 is a bar chart target image obtained from the 1728-detector array and several image artifacts are identified. The artifacts are:

a. Nonoperating Elements

These are either seen as either black or white or white streaks and may be due to:

(1) The detector does not respond to light.

(2) The detector has a characteristic such as offset which is much different than the normal value.

(3) The detector has a high offset (or low) such that only a portion of the illumination range is within the linear processor range. This artifact is not likely to be observed on a bar target, but appears to be operating intermittently in a general scene.

b. Wave Effects

(1) In the across-scan direction, a waviness is seen which is due to phasing between detector and the scene edge (see figure 34).

(2) In the along-scan direction, both waviness and steps can be seen. This is due to both phasing between detector and scene edge and chip-to-chip alignment error.

c. Leakage Lines at Chip Edges

This is seen as a white line protruding into a dark area and is due to light leakage at non-metallized chip edges.

d. Tooth-Effect

The tooth-effect as shown in the figure is not an artifact and is included to show the effect of a computer program error. This error shows the detector stagger effects.

66
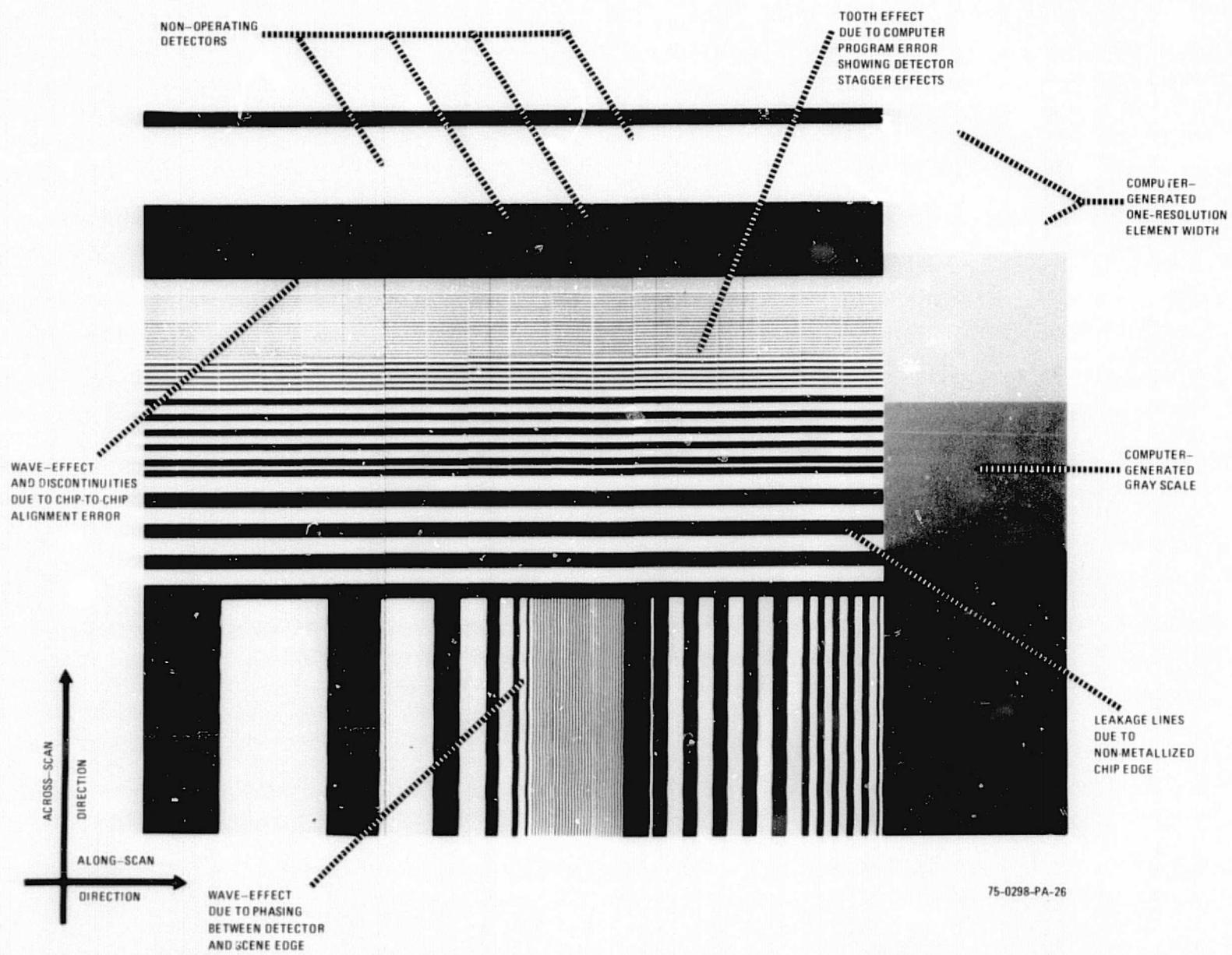
Figure 33. Examples of Image Artifacts on Bar Chart
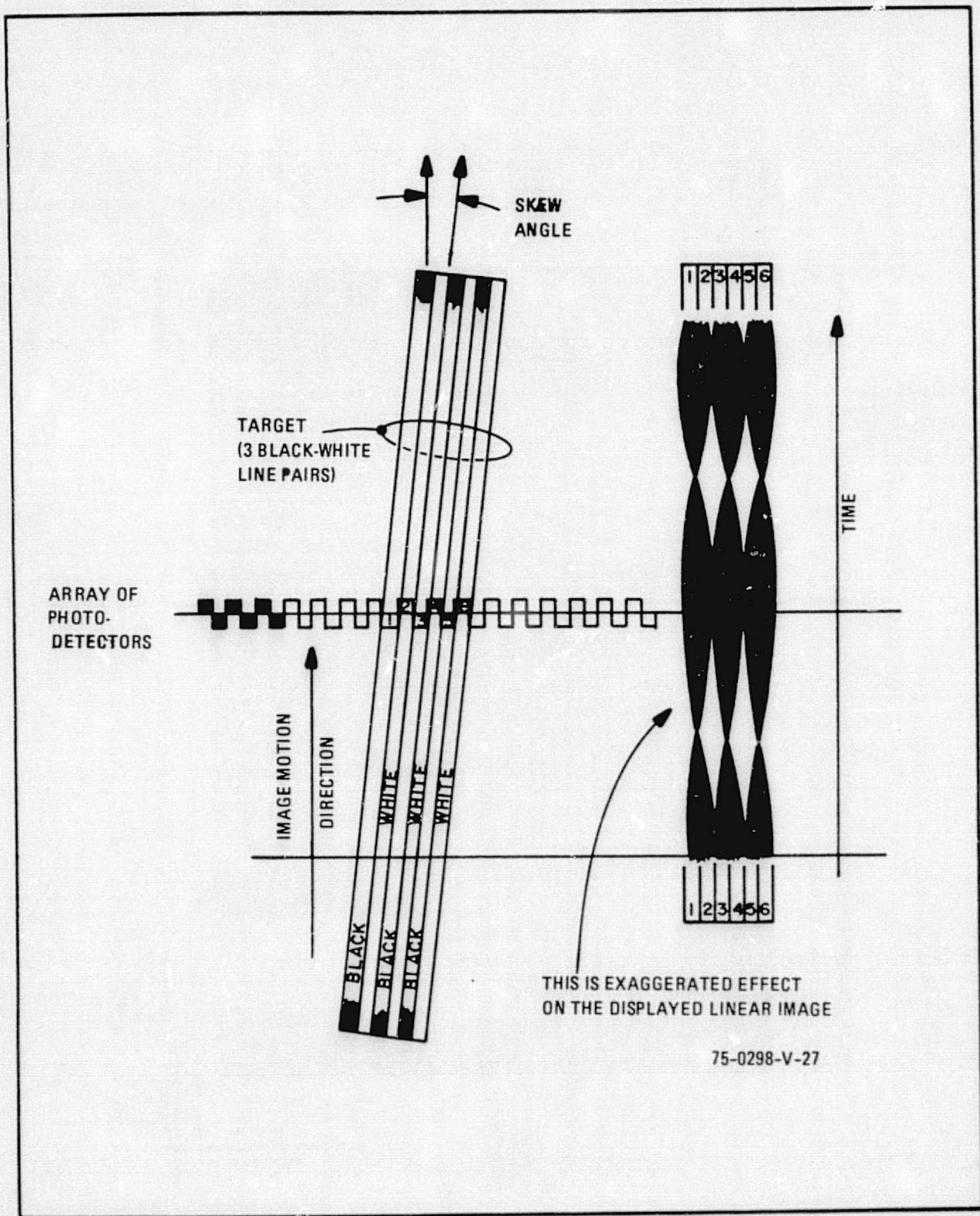
Figure 34. Wave-Effect Due to Phasing Between Detector and Scene Edge

e.   Thermal Streaking

This is due to the effect of the difference in temperature of detectors at calibration and when a real image is recorded.

2.5.2.5   Thermal Streaking

Tests performed on the breadboard system resulted in a phenomena which is referred to as thermal streaking.   This phenomena is common to highly parallel processing systems where it is caused by changes in dark current as a result of temperature changes of the detector array.   For example, a change of 10°C results in a 2:1 change in dark current (see Appendix F). Figure 35 shows two pictures, one with thermal streaking and one without. Full scale of these pictures is 211 $\mu J/m^{-2}$ and the streaking shown is equivalent to a 2°C temperature change at an ambient of +20°C.   The most predominant lines are equivalent to a 50 $\mu J/m^{-2}$ error or 25 percent of the full scale scene.   For an uncooled array (nominally 20°C) maintained at ±1°C, thermal streaks of ±2 percent of full scale would occur.   If the array is cooled to 0°C and maintained to within ±2°C, thermal streaks less than ±1 percent will occur.   The results of this test strongly indicate that for operational applications, thermal control of detector arrays is desirable.

2.6   ARRAY FABRICATION IMPROVEMENT STUDY

2.6.1   Introduction

In compliance with the Statement of Work, an array fabrication improvement study was performed.   The purpose of the study was to show the status of array fabrication, experience gained, and improved fabrication methods to achieve higher yield, reduced assembly and alignment time.

The methods proposed and the equipment recommended also serve the purpose of advancing detector array fabrication from the development to a limited production stage, a transition necessary prior to entering into a flight program.
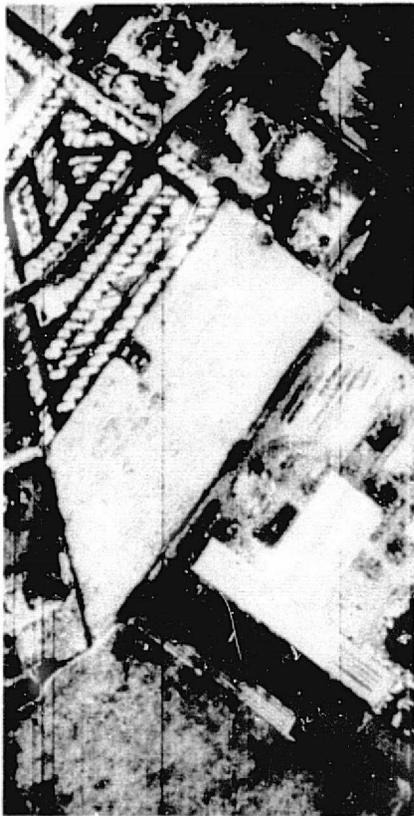
This scene includes lines attributed to a thermal streaking phenomena. The calibration curve used for data normalization and the scene data were taken at different times (and temperatures) in a laboratory without temperature control. Since the offset varies 5 percent/$^\circ$C, the 10 percent change in level between the calibration and scene runs indicates a 2°C temperature difference, well within the temperature range encountered in the room.
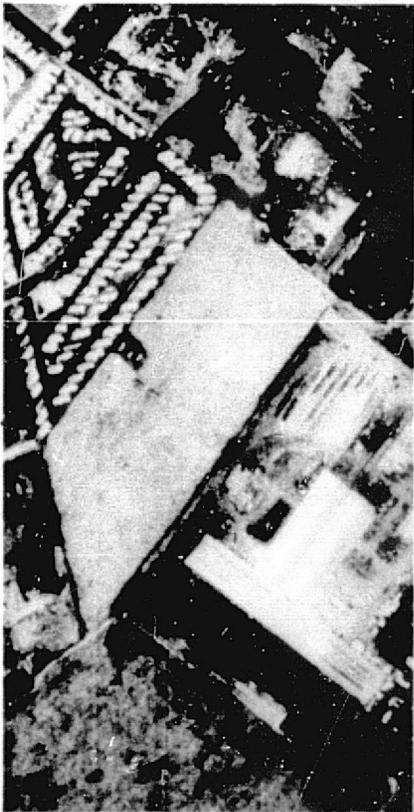
This scene was made with the calibration and scene data taken within a short time interval; i.e., 15 minutes. With the short interval involved, the array temperature did not change significantly. This shows the data improvement which can be obtained by thermal control of the array.

Figure 35. Example of Thermal Streaking

Since the beginning of the breadboard linear array program, three detector arrays have been fabricated, two 576 diode arrays and one 1728 diode array. In the assembly of a detector array there are many stages in assembly; the most complex steps are the joining of the photodiode chip to the chip carrier, the assembly of the chip carrier assembly to the baseplate, and alignment of the photodiode chips in the desired geometric position.

2.6.2 Alignment Results

As was expected, using manual methods of alignment resulted in some positional error in the arrays. Measurement results taken on the 6-chip (576-detector) array in the across-scan direction were:

- Average deviation from nominal position = 2.3 µm
- Maximum deviation from nominal position = 5.1 µm

In the along-scan direction, or along the chip common axis, the measurements were:

- Average deviation from nominal position = 2.5 µm
- Maximum deviation from nominal position = 5.1 µm

From these test results, it is concluded that the maximum deviation from the reference (best fit) line is:

- 0.28 (or 5.1 µm/18.0 µm) of the detector dimension in the across-scan direction
- 0.23 (or 5.1 µm/22 µm) of the detector dimension in the along-scan direction

With the use of a measuring microscope, an imaginary reference line (best fit) was developed which minimized the detector lateral excursion from the reference line. For the 6-chip array, the maximum lateral excursion was 0.2 mil (5.1 µm) and for the 18-chip array, the maximum lateral excursion was 0.3 mil (7.5 µm). These results are within the specification requirement.

In terms of resolution elements, the results of breadboard programs indicate that a positional accuracy of about 1/4 resolution element has been achieved. Expressed in terms of the linear dimension of an array chip, the alignment error is less than 0.3 percent of that dimension.

2.6.3 Problem Areas

When assembling and aligning chips in the detector arrays, two problems were observed. First, due to manual alignment and assembly, there is no mechanical control or assistance present during the movement of the chip into position. The operator must rely solely on manual dexterity. Occasionally this will result in collision between the chip being aligned and an adjacent assembled chip. This can result in a chip edge damage and possibly the loss of an end photodiode.

The second problem arises during chip positioning or alignment when the chip carrier assembly is assembled to the baseplate. The fixing screws are lightly torqued so that further damped movement of the chip carrier assembly in relation to the baseplate is possible. It is at this stage that final alignment takes place and is implemented by very light taps at suitable points on the chip carrier. Due to the several variables, including variations in surface roughness at the baseplate and chip carrier interface, and slight variations in applied torque, overshoot and undershoot may occur during alignment. There is also the possibility that while positioning on the X and Y axis, the chip carrier may commence to turn about the Z-axis (optical axis). This adds complications and increases time required to complete the alignment.

Therefore, techniques used on the breadboard were costly both in time and materials. To eliminate this condition for future applications, a study was performed to determine improved methods of assembly.

2.6.4 Study Objective

The objective of the fabrication improvement study is to identify improved methods of array assembly intended to improve manufacturing efficiency and reduce cost.

Improved manufacturing methods will not only result in efficiency and lower cost, but will also permit greater accuracy in chip alignment. Therefore, it is reasonable to reduce the experimentally achieved deviation of 1/4 resolution element to 1/10 resolution element.

Another important parameter is the chip Z-axis dimensional tolerance and is directly related to focus. For the breadboard, this adjustment was made manually during the process of cementing the chip to the chip carrier. This procedure resulted in lack of good control of chip face angle and coincident chip-to-chip face position on the Z-axis.

Figure 36 shows the relationship between depth of field and f/No. for the wavelength covered by the photodiode chips, assuming that the Rayleigh criterion is a reasonable design objective. For a candidate future sensor, an optical system with a focal ratio of f/4 is required. It is seen from the figure that the depth of focus for $\lambda = 0.5$ μm will be ± 16 μm. Improved techniques will ensure placement of chip within this limit.

2.6.5 Candidate Approaches

The operator skill required to align photodiodes on the breadboard model detector arrays was of the highest order. It follows, therefore, that for future applications, the number of operators available to perform such a function will be minimal, and the skill required from the operator cannot be guaranteed to be continuous. The degree of skill will vary from day to day because of human factors. The higher the degree of skill required, the lower the chances of maintaining such skill at peak level.

It is clear that in a flight program involving many arrays, it would be advantageous to find a way to reduce the necessity for highly skilled operations with attendant low yield high cost and prolonged assembly time.

The type of equipment required to minimize manual skills must be of a kind which eliminates the necessity for direct contact between the operator's hands and the parts to be aligned.

The approaches available generally fall into two categories. The first approach using micropositioners has certain disadvantages such as the greater possibility of involuntary overshoot while positioning and the possibility of mechanical crosstalk because of the need to control several axes from one source. All this can be avoided by using the second choice –

73
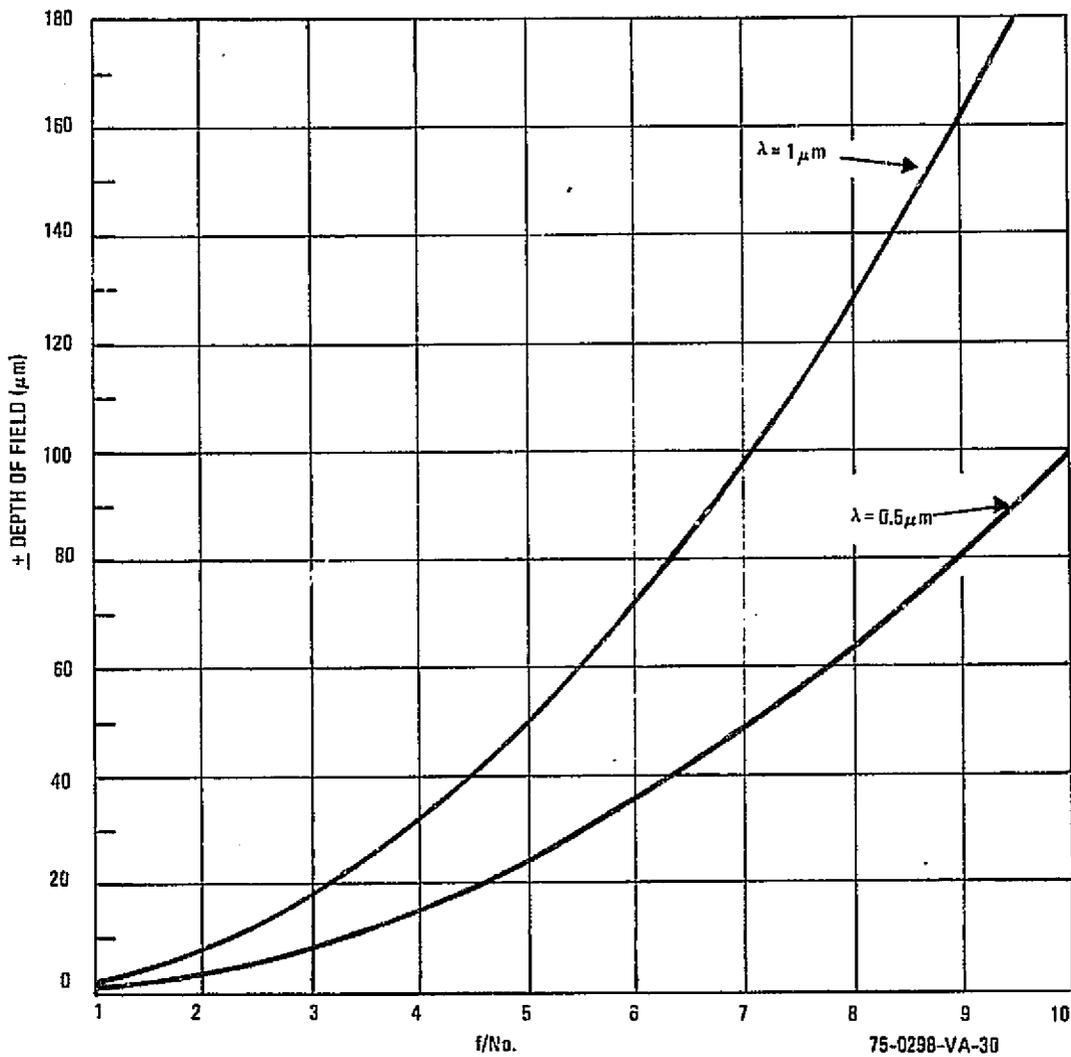
Figure 36. Depth of Field vs F-Number (Assumes Rayleigh λ/4
Criterion and Depth-of-Field Given as Deviation From Nominal)

whereby each axis movement is controlled separately, thus eliminating the possibility of crosstalk. Direct axis movement would be implemented using micrometer controlled positioning. The latter ensures smooth, damped, predictable movement without overshoot. Thus, this latter approach has been selected as the preferred approach.

2.6.6 <u>Preferred Approach</u>

The preferred micropositioner, including the microscope used for observation during positioning, is shown in figure 37 and comprises the following:

    a. Detector Array Fixture

    b. Goniometric Turntable, Phase Z

    c. Extension Plate

    d. Translation Stage, X-Axis

    e. Translation Stage, Y-Axis

    f. Laboratory, Z-Axis

    g. Baseplate

    h. Device for Holding Chip Carrier during Assembly.

Additional views of the micropositioner are shown in figures 38 and 39. The entire equipment is mounted on the microscope stage plate. During assembly of the development arrays, a microscope with total magnification of 25X was used for observation during assembly, and 100X magnification for final alignment. Illumination during assembly is obtained from a source in the base of the microscope which provides a silhouette of the chip carrier as it approaches its optimum position in the detector array. In this way, an observed clearance can always be maintained while the carrier is moved into position, thus minimizing the possibility of chip edge damage.

Before operating the micropositioner, the chip carrier will be placed and held on an electromagnet so that the center of chip will be aligned with the axis of the turntable. By appropriate setting of the various micrometer controls of the positioning equipment, the chip carrier assembly will be

MICROSCOPE

ARRAY ASSEMBLY

GONIOMETRIC TURNTABLE

Z-AXIS POSITIONING

MICROSCOPE STAGE PLATE

75-0296-VA-32
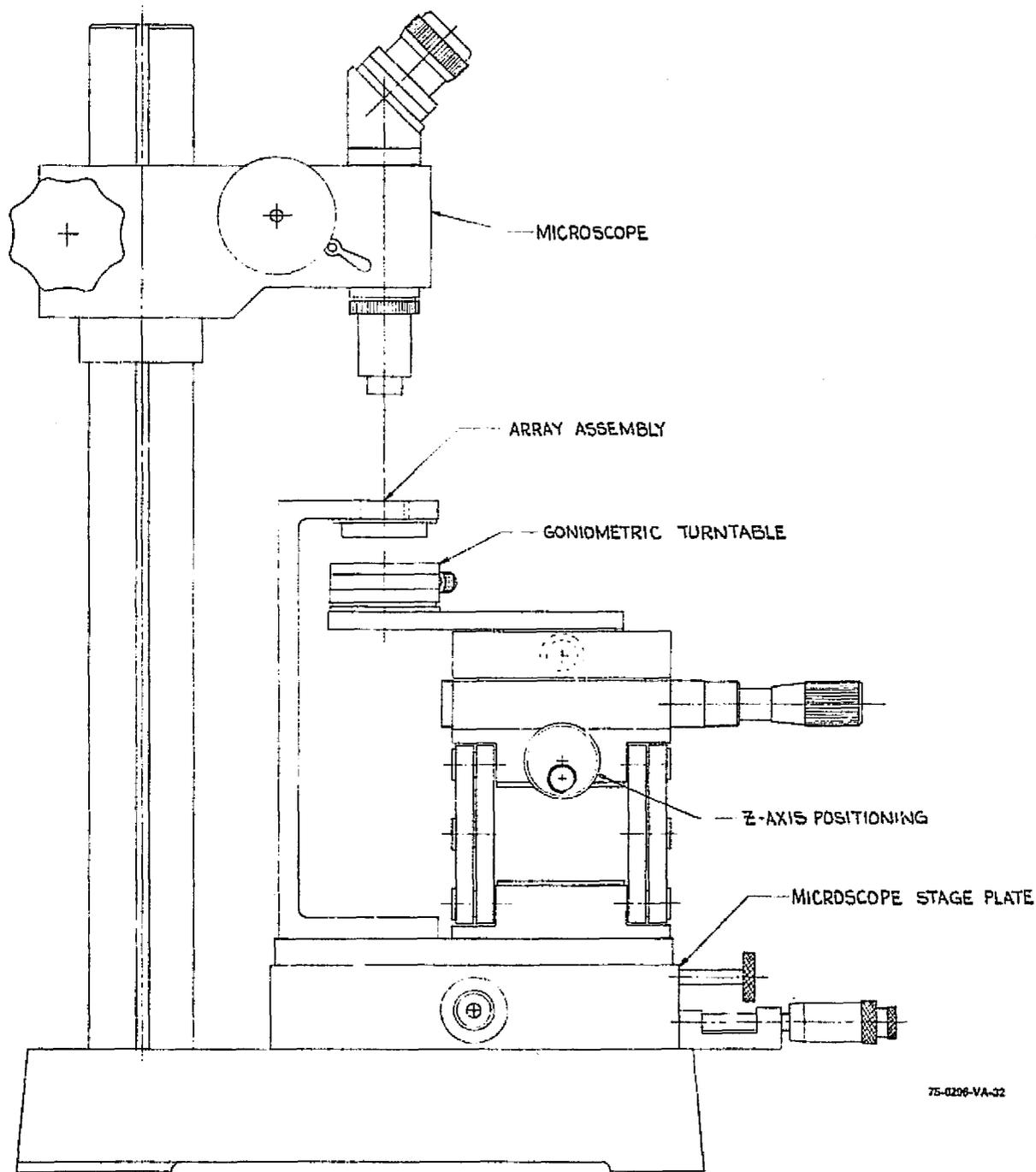
Figure 37. Chip Carrier Assembly Micropositioner and Microscope

76
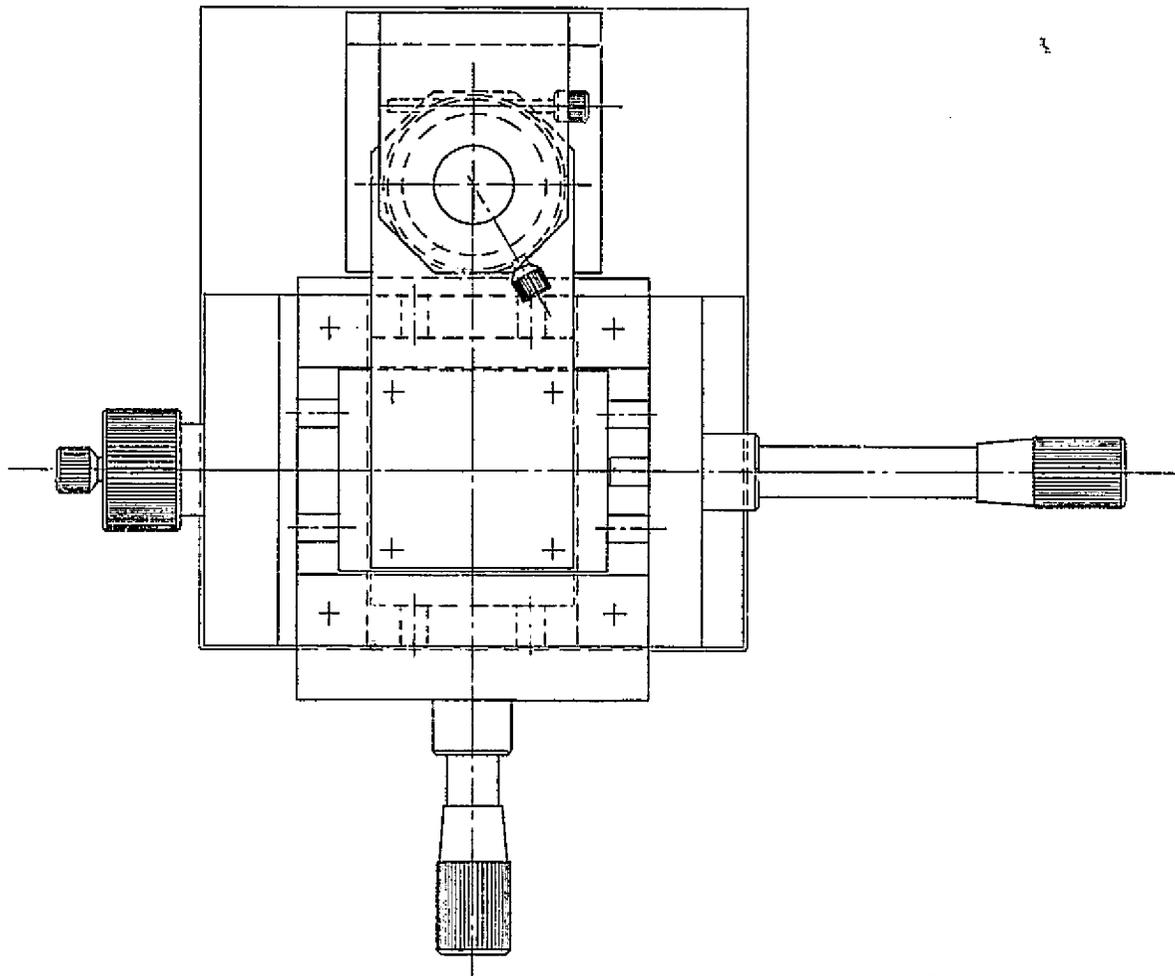
76-0298-VA-34

Figure 38.   Chip Carrier Assembly Micropositioner (Top View)

77

GONIOMETRIC TURNTABLE

TRANSLATION STAGE

LABORATORY JACK

75-0288-VA-33
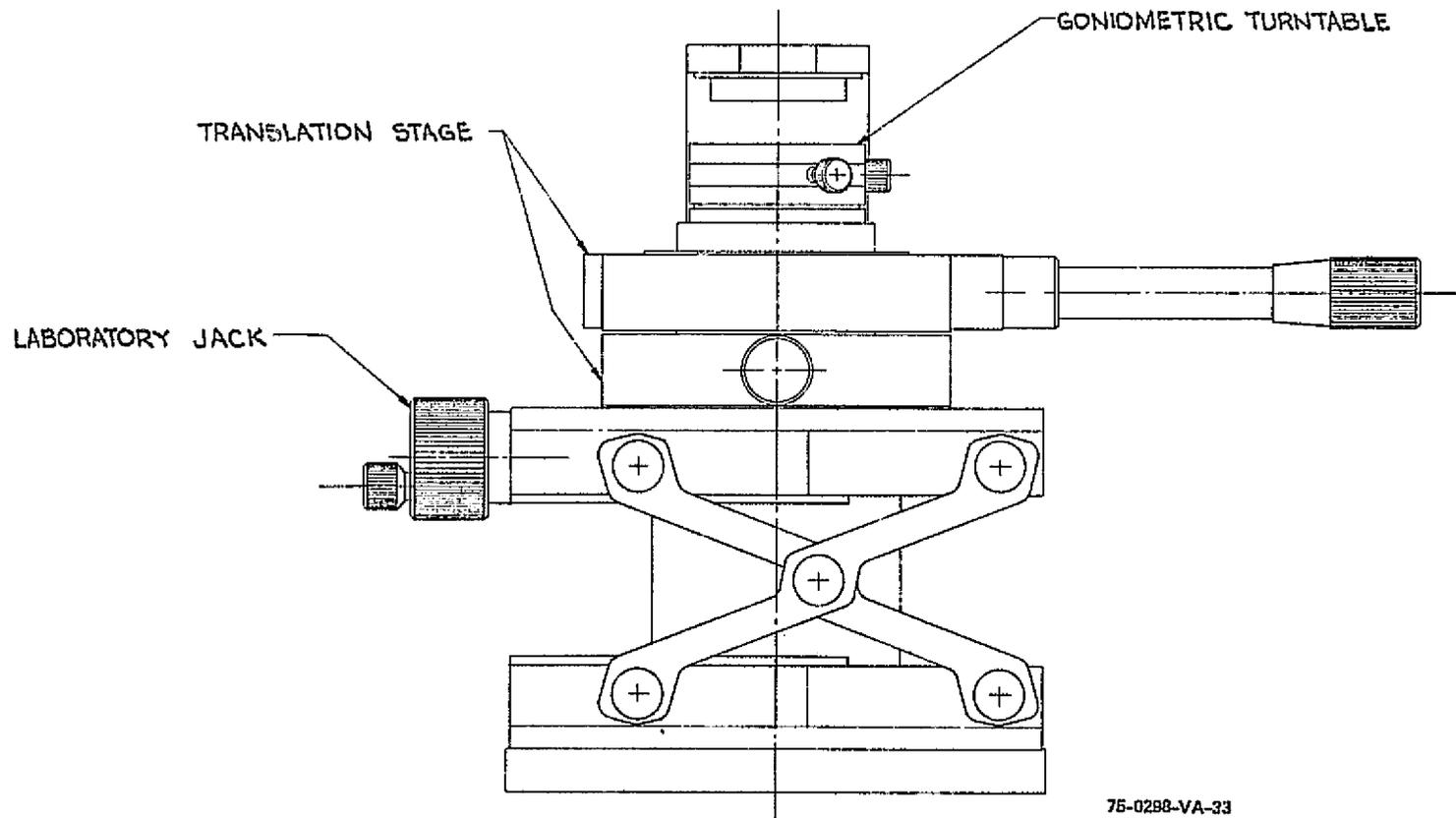
Figure 39. Chip Carrier Assembly Micropositioner
(Side View Showing Jack)

elevated to the level of the detector array baseplate and then moved to and held in the desired position - at which time the chip carrier screws will be inserted and tightened. The process will be repeated until the whole array is finally assembled. Figure 40 shows an exploded view of the array assembly. Figure 41 is a view of the assembled chip carrier.

There are indications that, in the future, greater detector positional accuracy will be required although not yet precisely specified. With this in mind, the micropositioning equipment chosen will have the capability of positioning chips within 1/10 of a resolution element. To achieve this result depends on the use of high sensitivity micrometers and the rigidity of structural members holding the positioning system together.

Due to the variation in chip thickness, it was not possible in the breadboard program to control chip surface height variation in the image plane. However, a jig has been designed (see figure 42) which reduces the variation in height of the chip surface plane above the chip carrier mounting surface to an acceptable value. The jig is constructed in such a way to make it fully adjustable and capable of being set to a precise position by the use of gage blocks.

In the sequence of chip-to-chip carrier assembly, the chip is placed face down in the bottom of the jig resting on a reference surface. The part of the chip in contact with this surface contains none of the circuitry or bonding pads associated with the electrical-optical configuration and, therefore, no damage to the active surface of the chip is anticipated. Physical contact is made only with the bare silicon chip which presents a standard reference contact for all chips.

The insertion of the chip will be followed by the chip carrier with chip mounting surface facing down. The mounting surface contains a narrow slot into which is pressed a preformed epoxy film adhesive of suitable volume.

79

Substrate
Assy

Base

Chip Assys

Interconnection
Board

Housing

Sensor Assembly

Interconnection
Layer

Dielectric
Buss Layer
Dielectric
Gold Shield
Sapphire
Substrate

Substrate Assembly
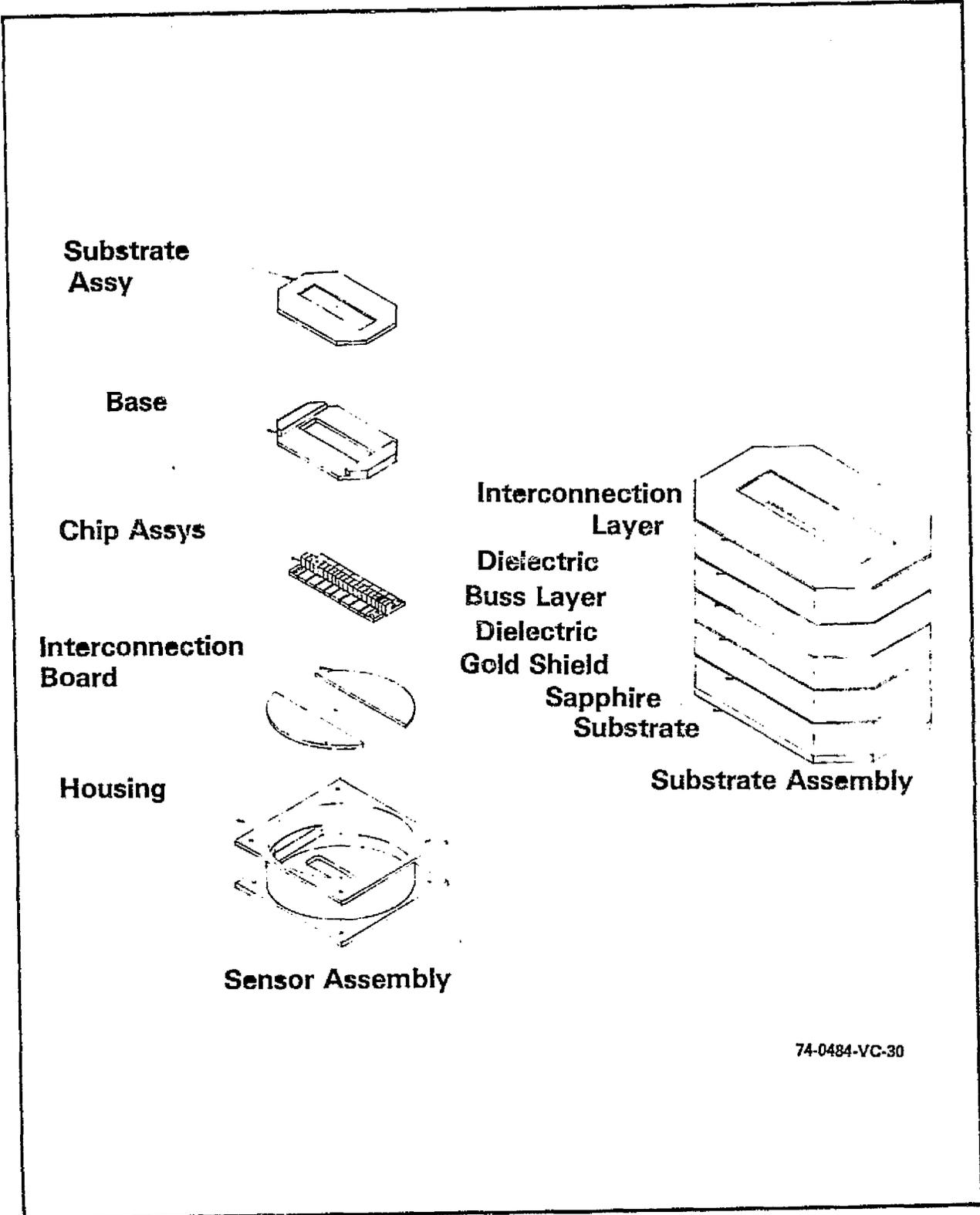
74-0484-VC-30

Figure 40. Exploded View of Array Assembly

80

CHIP CARRIER
MOUNTING SURFACE

EPOXY FILM

CHIP

CHIP

EPOXY
BOND

BASE
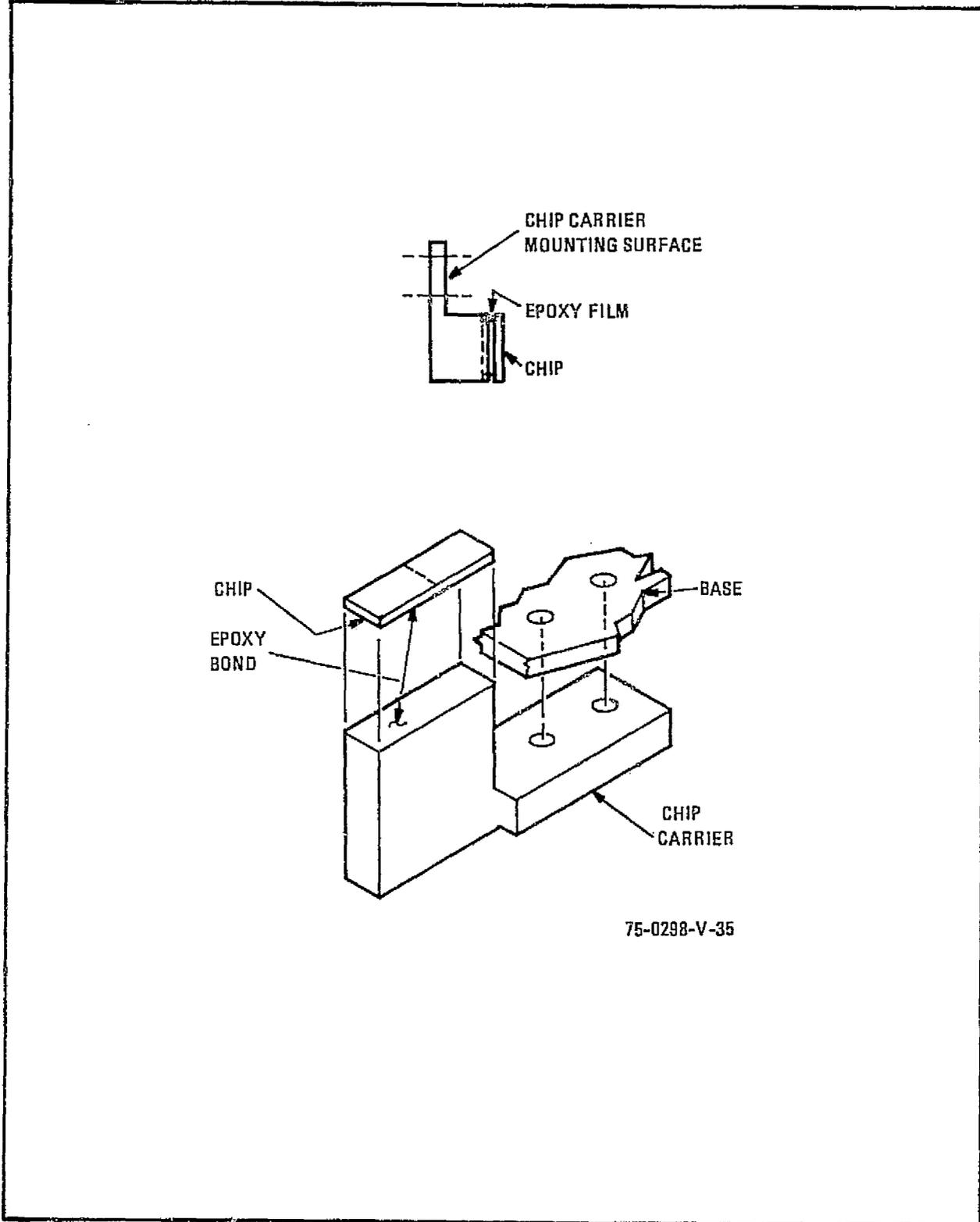
CHIP
CARRIER

75-0298-V-35

Figure 41. Assembled Chip Carrier

81

CHIP CARRIER-JIG
CONTACT SURFACE

CHIP CARRIER

CHIP

A

B

B

A

SECTION A-A
SCALE 4/1

SECTION B-B
SCALE 4/1

75-3294-VA-36
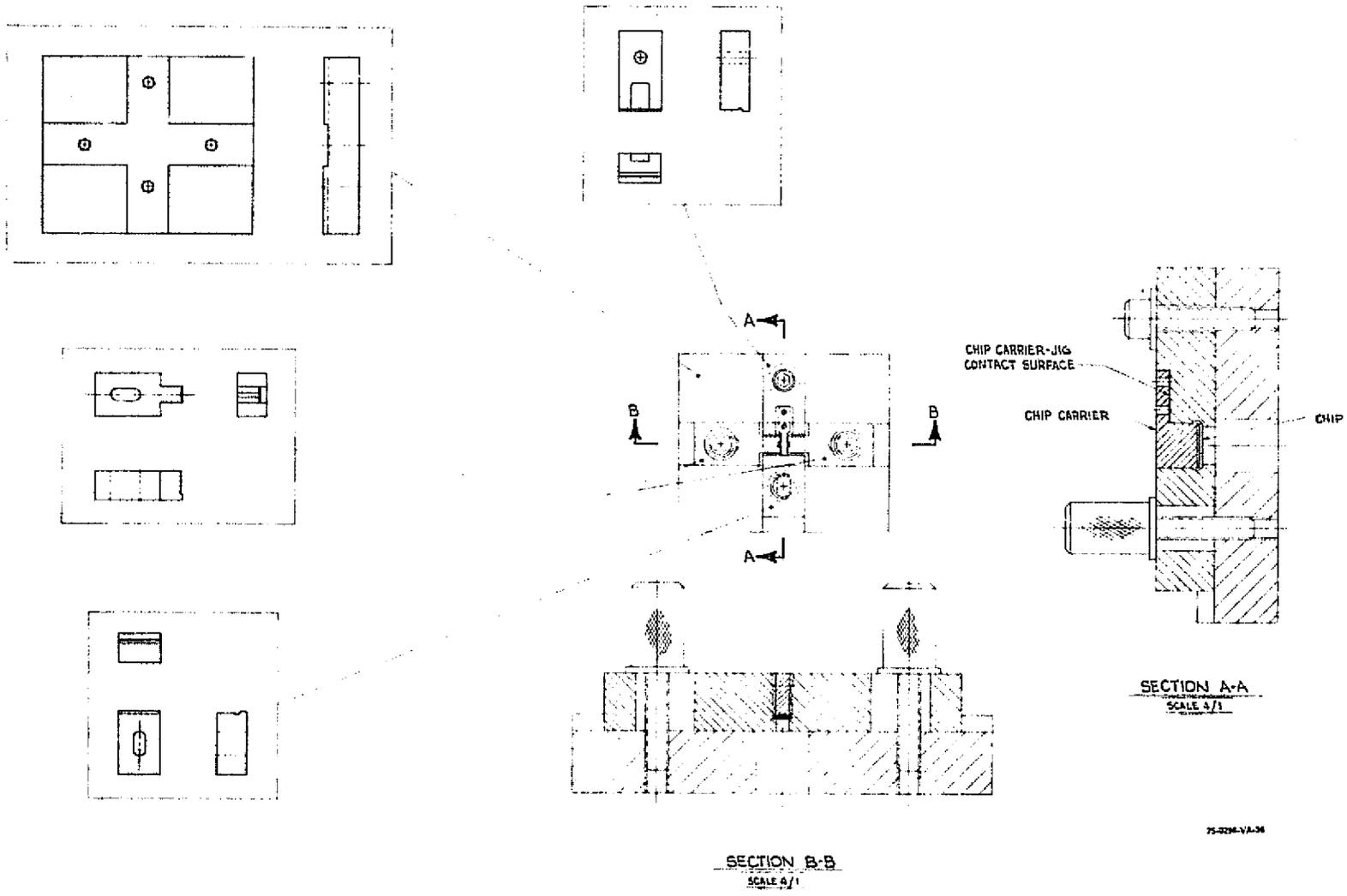
Figure 42.   Chip Carrier Assembly Jig

With the chip carrier in place, there will be a gap between the chip carrier mounting surface and the chip carrier jig contact surface. The gap is caused by the thickness of the epoxy film now in contact with the underside of the chip.

Upon application of heat to the jig of a temperature sufficient to cause the film epoxy to flow, and upon the application of a light pressure to the chip carrier base, the epoxy will flow and the gap will close. This will ensure that the distance between the active surface of the chip and the carrier mounting surface will be uniform on all chip carrier assemblies. Further application of heat will cause the epoxy to cure. All chip carrier mounting surfaces will be assembled to a common baseplate reference in the detector array. This will keep the Z-axis chip surface deviation to a minimum.

There are many factors contributing to the quality of the final product. Reference has been made to suitable equipment to assist in accurate positioning of detectors. However, the operator must have the means to observe and check the accuracy of his operation. Not only must the positioning of detectors be accurate, they must be seen to be accurate.

This brings to mind the problem of seeing. During the assembly of the development arrays, use was made of Leitz Simplex Microscope System, and the accuracy of observation of this system depends upon the operator's ability to achieve parallax focusing. Failure to do this causes an apparent shift of the filar line in relation to the object being measured. This occurs if the eye is unconsciously moved off the optical center. This may happen after many observations and is probably due to eye fatigue.

A system that will eliminate subjective errors of this nature is the Tele-Microscope, a closed circuit television system. This comprises a Leitz microscope, and a video camera head and display. The camera head is fitted to the microscope tube and replaces visual observation by the eye through the normal microscope eyepiece. Unlike the human eye, the video

head cannot move and parallax error is eliminated and thus improves overall fabrication accuracy. A further added advantage with the Tele-Microscope is the useful magnification up to 400X, and the electronically generated filar lines displayed. Together with an associated measurement computer and digital readout, measurements as small as 0.1 µm can be made provided the edges of the photodiodes are sharply defined. Such a system will mean faster and more accurate measurements with only moderate operator skill requirements.

A flow diagram of the entire fabrication procedure for potential use on a future flight program is shown in figure 43.

2.6.7 Fabrication Study Summary

The experiential learning gained from the breadboard program has been extraordinarily beneficial in many areas. The experience gained in the fabrication arrays has shown that it is totally feasible to fabricate long arrays. Although positional accuracies of about 1/4 resolution element were achieved, where 1/10 is a suggested goal, the experience gained in this preliminary program strongly indicates that the latter positional accuracy can be achieved for future requirements.

CHIP CARRIER
MANUFACTURE

PHOTO-DIODE CHIP
PROCUREMENT

BASE PLATE
MANUFACTURE

GLASS - METAL
SEAL FABRICATION

SAPPHIRE INTERCONNECTION
SUBSTRATE
ARTWORK - ELECTRON BEAM
DEPOSITION

AMPLIFIER & FILTER
CHIP PROCUREMENT

P/C DISTRIBUTION BOARD
ARTWORK
& MANUFACTURE

DETECTOR ARRAY
CASE
MANUFACTURE

BOND CHIPS
TO CHIP CARRIERS
USING SPECIAL
JIG

ASSEMBLE
GLASS FEED THRUS
TO BASE PLATE

BOND CHIPS TO
FINISHED SAPPHIRE
INTERCONNECTION
SUBSTRATE

ASSEMBLE
CHIP CARRIERS
TO BASE PLATE
AND ALIGN

ASSEMBLE SAPPHIRE
INTERCONNECTION
SUBSTRATE TO
BASE ASSEMBLY

WIRE BOND SAPPHIRE
INTERCONNECTION
SUBSTRATE TO PHOTO-
DIODE CHIPS AND GLASS-
METAL FEED THRUS

ASSEMBLE DETECTOR
ARRAY ASSEMBLY
IN DETECTOR ARRAY
CASE

75-0298-V-37

Figure 43. Detector Array Assembly Functional Flow Diagram

APPENDIX A
MTF COMPARISON FOR IDEAL SYSTEM

Throughout the text, several MTF measurements have been presented. The data presented is for non-diffraction limited optical systems and square-wave targets at f/4.7 and f/12.8. It is considered of interest to include (in this appendix) theoretical MTF for diffraction limited optics and theoretical detector response. Figure 44 compares the diffraction limited MTF (sine-wave) of an f/4 and f/2 optical system. Figure 45 presents the ideal square-wave response of the detector (along scan) and the system MTF for various lens parameters. The detector corner frequency relationship (on the normalized frequency scale) is detector center spacing/detector linear dimension in direction of MTF.
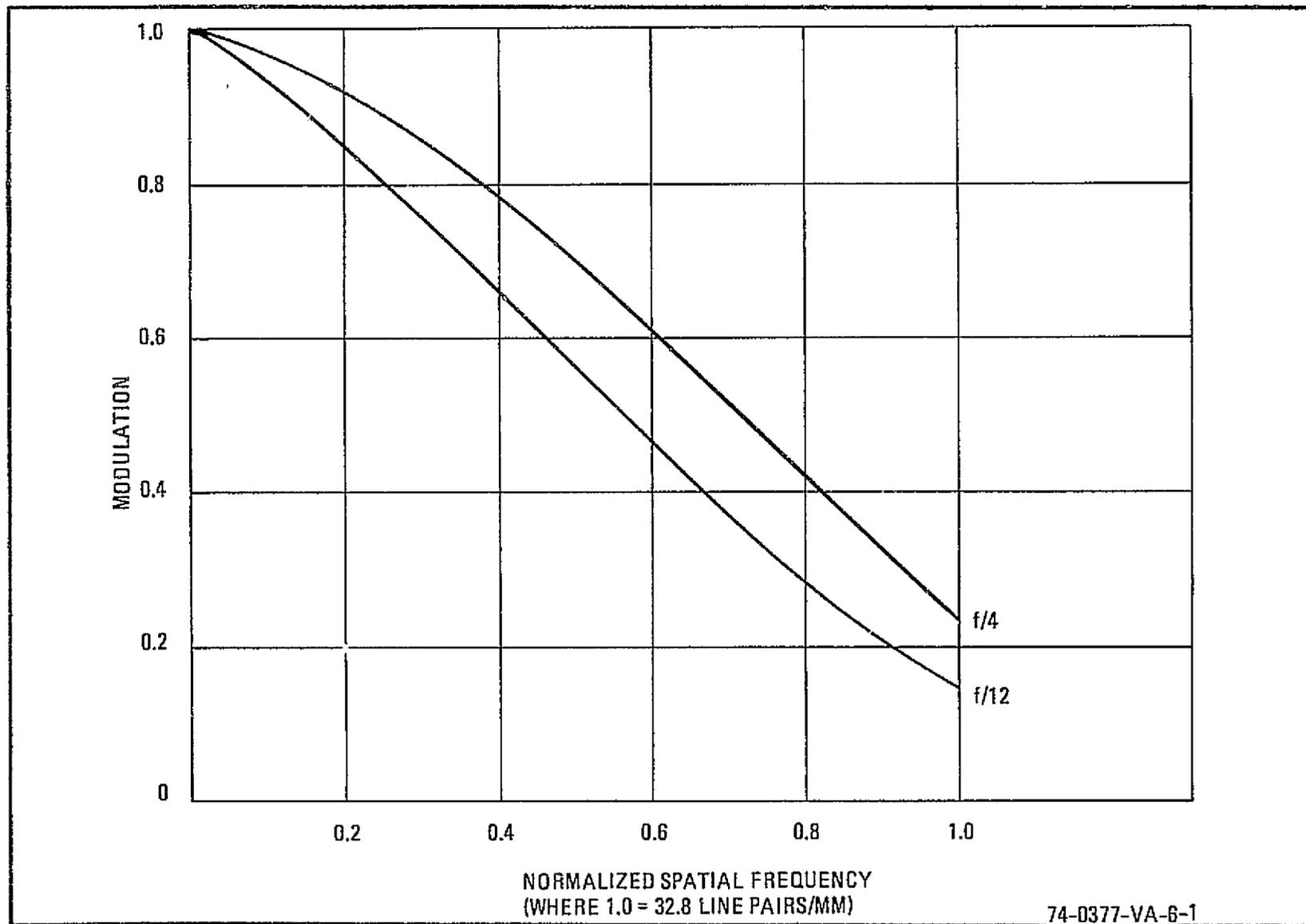
Figure 44.   Comparative MTF with f/4 and f/12 Optics for $\lambda = 1.0\ \mu m$
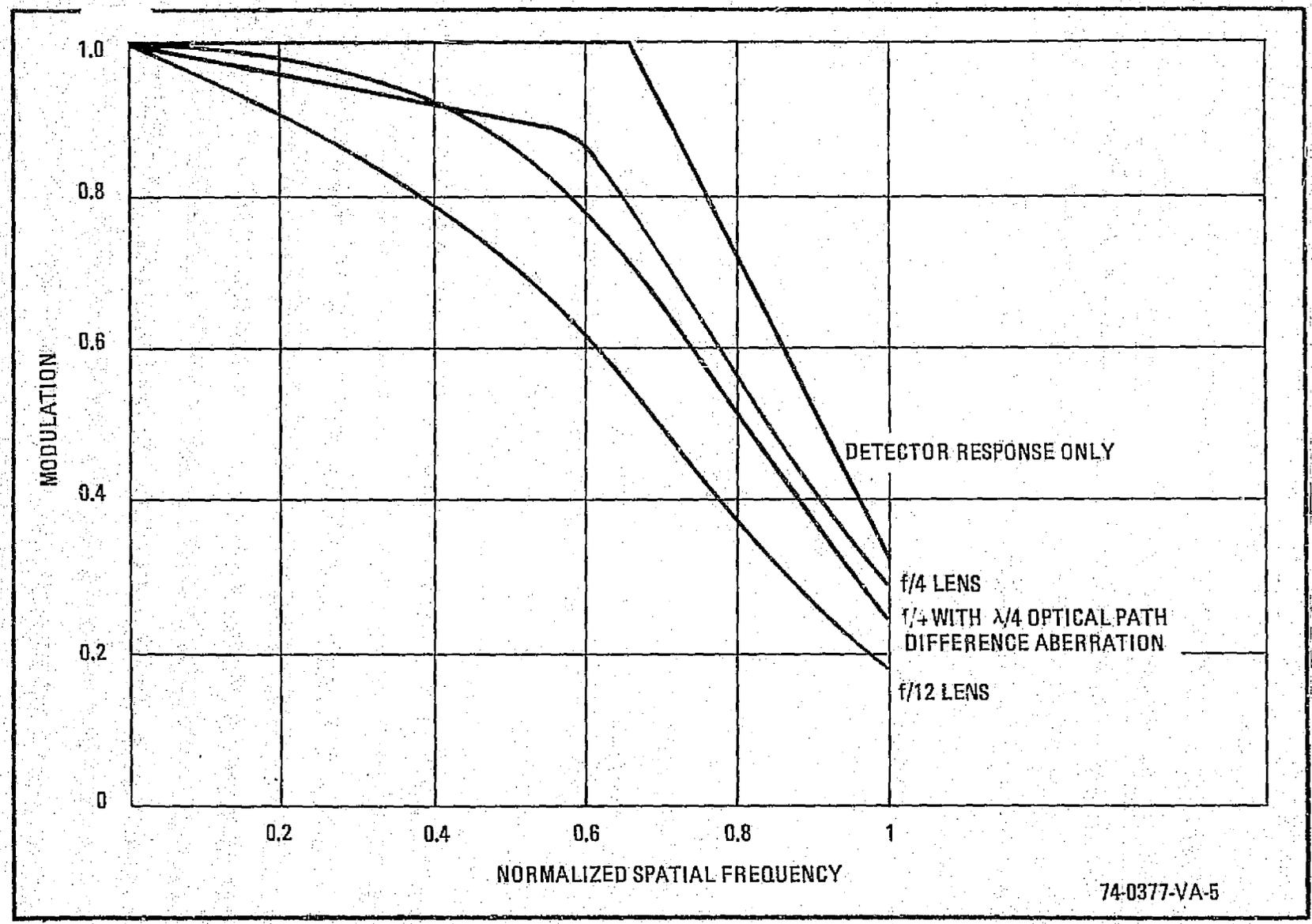
Figure 45. Comparative MTF Response to Squarewave Input

APPENDIX B

BREADBOARD LINEAR ARRAY SCAN IMAGER NOISE PROGRAM

A computer program was written to process the linear array data and provide a rms noise output. The listing of the program is included in figure 46.

This program collects 576 samples from each detector element at each of two input radiance levels. These inputs are averaged to provide a gain measurement for each element. The rms deviation from the average is calculated for each element and referred to the input using the measured gain factor. A composite noise level is also determined. For the composite value, nonoperable elements are not included.

An additional feature of the noise program is to generate the quantization noise uncertainty for each element. This value is also referred to input irradiance.

@FOR,SNR MAIN,MAIN
FOR C3/12/75-09:59:57 (0,)
*5   COMMON/DPLOT/DUM(40),D(1000)

*66

      DO 202 IA=1,4
      DO 203 IB=1,111
      IC=18+(IA-2)*111
      ID=IFIX(EL(16,IC)-CAL(226,2)*26.)
      ID=HINO(5,ID)
      ID=MAXO(ID,0)+1
      D(ID)=D(ID)+1
  203 CONTINUE
      CALL PLOT
  202 CONTINUE

MAIN PROGRAM

STORAGE USED: CODE(1) 005491 DATA(0) 067216; BLANK COMMON(2) 000000

COMMON BLOCKS:

0003   DPLOT   002020

EXTERNAL REFERENCES (BLOCK, NAME)

0004   READ2
0005   PLOT
0006   CLOSIF
0007   NINTRS
0010   RMATHS
0011   SQRT$8
0012   NIOCB$
0013   NSCR$
0014   NNRE$
0015   NNRU$
0016   NNMFL$
0017   NNRU$
0020   NSTOP$
0021   NBFOR$

STORAGE ASSIGNMENT (BLOCK, TYPE, RELATIVE LOCATION, NAME)

(table of storage assignment values — illegible)

      DIMENSION EL(40,576),IZ(576),IZ1(576)
      DIMENSION CAL(0,47,5),IZ(576),IZ(576)
      DIMENSION RNS(576)
      DATA IMODE/1/,MODECL/1/,MODEF/2/
      COMMON/DPLOT/DUM(40),D(1000)
      DO 1201 NMP=1,3
      RAD=24.
      IF(NMP.EQ.2) RAD=39.4
      IF(NMP.EQ.3) RAD=72.7
      REWIND 31
      DO 100 I=1,576
      DO 100 J=1,5
      CAL(I,J)=0.0
  100

C   ACCUMULATE CAL DATA

      TOT = 0.
      SAMP = 0.
      DO 103 K=1,2
      NUM=0
      DO 101 I=1,575,2
      CALL READ2(IZ0,IZ1,IZ2)
      IF(K.EQ.2)GO TO 108
      GO TO 101
  108 WRITE(31) IZ1,IZ2,IZ(7161711)
  150 FORMAT(10X,2I10,//7(161711))

ORIGINAL PAGE IS
OF POOR QUALITY

FOLDOUT FRAME

```
        DO 103 K=1,2
        NUM=0
101     I=1,575,2
        CALL READ2(I,0,IZ1,IZ2)
        IF(K.EQ.2)GO TO 108
        GO TO 301
108     WRITE(3,1) IZ1,IZ2
150     FORMAT(10X,2I10,7(16I7))
301     CONTINUE
        IF(I.LT.1.OR.I.GT.567)GO TO 101
300     CONTINUE
        NUM=NUM+2
109     CAL(J,K)=CAL(J,K)+IZ1(J)+IZ2(J)
1302    CONTINUE
101     CONTINUE
        DO 103 J=1,576
        CAL(J,K)=CAL(J,K)/NUM
103     CONTINUE
        DO 104 K=1,2
104     WRITE (6,105) K,(CAL(I,K),I=1,576)
105     FORMAT (1H1/10X,ICAL FOR K = ,I2,/(16F6.1))
        IPIC = 0

C       PROCESS PICTURE DATA

210     REWIND 31
        FORMAT(6X,18HQUANTIZING ERROR    /(16F7.2))
        ILPL=1
        DO 701 I=1,576
701     Q(I)=(RAD/CAL(I,1)-CAL(I,K))/SQRT(12.)

        RMS(I) = 0.0
        ISUB = 1LPL*2
        WRITE(6,897) MNP,RAD
        DO 201 I=1,575,2
        READ(31) IN,IZ1,IZ2
        IF(ILIN.LT.II.OR. ILIN.GT.567) GO TO 201
        MM=G
971     M=1,576,15
        MM=MM+1
        EL(MM,K)=2 (IZ1(M))
        EL(MM,K)+1=2(IZ2(M))
971     ILIN=2
1108    RMS(I) = RMS(I)+(IZ1(I)-CAL(I,K)     )**2
201     RMS(I) = RMS(I)+(IZ2(I)-CAL(I,K)     )**2
202     CONTINUE
        IA=1,4
        ID=IB+1,111
        IC=IB+(CAL(I)IC)-CAL(226,2)+26.)
        ID=IFIX(EL(I6,IC)-CAL(226,2)+26.)
        ID=MAXO(1,ID)
        ID=MINO(111,ID)
        DID=DID*ID+1
203     CONTINUE
        CALL PLOT
202     CONTINUE
        DO 702 I=1,576
702     SCALE = RAD/CAL(I,1,I)=SCALE
        RMS(I)=SQRT(RMS(I)/NUM)=SCALE
        DO 1702 I=1,576
        IF(RMS(I).LT.5..AND.RMS(I).GT.0)) GO TO 111
        GO TO 500
        TOT = RMS(I)**2+TOT
111     CONTINUE
500     SAMP = SAMP + 1.
1702    CONTINUE
        WRITE (6,703) RMS
        TOT = SQRT(TOT/SAMP)
        DO 979 I=1,MN
897     FORMAT (1H10X,PICTURE NO.,I5/10X,17H512 CHIP NOISE
        15X,13H MAX INPUT =     F7.2)
979     WRITE (6,980) IELEMENT=(EL(I,K),K=1,574)
980     FORMAT (1H10X,ELEMENT,I3,7(16F7.2))
1201    CONTINUE
        CALL CLOSIF (MODECL,1)
510     STOP
703     FORMAT(10X,19HAVERAGE RMS NOISE = F8.3)
        FORMAT (1H1/(16F7.2))
        END
```

SUBROUTINE READ2   ENTRY POINT 000243

STORAGE USED: CODE(1) 000266; DATA(0) 006336; BLANK COMMON(2) 000000

EXTERNAL REFERENCES (BLOCK, NAME)

```
0003    OPNF
0004    ITEHIF
0005    NIOCBS
0006    NSCRW
0007    NNNFUS
0010    NBFOS
```

STORAGE ASSIGNMENT (BLOCK, TYPE, RELATIVE LOCATION, NAME)

```
SUBROUTINE READ2 (I1,I2,IZ1,IZ2)
DIMENSION INP(258),IA(576),IB(576),IC(576),ID(576),IZ1(576),IZ2(576),
1IZ2(576),KBUF(675),ITEHSZ(1948),ITMBLK/1/,MODEC/6H18FE /,IREC/0/
DATA IMODE/1/,ITEHSZ/1948/,ITMBLK/1/,MODEC/6H18FE /,IREC/0/
NUNIT =NE.1) GO TO 40
1       DO 100 I=1,576
100     IA(I)=0
40      IA(I)=0
        CONTINUE
        IF (I1.EG. 577) GO TO 101

C       INPUT TAPE RECORD
        CALL OPNF (KBUF,ITEMS2,ITMBLK,NUNIT,MODEC)
        CALL ITEHIF (INP,NUNIT)
        IF (NUNIT).400.401.402
        L=2*IU
        NUNIT=1
80      DO 80  IE=1,L
        INP(IE)=KBUF(IE)
        IF(L.EG.258) GO TO 11

401     GO TO 12
        L=258
        IU=258
402     GO TO 11
        IU=258
101     GO TO 11
13      DO 13 I=1,257
        INP(I) = 0
14      WRITE (6,141)
141     FORMAT (1H05X'READ ERROR' (3)
11      CONTINUE

C       DECODE ID WORD

C       UNPACK DATA INTO IC AND ID
        DO 15 I=1,129,2
        K=9*(I-1)/2
        DO 16 J=1,4
        N = J+K+5
        ICP(I) = FLD(8(J-1),8,INP(I+1))
        IC(K) = FLD(8(J-1),8,INP(I+2))
        IDP(I) = FLD(8(J-1),8,INP(I+13))
        ID(N) = 16*FLD(32,4,INP(I+13))
16      IDK(K+5) = 16*FLD(32,4,INP(I+2))
        IDK(K+5) = 16*FLD(129,4,INP(I+130))
15      CONTINUE

C       REORDER INTO IZ1 AND IZ2 ARRAYS
        DO 301 I=1,576
        IZ1(I)=ID(I)+255
        IZ2(I)=ID(I)+255
301     CONTINUE

C       RETURN ON EOF
        IF (L.EG.-2) GO TO 1000
```

Figure 46. Computer Program for rms Noise Output

FOLDOUT FRAME

75-0298-VT-42

APPENDIX C

FAILURE ANALYSIS OF A WESTINGHOUSE PHOTODIODE ARRAY INTEGRATED CIRCUIT

This appendix is a failure analysis report performed by the NASA Goddard Space Flight Center on a 96-element photodiode detector array. Figure 47 is a copy of a Failure Analysis Report; figures 48 and 49 are micrographs.

FAILURE ANALYSIS SECTION __TERMINATION__ REPORT

Serial No. __2979__

TASK DESCRIPTION (BRIEF)			PROJECT NAME SRT
Failure analysis of one Westinghouse Electric Corporation photodiode array integrated circuit.			JOB ORDER NO. 311-160-20-53-40
			REQUESTED BY L. Thompson (731)
			INITIATED DATE 6/6/73
REPORTED BY (INVESTIGATOR) M. Baluck	DATE	MANHOURS THIS PERIOD	COMPLETION DATE (ASSIGNED) 7/11/73
GROUP LEADER	DATE	MANHOURS TOTAL 90	SUBMISSION DATE 7/27/73
SUPERVISOR R. Grant	DATE	STATUS ☐ TESTING	☐ DATA ANALYSIS ☐ REPORT IN PROCESS

A Westinghouse Electric Corporation custom photodiode array integrated circuit (SN A14) failed during system tests of an SRT linear sensor circuit at Westinghouse Electric Corp., Baltimore, Maryland. It was reported that the shift register stage in one of the two halves of the die had an output which remained in a constant "logic 1" state. The integrated circuit was submitted to the GSFC Failure Analysis Laboratory for investigation.

The subject device (Figure 1) is a multilayer, silicon, monolithic integrated circuit. The center portion of the die contains an array of 96 photodiode light sensors. This array is flanked on each side by an MOS electronic section which contains 24 shift register stages, 24 AND gates, and 48 amplifiers. (The dimensions of the die are 1.47 millimeters (mm) (58 mils) x 5.33 mm (210 mils)). There are three layers of aluminum contact metallization which are separated by insulating oxide layers. The die surface is covered with a protective overlay. Gold wires are used for interconnecting to the die metallization.

REVIEWED BY	DATE	REPORT ISSUED

PROJECT MANAGER — COPY NO. 5

75-0298-VA-43

Figure 47.   Failure Analysis Report (Sheet 1)

The submitted die, which was bonded to a gold sheet, was received mounted on a stainless steel block with non-conductive epoxy. It was not housed within a package. There were no identification markings on the die. The inter-connection wires had been severed, presumably when the device was removed from the failed circuit.

The submitted integrated circuit was manufactured by Westinghouse Electric Corporation, Advanced Technology Laboratory, Baltimore, Maryland. The device was not screened or incoming tested.

No functional electrical tests could be performed because all the interconnection wires had been severed.

An examination of the die surface using an optical microscope disclosed two anomalies in the failed half of the die: a severe scrape in a metallization stripe associated with the "ϕ_4 shift" bonding pad and one dark region on the die surface where some of the metallization stripes appeared to be irregular.

Pin-to-pin electrical tests of both the good and failed halves of the die surface were performed using a micromanip-ulator in conjunction with a curve tracer. These tests showed that the B⁻ power supply pin associated with the failed half of the die was open-circuited. No other serious anomalies were detected.

The die surface was examined using a scanning-electron microscope. It was observed that the scrape in the "ϕ_4 shift" metallization stripe previously mentioned had nearly open-cir-cuited this stripe. There were only small filaments of alu-minum maintaining continuity (Figure 2a). This scrape appeared to have resulted during probing of the bonding pads by the manufacturer.

The region of the irregular appearing metallization stripes noted earlier was examined more closely. This exam-ination disclosed that several of the stripes had been smeared (apparently during manufacturing) and that two of the stripes were open-circuited. One of these stripes was common with ground and the other was common with the B⁻ supply. In addi-tion, there was a small portion of apparently melted aluminum

310-14A (7/71)

Figure 47. Failure Analysis Report (Sheet 2)

at the site of the open-circuited metallization stripes
(Figure 2b).

(The open circuit in the B⁻ supply metallization
isolated this pin from all the other pins and accounted for
the pin-to-pin electrical test results. The open circuit in
the ground metallization apparently isolated this pin from
some, but not all of its normal connections. This explains
why this pin was not open-circuited during pin-to-pin tests.)

Electrical probing of the B⁻ metallization (beyond the
point of the open circuit) disclosed that this metallization
was short-circuited to several other points including ground.
Because of the damage to the die, it was not possible to deter-
mine whether or not these short circuits contributed to or
resulted from the failure.

Removal of the various metallization and insulating
oxide layers and additional SEM examinations did not reveal
any further anomalies.

Conclusions

Although no functional tests could be performed in
an attempt to reproduce the exact reported failure, the in-
vestigation of the submitted integrated circuit disclosed an
anomaly which would explain why the failed half of the die
would not function. The B⁻ supply line was completely open-
circuited and the ground line was open-circuited from some of
its normal connections. Based upon the melted aluminum
detected at the site of these open circuits, it is concluded
that the damage resulted from an electrical stress. However,
it should be noted that these open-circuited stripes had been
smeared initially during manufacturing. It is possible that
this smearing either reduced the cross-sectional area (and
consequently, the current handling capability) of the metal-
lization or damaged the underlying insulating oxide between
metallization layers (permitting a short circuit between
metallization layers to occur). These factors may have per-
mitted the failure to occur under normal electrical conditions.

The scrape detected in the "φ₄ shift" metallization
stripe is considered to be a serious reliability hazard. This
damage can result in an open circuit or a short circuit be-
tween metallization layers and cause a catastrophic failure.

310-14A (7/71)

Figure 47. Failure Analysis Report (Sheet 3)

FAILURE ANALYSIS SECTION ~~TERMINATION~~ REPORT
(Continuation Sheet)

Serial No. 2979

PAGE 4 OF 4

Due to the complexity of the multilayer construction
and the high density of the die in submitted part type, it
is recommended that in the future, similar parts be subjected
to stringent internal microscopic examinations to eliminate
devices containing defects such as serious metallization
scrapes and smears. In addition, all devices being considered
for use in GSFC high-reliability applications should be screen-
ed and incoming tested.

310-14A (7/71)

PROJECT MANAGER — COPY NO. 5

75-0298-VA-46

Figure 47. Failure Analysis Report (Sheet 4)

PHOTODIODE ARRAY

AMPLIFIER/GATE
SECTIONS

SHIFT REGISTER
SECTION

FAILURE SITE.
(SEE FIGURE C-3,
LOWER)

SCRAPE IN
METALLIZATION
(SEE FIGURE C-3,
UPPER)

GROUND

$\emptyset_4$ SHIFT

B—

75-0298-PA-47
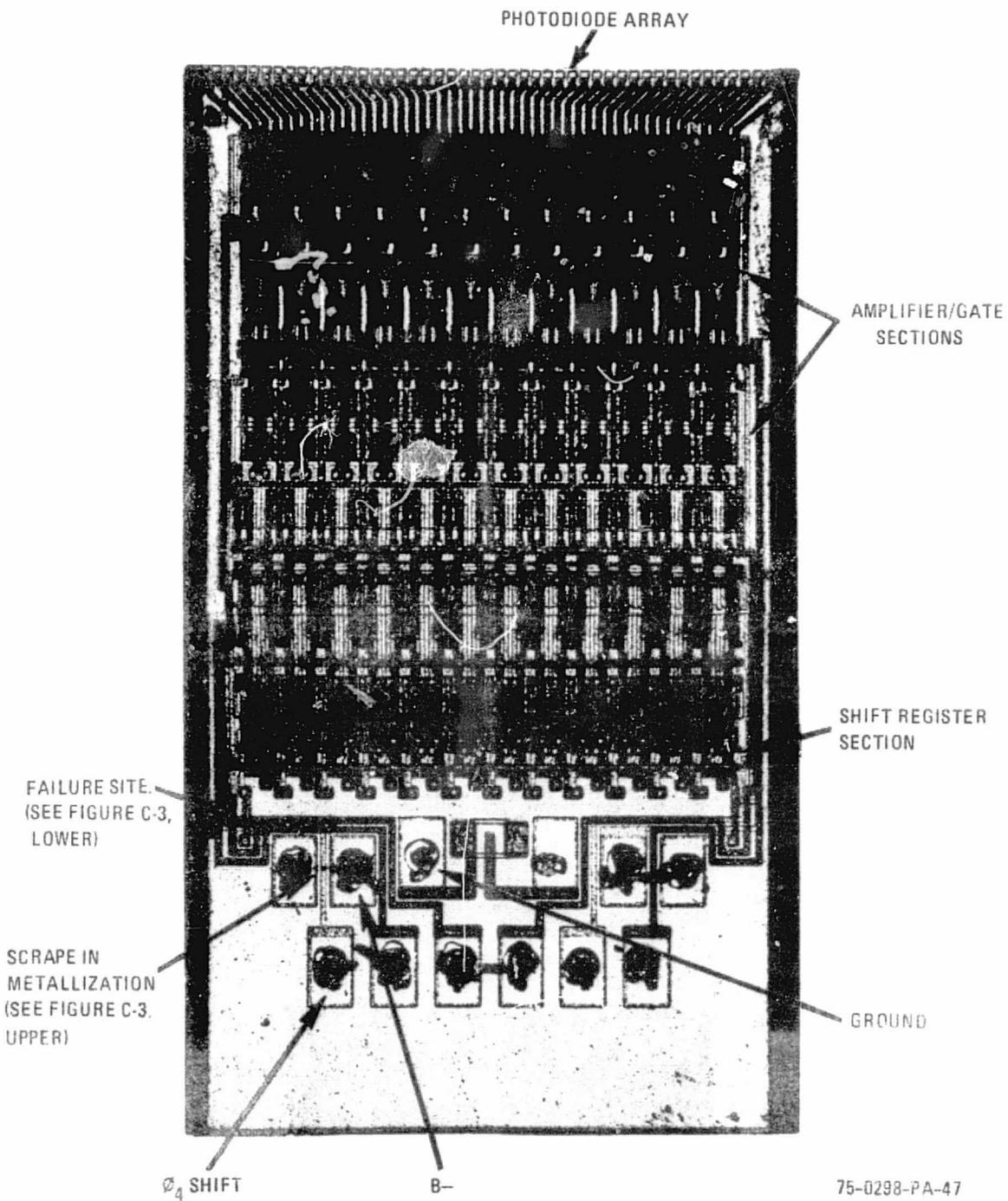
Figure 48.   Failed Half of Silicon Die of Submitted Westinghouse
Integrated Circuit - 65 X Magnification

100

CONNECTING
FILAMENT

ALUMINUM
METALLIZATION

SCRAPE IN "$\emptyset_4$ SHIFT" METALLIZATION STRIPE. 1200X

OPEN-CIRCUITED
GROUND
METALLIZATION
STRIPE
(TOP LAYER
METALLIZATION)

SMEAR

MELTED
ALUMINUM

SMEAR

OPEN-CIRCUITED
B⁻ METALLIZATION
STRIPE
(MIDDLE LAYER
METALLIZATION)

FAILURE SITE   800X

75-0298-PA-48
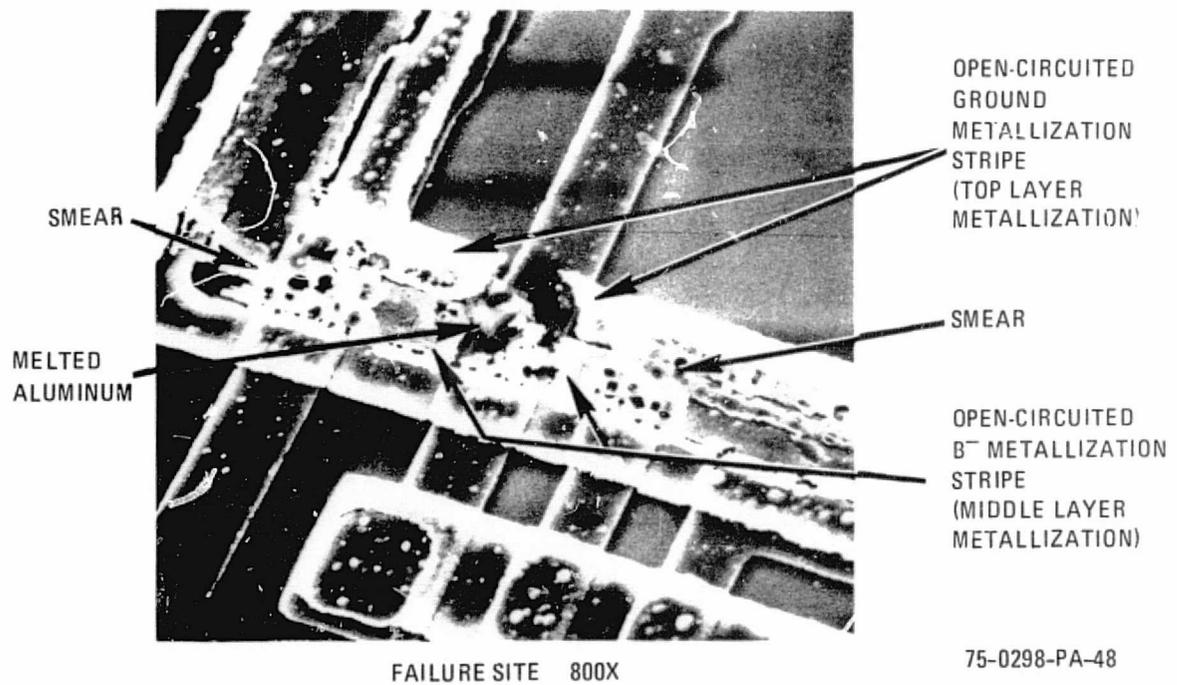
Figure 49.   Scanning Electron Micrographs of Anomalies Detected
in Submitted Device

101/102

APPENDIX D

WESTINGHOUSE FAILURE ANALYSIS REPORT ON FOUR PHOTODIODE LINEAR ARRAY CHIPS (NAS 5-21806)

MICROANALYSIS REPORT #451

February 7, 1957

SUBJECT: The Westinghouse Failure Analysis Laboratory was authorized to perform a failure analysis of four 96-detector element photodiode linear arrays. The chips were removed from the 18-ch', array developed under NASA contract NAS 5-21806, Breadboard Linear Array Scan Imager. The purpose of the failure analysis was to determine the probable nature of failures which occurred during system level testing.

PROBLEM: Four (4) photodiode chips were submitted for failure analysis with the following comments:

Chip 5 (229-9-68)

    Alpha side - phase B shorted to GND since initial turn on

    Beta side - Bus C shorted to GND after 2 to 3 months
                 of operation

Chip 9 (262-7-35)

    Beta side - Bus B shorted to GND since initial turn on

Chip 10 (237-9B-38)

    Beta side - V_R shorted to GND since initial turn on

Chip 14 (262-4-6)

    Alpha side - Bus A shorted to GND since initial turn on

RESULTS OF ANALYSIS

The procedure used in this analysis was to mount the chips in 40 pin dual-in-line packages (for ease in handling), verify the shorts electrically, and trace the shorted bus lines to intersections with GND areas to search for possible physical damage.

Chip 5 - No shorts to GND were found on either side of this chip. Figures 50 and 51 show scratches in the third metal shield.

Chip 9 - No shorts to GND were found on the beta side. On the alpha side phase B, B⁻, and bus B were all shorted to GND. Figure 52 shows phase B, B⁻, and GND along with smeared metal from Pad B⁻ intersecting all three (3) lines. (GND is third metal, B⁻ and phase B are second metal lines.) Figure 53 shows a scratch in the third metal GND shield over the second metal bus B line. Figure 54 shows scratches in the third metal shield on the beta side (one scratch is over the second metal bus B line).

Chip 10 - The V_R line was found shorted to GND on the beta side. Figures 55 and 56 show scratches in the third metal GND shield over the second metal V_R line.

Chip 14 - Output bus A was found shorted to GND on the alpha side. Figure 57 shows scratches in the third metal GND shield over the second metal bus A line.

CONCLUSIONS

The shorts found on chips 9, 10, and 14 were low resistance shorts (10 ohms). Based on previous work with chips of this type, these shorts were probably caused by physical damage which breaks through the layer of glass separating third and second metal. Shorting of these metal layers usually results. The B⁻ and phase B shorts to GND were probably caused by physical damage at the time of bond removal, as suggested by figure 53.
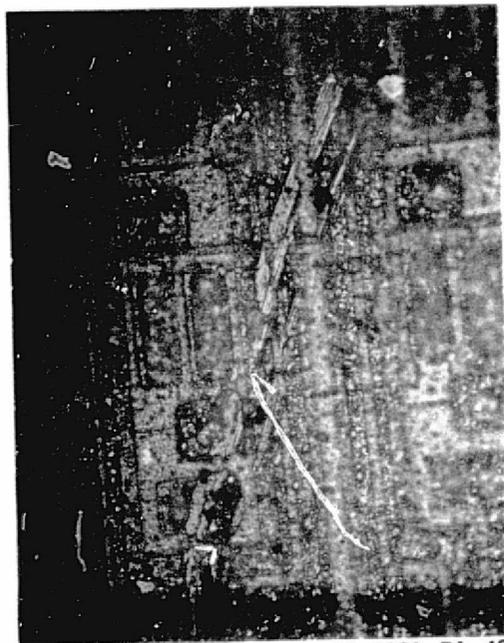
75-0298-PA-49

Figure 50. Scratches in the Third Metal Shield
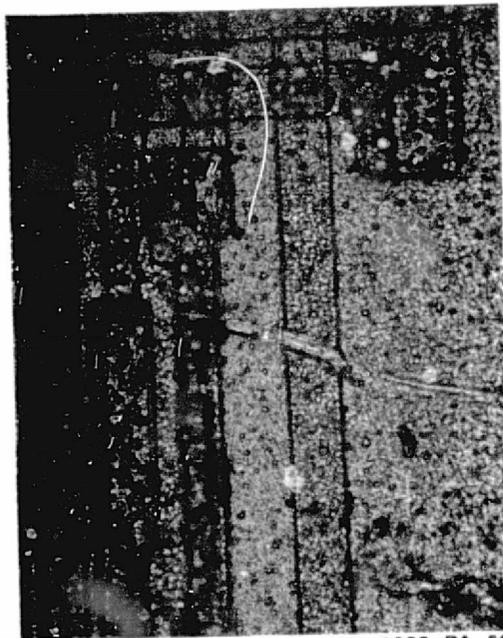
75-0298-PA-50

Figure 51. Scratches in the Third Metal Shield
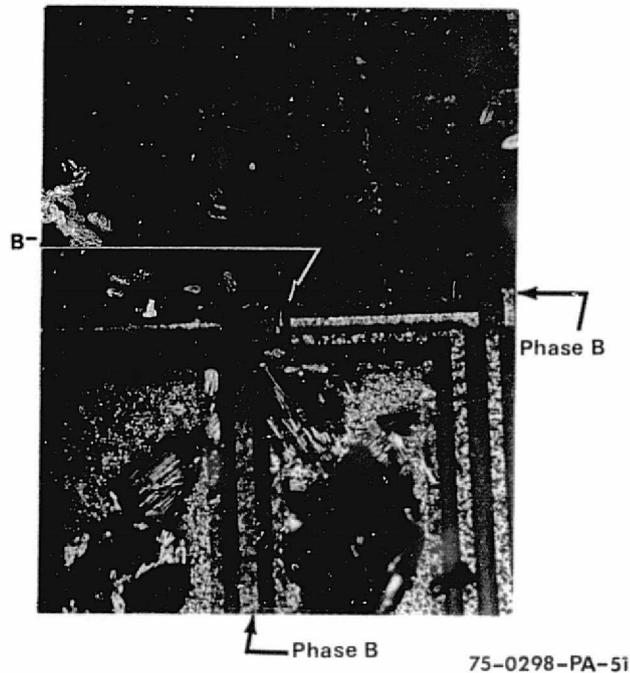
Figure 52. This Photo Shows a Scratch Causing Phase B, B⁻, and Bus B all Shorted to Ground and Smeared Metal from Pad B⁻ Intersecting all Three Lines
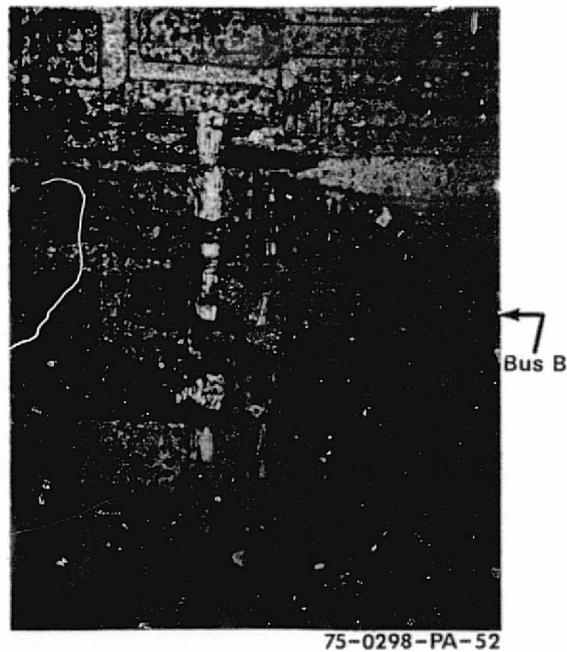
Figure 53. This Photo Shows a Scratch in the Third Metal GND Shield
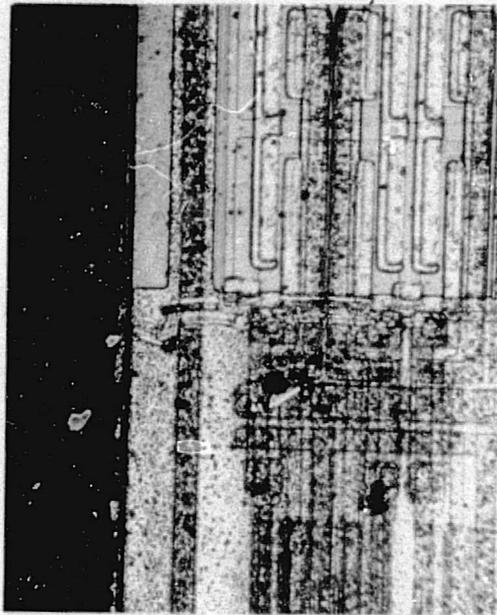
75-0298-PA-53

Figure 54. This Photo Shows Scratches in the Third Metal Shield
on the Beta Side

V_R

75-0298-PA-54

Figure 55. This Photo Shows Scratches in the Third Metal GND Shield
Over the Second Metal V_R Line

107

75-0298-PA-55
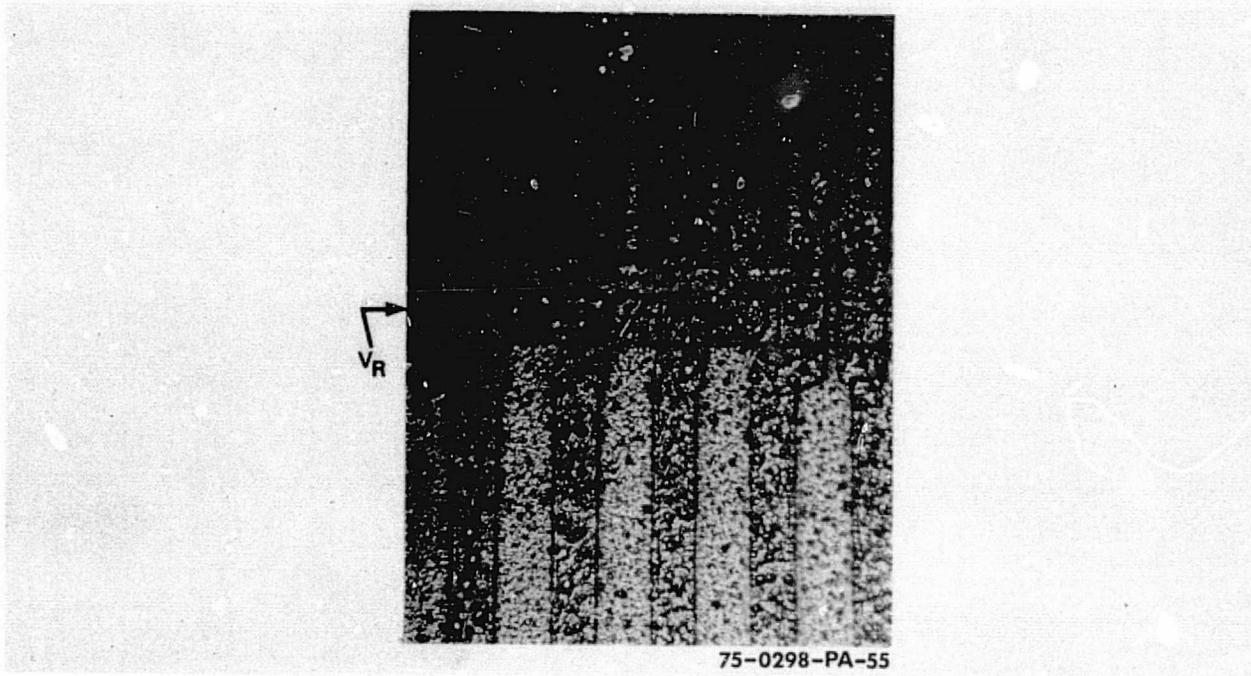
Figure 56. Shows Scratch in Third Metal GND Shield
Over the Second Metal V_R Line

Bus A   75-0298-PA-56

Figure 57. Shows Scratches in the Third Metal GND Shield
Over the Second Metal Bus A Line

The information received with chip 9 may have been mislabeled since the bus B short was found on the alpha side. Although no electrical shorts were found on chip 5, scratches were found on the third metal shield. Heating these chips during the mounting process may have caused previously shorted intraconnects to open.

Although laser debris can be seen (by a skilled observer) in several photographs, the debris is not considered a source of scratches.

APPENDIX E

COMPUTER PROCESSING OF PHOTODIODE
LINEAR ARRAY DATA

This appendix describes the use of the computer in processing image data on the breadboard program.

The computer has two primary functions in this program – reordering of the staggered geometry and normalizing the data. During the data manipulation, other capabilities of the computer were also used for image cosmetics and data analysis. Although the listing in figure 58 is lengthy, the actual function is not complex as can be seen with the simplified flow diagram in figure 59. The following paragraphs provide a more informative description of the computer functions.

The first information entered into the computer is the calibration data. These are array outputs for each element at five predetermined radiance levels. A total of 576 samples are run for each element at each level. The computer averages these samples and stores the results for use in normalizing the picture data. While reading the tape data, the computer also smooths malfunctioning elements by averaging between the two adjacent elements.

The next step is for the computer to read and store the image data. During the reading of this data, the malfunctioning elements are also removed by adjacent element averaging. Two 576 element data lines are read into the computer per tape access. The even numbered elements are stored for one tape access interval and then placed into the storage array with the data from the odd numbered elements read during the next interval forming a 576-element line. This removes the two pixel delay (across scan) inherent

in the staggered photodiode array. The elemental data values are compared to the calibration data and, by interpolation between the nearest higher and lower calibration values, normalized to a range of 0 to 255. A total of 1,728 lines of normalized data from each 6-chip section are accumulated in a drum storage area until the scene data from all three sections have been read.

The final step of a scene data process is to retrieve the data from the drum to form a single 1,728-element data line. Values equivalent to each of the five calibration levels are added to the data lines. This data is recorded on a magnetic tape for playback on a film recorder.

Another benefit obtained from the computer usage was the obtaining of noise calculations. The same scene software was used except the scene processing was removed and an rms routine inserted. The rms deviation from the average level was calculated using 557 samples. This rms value was normalized to the 0 to 255 range for easy comparison to the signal levels. An rms value was then printed for each of the 1,728 elements.

The computer was also used to obtain a comparison of temperature data. This was a simple plotting routine using the peripheral plotter. Room temperature and 0°C plots were made of the dark level for the 6-chip array. The effects of temperature become readily apparent with the plotted data.

```
WFOR,SWH MAIN,MAIN
FOR 0T20-02/25/75-17:50:36 (0,)
-164,164
      ISH1=ISTRTL+1
      IENDLM=IENDL-1
      DO 226  LI=ISH1,IENDLM

 MAIN PROGRAM

 STORAGE USED: CODE(1) 001156; DATA(0) 012320; BLANK COMMON(2) 000000

 EXTERNAL REFERENCES (BLOCK, NAME)

  0003   NTRAN
  0004   READ2
  0005   CLOSIF
  0006   OUTLIN
  0007   NINTR$
  0010   RMATH$
  0011   XPRI$
  0012   NIOCH$
  0013   NSCK$
  0014   NNPLW$
  0015   NNWFU$
  0016   NNWU$
  0017   NNRU$
  0020   NSTOP$
  0021   NAFU$

 STORAGE ASSIGNMENT  (BLOCK, TYPE, RELATIVE LOCATION, NAME)

  0001   000142 101L      0000   032124 105F      0001   000005 113G      0000   032155 117D      0000   032157 120D
  0000   032161 121D      0001   000057 132G      0001   000071 136G      0001   000072 141G      0001   000103 147G
  0001   001102 15009L    0001   001110 15010L    0001   000112 152G      0001   000132 160G      0001   000145 167G
  0001   000156 175G      0001   000462 201L      0001   000306 203L      0001   000207 210G      0000   032163 212D
  0001   000540 213L      0001   000545 214L      0000   032170 215G      0001   000272 215L      0001   000276 216L
  0001   000177 221L      0000   032174 222D      0001   000570 222L      0001   000572 2227L     0000   032201 226D
  0000   032207 230G      0000   032213 241D      0001   000517 242L      0001   000247 247G      0000   032220 257D
  0001   000300 266G      0001   000310 275G      0001   001125 3010L     0000   032150 302F      0001   000337 311G
  0000   032231 327D      0001   000453 337G      0001   000502 360G      0000   032236 414D      0000   032240 415D
  0000   032242 416D      0001   000623 420G      0001   000631 425G      0000   032244 430D      0001   000643 434G
  0001   000711 457G      0001   000751 472G      0001   001075 5010L     0001   001001 504G      0001   001063 521G
  0001   001073 530G      0000   032251 547D      0000   032257 552G      0000   032140 700F      0000   032146 802F
  0000   032147 803F      0000   032133 897F      0000   032116 989F      0000   032121 990F      0000 R 000000 CAL
  0000 R 032112 DFSF      0000 R 032101 DSFSF     0000 R 032046 FNUM      0000 I 032042 I         0000 I 032045 IA
  0000 I 032036 IC        0000 I 032102 ICNT      0000 I 032040 ICOL      0000 I 032041 ICOUNT    0000 I 032066 ID
  0000 I 032063 IDC       0000 I 032076 IDEL      0000 I 032071 IDM       0000 I 032070 IDI       0000 I 032064 IE
  0000 I 032100 IENDL     0000 I 032104 IENDLM    0000 I 032065 IG        0000 I 032074 IH        0000 I 032106 IHM1
  0000 I 032075 IH1       0000 I 032072 II        0000 I 032047 IJ        0000 I 032107 IK        0000 I 032051 ILIN
  0000 I 032026 IMODE     0000 I 032115 IP        0000 I 032037 IPCNT     0000 I 032050 IPIC      0000 I 032103 ISH1
  0000 I 032077 ISTRTL    0000 I 032062 ISW       0000 I 032053 IT        0000 I 026526 IZ1       0000 I 027626 IZ2
  0000 I 032043 J         0000 I 022240 JEL       0000 I 032031 JJ        0000 I 032044 K         0000 I 022550 KEL
  0000 I 032113 KELC      0000 I 032110 KELM1     0000 I 032111 KELP1     0000 I 032073 KT        0000 I 032052 K2
  0000 I 032114 L         0000 I 022714 LEL       0000 I 032105 LI        0000 I 032054 M         0000 I 032061 MM
  0000 I 032056 MNM       0000 I 032027 MODECL    0000 I 032030 MODEF     0000 I 032055 N         0000 I 032067 NC

  0000 I 032035 NCALU     0000 I 032034 NIN       0000 I 032032 NINPUT    0000 I 032057 NNN       0000 I 032033 NUNIT
  0000 I 023060 SFSF      0000 R 022020 XSTR      0000 R 030726 XZ        0000 R 032060 Z

 00101      1*             DIMENSION  CAL(577,16),         XSTR(144)                          000000
 00103      2*             DIMENSION JEL(200),KEL(100),LEL(100)                                000005
 00104      3*             INTEGER SFSF(1830)                                                   000005
 00105      4*             DIMENSION              IZ1(576),IZ2(576),XZ(576)                     000005
 00106      5*             DATA IMODE/1/,MODECL/1/,MODEF/2/                                     000005
 00112      6*             DO 106  JJ=1,16                                                      000005
 00115      7*        106  CAL (577,JJ)=255./ (1.414214)**(JJ-1)                                000005
 00117      8*             REWIND 31                                                            000021
 00120      9*             REWIND 32
 00121     10*             REWIND 33
 00122     11*             NINPUT=1
 00123     12*             NUNIT = 2                                                            000037
 00124     13*             NIN = 3                                                              000041
 00125     14*             NCALU=4                                                              000043
 00126     15*             CALL NTRAN(NUNIT,12)                                                 000045
 00127     16*             IC=0                                                                 000050
 00130     17*             IPCNT=1                                                              000051
 00131     18*             DO 1201 ICOL=1,                                                      000057
 00134     19*             ICOUNT=0                                                             000065
 00135     20*             DO 100 I=1,576                                                       000072
 00140     21*             DO 100 J=1,5                                                         000072
 00143     22*        100  CAL(I,J) = 0.0                                                       000072
                                                                                                000072
```

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OF POOR QUALITY

FOLDOUT FRAME

```
      DO 103 K=1,5,4
      CALL READ2(I=0,IZ1,IZ2,NCALU,ICOL)
      IF (I.LT.10) GO TO 101
102   DO 102 J=1,576
      CAL(J,K) =CAL(J,K)+FLOAT (IZ1(J)+IZ2(J))
101   CONTINUE
103   DO 103 J=1,576
      CAL(J,K)=CAL(J,K)/566.
      DO 221 IA=1,578
      FNUM=CAL(IA,1)-CAL(IA,5)
      IF (FNUM.GT.30.) GO TO 221
232   IC=IC+1
      ICOUNT=ICOUNT+1
      JEL(IC)=IA+(ICOL-1)*576
221   CONTINUE
104   DO 104 I=1,5,4
      WRITE (6,105) K,(CAL(I,K),I=1,576)
989   WRITE (6,989) ICOUNT
      FORMAT (3X,='ICOUNT',I3)
      WRITE (3X,990)(JEL(IJ),IJ=IPCNT,IC)
990   IPCNT=IPCNT+ICOUNT
105   FORMAT (3X/JEL=,2016)
      FORMAT (1H1,/10X,=CAL FOR K = =,I2,/(16F6.1))
C     IPIC = 0

C     PROCESS PICTURE DATA
C
200   IPIC = IPIC+1
      WRITE (6,897) IPIC
897   FORMAT (1H1,10X,PICTURE NO.,I5)
      CALL NTRAN (NUNIT,22)
200   DO 201 ILIN = 1,1729,2
      CALL READ2 (ILIN=0,+,IZ2,NINPUT,ICOL)
      IF (ILIN.GE.1725) GO TO 215
      GO TO 216
215   WRITE (6,700) ILIN,IZ1,IZ2
700   FORMAT (1H1,10X,LINE INPUT,I4/(32I4))
202   DO 202 I=1,576
      XZ(I) = IZ1(I)
203   CONTINUE
204   DO 204 I=1,576
      XZ(I)=255.*(XZ(I)-CAL(I,5))/(CAL(I,1)-CAL(I,5))
      IF (XZ(I) .LT. 0.0) XZ(I) = 0.0
      IF (XZ(I) .GT. 255.) XZ(I) = 255.
      CONTINUE
      IT = 0
      K=D            DO 207  I=1,576,4
207   K=K+1
      M=XZ(I)+0.5
      N=XZ(I+1)+0.5
      HHH=XZ(I+2)+0.5
      NNN=XZ(I+3)+0.5
      FLD (0,9,9,Z)=M
      FLD (9,9,Z)=N
      FLD (18,9,Z)=HHH
      FLD (27,9,Z)=NNN
      HH=30+ICOL
      XSTR(K)=Z
      WRITE (HH) XSTR
802   FORMAT (MH 2)
      FORMAT (2H 3)
209   IF (K2.EQ.2) GO TO 201
      DO 209 I=1,576
      XZ(I)=IZ2(I)
      K2=2
      GO TO 203
201   CONTINUE
      CONTINUE
C
C     LEL IS THE ARRAY CONTAINING ALL BAD ELEMENTS.
C     LEL IS THE ARRAY CONTAINING THE INDEX OF THE LAST GOOD ELEMENT,ODD
C         NUMBER POSITION AND THE BEGINNING POSITION OF THE THE NEXT SET OF
C         GOOD ELEMENTS,EVEN POSTION.
C     KEL IS THE ARRAY CONTAINING THE INDEX OF ADJACENT GOOD ELEMENTS TO A
C         SINGLE BAD ELEMENT.
      IFIC.EQ.0)GO TO 2229
      ISW=0
      INC=0
      IE=0
      IG=0

      DO 222,ID=1,IC
      NC=JEL(ID)+1
      ID=ID+I
      IF(ID.EQ.IC)GO TO 242
      JEL(ID)JLED,NC,GO TO 213
```

```
      NC=JEL(ID)+1
      ID1=IC+1
      IF(ID.EQ.IC)GO TO 242
      IF(JEL(ID).EQ.NC)GO TO 213
      IF(ISW.EQ.1)GO TO 214
      KEL(IE)=JEL(ID)-1
242   KEL(IE)=JEL(ID)-1
      KEL(IE)=JEL(ID)+1
      GO TO 222
      ISW=1
      IDC=IDC+1
213   GO TO 222
      IDH=ID-1
214   IG=IG+1
      LEL(IG)=JEL(ID)-1-IDC
      IG=IG+1
      LEL(IG)=JEL(ID)+1
      ISW=0
      IDC=0
222   CONTINUE
2229  CALL CLOSIF (IMODE,NCALU)
      REWIND 31
      REWIND 32
      REWIND 33
      DO 1700  I=1,1730
      ILIN=(I
      KT=0
      DO 601 I=1,3
      HH=30+I XSTR
      READ (HH) XSTR
      M=FLD (0,9,XSTR(J))
      DO 602 J=1,44
      N=FLD (9,9,XSTR(J))
      HHH=FLD (18,9,XSTR(J))
      NNN=FLD (27,9,XSTR(J))
      KT=KT+1
      SFSF(KT)=M
603   KT=KT+1
      SFSF(KT)=N
604   KT=KT+1
      SFSF(KT)=HHH
1603  KT=KT+1
      SFSF(KT)=NNN
1604  CONTINUE
602   CONTINUE
601   CONTINUE
C     IC IS THE NUMBER OF BAD ELEMENTS-TOTAL
      DO 225 IH=1,IG,2
      IH1=IH+1
      IDEL=LEL(IH1)-LEL(IH)
      ISTRTL=LEL(IH)
      IENDL=LEL(IH1)
      DSFSF=FLOAT(SFSF(IFNDL)-SFSF(ISTRTL))/FLOAT(IDEL)
      ICNT=ISTRTL+1
      IENDLM=IENDL-1
```

```
      DO 226 L=ISR1,IENDLH
      IHH=LEL(IH)
      ICNT=ICNT+1
      SFSF(L)=SFSF(IHH)+IFIX(DSFSF*FLOAT(ICNT))
225   CONTINUE
226   CONTINUE
      DO 217 IK=1,IE,2
      KELPI=KEL(IK)+2
      KELPI=KEL(IK)+2
      DFSF=FLOAT(SFSF(KELP1)-SFSF(KELH1))/2.
      KELC=KEL(IK)+1
      SFSF(KELC)=SFSF(KELH1)+IFIX(DFSF)
217   CONTINUE
      L=ILIN/108+1
      L=ILIN/108+1    L=16
      IF (L.GT.14) L=16
2080  SFSF(I)=CAL(577,1830
      IF (I1.NE.61) GO TO 5010
      DO 5020 I=1729,1830
      SFSF(I)=0
5020  IF (I.GT.864)  GO TO 15009
5010  SFSF(1801)=0
15009 CONTINUE
      SFSF(I.LT.864)  GO TO 15010
      SFSF(1801)=255
15010 CONTINUE
      IP=0
      IF (MOD(ILIN,10) .GT.8 ) GO TO 3010
      WRITE (6,302) ILIN,(SFSF(HH),HH=1,1728)
      IP = IPIC
3010  CONTINUE
      CALL OUTLIN (SFSF,NUNIT,IP)
1700  CONTINUE
212   CONTINUE
      CALL NTRAN (NUNIT,9)
      CALL NTRAN (NUNIT,9)
      CALL CLOSIF (MODECL,I)
      CALL NTRAN (NUNIT,10)
      CALL CLOSIF (MODECL,NCALU)
      STOP MAIN
302   FORMAT (1H0,10X,*LINE*,14/(32I4))
      END
```

Figure 58. Computer Listing for Photodiode Linear Array
Data Processor (Sheet 1)

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```
   80    QR 80, IF(IE)
         INP(IE)=KBUF(IE)
  401    GO TO 12
         LE=2
         IU=25B
         NUNIT=IUNIT
  402    GO TO 11
         IU=25B
  101    GO TO 11
         CONTINUE
         DO 13 I=1,257
  13     INP(I)=0
  12     INP(I)=0
         IF (IL.EQ.458) GO TO 11
         WRITE (6,14) L
  11     FORMAT (1H0,5X*HEAD ERROR* I3)
         CONTINUE

C        DECODE ID WORD

         IFRNO = 100*FLD(0,4,INP(1))+10*FLD(4,4,INP(1))+FLD(8,4,INP(1))
         IHON  = 10*FLD(12,4,INP(1))+FLD(16,4,INP(1))
         IDAY  = 10*FLD(20,4,INP(1))+FLD(24,4,INP(1))
         IYEAR = 10*FLD(28,4,INP(1))+FLD(32,4,INP(1))

C        UNPACK DATA INTO IC AND ID

         DO 15 I=1,19,2
  16     K=7*(I-1)/2
         KK=16*K+J+K+5
         N=J+K+5
         IC(N)  = FLD(8,8,INP(I+1))
         ID(N)  = FLD(8,8,INP(I+1))
         IC(N)  = FLD(8,8,INP(I+1+30))
         ID(N)  = FLD(8,8,INP(I+1+30))
         IC(K+5)= 16*FLD(32,4,INP(I+1+29))+FLD(0,4,INP(I+1+30))
         ID(K+5)= 16*FLD(32,4,INP(I+1+29))+FLD(0,4,INP(I+1+30))
  15     CONTINUE

C        REORDER INTO IZ1 AND IZ2 ARRAYS

         DO 17 I=1,57,2
         IZ1(I)   = IC(I)
         IZ2(I)   = ID(I)
         IZ1(I+1) = IA(I+1)
         IZ2(I+1) = IB(I+1)
  17     CONTINUE

C        OUTPUT DISPLAY

         IF (I1.NE.1) GO TO 50
         WRITE (6,411) IFRNO,IHON,IDAY,IYEAR,IREC
  411    FORMAT (1H10X*FRAME*I4,5X*MM*I3,5X*DD*I3,5X*YY*I3,5X*RECORD*I4)
         WRITE (6,412) IZ1,IZ2
  412    FORMAT (2X,32I4)

         WRITE (6,602) INP
  602    FORMAT (180I3)
  501    CONTINUE

C        RETURN ON EOF

         IF (IL.EQ.-2) GO TO 1000

C        MOVE IC - ID TO IA - IB ARRAYS

         DO 20 I=1,576
         IA(I) = IC(I)
         IB(I) = ID(I)

C        RETURN FOR NEXT PHYSICAL RECORD
```

BFOR,IS OUTLIN,OUTLIN
FOR 12B-02/25/75-17:57:09 (,D)

SUBROUTINE OUTLIN   ENTRY POINT 000216

STORAGE USED: CODE(1) 000234; DATA(0) 000701; BLANK COMMON(2) 000000

EXTERNAL REFERENCES (BLOCK, NAME)

```
0003   NTRAN$
0004   NICCB$
0005   NSCR5$
0006   NWHFU$
0007   NSTOP$
0010   NBFO5$
```

STORAGE ASSIGNMENT (BLOCK, TYPE, RELATIVE LOCATION, NAME)

```
0001  000165 10L      0001  000201 101L     0001  000005 106G     0001  000005 101L
0000  000656 DYN$     0000  000630 15       0000  000631 11       0000  000651 144D     0000  000645 401F
0000  000634 14       0000  000635 15       0000  000636 16       0000  000637 12       0000  000633 13
0000  000641 19       0000  000644 L        0000  000000 OUT      0000  000642 X        0000  000640 18
                                                                                        0000  000643 Y
```

```
C         THIS DECK FOR OPTRONICS MSACHINE.
1*        SUBROUTINE OUTLIN (TWFE,NUNIT,IP)
2*        INTEGER TWFE
3*        DIMENSION TWFE(1),OUT(4DB)
4*        DO 100 I=1,907,2
5*        I1=(I+1)/2)+1
6*    C   I1=I+1
7*    C   I2=I2+1
8*    C   I3=I3+1
9*    C   I4=I4+1
10*   C   I5=I5+1
11*   C   I6=I6+1
12*   C   I7=I7+1
13*   C   I8=I8+1
14*       FLD(0,8,X) = TWFE(I1)
15*       FLD(16,8,X) = TWFE(I2)
16*       FLD(8,8,X) = TWFE(I3)
17*       FLD(24,8,X) = TWFE(I4)
18*       FLD(32,4,X) = TWFE(I5)/16
19*       FLD(0,8,Y) = TWFE(I6)
20*       FLD(12,8,Y) = TWFE(I7)
21*       FLD(20,8,Y) = TWFE(I8)
22*       FLD(28,8,Y) = TWFE(I9)
23*       OUT(I+1) = X
24*       OUT(I+1) = Y
25*  100  CONTINUE
```

Figure 58. Co

STORAGE ASSIGNMENT (BLOCK, TYPE, RELATIVE LOCATION, NAME)

```
0005  NNNFUS
0007  NSTOPS
0010  NBFUS

0001  000145  IOL    0001  000201  IOIL    000005  IOIG    0000  II  000450  IINHD    0000  II  000645  IIOIF
0000  II  000554  DYNS   0000  II  000630  IS    000005  15    0000  II  000632  I7    0000  II  000633  I13
0000  II  000640  I9    0000  II  000635  L     000005  16    0000  R  000642  X     0000  R  000640  Y

U        000005        00024
         000005        00030
         000005        00034

                  THIS DECK FOR OPTRONICS MSACHINE.
 1**    SUBROUTINE OUTLIN ((TWFE,NUNIT,IOP))
 2**    INTEGER TWFE
 3**    DIMENSION TWFE(11),OUT(4*08)
 4**    DO 100 I=1,407,2
 5**    I1 = 90(I/2)+1
 6**    I2 = I1+1
 7**    I3 = I2+1
 8**    I4 = I3+1
 9**    I5 = I4+1
10**    I6 = I5+1
11**    I7 = I6+1
12**    I8 = I7+1
13**    I9 = I8+1
14**    FLDI(I0,8,X1)  = TWFE(I1)
15**    FLDI(I8,8,X2)  = TWFE(I2)
16**    FLDI(I16,8,X3) = TWFE(I3)
17**    FLDI(I24,8,X4) = TWFE(I4)
18**    FLDI(I32,4,X5) = TWFE(I5)/14
19**    FLDI(I4,8,Y1)  = TWFE(I6)
20**    FLDI(I8,8,Y2)  = TWFE(I7)
21**    FLDI(I12,8,Y3) = TWFE(I8)
22**    FLDI(I20,8,Y4) = TWFE(I9)
23**    OUT(I1) = X
24**    OUT(I) = Y
25**100  CONTINUE
26**
27**
28**    CALL NTRAN (NUNIT,1,1,608,OUT,L, 22)
29**    IF (L .EQ. -1) GO TO 10
30**    IF (L .EQ. 608) GO TO 101
31**    WRITE (6,401) L
32**401  FORMAT (1HD5X*WRITE (ERROR*I3))
33**    STOP
34**101  RETURN
35**    END
```

END OF COMPILATION   NO   DIAGNOSTICS.

END OF COMPILATION: NO   DIAGNOSTICS.

BMAP
MAP D026-02/25-17:58

1•   LIB SYS$*BEF70$

ADDRESS LIMITS   001000 006704   3013 IBANK WORDS DECIMAL
                      040000 110212   20619 DBANK WORDS DECIMAL
STARTING ADDRESS   005527 005527

SEGMENT $MAIN$ 001000 006704   040000 110212

NRECA$/FORV7 $(2)   040000 040111
NTAB$/FORV7 $(2)   040112 040226
NBFD$/FORV7 $(2)   040227 042330

NOO$(COMMONBLOCK) $(4)   N$OO 042331 042332
NCR/FORV7 $(2)   042333 042460

HOERO$(COMMONBLOCK) $(4)   N$OO 042461 042464
NNTR/FORV7A   042465 043443

NTRANS/FORV7 $(1)   001000 002305 $(034) HOERO$ 043444 044105
                   $(037) INFO=010=LC   044106 044561

TABL2$/BEF70 $(1)   002306 002552 $(0)   044106 044561
ARCD$$/BEF70 $(1)   002553 002556 $(0)   044562 044617
EBD$/BEF70• $(1)   002556 003021 $(0)   044620 044676
BEFX11/BEF70 $(1)   003022 004457 $(0)   044677 046341
IOPKF$/BEF70   046342 047242
BLANK$COMMON(COMMONBLOCK) $(1)   004660 005113 $(0) 046392 047242
OUTLIN $(3)   INFO=010=LC $(0) BLANK$COMMON

RD2 $(3)   005114 005526 $(1)   BLANK$COMMON 055672
                   $(43) INFO=010=LC $(2)   BLANK$COMMON
MAIN $(1)   005527 006704 $(0)   055673 110212
                   $(3)   INFO=010=LC $(2)   BLANK$COMMON

SYS$*RL.IB$•.LEVEL 69
END OF COLLECTION = TIME 2.081 SECONDS

@XQT

75-0208-VC-58

START PROGRAM

INPUT CAL LEVELS

SET CAL ARRAY CAL(I,J) TO ZERO

CALIBRATION TAPE

READ CAL DATA (INP) 2 LINE INCRE

DECODE ID WORDS FRM, MON, DAY, YR

LOADS ODD LINES INTO IL EVEN LINES INTO ID

MESHES DELAYED LINE (IA, IB) WITH IC, ID TO FORM IZ1, IZ2

SMOOTH ELEMENTS

STORE IC, ID IN IA, IB

LINE I < 576

AVG EL CAL

Figure 59. Eight

Figure 59.   Eighteen Chip Image Processing Flow Diagram

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APPENDIX F

DETECTOR TEMPERATURE TEST RESULTS

The data shown plotted in figure 60 is the measured dark level at +22°C
and 0°C using five bilinear staggered chips. Only the chip temperature was
varied. Each data point is the average of 576 samples. The channel gain is
2.3 digital counts/mW/m^2. The plots show that at 0°C, a significant ($\approx$ factor
of 4) reduction of the peak-to-peak difference in elemental offsets occurs.
This means that less of the dynamic range needs to be reserved for trans-
mitting offsets. It also reduces the temperature sensitivity allowing coarser
temperature control requirements.
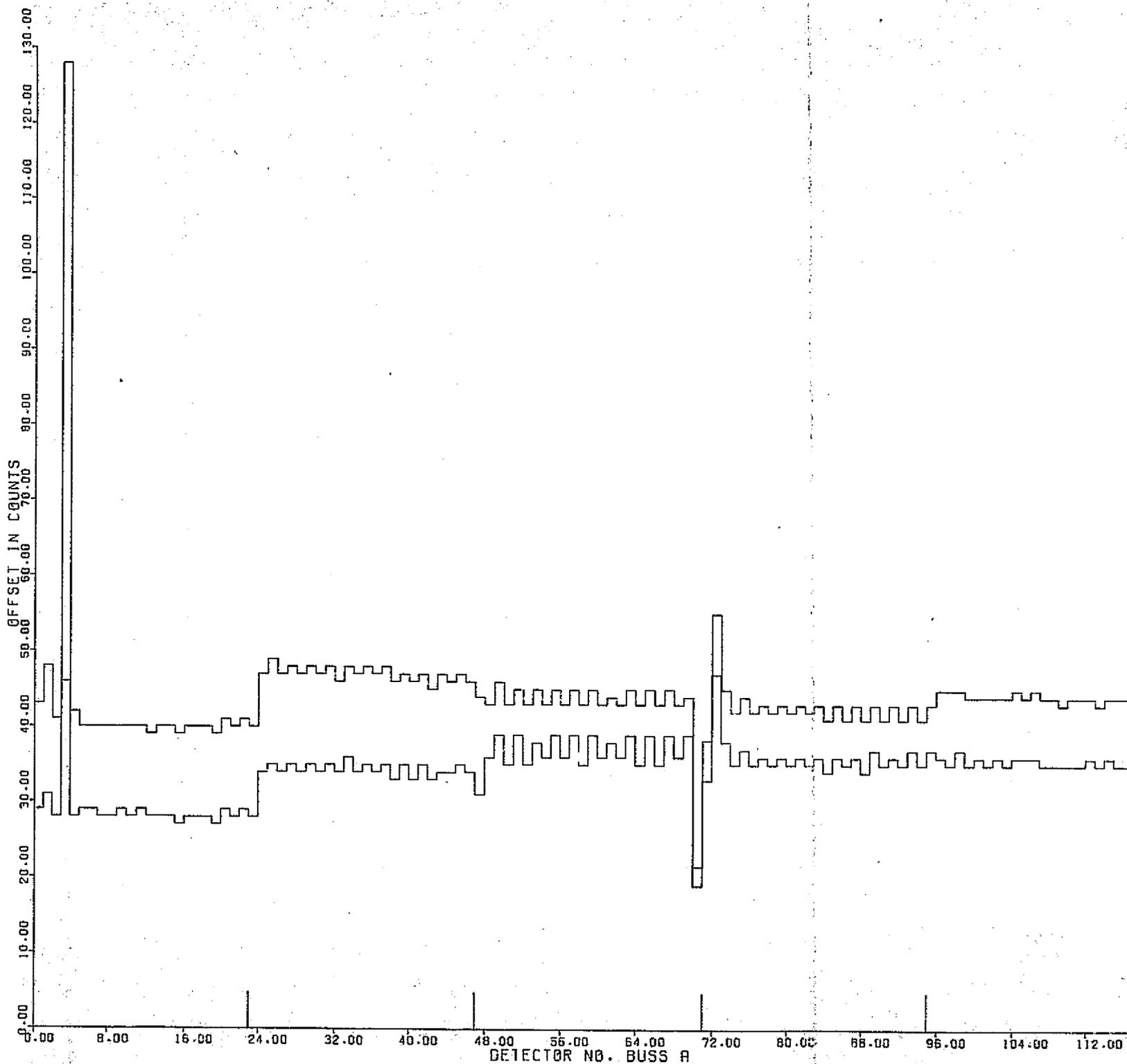
OFFSET IN COUNTS

DETECTOR NO. BUSS A

12.00   1.00   8.00   16.00   24.00   32.00   40.00   48.00   56.00   64.00   72.00   60.00   88.00   96.00   104.00   112.00

DETECTOR NO. BUSS B

DETECTOR NO. BUSS C

1.00   8.00   16.00   24.00   32.00   40.00   48.00   56.00   64.00   72.00   80.00   88.00   96.00   104.00   112.00   1.00
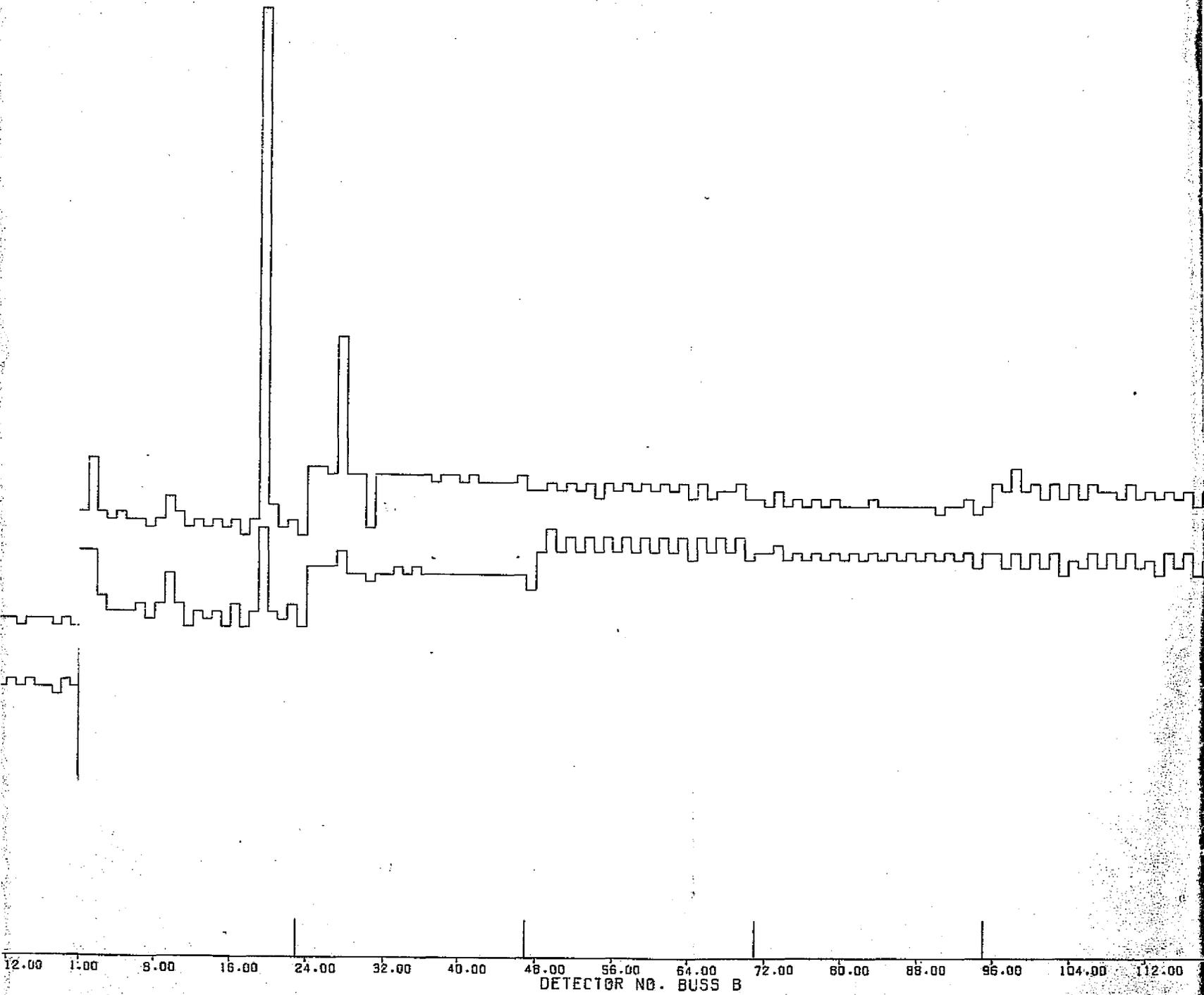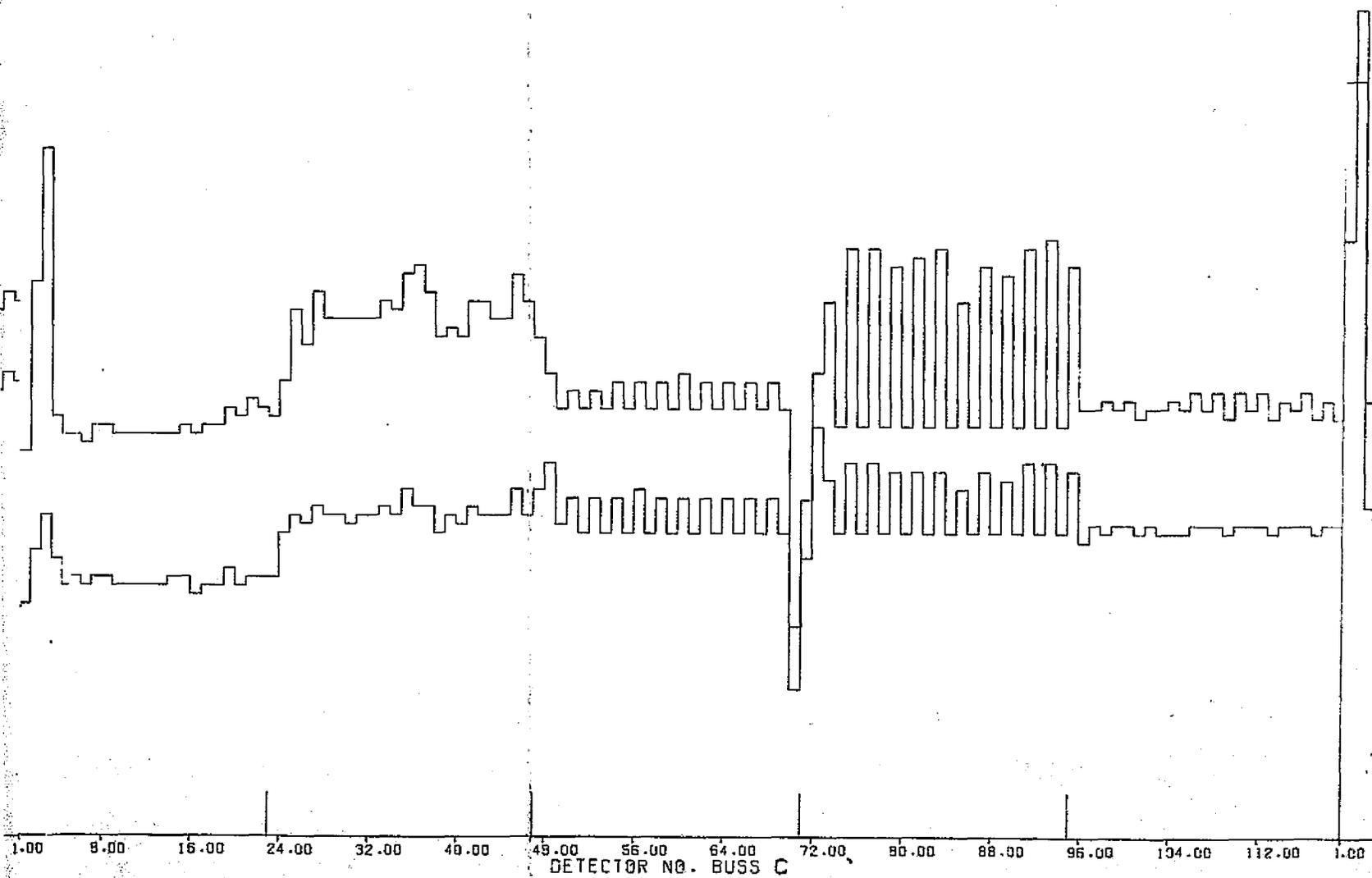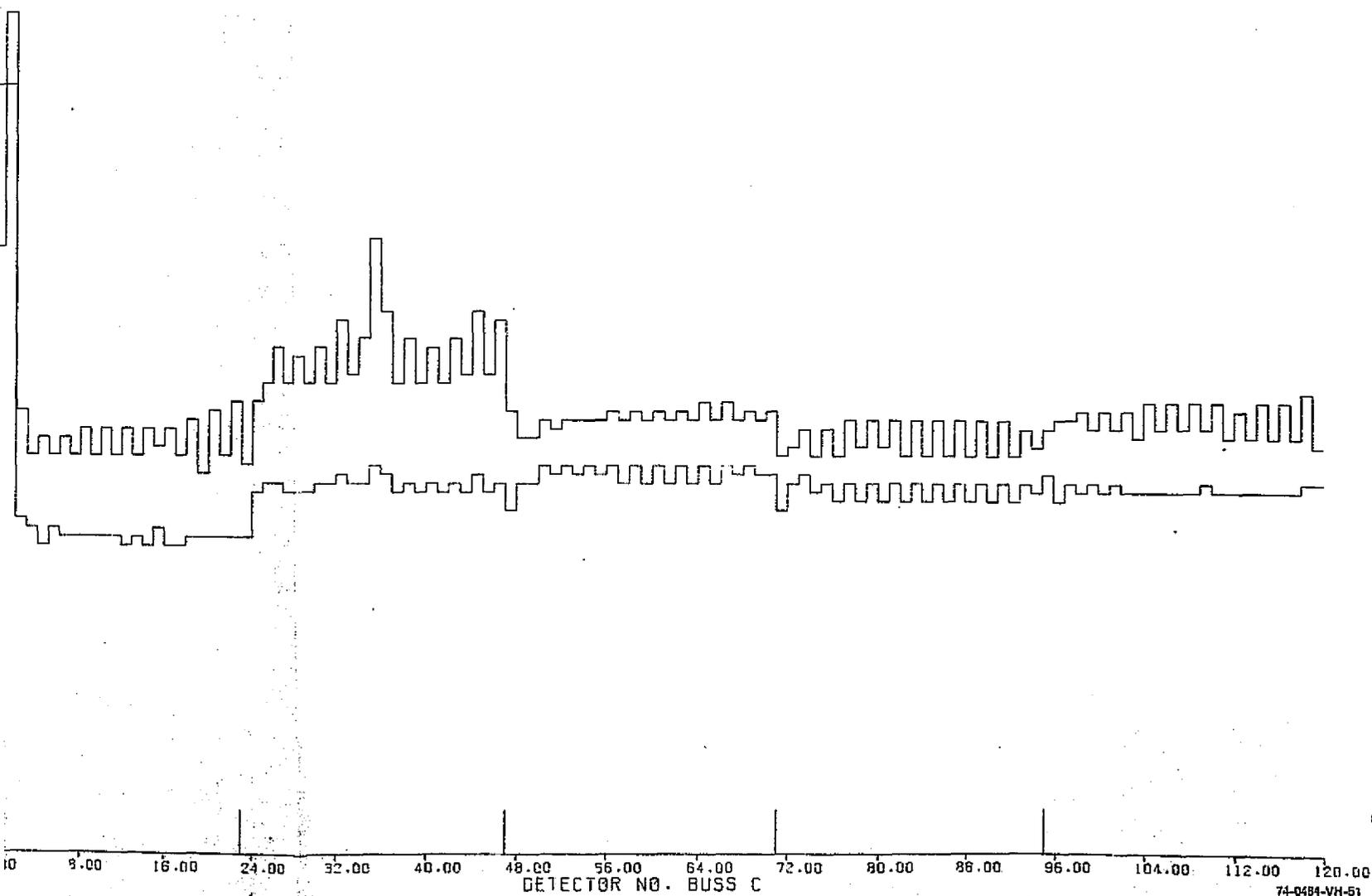
Figure 60. Dark Level Current at Two Temperatures for All
Detectors of a 576-Detector Array

FOLDOUT FRAME 4

APPENDIX G
TEMPORAL TEST

A rigorous test for temporal stability has not been performed, therefore no conclusion about time related drifts can be made. However, measurements of offset in the room ambient environment were conducted over a 3-month period during which the baseplate temperature was monitored. Some of these results are plotted in figures 61 through 65.

Figure 61 data was taken over a period of 35 minutes with an initial measurement made, one at 20 minutes and one at 35 minutes. Although during this period the level changed, it was accompanied by a temperature change of 2.2°C. The magnitude and polarity of the change are consistent with the change in temperature. The average change is only 6 $\mu J/m^2$ equivalent input which indicates that, if a short term temporal change occurred, its magnitude is very low and undetectable with the 1.4 $\mu J/m^2$ NEI.

A longer temporal run three runs over a 2-month period is shown in figures 62 through 65. These again show variations attributable to the ambient temperature differences with little change in the general level. There is again no evidence of a temporal drift.
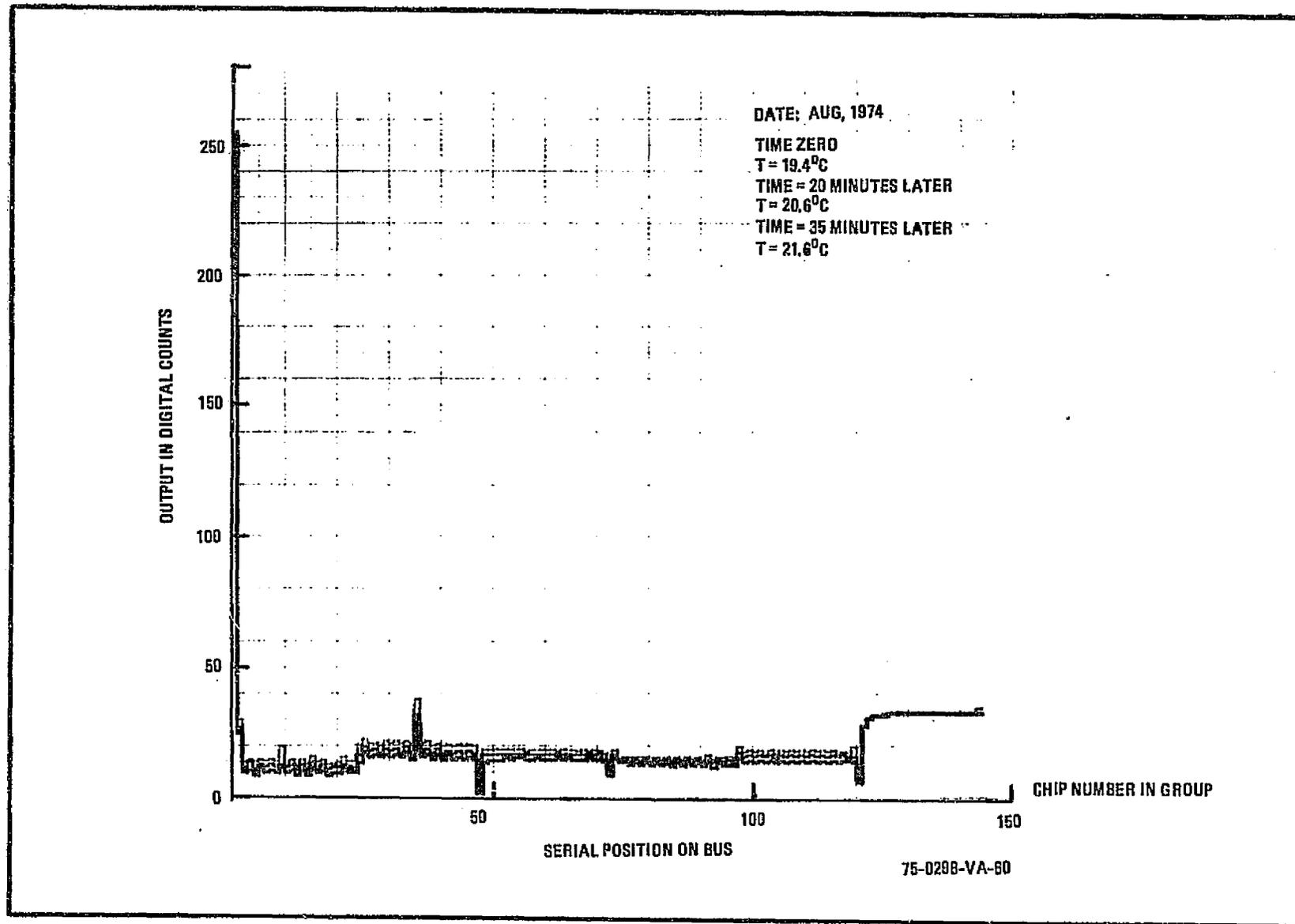
Figure 61. Output at Dark vs Time and Temperature
Six Chip Array - Bus A
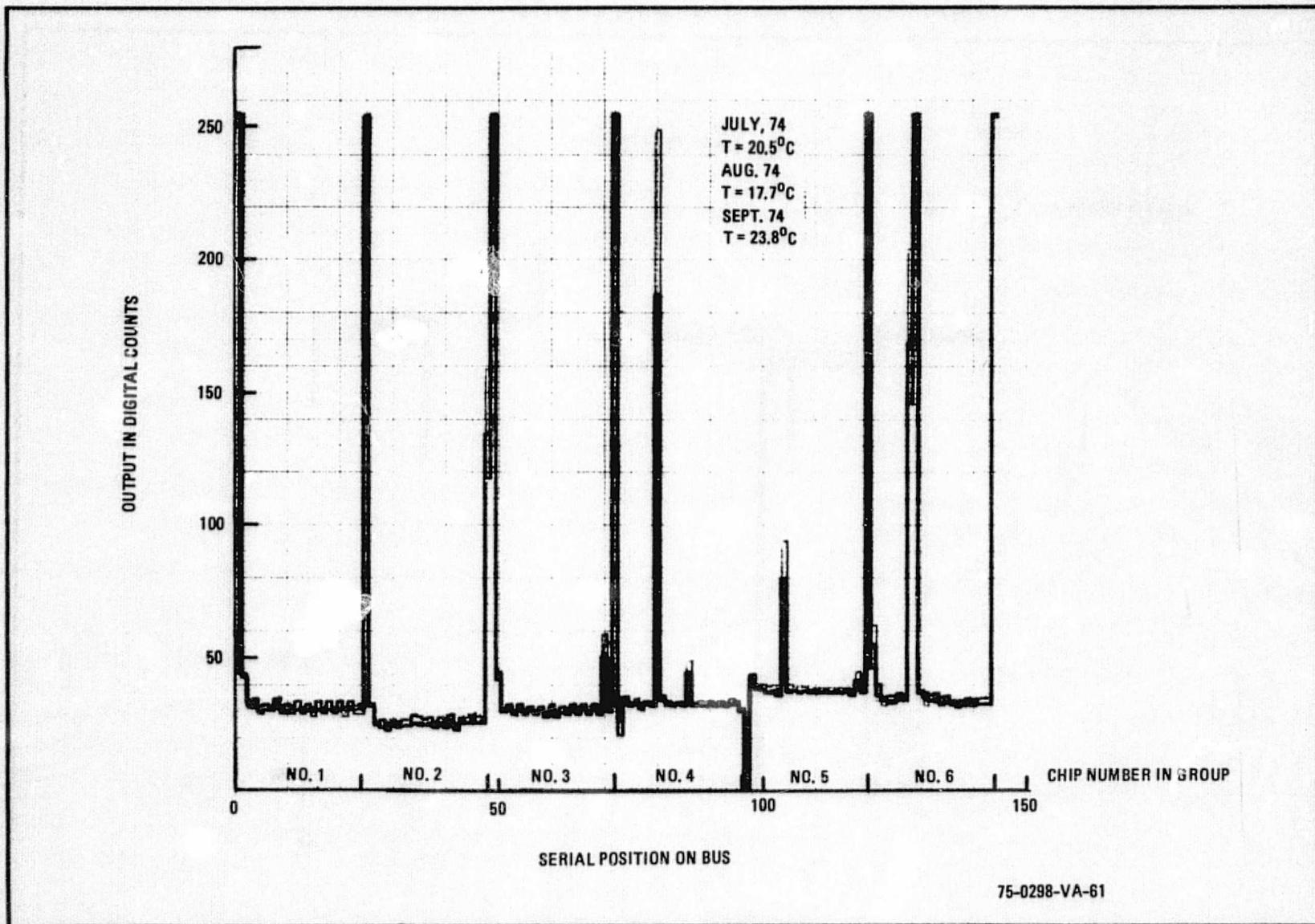
Figure 62. Output at Dark vs Time and Temperature
Bus A of Group 2

75-0298-VA-61
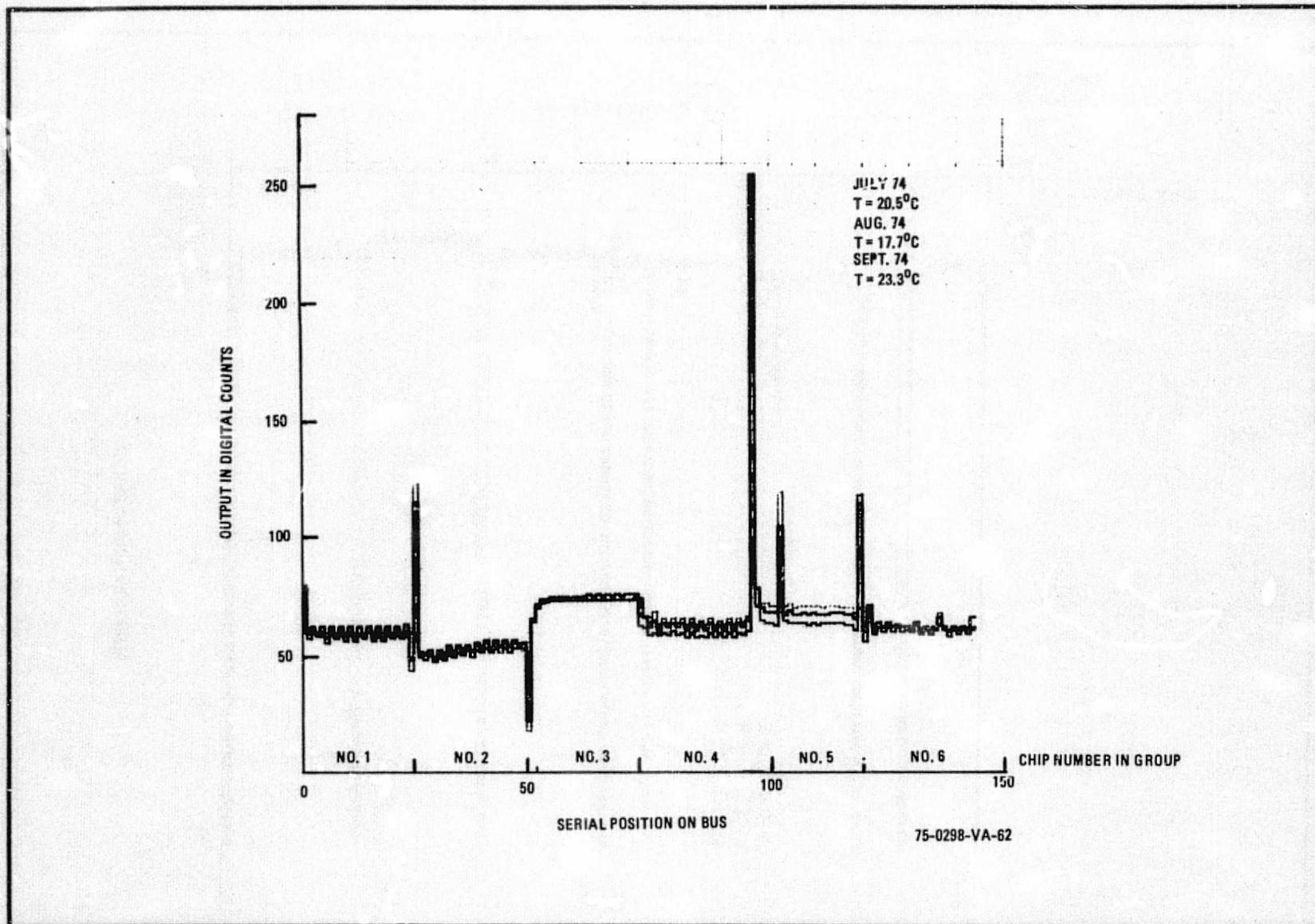
Figure 63.   Output at Dark vs Time and Temperature
Bus B of Group 2

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75-0298-VA-62
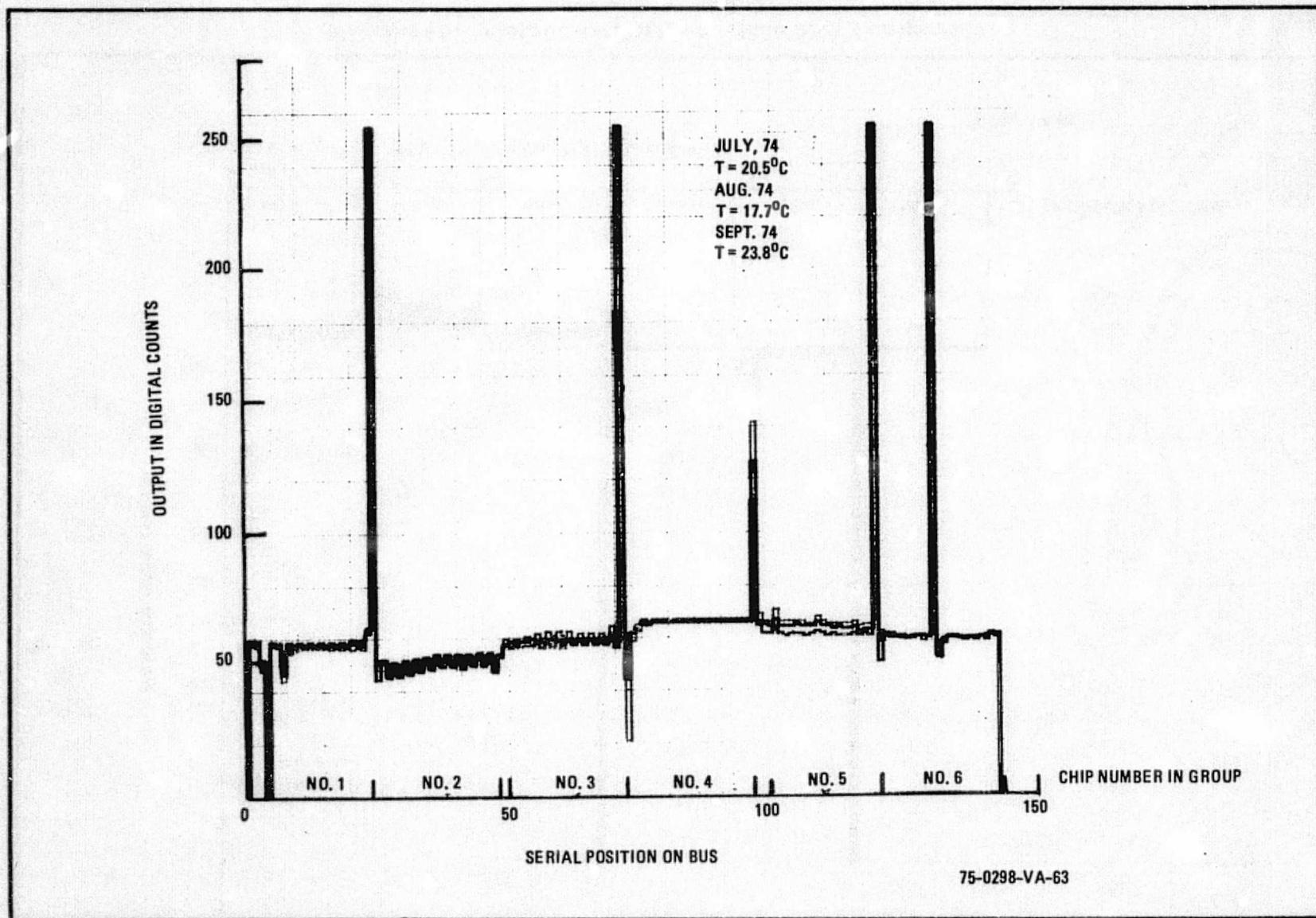
Figure 64. Output at Dark vs Time and Temperature
Bus C of Group 2

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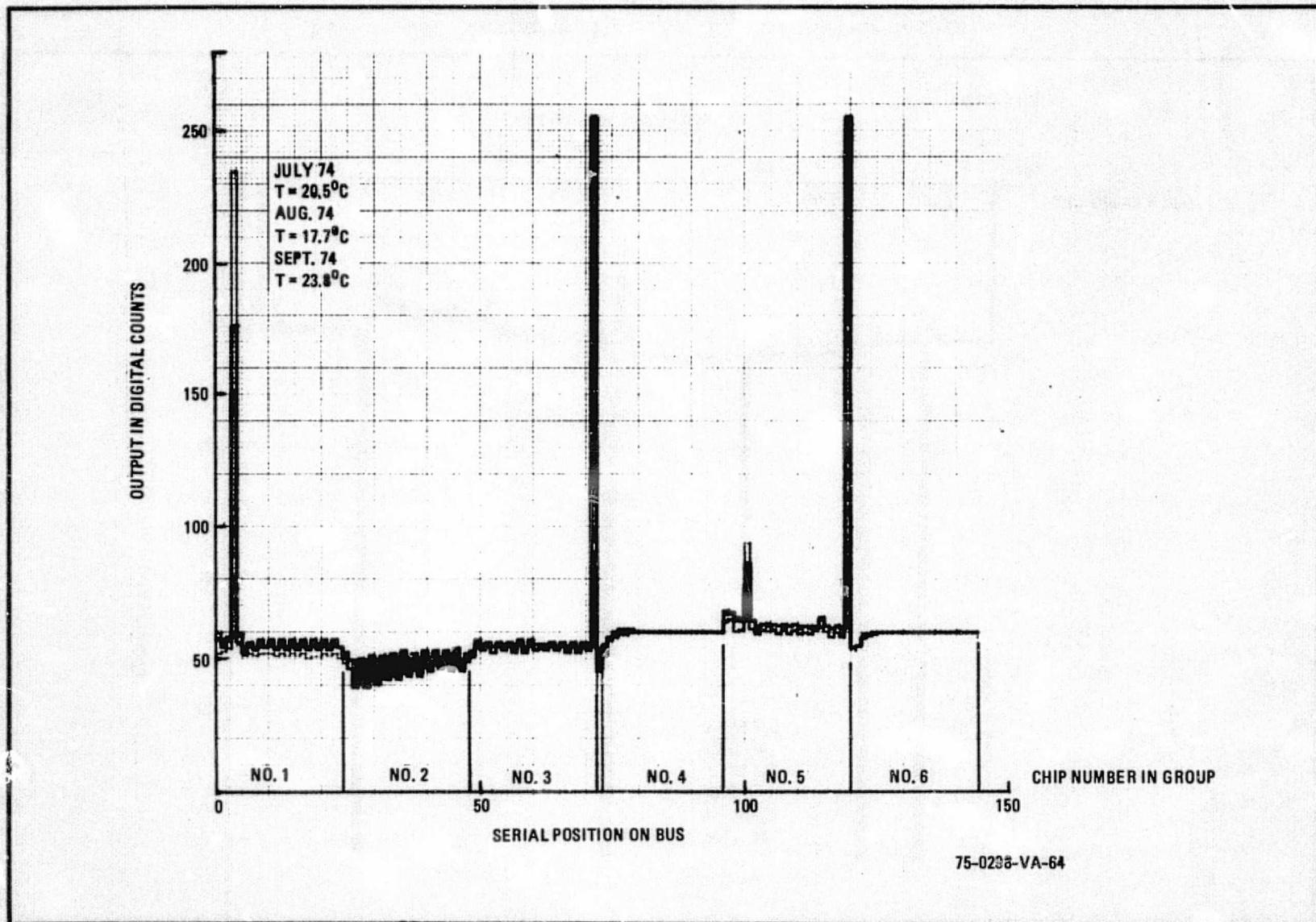
Figure 65. Output at Dark vs Time and Temperature
Bus D of Group 2

75-0236-VA-64

APPENDIX H
EIGHTEEN CHIP ARRAY DETECTOR TEST DATA

This appendix contains actual test data for a 96-element photodetector array chip. This performance data is typical of the chips used to fabricate the eighteen-chip array.

Included herein are six data tables which are:

Table 7	Summary Tables
Table 8	Response Minus Dark Current
Table 9	Quantizing Interval
Table 10	RMS Deviation
Table 11	Noise
Table 12	Linearity

TABLE 7

SUMMARY

```
                            CMOS FUNCTION TEST DATA TABLES
CHIP:   TYPE 808    LOT 168    WAFER 4      CHIP 3      RUN 24
        BIAS:  B1 285, B2 291, B3 287, B4 297,  1024 SAMPLES PER ELEMENT  2 A DUAL FUNCTION  IT=1,0MSEC
        COMMENTS:                                      20.530  32.260  19.940  32.84
        HEATER A=   2     HEATER B=   1
```

RESPONSE MINUS DARK (PERCENT FULL SCALE)   # IT=4.0MSEC
    EXPOSURE LEVELS (MICROJOULES/SG. METER)   #   #   #

ELE	0	48.5	144.7	236.0	354.8	578.9	943.5	1419.2
B1	22.54	4.26	12.56	20.62	30.92	50.61	75.58	76.43
B2	20.03	4.28	12.76	20.78	31.37	49.54	74.03	76.58
B3	21.00	4.78	13.51	22.67	34.17	54.56	76.11	77.42
B4	20.94	4.93	14.57	23.71	35.81	55.51	78.16	78.16

QUANTIZING INTERVAL (MICROJOULES PER BIT)

B1	1.12	1.13	1.13	1.13	1.15	1.22	1.82
B2	1.13	1.12	1.12	1.12	1.15	1.34	1.94
B3	.99	1.02	1.02	1.02	1.04	1.22	1.81
B4	.96	.97	.97	.97	.97	1.18	1.78

RMS DEVIATION (PERCENT FULL SCALE)

B1	.12	.13	.13	.13	.13	.14	.08	.00
B2	.13	.13	.15	.15	.15	.14	.02	.00
B3	.12	.13	.14	.13	.14	.16	.01	.00
B4	.14	.14	.15	.15	.14	.16	.00	.00

NOISE (MICROJOULES PER SQ. METER)
    EXPOSURE LEVELS (MICROJOULES/SG. METER)

	24.2	96.6	150.3	255.4	386.4	761.4	1181.5
B1	1.47	1.50	1.49	1.53	1.51	1.13	1.73
B2	1.52	1.63	1.74	1.72	1.69	1.13	.24
B3	1.27	1.41	1.41	1.39	1.52	2.63	.06
B4	1.36	1.44	1.45	1.42	1.44	1.48	.00

LINEARITY (ABSOLUTE UNITS) = BETWEEN LEVELS 2 AND 3

B1	.9863
B2	.9997
B3	.9756
B4	.9897

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TABLE 8

RESPONSE MINUS DARK CURRENT

RESPONSE MINUS DARK (PERCENT FULL SCALE)   BUS NUMBER 81
CHIP 3   RUN 24

The tabular data below is a densely printed computer listing with columns labeled (approximately):

CHIP1 / EXPCE | TYPE 808 / ±0 | LOT 168 / 48±5 | 144±7 | WAFER 4 / 236±C | 354±8 | 376±5 | 943±5 | 1419±2

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TABLE 9

QUANTIZING INTERVAL

QUANTIZING INTERVAL (MICRO-ELLES PER BIT) BUB NUMBER 81							
CHIP: TYPE 808	LOT 168		WAFER 4	CHIP 3		RUN 24	
E3FEE =0	68.5	144.7	236.C	394.8	578.5	543.9	1415.2
1	1.25	1.75	1.25	1.27	1.23	1.27	1.81
7	1.05	1.12	1.13	1.12	1.12	1.21	1.81
5	1.13	1.13	1.13	1.13	1.13	1.19	1.80
15	1.15	1.17	1.16	1.17	1.16	1.22	1.84
17	1.24	1.23	1.2C	1.21	1.21	1.21	1.79
23	1.13	1.16	1.16	1.15	1.15	1.2E	1.83
2C	1.15	1.15	1.17	1.17	1.17	1.2C	1.81
31	1.10	1.13	1.13	1.13	1.13	1.13	1.79
33	1.10	1.12	1.12	1.12	1.11	1.21	1.82
35	1.08	1.C5	1.C5	1.08	1.C8	1.2C	1.81
41	1.08	1.C7	1.C7	1.07	1.C7	1.21	1.82
47	1.08	1.C6	1.C6	1.05	1.C4	1.2C	1.80
45	1.05	1.C6	1.C6	1.06	1.C6	1.21	1.83
55	1.08	1.C8	1.C8	1.C8	1.C2	1.2C	1.80
57	1.10	1.11	1.11	1.11	1.1C	1.3C	1.95
63	1.08	1.1C	1.C9	1.09	1.CF	1.2C	1.81
6C	1.06	1.C5	1.C5	1.C8	1.C6	1.2C	1.81
71	1.08	1.1C	1.1C	1.10	1.C5	1.2C	1.81
73	1.08	1.11	1.11	1.11	1.11	1.21	1.81
75	1.05	1.C7	1.C7	1.07	1.C7	1.2C	1.81
83	1.03	1.C6	1.C6	1.05	1.C2	1.2C	1.81
87	1.05	1.C7	1.C7	1.07	1.C4	1.2C	1.81
85	1.09	1.C7	1.C7	1.07	1.C7	1.21	1.81
5E	1.51	1.56	1.53	1.53	1.45	1.45	1.80
2	1.94	1.72	1.72	1.76	1.74	1.74	1.80
8	1.13	1.1C	1.11	1.10	1.1C	1.14	1.71
1C	1.08	1.1C	1.1C	1.C9	1.C5	1.17	1.75
16	1.15	1.13	1.14	1.12	2.13	3.47	5.22
1E	1.13	1.14	1.13	1.13	1.13	1.15	1.73
24	1.13	1.14	1.15	1.14	1.14	1.22	1.84
2C	1.08	1.11	1.11	1.11	1.11	1.15	1.78
38	1.08	1.C7	1.C7	1.C7	1.CC	1.16	1.75
34	1.08	1.C8	1.C8	1.C8	1.C7	1.15	1.73
4C	1.C5	1.C5	1.C4	1.05	1.56	2.52	3.33
42	1.05	1.C6	1.C6	1.06	1.CC	1.19	1.79
4E	1.03	1.CE	1.C4	1.03	1.C3	1.15	1.73
CC	1.03	1.C3	1.C4	1.03	1.C3	1.16	1.74
84	1.C8	1.C8	1.C7	1.C8	1.C7	1.15	1.73
8E	1.03	1.C7	1.C8	1.C7	1.C7	1.16	1.74
84	1.C8	1.C5	1.C5	1.C8	1.28	1.2C	1.59
A6	1.08	1.C5	1.C5	1.08	1.C2	1.18	1.74
72	1.05	1.CC	1.C7	1.07	1.C6	1.16	1.73
74	1.08	1.CF	1.C8	1.07	1.C7	1.15	1.73
8C	1.05	1.C6	1.C6	1.05	1.C4	1.14	1.74
82	1.05	1.C6	1.C6	1.06	1.CE	1.15	1.73
88	1.05	1.C6	1.C7	1.07	1.CE	1.15	1.73
8C	1.C8	1.CE	1.C7	1.07	1.CC	1.16	1.74
84	1.43	1.42	1.4C	1.41	1.38	1.32	1.72
3	1.01	1.CC	1.CC	1.00	.55	1.18	.77
5	.93	.57	.58	.57	.57	1.18	1.77
11	1.05	1.C7	1.C8	1.07	1.C7	1.27	1.92
13	1.01	1.C6	1.C6	1.C6	1.C6	1.15	1.79
19	1.10	1.11	1.1C	1.11	.55	1.17	1.75
21	1.03	1.C6	1.C6	1.C6	1.C6	1.15	1.79
27	1.01	1.C6	1.C6	1.07	1.C7	1.17	1.76
28	1.C1	1.C3	1.C3	1.C3	1.C3	1.18	1.77
35	.99	1.CE	1.CE	1.C2	1.C1	1.18	1.78
37	.97	1.CC	1.CC	.99	.55	1.18	1.77
43	1.01	1.CC	.95	1.00	.55	1.47	2.22
4E	.93	.55	.58	.95	.95	1.18	1.77
81	1.01	1.CE	1.C2	1.02	1.4E	1.34	1.85
83	.95	.55	.55	.55	.53	1.85	2.59
85	1.01	1.C3	1.C4	1.03	1.C4	1.18	1.78
41	.57	1.CC	1.CC	1.00	1.CC	1.18	1.77
47	1.01	1.C3	1.C4	1.04	1.C4	1.18	1.78
45	.97	1.CC	1.CC	1.00	1.CC	1.18	1.77
75	.99	1.C3	1.C2	1.C2	1.C3	1.18	1.78
77	.99	1.C1	1.C1	1.00	1.CC	1.18	1.77
83	.99	1.CC	1.CC	1.00	1.CC	1.18	1.78
85	.95	.58	.58	.58	.52	1.18	1.77
51	.97	1.CC	1.CC	1.C0	.95	1.18	1.28
53	.97	1.CC	1.CC	1.00	.52	1.18	1.77
4	1.01	1.CC	1.C1	1.C1	1.CC	1.21	1.82
6	.97	.56	.56	.55	.55	1.16	1.75
12	1.01	1.C3	1.C4	1.03	1.C4	1.19	1.78
14	1.01	1.CC	1.CC	1.00	.55	1.18	1.78
2C	1.05	1.C4	1.C6	1.C6	1.C6	1.41	1.76
28	.97	.58	.58	.58	.58	1.19	1.79
28	.99	1.C2	1.C2	1.C2	1.C3	1.17	1.76
3C	.97	.56	.57	.57	.57	1.19	1.79
36	.95	.58	.58	.58	.57	1.18	1.77
3E	.93	.52	.03	.93	.53	1.19	1.78
44	.91	.56	.57	.56	.56	1.15	1.73
4E	.90	.5C	.51	.50	.5C	1.18	1.79
7C	.95	.1C	.57	.51	.56	1.15	.59
54	.06	.55	.55	.55	.54	1.16	.78
6C	.99	1.CC	1.C1	1.C5	1.CC	1.13	1.59
82	.93	.58	.58	.94	.54	1.12	1.78
88	.97	.58	.55	.55	.58	1.18	1.78
3C	.93	.52	.54	.83	.53	1.8C	1.81
32	.99	1.CC	.55	.55	.55	1.18	1.78
38	.95	.51	.54	.94	.54	1.15	1.73
84	.99	1.CC	1.CC	1.00	1.CC	1.18	1.78
86	.93	.55	.54	.54	.54	1.15	1.78
52	.95	.56	.57	.96	.55	1.19	1.26
54	.88	.5C	.85	.90	.95	1.13	1.69

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TABLE 10

RMS DEVIATION

RMS DEVIATION (PERCENT FULL SCALE)   BUS NUMBER B1
CHIP: TYPE 808   LOT 142   WAFER 6   CHIP 3   RUN 24
EXPES $0   43,5   144,7   236,C   354,8

1	+08	+09	+16	+12	+08	+1C	+1C	+00
7	+12	+15	+11	+1C	+15	+11	+CC	+00
9	+13	+11	+16	+1C	+11	+16	+CC	+00
15	+11	+15	+11	+13	+14	+12	+CC	+00
17	+11	+13	+C8	+11	+11	+1C	+14	+00
23	+11	+17	+11	+1C	+12	+13	+CC	+00
2C	+18	+1C	+13	+19	+15	+15	+00	+00
31	+11	+14	+1C	+1C	+13	+15	+CC	+00
33	+11	+11	+11	+11	+14	+15	+CC	+00
39	+10	+15	+1C	+18	+11	+16	+CC	+00
41	+11	+12	+14	+17	+14	+17	+CC	+00
47	+15	+17	+11	+19	+12	+18	+CC	+00
49	+11	+10	+11	+13	+10	+17	+CC	+00
55	+12	+09	+12	+23	+15	+12	+CC	+00
57	+13	+14	+11	+11	+13	+16	+CC	+00
63	+10	+16	+14	+12	+16	+15	+0C	+00
65	+10	+11	+11	+12	+14	+14	+CC	+00
71	+13	+11	+2C	+13	+18	+16	+0C	+00
73	+11	+15	+C5	+16	+11	+15	+CC	+00
79	+11	+11	+12	+11	+13	+16	+CC	+00
81	+19	+10	+1C	+18	+18	+12	+CC	+00
87	+12	+14	+11	+23	+15	+17	+CC	+00
89	+15	+13	+15	+12	+13	+13	+CC	+00
95	+17	+23	+C5	+1E	+16	+1C	+15	+00
1	+10	+07	+14	+11	+80	+C8	+14	+00
8	+22	+13	+11	+13	+15	+17	+CC	+00
1C	+12	+18	+1C	+14	+15	+15	+CC	+00
16	+17	+12	+17	+26	+11	+CC	+CC	+00
18	+13	+13	+14	+17	+16	+13	+CC	+00
24	+13	+15	+11	+11	+15	+21	+0C	+00
26	+15	+12	+26	+17	+08	+15	+CC	+00
32	+12	+15	+14	+16	+17	+17	+CC	+00
34	+12	+14	+21	+12	+12	+1C	+CC	+00
1C	+11	+13	+16	+16	+16	+CC	+CC	+00
42	+11	+16	+12	+12	+13	+15	+CC	+00
48	+08	+16	+1C	+14	+12	+CC	+CC	+00
5C	+11	+09	+12	+14	+12	+22	+CC	+00
56	+10	+12	+12	+19	+18	+17	+CC	+00
58	+12	+13	+1E	+12	+14	+14	+16	+00
64	+11	+16	+15	+13	+16	+17	+CC	+00
66	+13	+10	+12	+13	+13	+13	+CC	+00
72	+11	+13	+13	+16	+16	+14	+CC	+00
74	+11	+14	+14	+16	+17	+15	+CC	+00
1C	+20	+09	+14	+16	+17	+16	+CC	+00
82	+21	+11	+14	+12	+16	+14	+CC	+00
88	+12	+19	+12	+24	+80	+15	+CC	+00
8C	+15	+14	+16	+18	+17	+17	+16	+00
94	+13	+14	+18	+19	+12	+12	+CC	+00
3	+10	+11	+11	+C3	+15	+13	+CC	+00
8	+11	+14	+18	+C7	+15	+13	+CC	+00
11	+13	+16	+12	+C9	+12	+13	+CC	+00
13	+11	+13	+14	+12	+14	+15	+CC	+00
15	+11	+12	+14	+12	+13	+15	+CC	+00
21	+13	+13	+12	+11	+13	+14	+CC	+00
27	+12	+11	+13	+13	+13	+15	+CC	+00
29	+13	+12	+12	+12	+14	+17	+CC	+00
35	+11	+15	+13	+13	+14	+18	+CC	+00
37	+10	+13	+18	+13	+12	+14	+CC	+00
43	+13	+12	+14	+21	+15	+1C	+CC	+00
48	+14	+10	+14	+14	+14	+16	+18	+00
51	+12	+13	+14	+14	+12	+14	+CC	+00
53	+14	+12	+14	+14	+16	+14	+CC	+00
55	+12	+15	+14	+14	+13	+17	+CC	+00
61	+14	+12	+14	+1C	+15	+17	+CC	+00
67	+14	+12	+12	+12	+13	+16	+CC	+00
63	+14	+13	+1E	+16	+16	+18	+CC	+00
75	+11	+11	+11	+11	+13	+2C	+CC	+00
77	+13	+13	+17	+14	+17	+15	+CC	+00
33	+11	+11	+18	+13	+14	+14	+CC	+00
85	+12	+14	+16	+22	+12	+13	+CC	+00
91	+13	+14	+18	+15	+14	+16	+CC	+00
93	+11	+16	+11	+13	+16	+12	+CC	+00
4	+11	+10	+18	+17	+13	+13	+CC	+00
6	+15	+19	+14	+16	+15	+16	+CC	+00
12	+14	+13	+12	+17	+13	+15	+CC	+00
14	+16	+14	+14	+15	+12	+14	+CC	+00
2C	+12	+12	+14	+13	+15	+12	+CC	+00
22	+13	+14	+16	+14	+18	+17	+CC	+00
38	+17	+13	+11	+16	+13	+18	+CC	+00
1C	+18	+15	+16	+21	+13	+17	+CC	+00
36	+11	+06	+2C	+11	+16	+15	+0C	+00
38	+14	+14	+13	+13	+13	+18	+CC	+00
44	+14	+17	+18	+C8	+18	+14	+CC	+00
46	+12	+15	+13	+16	+11	+12	+CC	+00
52	+11	+14	+14	+15	+15	+2C	+CC	+00
94	+11	+16	+1C	+15	+11	+14	+CC	+00
4C	+12	+13	+14	+14	+18	+13	+CC	+00
66	+13	+16	+11	+14	+15	+16	+CC	+00
68	+18	+13	+18	+C8	+17	+14	+CC	+00
7C	+15	+17	+12	+16	+17	+12	+02	+00
76	+14	+11	+21	+14	+15	+17	+CC	+00
78	+17	+12	+12	+12	+13	+14	+CC	+00
84	+14	+13	+16	+1C	+12	+15	+CC	+00
86	+14	+16	+16	+12	+17	+14	+CC	+00
92	+12	+13	+14	+18	+14	+17	+CC	+00
94	+20	+15	+23	+16	+14	+14	+CC	+00

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TABLE 11

NOISE

```
NOISE (MICROJOULES PER SQ. METER)           BUS NUMBER  81
CHIP:    TYPE E08        LBT 168       WAFER 4      CHIP 3        RUN
EXPES     24.2       06.6     15C.3    25E.4
```

TABLE 12

LINEARITY

LINEARITY (ABSOLUTE UNITS) - BETWEEN LEVELS 2 AND 3 - BUS NUMBER 81
CHIP TYPE 308   LOT 14E   WAFER 4   CHIP 3   RUN 24

CHIP	VALUE
1	.9872
7	.9602
9	.9971
15	.9889
17	1.0134
23	.9737
29	.9730
31	.9744
33	.9820
35	.9900
41	1.0049
47	1.0198
45	.9903
53	.9974
57	.9897
63	.9825
69	.9900
71	.9825
73	.9676
75	.9830
81	.9835
87	.9830
85	.9830
55	.9738
2	1.0056
6	1.0204
10	.9825
16	1.0208
18	.9893
24	.9893
26	.9676
32	1.0049
34	.9974
40	1.0049
42	.9976
48	.9835
50	.9977
56	.9974
58	.9621
64	.9900
66	.9900
72	.9903
74	.9974
80	1.0049
82	.9976
88	.9903
90	1.0123
96	1.0049
3	1.0049
5	.9598
11	.9830
13	.9560
19	.9897
21	.9692
27	.9491
25	.9769
35	.9707
37	.9714
43	1.0118
46	.9791
51	.9909
59	.9695
65	.9770
61	.9714
67	.9769
69	.9647
75	.9707
77	.9775
83	.9844
85	.9720
51	.9714
59	.9714
4	1.0049
8	1.0116
14	.9639
18	1.0118
20	.9903
22	.9915
28	.9707
30	1.0049
36	.9658
38	1.0113
44	.9480
46	.9925
58	.9917
54	.9983
60	.9912
62	.9855
68	.9848
70	.9984
74	.9912
78	1.0114
84	.9844
86	.9855
58	.9852
94	.9806

74-D484-V-7

APPENDIX I

HP-8330A CALIBRATION REPORT

Westinghouse Electric Corporation   **Industry & Defense**

Defense & Electronic Systems Center
Aerospace & Electronic Systems Division

Friendship International Airport
Box 746
Baltimore Maryland 21203

Standardizing Laboratory

REPORT OF CALIBRATION

for

THERMOPILE
(Radiant Flux Detectors)

MFR: HEA   MODEL: 8330A   SERIAL NO: 00520

Submitted by

SDDE (Tracy)

The relative spectral response of this instrument was determined by comparison to an EPPLEY thermopile equipped with a window of known spectral transmittance. A 250 mm monochromator with a 20 nm bandpass was used to provide the monochromatic radiation.

The absolute response was measured at 632.8 nm using a helium-neon laser as the source. The radiation field was 3.0 cm in diameter and was produced with a spatial filter and lenses. The calibration factor was found to be 96%.

The uncertainties in the measurement arise from the repeatability of the test instrument, stray light in the monochromator and non-uniformity in the radiation field.

Uncertainty of the relative response is estimated to be within ± 2.0% with the absolute response estimated to be ± 5.0%.

The relative response normalized to 632.8 nm with a calibration factor of 96% is tabulated in Table 1.

For the Manager

Carroll G. Hughes, III
Senior Engineer

Test No: 75020606

Date: 11 February, 1975

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TABLE 13

RELATIVE SPECTRAL RESPONSE AT SELECTED WAVELENGTHS, NORMALIZED TO 632.8 nmi

Wavelength (nmi)	Relative Spectral Response
500	0.80
600	0.93
632.8	1.00
700	1.01
800	1.00
900	0.96
1000	0.99
1100	1.00
1200	1.08

Test No: 75020606

Date: 11 February 1975