REPORT

DESIGN AND DEVELOPMENT OF A FIXED AND A MOBILE DATA COLLECTION PLATFORM

CONTRACT NO: NAS5-21164

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND 20771

JUNE 1971

American Electronic Laboratories
COLMAR, PENNA.

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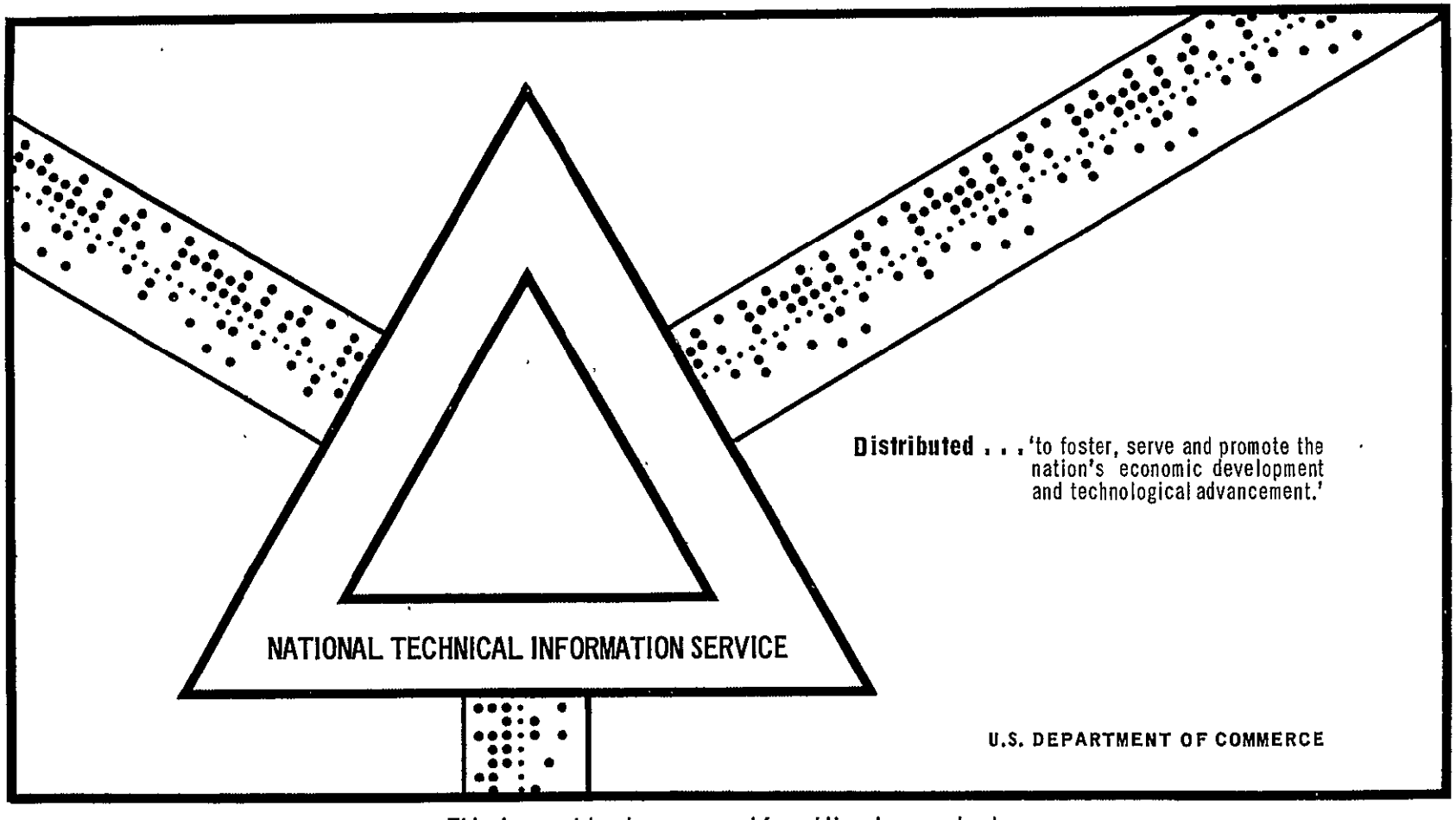

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AMERICAN ELECTRONIC LABORATORIES, INC.
RICHARDSON ROAD, COLMAR, PENNSYLVANIA

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont.)

TABLE OF CONTENTS (Cont.)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont.)

LIST OF TABLES

SECTION 1

INTRODUCTION

1.1 SYSTEM ASPECTS

Signals transmitted from data-collection platforms (DCP) in various parts of the world are received, processed, and stored by a low-orbit satellite on a one-way link. When the satellite is in view of a NASA ground station, the information is transmitted by the satellite to the ground.

The information obtained from the satellite is then processed at a data reduction center. Processing equipment detects each signal and extracts the frequency, time, platform signature, and sensor data. The extracted time information is referenced to the real time of receipt of the platform signals at the satellite. The signal-processing equipment is used to determine the position and/or velocity of each drifting platform as required.

1.2 PLATFORMS

Two types of platforms (see Figure 1-1) have been developed:

a. MOBILE DATA COLLECTION PLATFORM (MDCP) for use on constant level balloon vehicles.

b. FIXED DATA COLLECTION PLATFORM (FDCP) for use at remote ground locations.

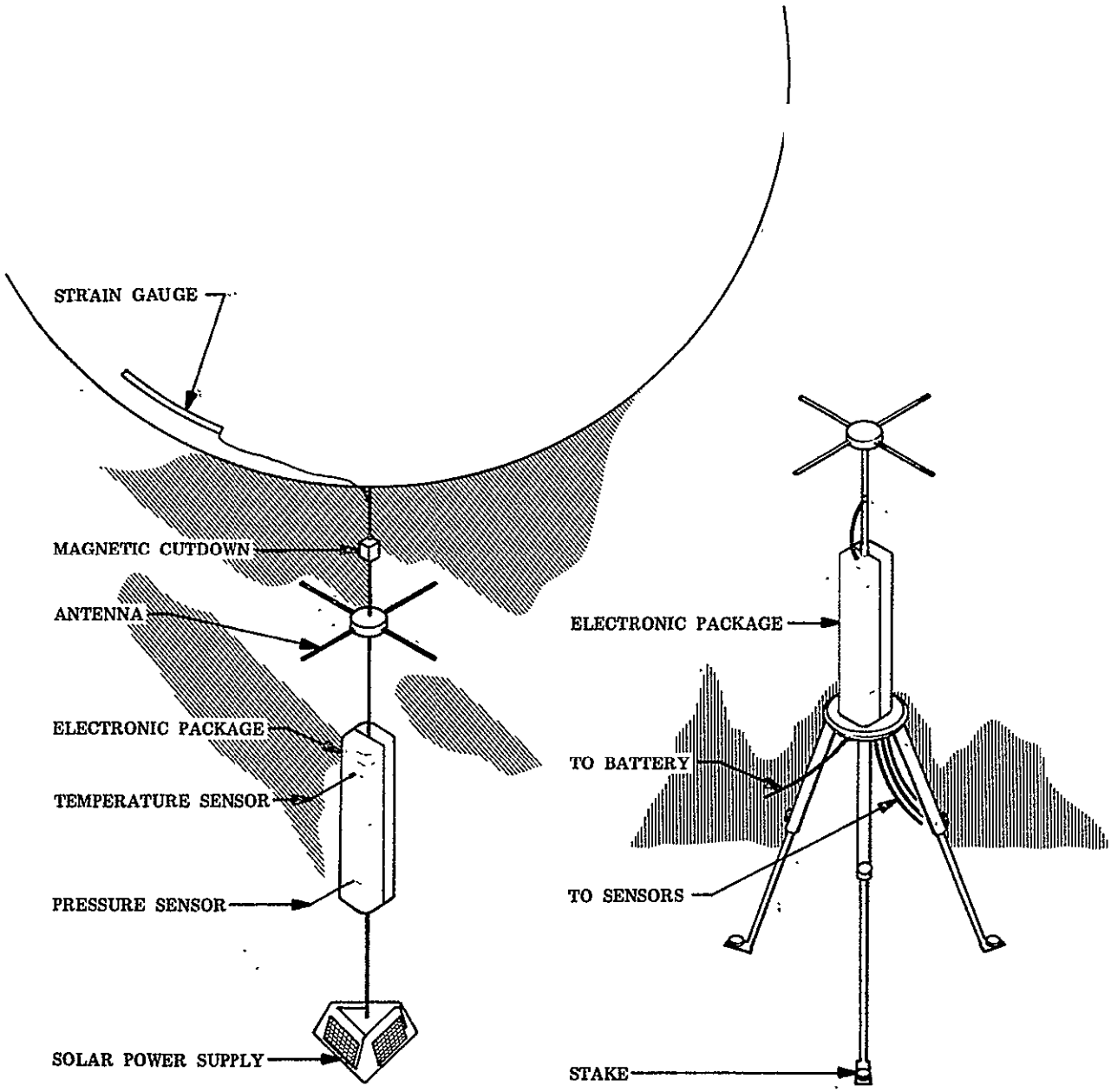


Figure 1-1. Data Collection Platform (Artist's Concept)

Those carried by balloons employ a highly stable oscillator to enable determination of platform position and/or velocity by use of Doppler techniques. An absolute a priori knowledge of the transmitted frequency is not required; what is important is that the frequency drift be controlled and small. Both types of platforms are randomly timed; their transmission of environmental data is independent of the receiving satellite. Since no satellite interrogation is necessary, no receiver or decoding equipment is required. As a result, low cost, reduced weight, and minimum power consumption are achieved.

Environmental information obtained by both types of platform sensors is sampled, converted to digital format, encoded, and used to phase-shift key an RF transmitter. The digital portion employs the latest COS/MOS technology to enhance low power dissipation and noise immunity. Exceptional transmission quality is attained through use of a sophisticated oscillator for high-stability, narrowband multipliers for spurious reduction, and stable high-Q amplifiers.

Since the demand for a large number of platforms are required, the electronic package costs should be minimum. Toward this end, American Electronic Laboratories, Inc. has developed an essentially common type of MDCP and FDCP to thus extend the low cost philosophy.

SECTION 2

SUMMARY

The DCP is shown in Figure 2-1. Because of the similarity between the mobile and fixed units, the layouts and components are essentially common. The three "spread" boards contain the digital logic sections; the oscillator assembly and buffers are in the center portion; and the RF assembly is at the end.

Examination of the specifications, on a line-by-line basis, indicates the successful performance of the platforms developed. A review of Section 8 further details how additional improvements can be incorporated to further reduce the overall cost of the low-cost high-quality data collection platform.

2.1 MOBILE PLATFORM

Table 2-1 indicates the specifications desired and the final performance criteria of the mobile platform. During the initial phases of this program, it was expected that the oscillator would require the greatest concentration of engineering expertise. Conferences were held with Fort Monmouth personnel and with leading crystal manufacturers in order to obtain technical and guideline information. As a result, an advanced oscillator assembly has been produced that features the essential component and technical qualities desired.

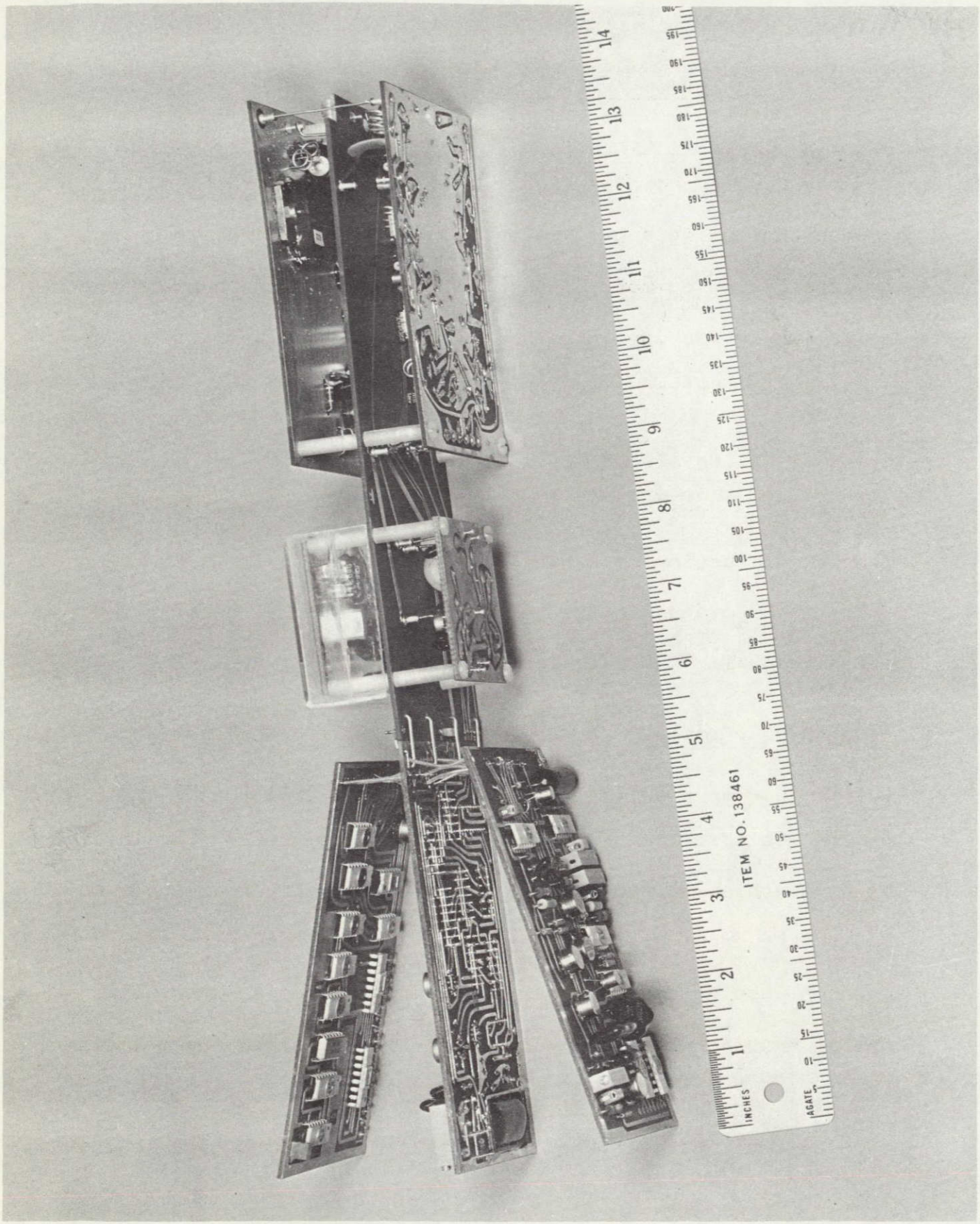


Figure 2-1. Data Collection Platform

TABLE 2-1. MOBILE PLATFORM RESULTS

PARAMETER	CUSTOMER SPECIFICATIONS	TYPICAL PERFORMANCE SPECIFICATIONS
Independent Sensor Inputs	2 Channel	3 Channel (Unused channels wired for CW output)
Symbol Rate	160 Symbol/sec ±0.125%	160 Symbols/sec ±0.125%
Output Symbol Length	80 Symbols	80 Symbols
Total Transmission Format Time	1 Second	1 Second
CW Tone Interval	0.5 Second	0.5 Second
Bits/Data Word	8 Bits	8 Bits
Identification Sequence Length	11 Bits	11 Bits
Sync Code Sequence	5 Bits, at zero	5 Bits, at zero
Timer Repetition Interval	60 ±4.5 Seconds	60 ±4.5 Seconds
Analog Data Inputs	7.5 - 9.5 VDC (△= 2V)	7.5 - 9.5 VDC (△= 2V)
Analog Input Z During Sample	> 100K	> 10M
Prime Power	12 VDC ±1 VDC	12 VDC ±1 VDC
Prime Power Ripple	1 mv RMS	1 mv RMS
Idc Peak @ 12 VDC	1.0a	0.40a
Idc Ave. @ 12 VDC	10 ma	10 ma
Pdc Peak @ 12 VDC	---	4.8W
Pdc Ave. @ 12 VDC	---	120 mw
Pdc Quiescent	---	22 mw
Logic Noise Tolerance	1V, either state	4.4V min., either state
A/D Conversion Accuracy	7 Bit (~ 1%)	7 Bit (> 1%)
Warmup Time	---	1.56 seconds
Operating Temperature Range	25°C ±5°C	25°C ±5°C
Storage Temperature Range	-54°C to +49°C	-55°C to +80°C
Weight	550g	614g incl. insulation
Osc. Short Term Stability	1 in 10^9 (for 1/2 sec.)	< 1 in 10^9
Mean Drift	0.2 Hz/min. for 15 min.	3.56 Hz/15 min. isothermal best
Tx. Output Frequency	403.1 MHz ±0.005%	403.1 MHz ±0.005%
Tx. Output Spur Rejection	> 60 dB	> 55 dB @ 12V
PSK Phase Shift	170° ±5°	170° ±5°
Transmitter Output Power	< 1 watt	1 watt
Total Volume	---	240 cu. in.

The logic section concentrated on using the latest COS/MOS components to thus reduce power consumption. A review of Table 2-1 indicates that the system peak current is 50 percent better than required in the specification. Further analysis is required in the A/D section to improve the temperature coefficient qualities in order to meet the bit tolerance over the environmental operating range.

The packaging technique employed features ease of assembly, interdependence of the RF and logic sections, and layouts compatible with frangability requirements.

2.2 FIXED PLATFORM

Table 2-2 indicates the applicable specifications and results obtained from the fixed platform. The same oscillator used in the mobile platform was utilized in this system. Because of the reduced symbol length (0.1 seconds) it is mandatory that the "turn on" stability be small to keep the variations in the transmit frequency at a minimum. The logic and transmitter assemblies are essentially identical with those of the mobile platform. This philosophy was utilized at the beginning of the program in order to plan and incorporate commonality factors.

TABLE 2-2. FIXED PLATFORM RESULTS

PARAMETER	CUSTOMER SPECIFICATIONS	TYPICAL PERFORMANCE SPECIFICATIONS
Independent Sensor Inputs	8 Channel	8 Channel
Symbol Rate	1600 Symbols/sec ±0.125%	1600 Symbols/sec ±0.125%
Output Symbol Length	160 Symbols	160 Symbols
Total Transmission Format Time	0.1 Second	0.1 Second
CW Tone Interval	---	---
Bits/Data Word	8 Bits	8 Bits
Identification Sequence Length	11 Bits	11 Bits
Sync Code Sequence	5 Bits, at zero	5 Bits, at zero
Timer Repetition Interval	120 ±10 sec.	120 ±10 sec.
Analog Data Inputs	7.5 - 12.5 VDC (Δ= 5.0V)	7.5 - 9.5 VDC (Δ= 2.0V)
Analog Input Z During Sample	> 100K	-> 10M
Prime Power	12 VDC ±1 VDC	12 VDC ±1 VDC
Prime Power Ripple	1 mv RMS	1 mv RMS
Idc Peak @ 12 VDC	3.0a	1.3a
Idc Ave. @ 12 VDC	4.0 ma	2.12 ma
Pdc Peak @ 12 VDC	---	15.6W
Pdc Ave. @ 12 VDC	---	25.5 mw
Pdc Quiescent	---	< 1 mw
Logic Noise Tolerance	1V, either state	4.4V min., either state
A/D Conversion Accuracy	7 Bit (> 1%)	7 Bit (> 1%)
Warmup Time	---	1.248 Seconds
Operating Temperature Range	-54°C to +49°C	Unit designed for, but not tested from -54°C to +49°C
Storage Temperature Range	-54°C to +49°C	-55°C to +80°C
Weight	4082g	614g incl. insulation
Osc. Short Term Stability	1 in 10^9	< 1 in 10^9
Mean Drift	±0.005%	±0.005%
Tx. Output Frequency	402.1 MHz ±0.005%	402.1 MHz ±0.005%
Tx. Output Spur Rejection	> 60 dB	> 60 dB
PSK Phase Shift	170° ±5°	170° ±5°
Transmitter Output Power	< 5 watts	5 watts
Total Volume	< 330 cu. in.	240 cu. in.

SECTION 3

PLATFORM TRANSMITTER SYSTEM DESCRIPTION

The transmitter assembly of the Data Collection Platform (DCP) shown in Figure 3-1 consists of an oscillator-buffer regulator, a multiplier modulator, and a RF amplifier. This functional block diagram suffices for the mobile and fixed platforms because of the commonality qualities of the platforms. The essential differences pertain only to their stability output power capability and the final transmitted frequency, as detailed in Table 3-1. From a circuit and theoretical standpoint, the two units can be considered identical. Therefore, this report will differentiate between the two types of platforms only where further clarification is necessary.

TABLE 3-1.

TRANSMITTER PLATFORM DIFFERENCES

FUNCTION	FIXED PLATFORM	MOBILE PLATFORM
Fundamental Oscillator Frequency	50.2625 MHz	50.3875 MHz
Final Transmitter Frequency	402.1 MHz	403.1 MHz
Power Output	5 watts	1 watt
Short-Term Stability	---	1 part in 10^9

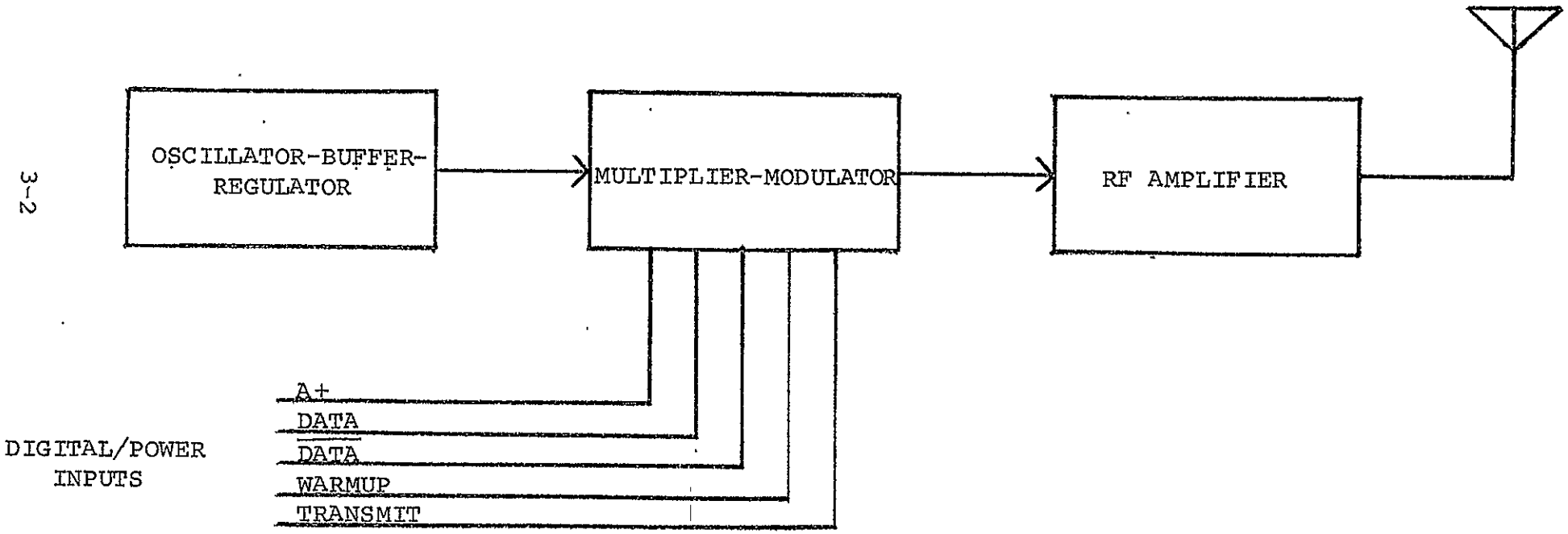


Figure 3-1. DCP Transmitter Assembly A1

The oscillator subassembly generates the highly stable frequency; the multiplier-modulator subassembly increases the frequency by a factor of eight and phase modulates the signal (phase states differ by 170 degrees ±5 degrees); an RF amplifier subassembly increases the power output level to the specified level.

The oscillator assembly exhibits a one-half-second, short-term stability of better than 1 part in 10^9, and has exhibited a drift rate (isothermal best) of 3.56 Hz in a 15-minute interval. The oscillator-buffer-regulator is designed to maintain 0.005 percent frequency tolerance from -54 degrees to +49 degrees C. A buffer amplifier prevents load variations from affecting the oscillator frequency. A separate regulator is used to control the oscillator voltage. The multiplier-modulator and RF amplifier and phase modulator is designed to increase the power level of the oscillator without degrading the short-term stability or generating spurious signals.

3.1 GENERAL DESCRIPTION

3.1.1 Oscillator-Buffer

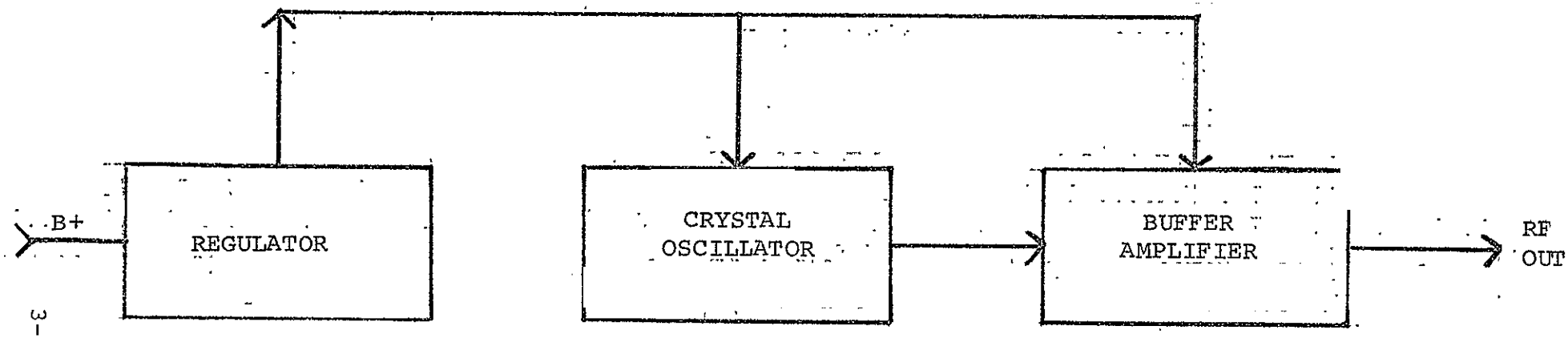
3.1.1.1 Crystal Oscillator Loop

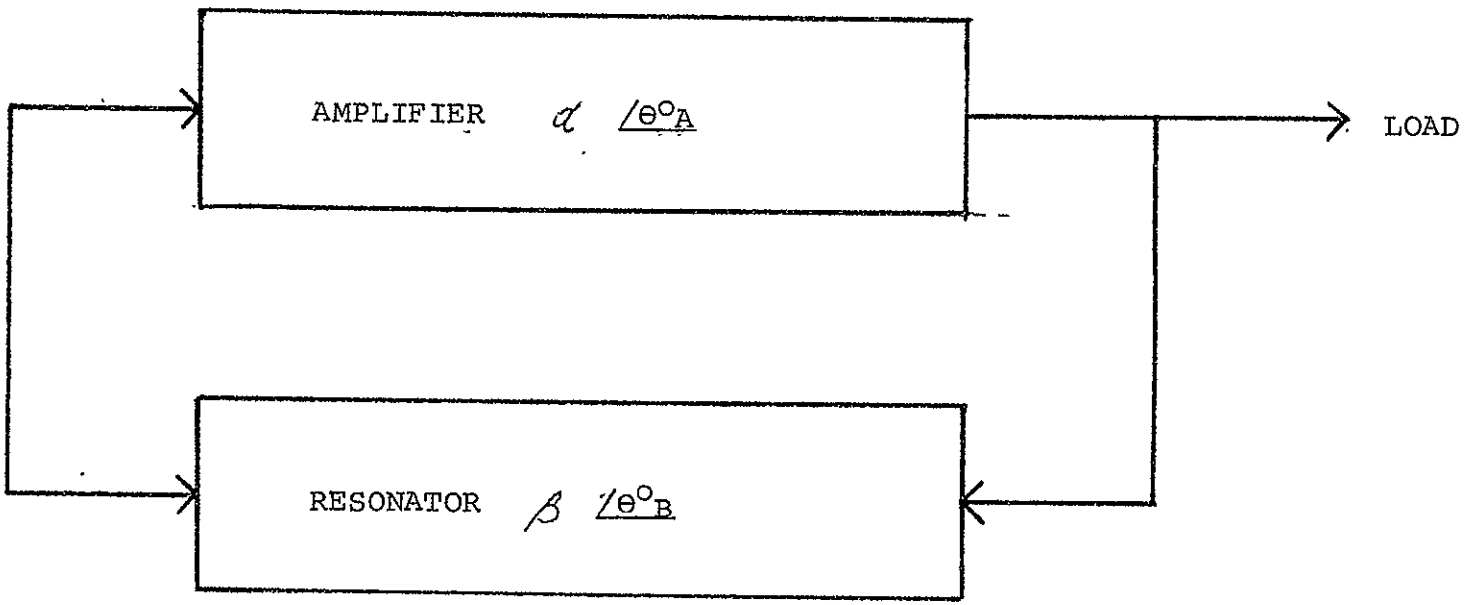
The crystal oscillator in the Mobile Data Collection Platform (MDCP) must exhibit a frequency jitter of better than 1 part in 10^9

for a one-half-second sampling interval with an average drift rate in a 15-minute period of 0.2 Hz/minute. Both the fixed and the mobile platforms must have an overall frequency tolerance of ±0.005 percent; the environmental operating range of the fixed platform is -54 degrees C to +49 degrees C; the mobile platform must operate from +20 degrees C to +30 degrees C.

The oscillator-buffer-regulator subassembly is shown in Figure 3-2. The condition for oscillation for the crystal oscillator loop shown in detail in Figure 3-3, is that the component of loss with zero phase shift in the crystal be offset by the zero phase shift component of amplifier gain. If a phase shift occurs in the amplifier, the oscillator loop must change frequency until the crystal provides a phase shift opposite to that of the amplifier. The less the oscillator loop changes in frequency to compensate for amplifier phase variations, the better the crystal. It can be shown that the fractional frequency shift caused by a phase shift in the amplifier is equal to the phase shift in radians divided by twice the effective Q of the crystal.

The effective Q of the crystal in the aforementioned relationship is determined not only by the unloaded Q of the crystal itself but also by the effective source and load impedances presented by the amplifier. Reducing the source and load impedances of the


B+
REGULATOR
CRYSTAL
OSCILLATOR
BUFFER
AMPLIFIER
RF
OUT



Condition for Oscillation

$\alpha \geq 1$

$\theta_A + \theta_B = n(360^{\circ})$

Figure 3-3. Oscillator Loop

crystal to as small a level as possible will provide the greatest fractional frequency stability. However, reducing the input and output impedances of the amplifier either reduces the gain or causes increased phase shift within the amplifier. A tradeoff must be made between the effective Q of the crystal and the gain of the phase shift of the amplifier to produce the best overall results.

The level of operation of the oscillator loop must also be chosen on the basis of conflicting requirements. The short-term stability is inversely related to the signal-to-noise ratio of the oscillator loop. This can be conceived as noise in the loop combining with the sinusoidal oscillation to slightly shift the positions of the zero crossings. Hence, on a short-time scale, noise causes a slight frequency jitter. Since the noise produced in any given amplifier is at some constant absolute level, the greater the level of oscillation the better the signal-to-noise ratio and the better the noise performance of the oscillator.

The crystal itself presents the conflicting requirement because the series resonant frequency of the crystal is related to the drive level. As a rule of thumb, the frequency-drive sensitivity is one part per million per milliwatt. If the crystal were operating at the one milliwatt level and the drive increased

by one hundred percent, the resonant frequency of the crystals would change by one part per million. If the crystal were operating at the microwatt level and the drive increased one hundred percent, the resonant frequency would change by one part per billion. The lower the operation level the better. A level of operation must be chosen that is low enough to minimize the amplitude effect while not requiring a costly low noise figure amplifier.

Often, oscillator circuits are designed with the level of oscillation being determined by the saturation level of one of the stages in the oscillator. Since this level is temperature dependent, it causes amplitude and hence frequency variations with changes in the ambient temperature; in addition, it requires that the circuit be allowed considerable time to warm up after initial turn-on. If, however, an amplitude limiter is included in the oscillator loop (see Figure 3-3) amplitude variations can be greatly limited and the absolute level of limiting can be made almost constant. Higher levels of operation with the associated improvement in short-term performance can be achieved without the amplitude frequency effect becoming the main source of oscillator degradation. Limiters are being utilized which require very little warmup and hence add greatly to the pulsed performance of the oscillators in the DCP.

Because of the direct relationship of the phase shift in the amplifier to the output frequency of the oscillator, the devices used in the oscillator loop must be biased as stably as possible. Devices self-biased with voltage feedback are utilized. This is the most stable form of self-bias.

3.1.1.2 Buffer Amplifier

It is important that the loading of the buffer amplifier on the oscillator loop does not change and thereby cause phase shifts in the loop. This requirement is met by designing the buffer amplifier to lightly load the oscillator, and designing the input impedance of the buffer amplifier to be constant. The input impedance is dependent upon biasing or supply effect, and the effect of reverse gain reflecting changes of load impedance to the input. This is necessary because the multipliers which load the buffer amplifier are operated in Class C and have wide variations in input impedance with supply voltage, temperature, and level of operation.

The RF/IF cascode amplifier configuration chosen has bias circuitry internally provided to maintain a set bias level and hence a very constant input impedance and an extremely low reverse transfer coefficient. The cascode configuration also has the gain of two cascaded stages in a single package. The output stage of the oscillator assembly is designed with a level of gain compression

to maintain constant output power over the temperature range of the fixed platform.

3.1.1.3 Regulator

The devices in the oscillator-buffer-regulator assembly must be biased in the most stable self-bias configuration so that the supply voltage variations do not effect the frequency of oscillation. An integrated circuit voltage regulator is used in lieu of a zener diode because of the improved ripple rejection ratio and DC stability. An IC regulator also has a shorter warmup period because a lower current flows through the internal reference element. The IC voltage regulator yields the additional advantage of short circuit and overvoltage protection.

3.1.2 Multiplier Modulator

3.1.2.1 Multipliers

The multiplier-modulator subassembly, shown in Figure 3-4, consists of six functional units: the multipliers, the premodulator linear amplifier, the phase-modulator driver, the C+ control, the postmodulator linear amplifiers, and the modulator driver.

The multipliers increase the frequency of the signal produced by the oscillator by a factor of eight. To minimize the total number of stages in the transmitter, each stage in the multipliers

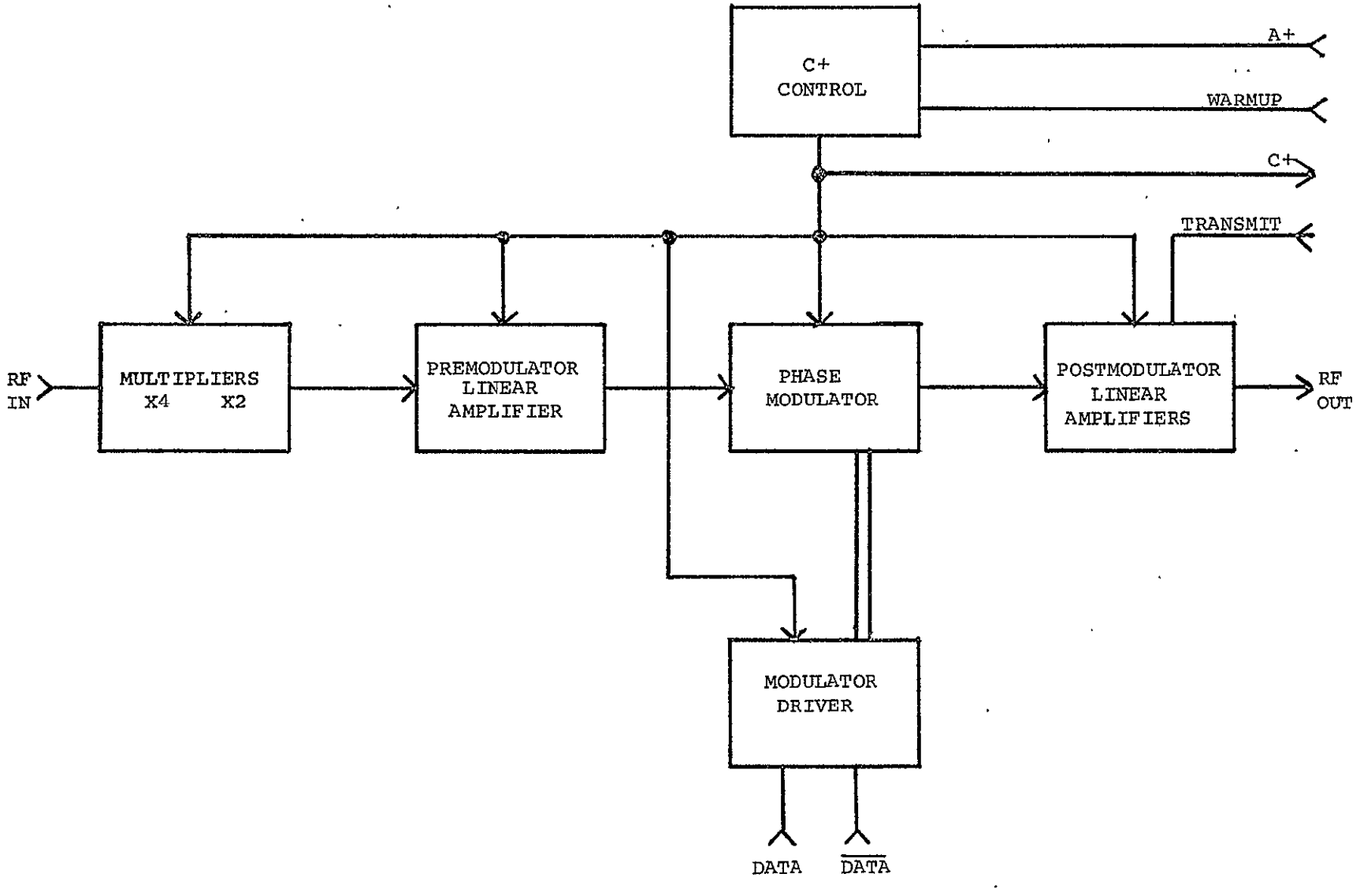


Figure 3-4. Multiplier-Modulator

must be designed for maximum power gain while maintaining absolute stability.

Harmonic rejection can be achieved by designing bandpass filters between the multipliers, at the expense of increased complexity and insertion loss. An alternate approach to suppressing the harmonics is to design narrowband matching networks between the multiplier sections and thus reject undesirable frequencies. The interstage matching thus becomes a tradeoff between power gain, harmonic rejection, and complexity (cost).

The multiplier chain must also be designed so that it does not degradate the carrier-to-noise ratio, and hence, the short-term (one-half-second) stability of the oscillator carrier. Maintaining the carrier-to-noise ratio, the short-term stability below 1 part in 10^9, for a one-half-second integration period, must be a prime consideration in the design of every stage in the amplifier. The multiplication process itself amplifies the noise of the frequency-modulated correlated noise component of the input oscillator signal. An "ideal" noiseless multiplier decreases the carrier-to-noise ratio by 20 log n (dB), where n is the frequency multiplication factor[1].

---

1. Power Stabilization of Microwave and Millimeter Wave Sources; Louis C. Cuccia, James Coogan; Microwave, February 1970.

Additional phase-modulated noise is generated when the amplitude-modulated noise of the oscillator is converted to phase modulation by phase shifting of the amplitude modulation side-bands in the multiplier sections. Thermal noise is contributed by the devices and components in the multiplier circuits. A well-designed multiplier chain minimizes contributions of all but the noise due to multiplication.

The two practical circuit configurations for the multiplier stages are common-base and common-emitter. For the same device, common-base will provide higher frequencies of operation, but since the input is in phase with the output, stabilizing a common-base stage is more difficult. A common-base stage will have greater power gain only if series-resonant idlers are provided for the intended harmonic and all the subharmonics generated. In comparison, a common-emitter needs an idler for only the harmonic frequency desired. The increased power gain obtainable from idler circuits and the increased alignment time they add must be compared against the cost of a corresponding amount of amplifier gain later in the circuit. Common-emitter multipliers are utilized in the DCP to minimize the number of tuning adjustments and overall component cost.

3.1.2.2 Premodulator Linear Amplifier

The premodulator amplifier is a common-emitter linear amplifier that provides power gain of the signal at the final output frequency. This stage must also provide harmonic rejection since it follows the harmonically rich multiplier section.

For the modulator following this section to maintain the phase shift of 170 degrees (±5 degrees), it is required that the source and load impedances presented to the modulator remain constant. This is the main reason for using linear amplifiers before and after the modulator.. Some compression of the signal from the multiplier is desirable to limit the amplitude excursions inherent in the Class C multipliers.

3.1.2.3 Phase Modulator and Driver

The phase modulator must develop two equal amplitude phase states for the signal that are electrically 170 degrees (±5 degrees) apart from each other. The modulator must be able to be operated at a maximum rate of 1600 symbols per second and present no source or load impedance during the switching period that causes any instability in the amplifiers preceding or following the modulator. The operation of the modulator is shown in Figure 3-5.

The driver circuitry for the phase modulator must drive the phase modulator at a maximum of 1600 symbols per second. The

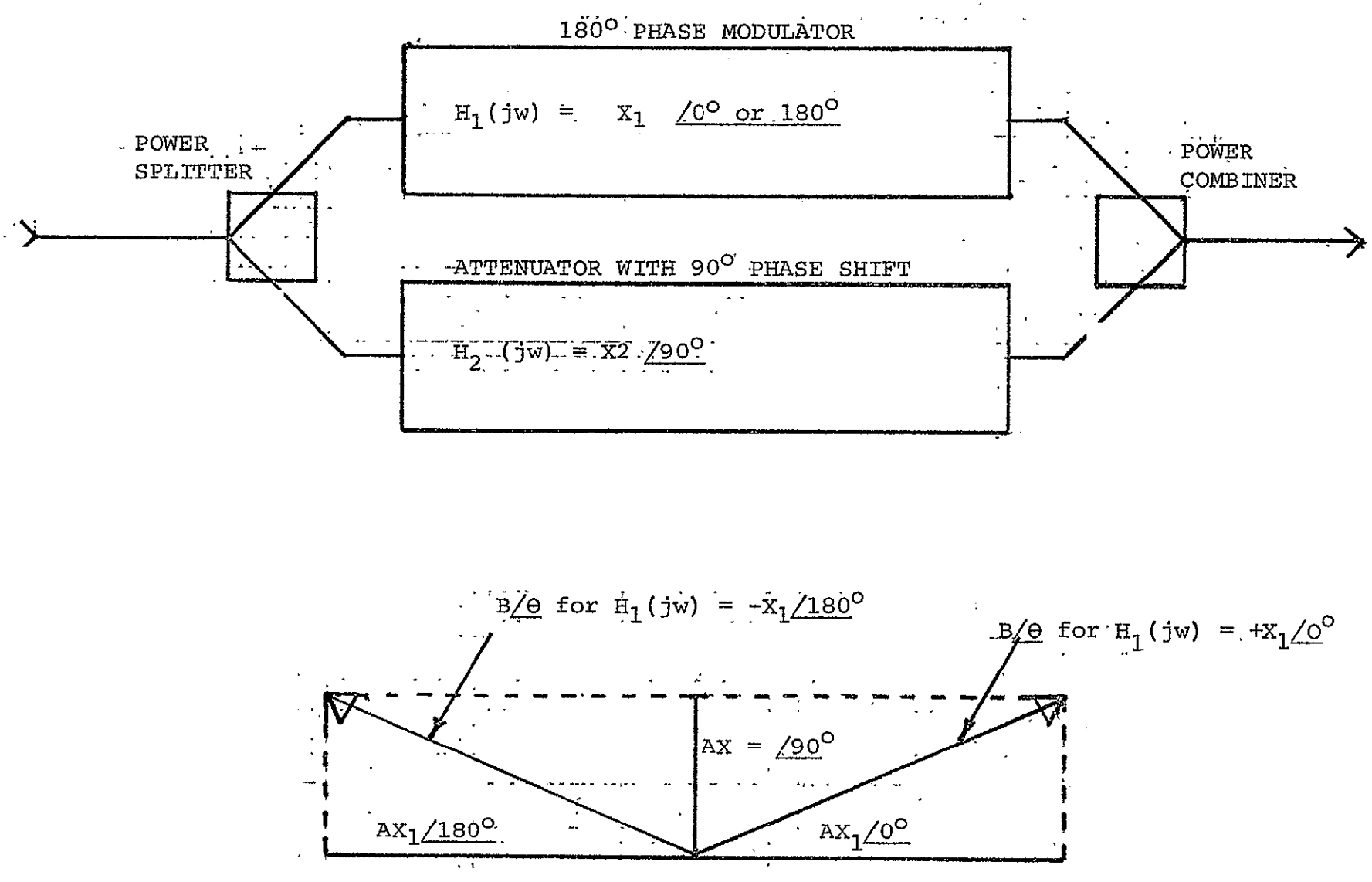


Figure 3-5. Phase Modulator

digital data from the digital section of the DCP is carried to the transmitter as a balanced pair to provide noise immunity. The design of the balanced input circuitry of the phase modulator driver must take into consideration the fact that the pull-down current in the C-MOS drivers is much greater than the source current.

3.1.2.4 Postmodulator Linear Amplifier

The postmodulator linear amplifiers are a series of common-emitter linear amplifiers that provide power gain for the signal at the final output frequency. This chain of linear amplifiers are designed to have sufficient bandwidth so that no tuning adjustments are required. The common-emitter configuration is utilized because of the inherent stability available in this configuration.

The input impedance of the amplifier chain is designed to be stable so as to keep the phase shift produced by the modulator at 170 degrees ($\pm$5 degrees) over all operating conditions. The output impedance of this chain must be designed to transfer maximum power into the RF amplifier subassembly while maintaining absolute stability at all frequencies.

3.1.2.5 C+ Control

The C+ control section of the multiplier-modulator assembly

provides switching between the prime power, A+, and the Class A circuits of the multiplier-modulator subassembly and the RF amplifier subassembly. This switching section prevents the Class A stages from dissipating power until control signals from the digital section signal the start of a transmission period. The design of this circuitry must take into account that the pull-down capability of the C-MOS is greater than the source current capability.

3.1.3 RF Amplifier

3.1.3.1 Linear Amplifier

The RF amplifier subassembly (see Figure 3-6) in the mobile version of the DCP consists of a linear amplifier, followed by a broadband microelectronic Class C IC amplifier with a low-pass filter. The fixed version differs from the mobile unit (Figure 3-7) in that the IC amplifier and associated component values are rated for a higher power of five watts.

The linear amplifier utilized in the mobile and fixed versions provides power gain. This amplifier must be designed to remain stable during bi-phase modulation of the carrier. This corresponds to remaining stable under pulsed conditions because, as the phase of the carrier is switched, the amplitude of the carrier during the switching period becomes in excess of 30 dB below the amplitude of the carrier in either phase state. The linear amplifier also

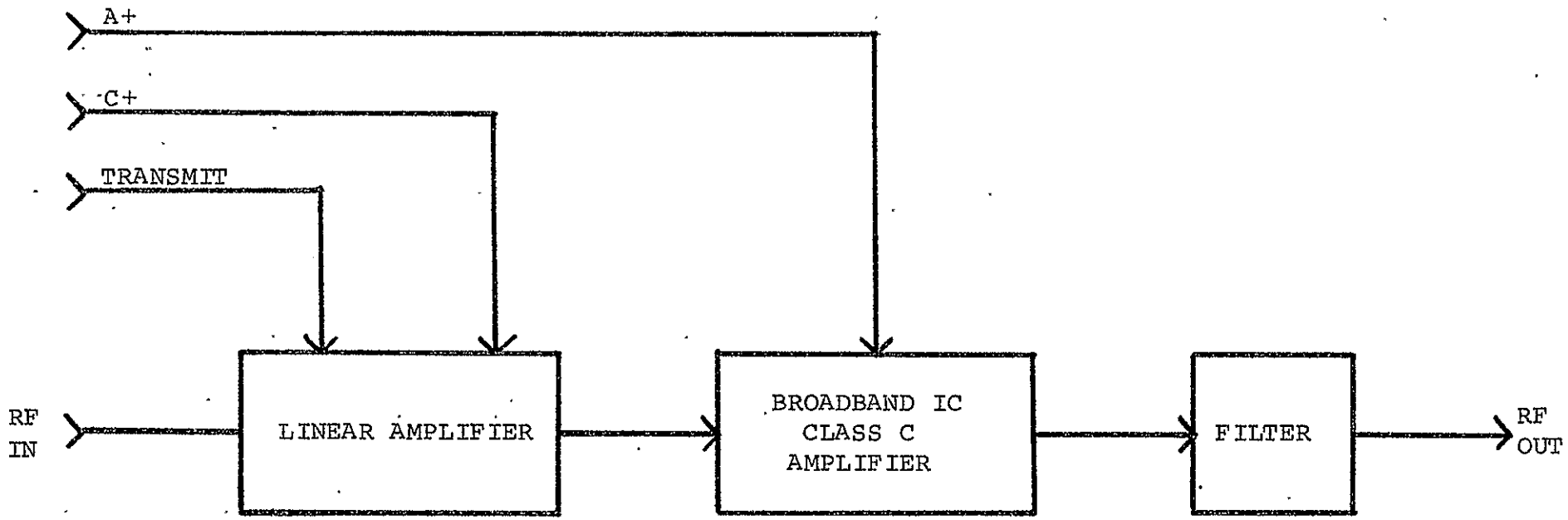


Figure 3-6. RF Amplifier, Mobile

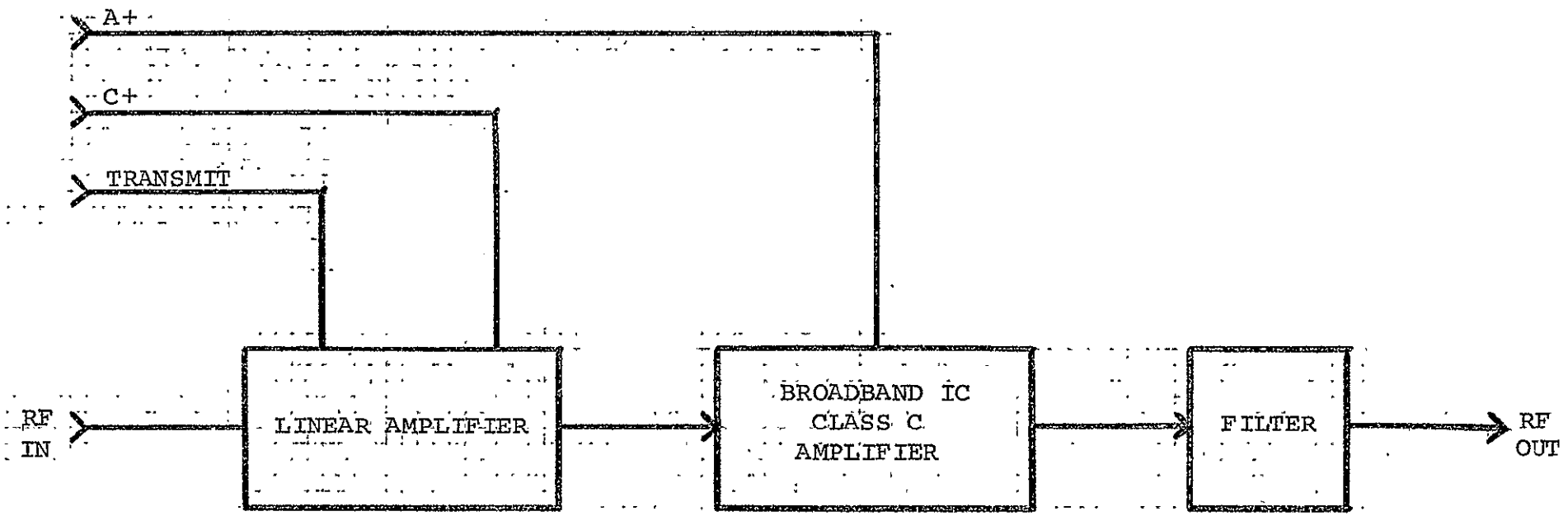


Figure 3-7. RF Amplifier, Fixed

functions as an RF switch and inhibits operation of the Class C amplifier when the base driver is removed. It must also be designed so that the bias can be controlled by the digital logic.

3.1.3.2 Broadband Power Module

A TRW broadband Class C integrated circuit (IC) is utilized to provide the large signal gain in the final output stage. It is not necessary that the IC be unconditionally stable, only that it be stable at all levels of drive within the range of source and load impedances presented by the linear-driving circuitry and the output filter, respectively.

The broadband, Class C, integrated circuit of the fixed platform differs from the mobile platform in that increased power output is required by the former. An IC with a correspondingly larger output power rating is used in place of the IC needed in the mobile platform. This approach maximizes the commonality between the mobile and fixed platforms.

3.1.3.3 Output Filter

The output filter is a three-element, T section, low-pass filter. This filter provides 18 dB/octave attenuation to the harmonics generated in the final amplifier. This filter not only provides the suppression specified but also demonstrates that a low-pass filter

of this form is compatible with the TRW output module. This indicates that additional harmonic rejection could be obtained simply by adding more elements to the filter without introducing any new considerations with regard to output stability.

3.2 DETAILED DESCRIPTION

3.2.1 Circuit Operation

3.2.1.1 Oscillator-Buffer-Regulator

The block diagrams of the transmitter section of the DCP's are shown in Figures 3-2, 3-3, 3-4, 3-5, and 3-6. The interwiring diagram of the transmitter assembly is shown in Figure 3-9. The circuit diagram of the oscillator-buffer is shown in Figure 3-10. Figure 3-11 is the circuit diagram of the multiplier-modulator subassembly. Figures 3-12 and 3-13 are the circuit diagrams of the RF amplifier mobile unit and the RF amplifier fixed unit.

The B+ line, as shown in Figure 3-2, carries power from the control circuitry on the multiplier-modulator subassembly to the oscillator-buffer subassembly. In the mobile DCP, this line can always be energized or energized only during the warmup and transmission period. The length of the warmup period can be varied from 1.56 seconds to 24.9 seconds in the mobile platform.

In the fixed form of the Data Collection Platform, the B+ line is energized during the transmission period and for a warmup period before the transmission period. The warmup period can be varied from 0.156 seconds to 2.496 seconds by moving a jumper wire on the multiplier-modulator subassembly. The longer the warmup period, the less warmup drift the oscillator will exhibit.

The voltage regulator limits the B+ to the DC level needed by the oscillator and the buffer amplifier. It also provides transient suppression of the AC components of the B+. The regulator is designed to provide short circuit and over voltage protection. The oscillator section is protected in this fashion because of the considerable time required to align the oscillator loop. Significant changes of device parameters in the oscillator loop would result from a voltage overload of even a very short duration. The cost of protection is much less than that of realigning the oscillator loop. The short circuit capability also protects the voltage regulator itself from a failure of a device or component within the oscillator buffer subassembly or from an unintentional grounding of the DC line during initial testing or troubleshooting.

The crystal oscillator loop of the oscillator-buffer-regulator subassembly is shown in Figure 3-3. The crystal is characterized at a given frequency and drive level as having an insertion gain

of β and a phase shift of θ_B degrees. The series resonant frequency of the crystal in the mobile platform is 50.3875 MHz and the frequency of the fixed platform is 50.2625 MHz. The amplifier block shown in Figure 3-3 consists of a bipolar amplifier and a fet amplifier-limiter. The amplifier is characterized with respect to frequency and drive level as having an insertion gain of α and a phase shift of θ_A degrees at the operating level.

The conditions for series oscillation are that the sum of the phase shifts of the amplifier and the resonator is an integer multiple of 360 degrees and the gain of the amplifiers be greater than or equal to the loss of the resonator. It is also required that the oscillation criteria be met by the oscillator loop only at the intended frequency. Tuning adjustments are provided to adjust the phase shift and the level of the crystal oscillator. When the phase shift of the amplifier is adjusted to zero degrees, the crystal will oscillate at the series resonant frequency. A variable temperature coefficient capacitor is provided within the oscillator loop to adjust the overall temperature coefficient of the amplifier. By this means the frequency-temperature coefficient of the oscillator can be changed without changing parts in the circuit.

A portion of the signal within the oscillator loop is sampled and amplified by the buffer-amplifier. The buffer is a cascode circuit that amplifies the oscillator signal to the level required by the multiplier circuits. Any change in input impedance of the buffer-amplifier will affect the phase shift in the oscillator loop, and hence the frequency of oscillation. The reverse transfer characteristics of the buffer-amplifier reflects changes in the load impedance to the input circuit. Since the input impedance of a transistor is related to the collector current, changes in bias will cause changes in the input impedance.

To minimize changes of these effects, a cascode RF/IF amplifier with constant current biasing is used as the buffer-amplifier. The internal constant current source maintains a constant bias, and the cascode configuration has an extremely low reverse feedback term. A tuning element is provided on the output of the cascode buffer-amplifier to adjust the output loading.

3.2.1.1.1 Frequency Stability Tests

Figure 1-2 of Appendix A is a block diagram of the test setup for measuring short-term stability. The oscillator under test is frequency mixed with the output of a Hewlett-Packard standard oscillator (Model 106B). The standard oscillator has a short-term stability of 1.5 parts in 10^{11} for sample periods as short as 0.1

second. The signal out of the mixer is then passed through a low-pass amplifier/filter which rejects the sum frequency and other harmonics from the mixer and passes the difference frequency to the counter. The period of successive 0.5 second count intervals are then recorded on the digital printer. The short-term stability is calculated as an average over one hundred of the 0.5 second count intervals.

The test setup for the 15 minute stability test is the same as that used in the short-term stability test and the same basic principles apply. The output of the amplifier/filter was recorded (to the nearest 0.1 Hz) every 10 seconds. This data taken over a 15 minute interval was used to compute the drift rate.

Typical data of a 15 minute sector taken from a 15 hour stability measurement are shown in Figure 3-8. In order to record tenths of a hertz the two most significant digits have been displaced and therefore are not shown in the print out. For example, Figure 3-8 has as the first reading 99999798 which in reality is 399,999,979.8 Hz; this reading is 0.2 Hz higher than the next frequency measurement. There are a total of 90 samples, each are separated by 10 seconds (total of 15 minutes). The standard deviation is used to compute the statistical inference of frequency stability from the 90 samples. The standard deviation, s, is then

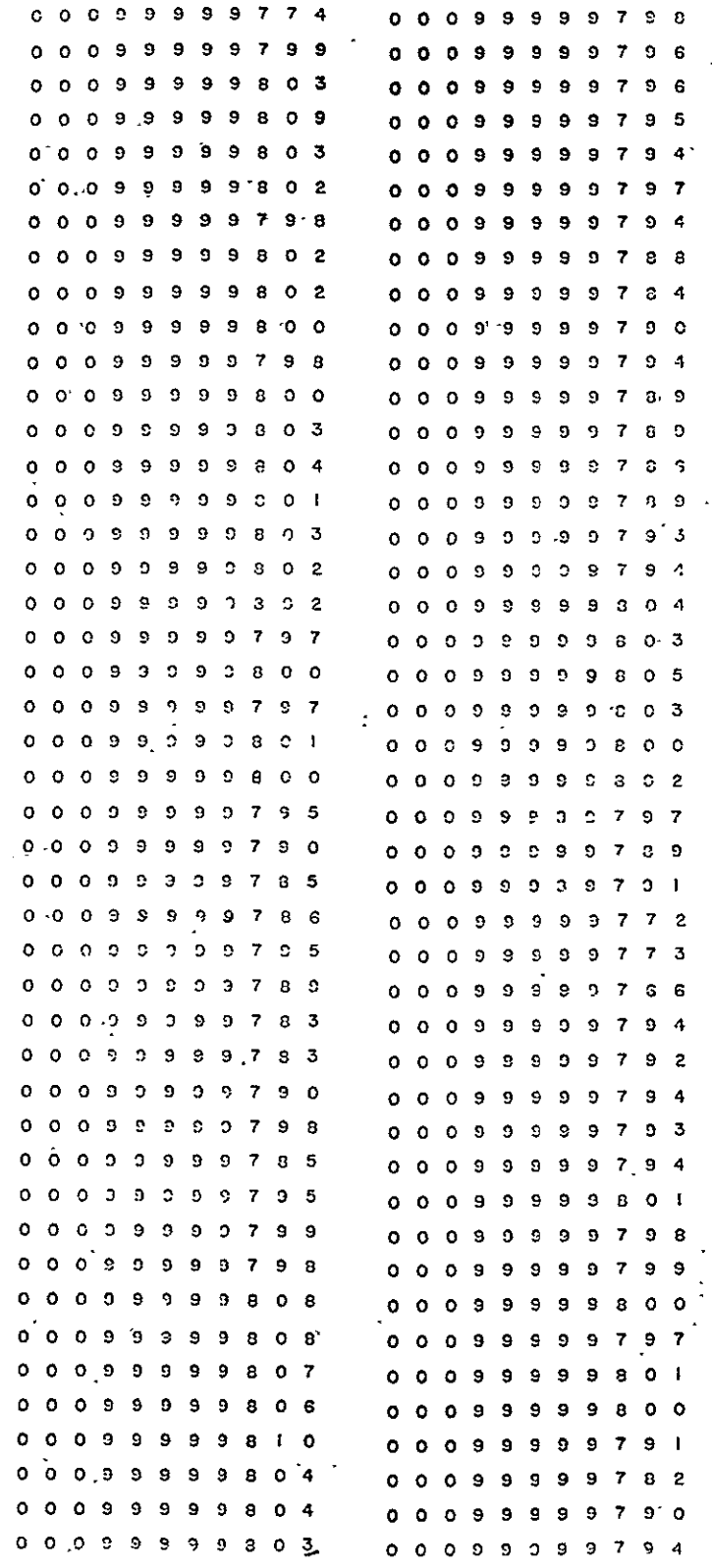


FIGURE 3-8. Frequency Stability Data

N71-32895

$$s = \sqrt{\frac{\sum_{i=1}^{n} (x_i - \bar{x})^2}{n-1}}$$

where: x_i = ith observation

$\bar{x}$ = mean

n = number of samples

We find that $\bar{x}$ is 79.6 Hz, $\Sigma(x_i - \bar{x})^2$ is 62 and s is calculated to be 0.8 Hz for this particular 15 minute random sample. The deviation is slightly in error due to rounding of the mean and square root calculations.

It should be noted that the crystal used for this data run had been aging for about a 6 month period. In addition, the sample was taken under essentially isothermal conditions. Further improvement on this oscillator circuit is necessary to achieve a consister 3 Hz mean drift for a 15 minute period.

3.2.1.2 Multiplier-Modulator

The operating operational sections in the multiplier-modulator subassembly is shown in Figure 3-4. The operational sections are: the multipliers, the premodulator linear amplifier, the phase-modulator and driver, the C+ control circuitry, and the postmodulator linear amplifiers.

The premodulator linear amplifier amplifies the final output frequency signal produced in the Class C multiplier and drives the

phase modulator. It is important that the premodulator linear amplifier maintains a constant driving impedance to the phase modulator in order to maintain the difference between the two-phase states within the proper bounds.

The postmodulator linear amplifier, Figure 3-4, provides a constant impedance load to the phase-modulator and provides power gain at the operating frequency. This section does not contain any tuning adjustments but is designed to be sufficiently narrow-band to provide additional harmonic rejection of the submultiple harmonic frequencies produced during multiplication.

The phase-modulator shifts the carrier into one of two-phase states that are different by 170 degrees (±5 degrees) dependent upon the data input from the digital control circuitry. To minimize common mode interference between the phase-modulator driver and the digital control circuitry, the data is transmitted from the latter to the former assembly, in balanced form, on a twisted pair of lines. The phase-modulator driver than converts the received signals to a current drive level required by the phase modulator.

The C+ control section is controlled by a warmup signal, originating in the digital section of the Data Collection Platform.

The warmup signal causes the C+ control circuitry to switch the A+ signal to the C+ line during the warmup and the transmit periods and thus activate Class A circuitry in the multiplier-modulator subassembly. The C+ signal also supplies power to the multipliers.

3.2.1.3 RF Amplifier

The operation of the mobile RF amplifier subassembly is shown in Figure 3-6 and the operation of the fixed RF amplifier is shown in Figure 3-7. The linear amplifier and the microelectronic broad UHF integrated circuit amplifier is common to the design of the mobile and the fixed platforms.

The line labeled C+ in Figures 3-6 and 3-7 supplies collector voltage to the linear amplifier during the warmup and the transmit period. The lines labeled TRANSMIT are enabled during the transmit period by the digital logic and allows the linear amplifier to drive the microelectronic broadband amplifier to the desired output level. Power to the broadband UHF amplifier, shown in Figure 3-6, is obtained from the prime power input line A+. No switching is provided in this line because the Class C circuitry does not draw current unless driven by the linear amplifier. Unfortunately, a small biasing current of 5 ma is drawn by the TRW Microelectronic Broadband Amplifier. However, TRW will bring the current drawing element to a separate external terminal so that it may be connected to the controlled C+ line.

However, the microelectronic units have to be driven from a 50-ohm generator if they are to remain stable. Since the narrow-band output circuitry of the linear amplifier preceding the TRW IC is 50 ohms, only at the operating frequency, some problems have been encountered in stabilizing the amplifier under phase modulation. The present solution is to provide excess gain in the linear amplifiers preceding the TRW module and use a 50-ohm pad to move effectively matched impedances between subassemblies. In this way, the linear amplifiers can be designed to assume a resistive 50-ohm driving impedance. TRW has been consulted and they have indicated that for any given linear driver, their broadband amplifier can be stabilized by changing the input matching configuration in the microelectronic amplifier.

The filter used at the output of the RF amplifier subassembly is a three-element reactive network of a low-pass form. This filter is used to reduce harmonics of the carrier only. If increased insertion loss is permitted, the number of elements in the filter can be increased and the harmonic rejection thus improved.

3.2.2 Device Selection

In the selection of devices for the oscillator subassembly, the devices were evaluated in terms of stability, gain, phase shift, noise figure, and cost. The specifications which were

instrumental in the selection of the particular devices are shown below:

40235

F_t	1 GHz
P_t	180 mw
V_{cbo}	45 v
I_c (Maximum)	50 ma

40673

P_t	330 mw
V_{ds}	20 v
I_c	50 ma
MAG (Maximum Available Gain)	20 dB

MC1550G

Y_{12}	0.001 mmhos
G_p (Power Gain)	30 dB
F_t	2 GHz
P_d	680 mw
V_{cc}	20 v

μA723

Average Temperature Coefficient	0.015 percent/^{o}C
Ripple Rejection	70 dB

μA723 (Cont.)

Line Regulation	0.01 percent v_{out}
Load Regulation	0.15 percent v_{out}
Overvoltage Protection	40 v

In the selection of devices for the mulitplier-modulator subassembly, the devices were evaluated in terms of stability, gain, phase shift, noise figure, and cost. The specifications which were instrumental in the selection of the particular devices are shown below:

40235

F_t	1 GHz
P_t	180 mw
V_{cbo}	45 v
I_c (Maximum)	50 ma

MPS-3638A

I_c (Maximum)	500 ma
V_{ce} (sat.)	0.25 v at 50 ma
h_{fe} (Minimum)	100 at 50 ma
P_t	310 mw
V_{ceo}	25 v DC
V_{eb} (Maximum)	4.0 v DC

Relcom M8E

Frequency	5 to 500 MHz
P_t	25 mw
I (Maximum)	25 ma

The selection of devices, for the RF amplifier subassembly, was made for stability, gain, pulsed performance, and cost. The specifications that were instrumental in the selection of the particular devices are shown below.

RCA 40235

F_t	1 GHz
P_t	180 mw
V_{cbo}	45 v
I_c (Maximum)	50 ma

Microelectronic Broadband UHF Amplifier, TRW MX 2.5

P_t	2.5 W min. at 12.6 v
G_p	21 dB min. (20 mw. max. input)
Efficiency	45 percent
VSWR	∞ at 15 v with filter
Operating Temperature Range	-30 degrees to +70 degrees C
Power Derating	2.0 dB max. from -30 degrees to +70 degrees C
Harmonic Rejection	-30 dB max.

Input Impedance	50 ohms
Output Impedance	50 ohms

Microelectronic Broadband UHF Amplifier, TRW MX 7.5

P_t	7.5 watts min. at 12.6 v
G_p	21.7 dB min. (50 mw. max. input)
Efficiency	45 percent
VSWR	∞ at 15 v with filter

3.2.3 Preferred Circuit Operation

3.2.3.1 Oscillator Buffer

The circuit of the oscillator and buffer of the Data Collection Platform is shown in Figure 3-10. The three interconnections are made from the A1 assembly to the oscillator-buffer subassembly. The B+ interconnection is terminal E1 to A1E15 (all interconnections shown on interwiring diagram, Figure 3-9); the RF interconnection is terminal E2 to A1E16, and the ground interconnection is terminal E3 to A1E17.

The B+ is regulated in a μA723 IC voltage regulator to 9 v. Short circuit and overvoltage protection is effected in this section by the selection of the resistive network of R1, R2, R3, and R4. Capacitor C1 is utilized for frequency compensation. Resistors R9, R10, and R11, and capacitors C3, C10, C17, and C18 comprise the decoupling network following the power supply.

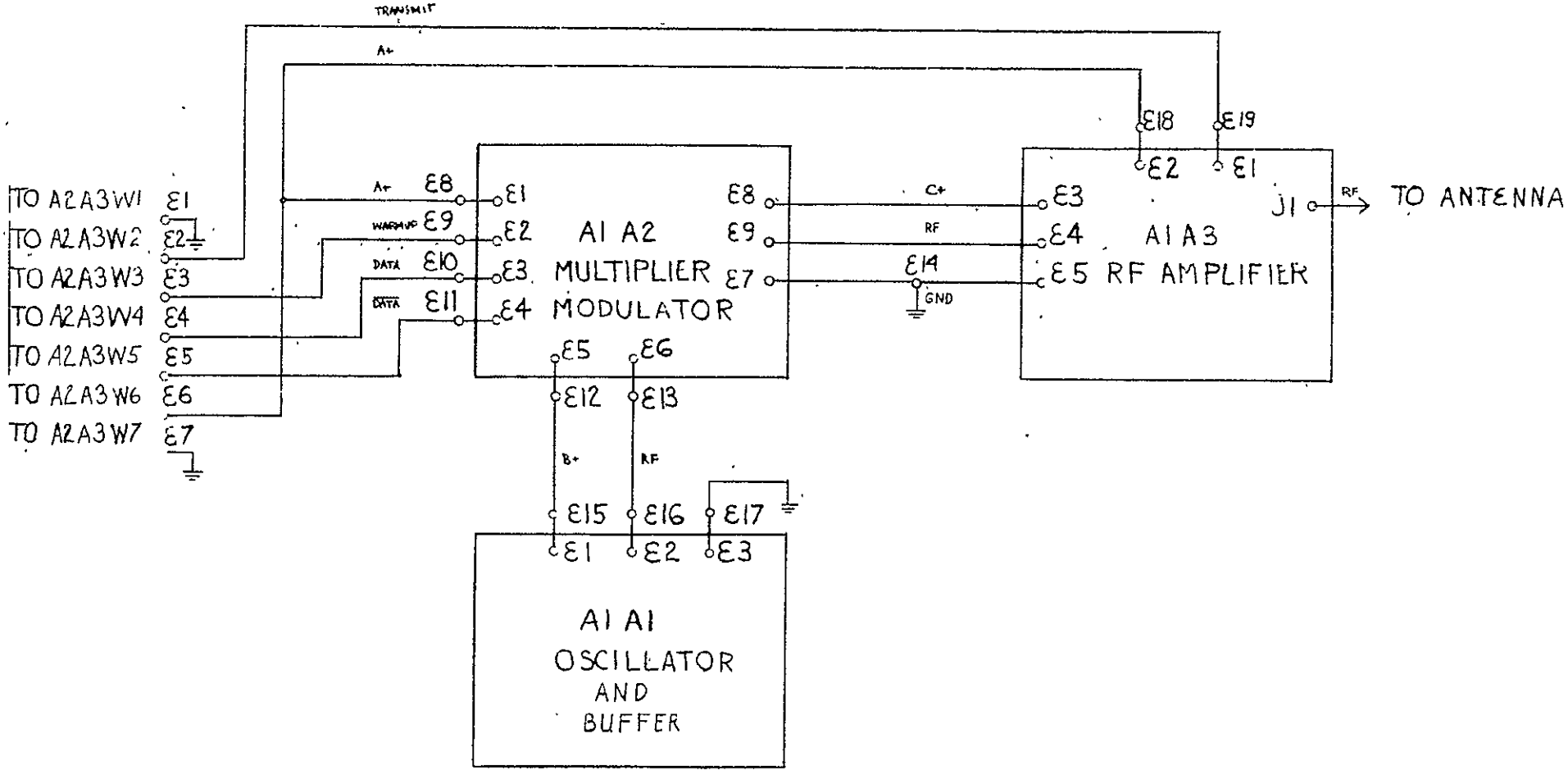


Figure 3-9. Transmitter (Dwg. No. 3050495)

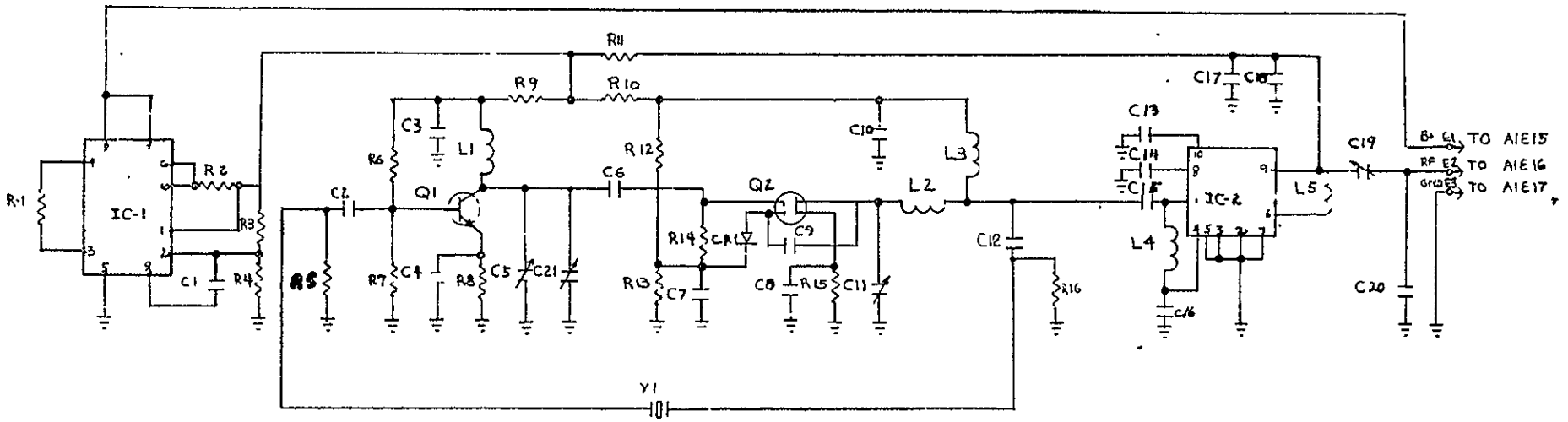


Figure 3-10. Oscillator and Buffer (Dwg. No. 3050494)

The oscillator loop is comprised of Q1, Q2, and the crystal Y1. Q1 is a NPN bipolar RCA 40235 in the common emitter configuration. This stage is essentially a narrowband amplifier. Q2 is a RCA 40673 MOS FET with internal transient and static protection utilized as a narrowband amplifier and limiter. R5 and R16 are shunt resistors that are properly chosen to lower the source and load impedance presented to the crystal.

The normal square law transfer characteristic of the MOS FET is nearly linearized by the negative feedback to gate 2 through C9. This stage provides limiting over a 30-dB range by clamping gate 2 to 0.4 v below the source. Negative signal excursions coupled through C9 will limit the gain of Q2 and provide limiting. Positive signal excursions exceediing 0.4 v will be shunted by CR1 and C7 to ground.

Q1 and Q2 have a minimum of 10 dB of excess gain at the crystal frequency. The AC signal amplitude at the drain of Q2 is designed to be 0.8 v peak-to-peak. When the oscillator loop is closed by inserting the crystal, the FET limiter stage automatically reduces its gain until the net gain around the loop is zero.

Since the input and output impedance is near 50 ohms, it is possible to characterize the part of the oscillator loop consisting of the amplifier and the limiter in terms of two port S parameters.

A set of parameters will completely characterize the amplifier and limiter for any given drive level, frequency, and temperature.

For oscillations to occur, it is necessary for the phase shift at the two terminals (defined by the crystal ports) to be zero at the series resonant frequency of the crystal. Furthermore, the above condition must be met when the amplifier and limiter operate at the same level of gain as the insertion loss of the crystal. If the amplifier and limiter are not to degradate the temperature coefficient of the crystal, it is necessary that the oscillator loop circuits be adjusted for zero phase shift over the 20 degrees C to 30 degrees C temperature range.

3.2.3.2 Multiplier-Modulator

The operation of the multiplier-modulator assembly is shown in Figure 3-11. The input power and control lines from the digital section for the subassembly are interconnected in the following manner: A+ on E1 to A1E8; warmup on E2 to A1E9; Data on E3 to A1E10; and Data on E4 to A1E11.

The interconnections between multiplier-modulator subassembly and the oscillator-buffer include: B+ E5 to A1E12, RF IN on E6 to A1E13, and GROUND on E7 to A1E14. The interconnections of A1A2 and the RF amplifier A1A3 include: C+ on E8 to A1A3E3, and RF OUT on E9 to A1A3E4.

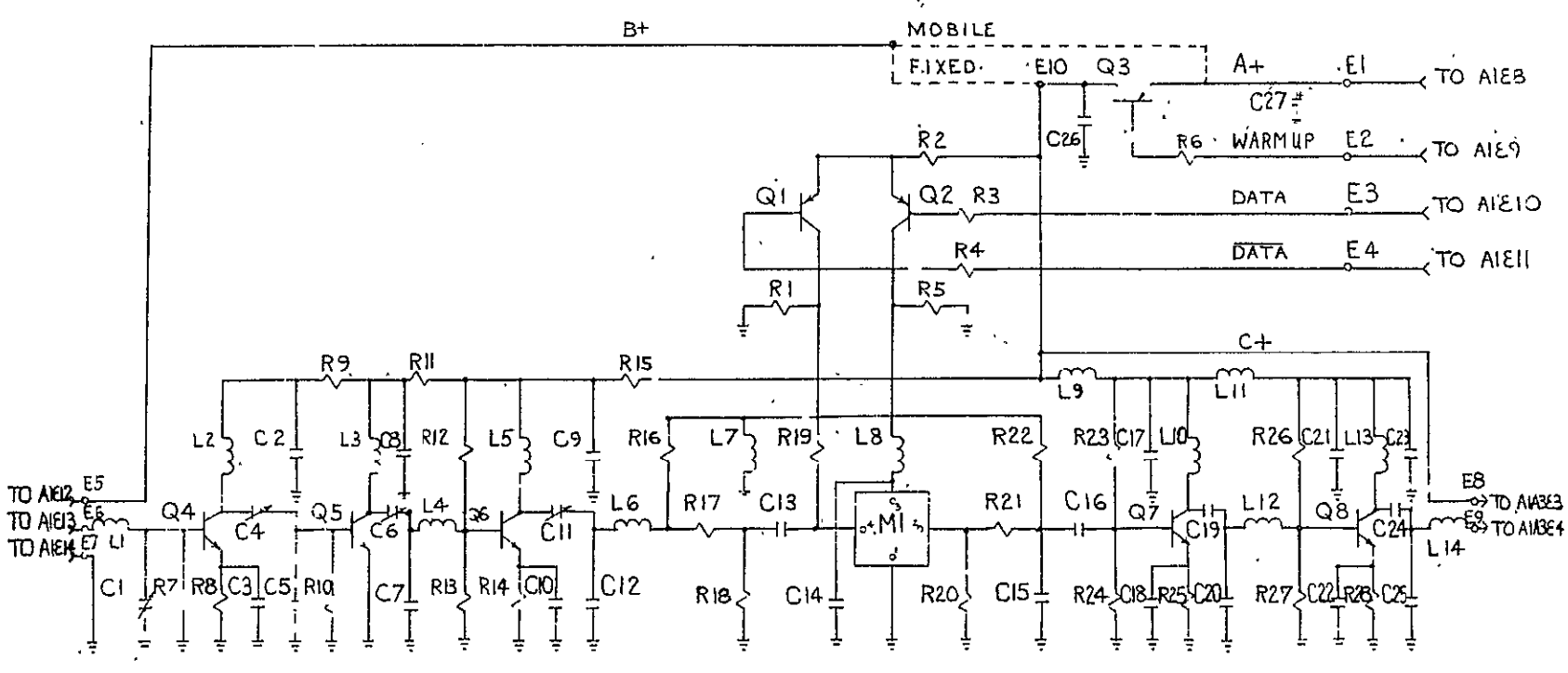


Figure 3-11. Multiplier/Modulator

The input signal to Q4 at 50.3875 MHz or 50.2625 MHz, mobile and fixed platforms, respectively, excites Q4 into Class C operation at a conduction angle optimum for 4th harmonic generation. The output matching circuit of Q4, consisting of L2, C5, and the variable capacitor C4, selectively matches the 4th harmonic into the base of Q5, in an analogous manner, doubles this signal and matches it into the base of Q6. C1, C4, C6, and C11 are tuned for minimum subharmonics.

Q6 is a narrowband common-emitter linear amplifier that simultaneously amplifies the 8th harmonic of the oscillator and provides buffering between the modulator and the Class C amplifiers. Decoupling is provided between Q4, Q5, and Q6 by RC filtering consisting of R9, R11, and R15, and C2, C8, and C9. Resistors were able to be used, rather than more expensive inductors, because of the very low current drain in the stages, and the low voltage sensitivities inherent in the design. This occurs because the stages were optimized first for harmonic rejection and secondly for power gain.

The input impedance at the node of R16, R17, and L6 and the output impedance at the node at R22, R21, C15, and C16 is 50 ohms. The incident power to the modulator from Q6 is split into two parallel channels by the resistive power divider, comprised of R16, R17, and R18, and recombined to form the input to Q7 by R20, R21, and R22.

The 90 degree phase shifter and attenuator in the upper channel is comprised of R16, L7, and R22. R16 and R22 are of equal resistance and much larger than the impedance of L7. This gives the large attenuation required and provides a 90 degree phase shift over a moderately large frequency range. The lower channel is comprised of a single-balanced mixer with the signal incidence on the IF port of the mixer. The biphase states are controlled by driving a set current through the local oscillator ports of the mixer. The differential pair comprised of Q1 and Q2 converts the balanced mixer input signal consisting of DATA to the level of balanced current drive needed by the biphase modulator in the lower channel.

The signal at the output of the modulator is fed through the DC blocking capacitor C16 to the base of Q7. Q7 and Q8 are broadband linear amplifiers in the common-emitter configuration that provide signal power gain at the final output frequency. The stages are biased at a level that causes each of the stages to exhibit an input impedance of nearly 50 ohms. L10, L12, C19, and C20 conjugatively match the collector impedance of Q7 to the base of Q8 and L13, L14, C24, and C25 conjugatively match the collector impedance of Q8 to 50 ohms.

DC control of the stages in the Data Collection Platform that draw quiescent power is obtained by gating the A+ line with a series pass PNP transistor, Q3. The C+ line supplies the modulator driver in the A1A3 subassembly. The B+ line has the option of being connected to the C+ line, and thus controlled by Q3, or of being connected directly to the A+ line.

3.2.3.3 RF Amplifier-Mobile

The schematic of the mobile RF subassembly of the Data Collection Platform is shown in Figure 3-12. The inputs to the subassembly are: A+ on E2 to A1E19; C+ on E3 to A1A2E8; TRANSMIT on E1 to A1E20; RF on E4 to A1A2E9; and GROUND on E5 to A1E18. The output is at the edge of the board on jack J1.

Q1 is a common-emitter linear amplifier that provides power gain. The base current, and hence the collector current is inhibited during the warmup period to keep the TRW amplifier (IC1) from operating. Capacitors C5 and C6 provide tuning of the stage into the 50-ohm pad formed by R4, R5, and R6.

IC1 amplifies the output signal; capacitor C7 is utilized to provide low-frequency filtering of the A+ line. The output of the module is then low-pass-filtered by L3, L4, and C8 to reduce the harmonics of the output signal.

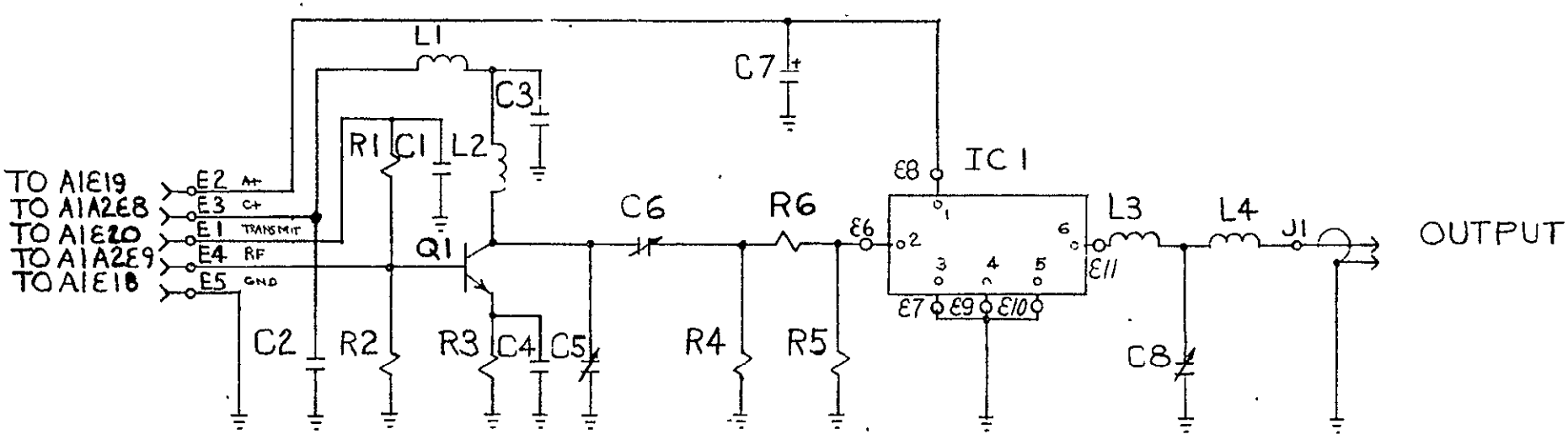


Figure 3-12. RF Amplifier, Mobile (Dwg. No. 3050492)

3.2.3.4 RF Amplifier-Fixed

The schematic of the fixed RF amplifier subassembly of the Data Collection Platform is shown in Figure 3-13. The input to the subassembly is A+ on terminal E2 to A1E19, C+ on terminal E3 to A1A2E8, TRANSMIT on terminal E1 to A1E20, RF on terminal E4 to A1A2E9, and GROUND on terminal E5 to A1E18. The final output signal emanates from J1.

Q1 is a common-emitter linear amplifier that provides power gain. The base current, and hence the collector current, is inhibited during the warmup period to keep the IC1 from operating. Capacitors C5 and C6 provide tuning of the stage into the 50-ohm pad formed by R4, R5, and R6.

The IC1 increases the power level of the output signal, capacitor C7 provides low-frequency filtering of the A+ line. The output of the module is then low-pass-filtered by L3, C4, and C8 to reduce the harmonics of the output signal.

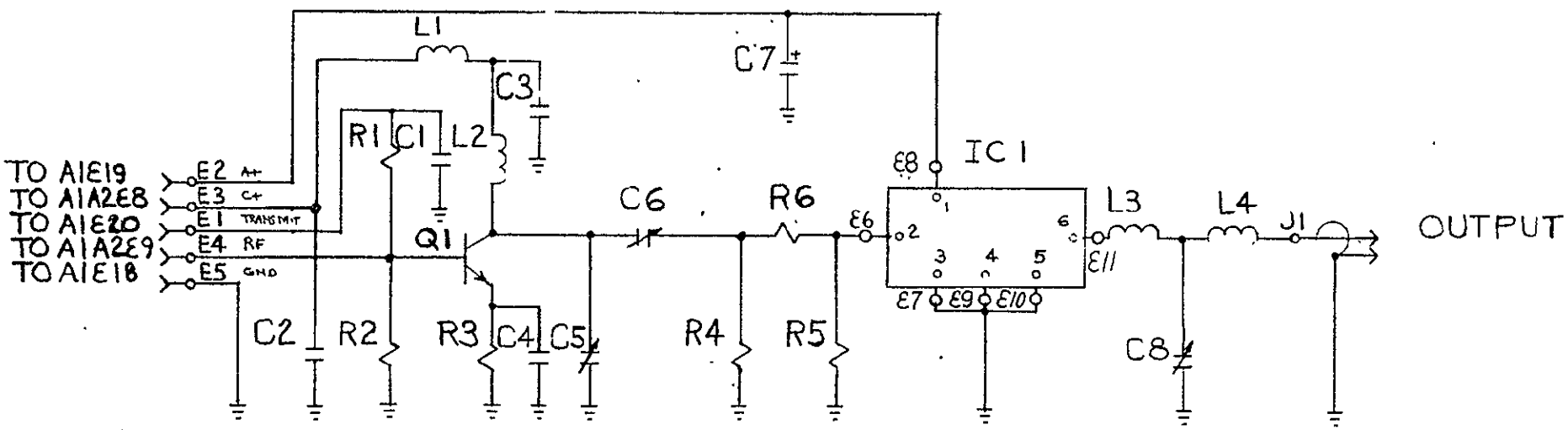


Figure 3-13. RF Amplifier, Fixed (Dwg. No. 3050492)

SECTION 4

PLATFORM DIGITAL LOGIC

4.1 GENERAL DESCRIPTION

The circuits and description for the mobile and fixed platforms are identical except as noted below.

TABLE 4-1. DIGITAL PLATFORM DIFFERENCES

PARAMETER	FIXED PLATFORM	MOBILE PLATFORM
Number of Sensor Inputs	8	3
Symbol Rate	1600 sym/sec	160 sym/sec
Repetition Rate	120 sec	60 sec

4.1.1 Circuitry

The purpose of the digital portion of the Data Collection Platform (Figure 4-1) is to monitor up to eight independent analog sensors, quantize the information, add an identification sequence, and in coded form, modulate the RF transmitter.

At the beginning of the transmission interval, the multiplexer begins sequencing through the eight sensor inputs. Each sensor input (Figure 4-2) is coupled to the A/D converter and the voltage presented there is converted to an 8-bit binary word. The A/D converter temporarily stores the binary word and shifts it out serially to the format switch. The format switch couples the first eight data words from the converter to the encoder. At the end of the data word interval, the signature word is coupled from the signature logic through the format switch to the encoder. The encoder processes the digital information and couples it to the transmitter through the output gating circuitry.

FOLDOUT FRAME 1

FOLDOUT FRAME 2

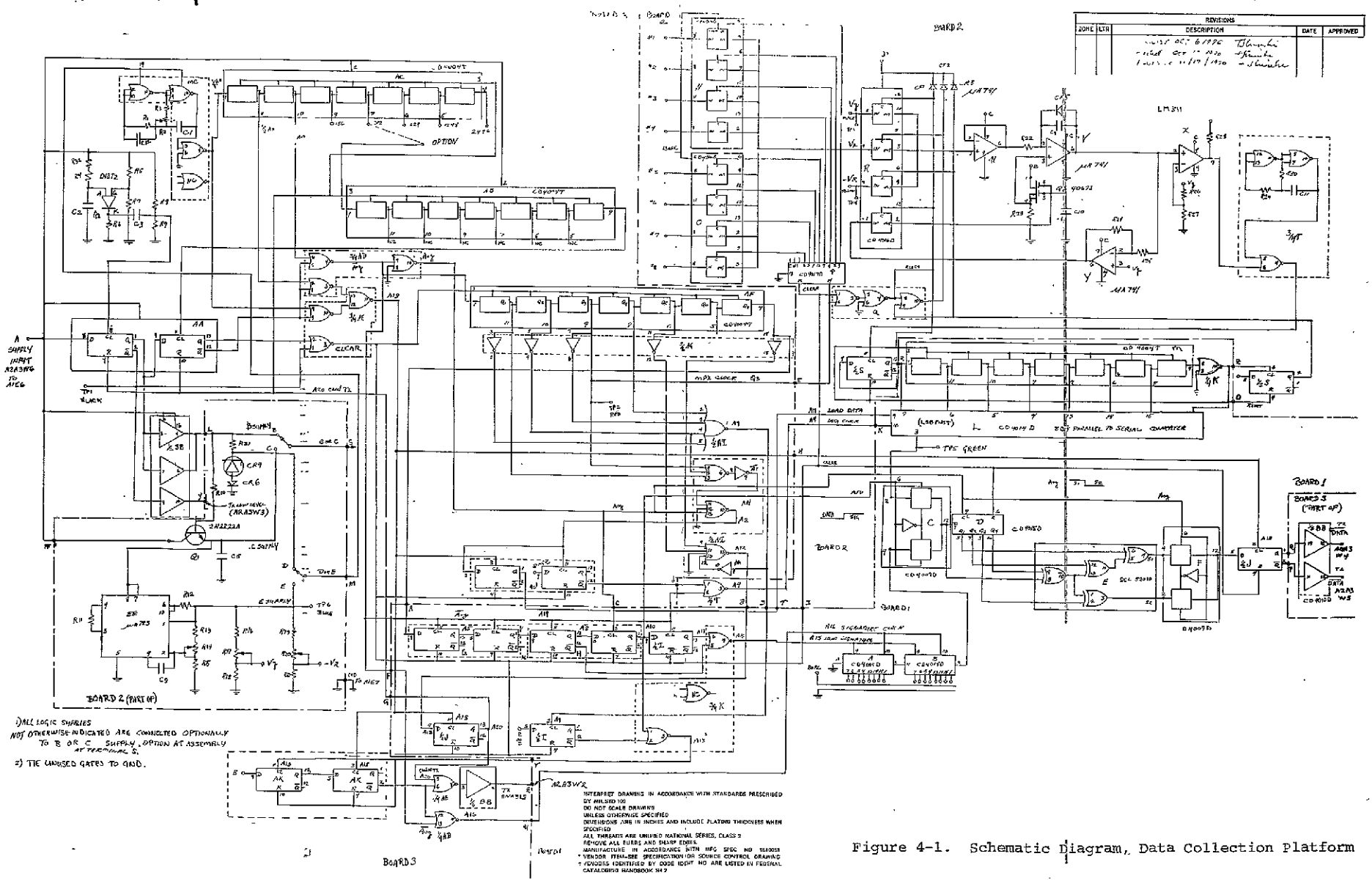


Figure 4-1. Schematic Diagram, Data Collection Platform

(Dwg. No. 4050849)

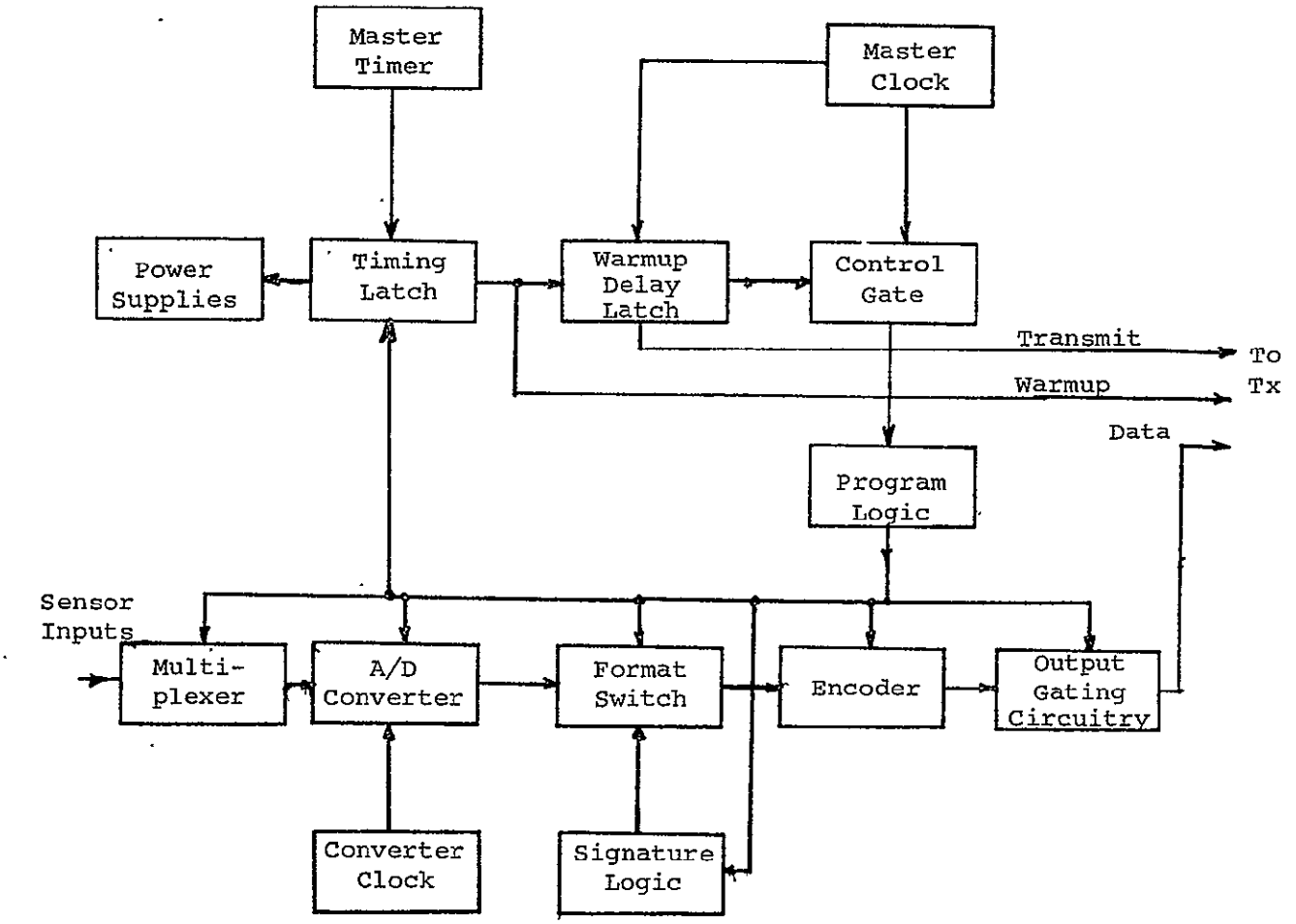


Figure 4-2. Data Collection Platform, Digital Logic, Block Diagram

4.1.2 Timing

The transmission-time format is divided into 80 bit-times. The first 64 bits are reserved for up to eight 8-bit data words. The next eleven bits are reserved for the identification sequence, and the last five bits are for the synchronization sequence. The mobile and fixed platforms are identical, except for clock rates, repetition interval, and number of sensor inputs.

4.1.2.1 Mobile Platform Timing

The mobile platform is required to have two sensor inputs. The last two words (bits 49 through 64) are reserved for these data channels. During the first 48 bit times, the RF transmitter output is unmodulated. The 80 bit-time data frame is one second in length. The mobile platform is timed to convert and transmit every 60 seconds as long as prime power is applied (Figure 4-3).

4.1.2.2 Fixed Platform Timing

The fixed platform is required to have eight sensor inputs. The first 64 bits contain the binary information for the eight channels monitored. Unlike the mobile platform, modulation of the fixed transmitter begins coincidentally with the beginning of transmission. The 80 bit data frame is 0.1 second in length. The fixed platform is timed to transmit every 120 seconds as long as prime power is applied (Figure 4-4). The time during which no transmission is made is known as the "quiescent period".

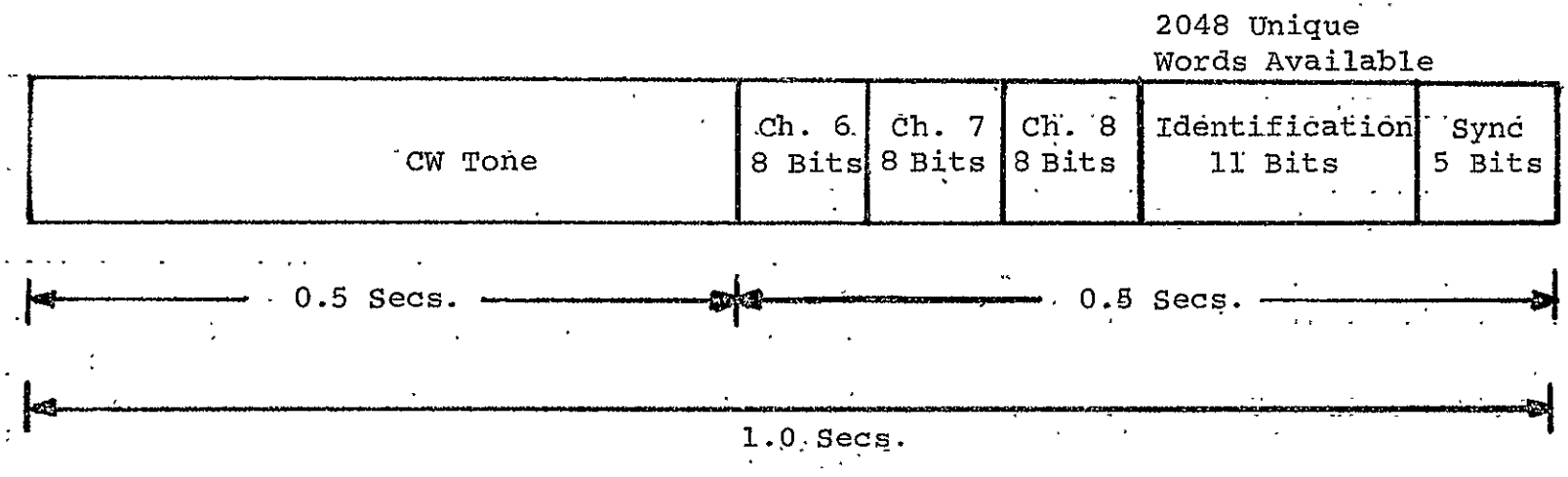


Figure 4-3. Data Frame Format, Mobile Platform

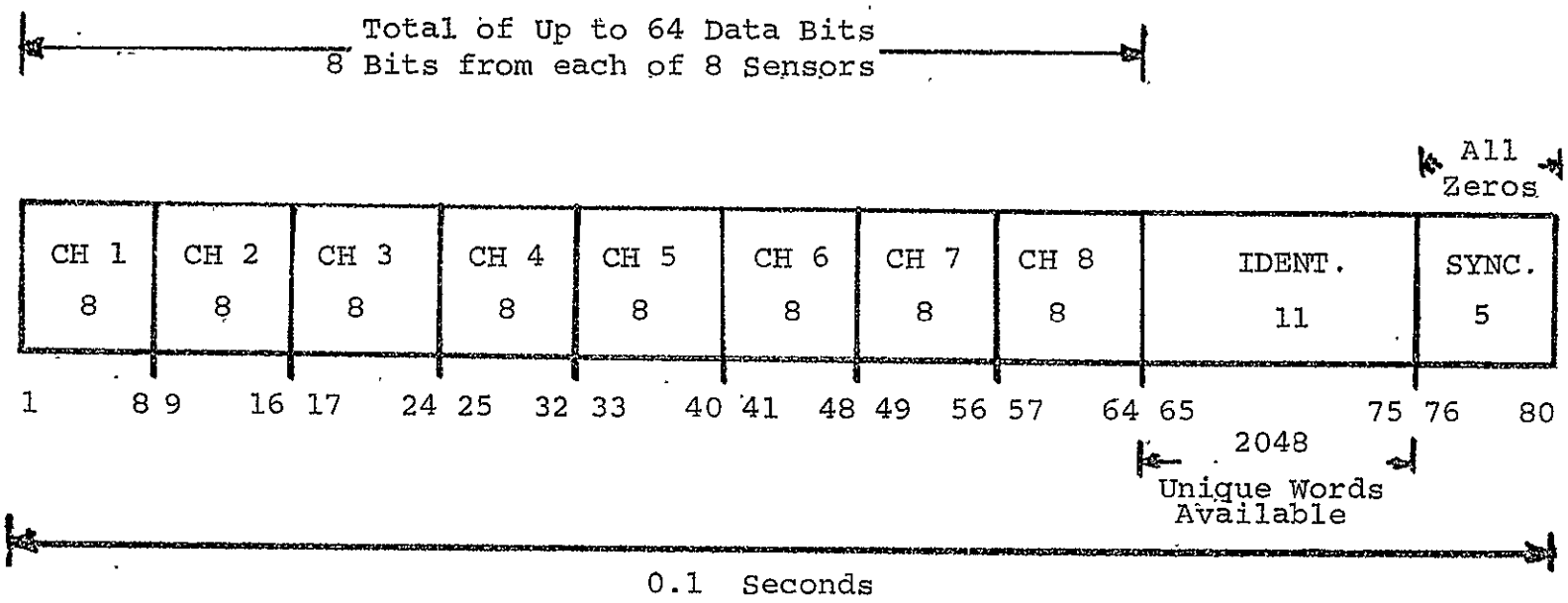


Figure 4-4. Message Format, Fixed Platform

4.2 DETAILED DESCRIPTION

4.2.1 Master Timer

Refer to schematic, Data Collection Platform, Figure 4-1.

The master timer is implemented using a programmable unijunction circuit. A programmable unijunction is used because of the design flexibility gained by using its programmable "trip point" characteristic. Transistor Q2 is a programmable unijunction whose trip point is determined by resistor dividers R5 and R7. Assuming a supply voltage of 12 volts, with R5 and R7 equal, the voltage at the gate of Q2 (voltage V_s in Figure 4-5) is six volts. Since the programmable unijunction is a negative resistance device, impedance from the anode to ground is initially high. C2 then charges at a rate determined by the value of C2 and resistor R4. When the voltage on the capacitor is equal to the gate voltage (V_s) plus the unijunctions threshold voltage (V_p-V_s) the anode to cathode impedance of the device becomes very low and capacitor C2 discharges through resistor R6. This produces a pulse approximately 6 volts in amplitude with a rise time of 75 microseconds and a duration of 500 microseconds. When the capacitor completely discharges, the impedance from the anode to the cathode again becomes high, C2 begins to recharge to resistor R4. Resistors

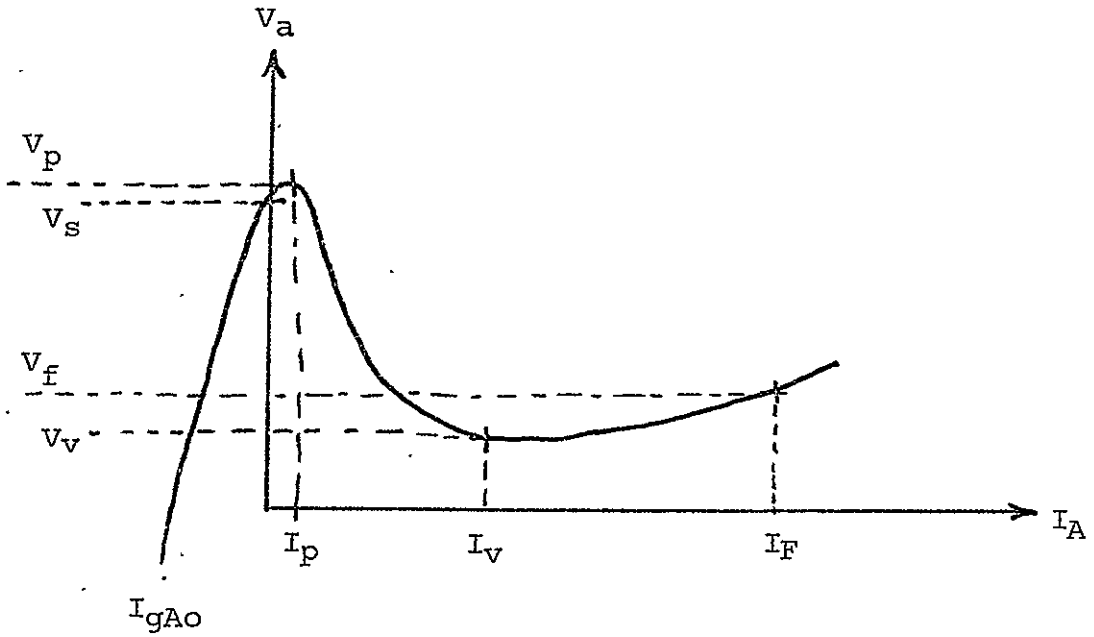


Figure 4-5. Programmable Unijunction, V_a, I_a Curve

R8 and R9 bias the input of the timing latch to insure that, for variations in the timing latch threshold voltage, the timing latch will always respond to the latching impulse from the master timer.

4.2.2 Timing Latch

At the platform repetition interval, the master timer supplies a latching pulse to the timing latch. The timing latch output goes high enabling the warmup delay circuitry, and in turn, the transmitter warmup circuitry and system power supplies. At the end of the conversion-transmission sequence, the program logic sends an "end of transmission" reset pulse to the timing latch (Figure 4-6).

The timing latch is a D type flip-flop. During the quiescent period the Q output (pin 1) is low and the $\overline{Q}$ output (pin 2) is high. The D input (pin 5) is always high. When a fast positive transition appears at pin 3 (the master timing pulse) the clock input, the level at pin D is transferred to the Q output of the D flip-flop. The Q output of the D flip-flop then goes high with the positive transition of the master timer output. The $\overline{Q}$ output goes low. The output of the timing latch remains in this state until a positive going pulse at pin 4 (end of transmission pulse) resets the flip-flop to its original quiescent state.

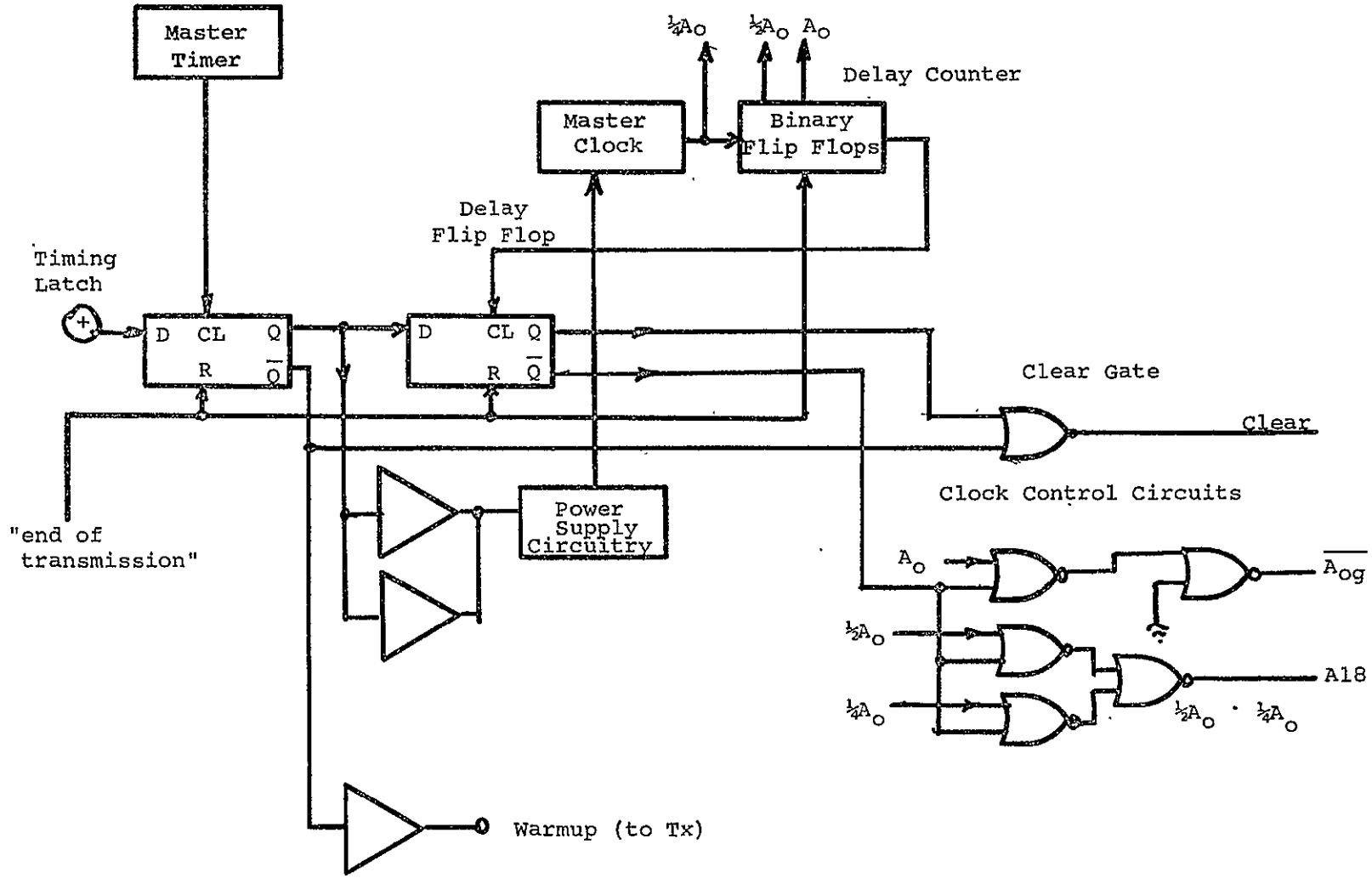


Figure 4-6. Timing Latch, Delay Latch, Clock Control, Clear Circuits, Schematic Diagram

The Q output of the timing latch is connected to the input gates of IC BB, a noninverting buffer circuit. Two stages of the buffer circuit are used in parallel to enable the power supply circuitry.

4.2.3 Warmup Delay Circuitry

The warmup delay circuitry (Figure 4-6) consists of a ripple counter and delay latch. The ripple counter is programmed to count a predetermined number of master clock alternations. At the end of the predetermined delay interval, the delay latch output enables the transmitter circuitry and clock control gate. The conversion-transmission sequence starts when the clock control gate is enabled. During the warmup delay time the "clear" logic supplies a clear signal to all functional and program logic (Figure 4-7).

When the timing latch Q output goes high (pin 1), the power supplies are turned on to enable the master clock. The high output of the timing latch is also presented to the D input of the warmup latch. At the "end of transmission" pulse, the output of the warmup latch (pin 13) was low. During the warmup interval, the master clock frequency is divided by the binary flip-flop integrated circuits AC and AB. When the output of the last binary flip-flop of integrated circuit AB (pin 4) goes high, the high level on the D input of the delay latch is transferred to the Q output of

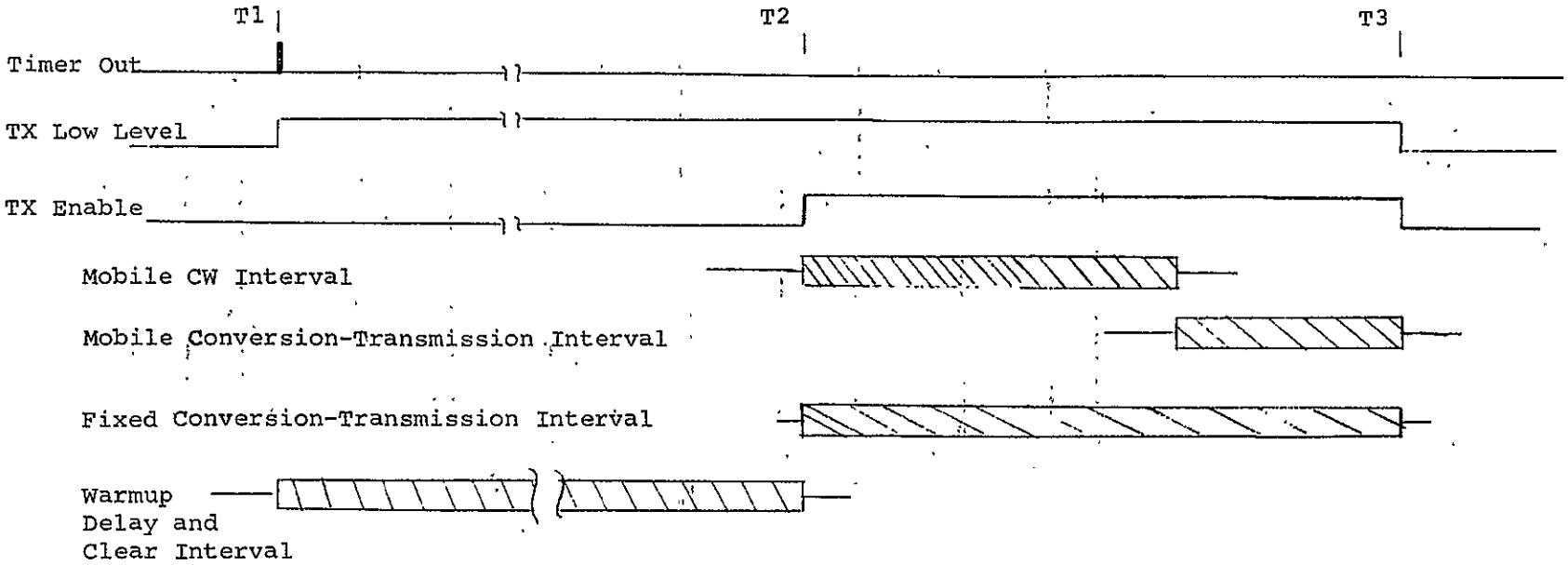


Figure 4-7. Data Collection Platform, Overall Timing Diagram

the delay latch (pin 13). The delay latch remains in this state until the "end of transmission" pulse resets it. The warmup delay options are shown in Table 4-2 for both the mobile and fixed platforms.

4.2.4 Control and Clear Gates

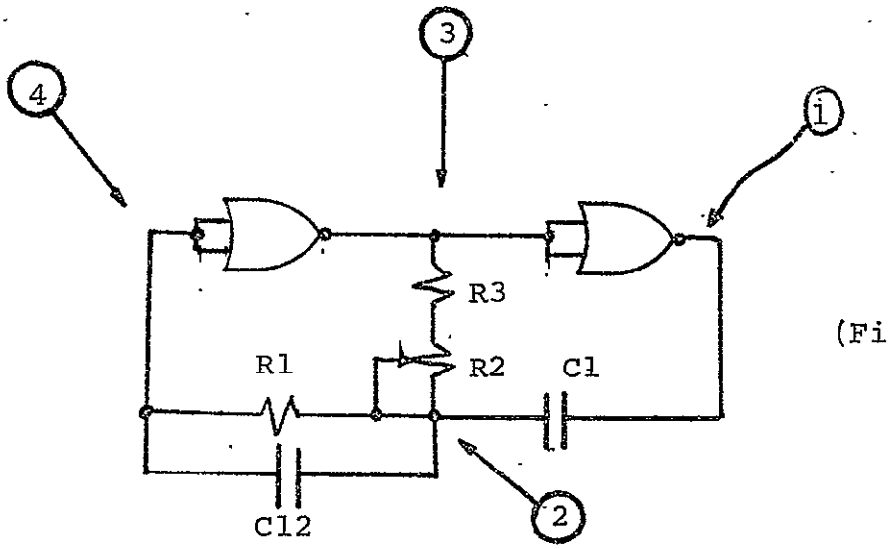
During the quiescent interval, pin 1 of the NOR clear gate is high, forcing the output of the clear gate to be low (Figures 4-6 and 4-7). When the timing latch is latched, the $\overline{Q}$ output of the timing latch goes low and pin 1 of the clear gate goes low. Pin 2 of the clear gate remains low and the output of the clear gate goes high. This high level on the output of the clear gate clears all functional and program logic during the warmup interval. After the warmup interval, the delay latch Q output goes high, forcing the clear gate output to go low. During the quiescent period, the system clock (A_{OG}) and the output gate clock (A18) are both forced to the high level. After the warmup delay, the high input on pins 5, 1, and 9 is removed to allow the system clock (A_{OG}) and the delaying clock (A18) to be enabled.

4.2.5 Master Clock

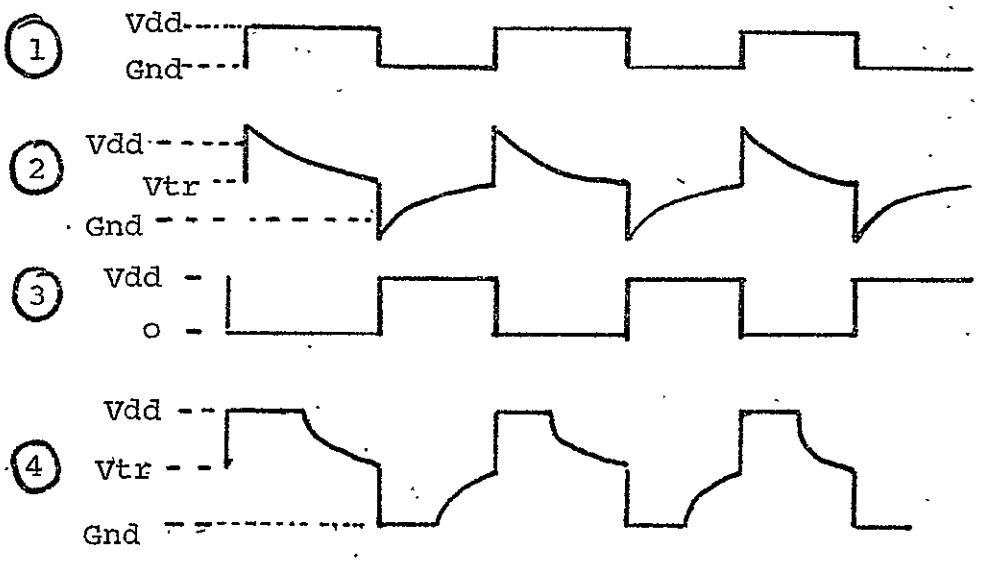
The master clock (Figure 4-8A), integrated circuit MC, is an astable multivibrator whose period is controlled by resistors R2,

TABLE 4-2. WARMUP DELAY OPTIONS

PIN	FIXED PLATFORM	MOBILE PLATFORM (sec)
9	156 msec	1.56
7	312 msec	3.12
6	624 msec	6.24
5	1.248 sec	12.48
4	2.496 sec	24.96



(Figure 4-8A.)



(Figure 4-8B.)

Figure 4-8. Timing Diagram for Master Clock

R3, and capacitor C1. Resistor R1 is used to negate the effect of supply variations on the astable multivibrator frequency. Capacitor C12 is used to improve the internal rise times and thereby improve the frequency stability. When the output of the astable multivibrator (pin 10) goes high, C1 must discharge through resistors R2 and R3 (Figure 4-8B). A high level at pin 10 implies a low level at pins 8 and 9. As long as the voltage at point 2 in the circuit remains above the threshold voltage of the gates connected to pins 12 and 13, the astable multivibrator remains at this state. When the capacitor discharges to a point below the threshold voltage, the input at pins 12 and 13 is effectively low causing the output to switch high. This forces the output at pin 10 to switch low and capacitor C1 must charge through resistors R2 and R3. When the voltage at point 2 reaches the threshold voltage of the gates connected to pins 12 and 13, the gate output (pin 11) switches low thereby completing one cycle. The master clock normally is highly independent of variations in the supply voltage. To increase the supply line immunity, the master clock uses the regulated 7.5 volt supply as prime power.

4.2.6 Power Supply Circuitry

Refer to the schematic, Figure 4-1.

At the beginning of the warmup period (when the timing latch Q output goes high) the output of the buffer output goes high and enables emitter follower Q1 and provides supply current to zener regulator CR4. The zener supply (called supply D) provides a regulated 10 volts to the converter multiplexer. CR6 is optional and provides the ability to change the output D supply voltage by ±0.7 volts as required by possible variations in the performance characteristics of the converter multiplexer and production variables in the zener regulator. The output of transistor Q1 is the C supply. When the C supply goes high, the 7.5 volt regulator, consisting of integrated circuit EE and its associated passive components, is enabled. The 7.5 volt supply is also called the E supply. When the E supply is enabled, resistor dividers R16, R17, R18, and R19, R20, R21 provide supplies V_g and $-V_R$, respectively (both are used in the A/D converter). Operation of the regulated supply (Figure 4-9) is as follows: The threshold integrated circuit μA723 consists of four sections. The first section, the voltage reference, is a buffer zener voltage whose zener is supplied with constant current source. The second section is a normal, single-ended operational amplifier with an inverting and non-inverting input. The third section is a current-limiting sensing transistor, the fourth, a series pass transistor. The operational

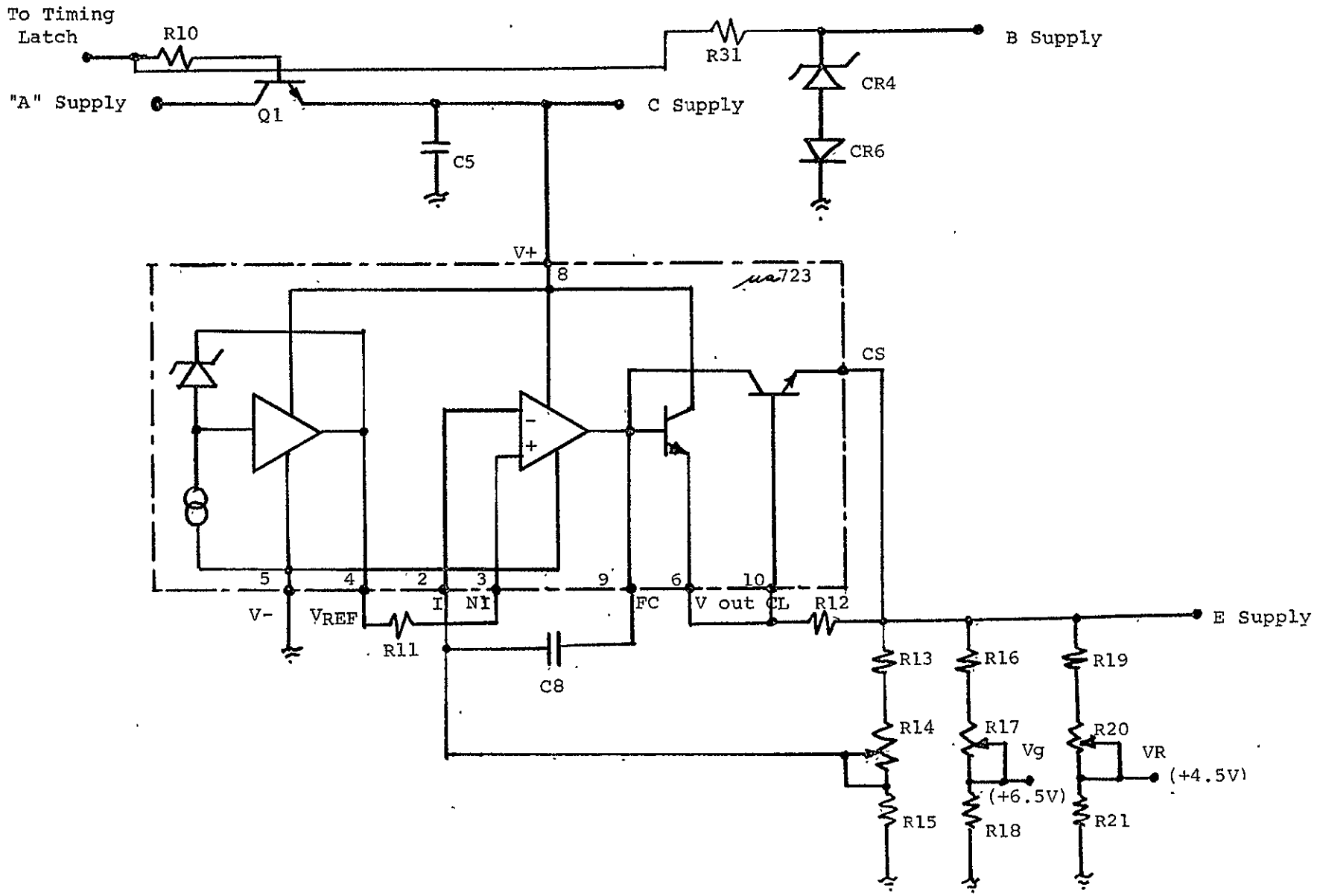


Figure 4-9. Power Supply, Schematic Diagram

amplifier compares the voltage on a range adjustment divider to the internal reference voltage. The range adjustment divider is supplied by the regulator output. The adjustment divider is supplied to the inverting input of the operational amplifier. If the regulator output voltage drops, the output of the operational amplifier increases thus increasing the drive to the series pass transistor, which in turn increases the current to the load to bring the supply voltage back to its original point. Resistor R12 is the current-limiting resistor. If the voltage across R12 increases to approximately 0.7 volts, the current-limiting transistor turns on and shunts the drive to the series pass transistor to the load. This effectively increases the internal impedance of the regulator and thereby decreases its ability to deliver the current at rated voltage. Resistor R11 is for temperature compensation, capacitor C8 is for frequency compensation.

4.2.7 Input Multiplexer

Refer to the schematic, Figure 4-1.

The analog input multiplexer consists of three integrated circuits, N. O, and P. Integrated circuits N and O are quad-transmission gates. A transmission gate is a parallel-complimentary pair offering a characteristic bidirectional low impedance from

input to output when the control input is high. When the control input is low, the input to output impedance is bidirectionally high. Integrated circuit P is a decade counter-divider. The multiplexer inputs 1 through 8 are sampled, in turn, by the action of the decade counter-divider on the quad-transmission gates. Each transmission gate amounts to a single-pole, single-throw switch controlled by the control input. For example, if the channel 1 control input (pin 5) is high, the signal analog input (pin 4) is connected to the signal analog output (pin 3). The output of all the quad-transmission gates are common. As each control input is turned on and the previous control input turned off, the respective gate samples the signal on its input and connects it to the common output. Only one output line of the decade counter is high at any time. When the clear input is high, pin 3 of the decade counter is set to high and channel 1 is sampled. After the clear signal is removed and the multiplex clock signal (Q3) goes high, the decade counter, output pin 3, goes low and output pin 2 goes high. After each positive transmission of the multiplex clock, the next succeeding output goes high and the previous output goes low.

4.2.8 Signature Logic

The data collection platform signature logic consists of two synchronous parallel input-serial output shift registers. The

first eleven parallel inputs are wired to a high or low line as required by the platform's identification. The last five lines are wired low for the synchronization code. Pin 3 of integrated circuit B is a serial output. After the "load signature" input goes high, the next positive transition of the signature clock gates the first parallel input to the serial output. At each successive positive transition of the signature clock (after the "load signature" signal has been removed), each successive parallel input is gated to the serial output.

4.2.9 Format Switch

The format switch (integrated circuit C) is similar in operation to the multiplexer transmission gates. With a low output on pin 6 of integrated circuit C, pin 2, the A/D converter serial output is connected to pin 12. With a high level on pin 6 of integrated circuit C, pin 4, the signature logic serial output is connected to pin 12 of the format switch.

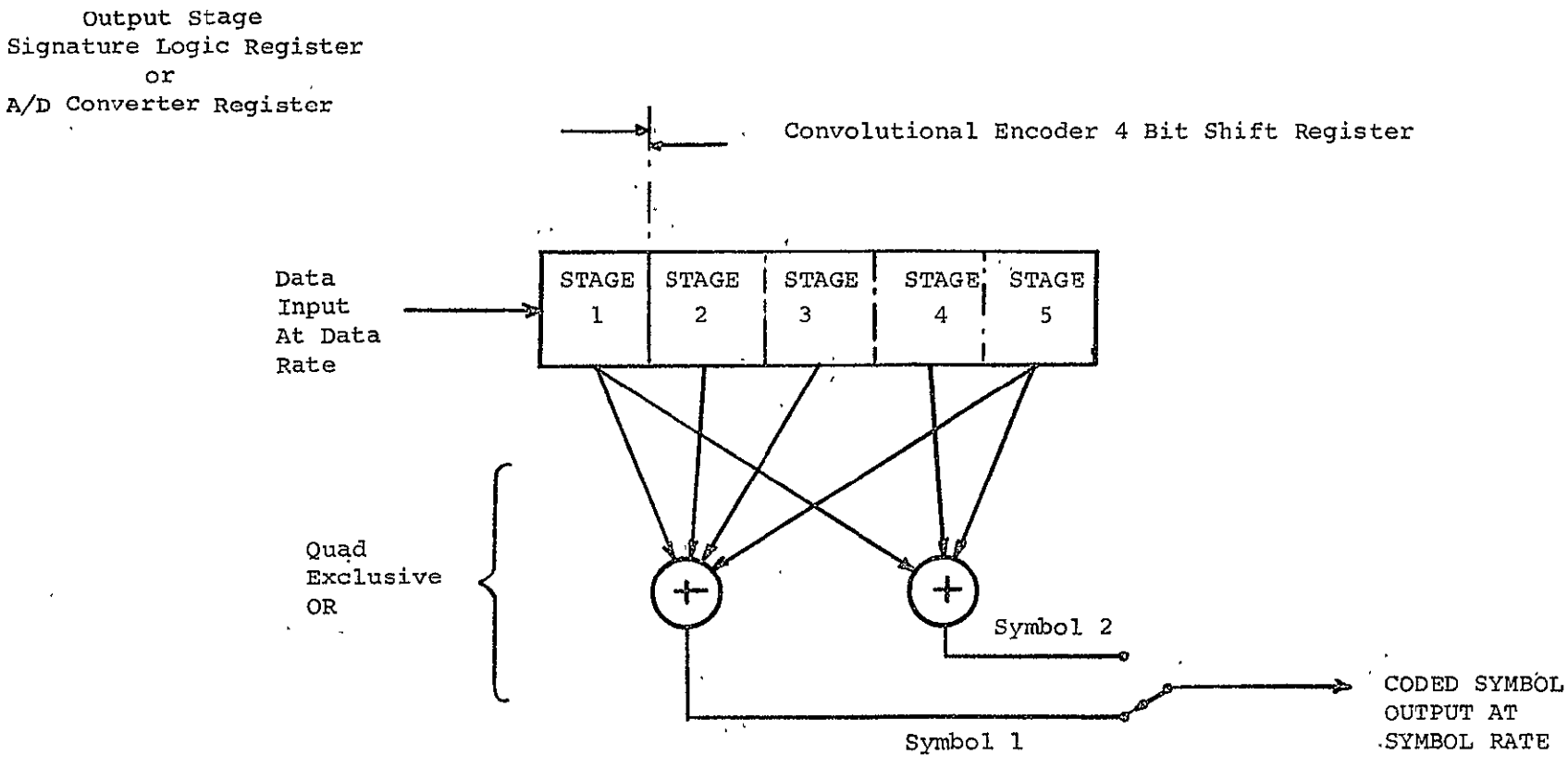
4.2.10 Convolutional Encoder

Three integrated circuits, integrated circuit D (a four-bit serial to parallel converter), integrated circuit E (a quad exclusive-or) and integrated circuit F (a single-pole, double-throw switch, identical to the format switch), comprise the convolutional type encoder. At each positive transistion of A_{OG} (the system clock), the data at the output of the format gate is shifted into

a four-bit register. At each positive transistion of the clock, the data is shifted to the right one bit. After four positive transitions of the system clock, the data that was presented at the output of the format gate will be presented at the last output of the shift register (Figure 4-10). The quad exclusive-or integrated circuit is wired so the output at pin 4 is the sum of the first, second, third, and fifth outputs of the serial-to-parallel converter. This output is entitled S1 for symbol 1. The second output at pin 3, entitled S2 for symbol 2, is the sum of the outputs from the shift register one, four, and five. At each clock period interval, first symbol 1 is presented at pin 12 of integrated circuit F, then symbol 2. Figure 4-11 shows, for a sample word, the input-output logic waveforms for the convolutional encoder group.

4.2.11 Output Gating Circuitry

Half of integrated circuit J, a D flip-flop, is used to delay the encoder output by 1/4 bit. Since A18 is coincident with no other transition, the Q outputs of integrated circuit J will not present false signal transitions. Two sections of integrated circuit DD, a hex buffer circuit, are used to buffer the digital collection platform logic from the transmitter section.



1st Output Symbol Summation = 11101

2nd Output Symbol Summation = 10011

Output symbol rate is twice data rate

Figure 4-10. Convolutional Encoder, Block Diagram

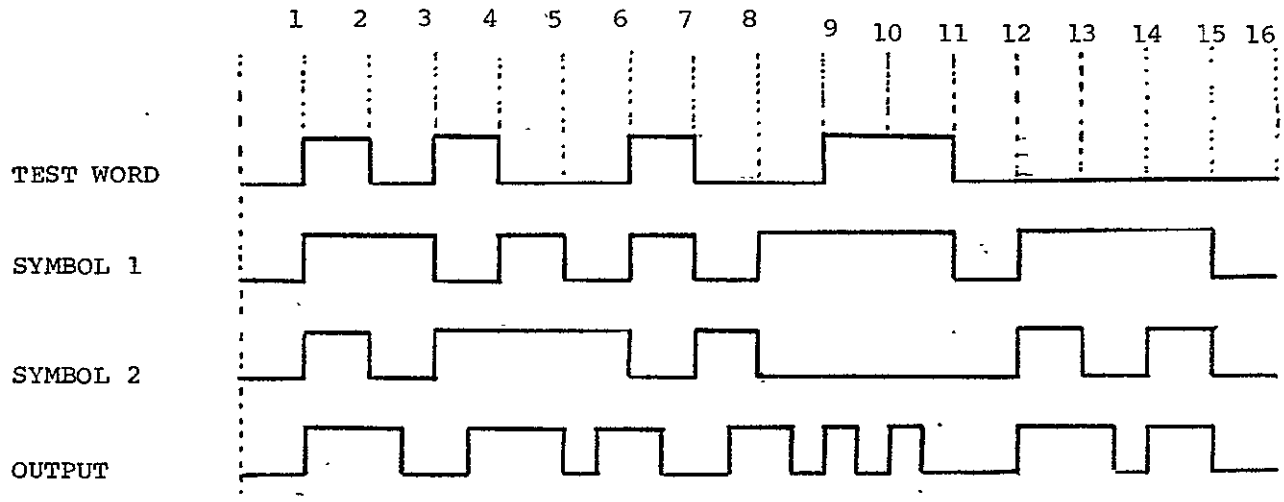


Figure 4-11. Convolutional Encoder Waveforms

4.2.12 A/D Converter

4.2.12.1 General

The A/D converter circuit (Figure 4-12) consists of a reference multiplexer, a voltage-follower buffer, an integrator stage, an analog comparator, an error offset-correction amplifier, an offset memory, a converter clock, a converter clock gate, a converter-counter, and a parallel-to-serial converter.

The "clear" and "multiplex clock" lines initiate the A/D conversion process.

At the end of the conversion cycle, the digital information stored in the counter is gated out in parallel form to a parallel-to-serial converter (IC-L) and in serial form to the format gate.

Four transmission gates are used in the A/D converter. A TG is a parallel complementary pair offering a characteristic bidirectional low impedance from input to output when the control input is high. When the control input is low, the input to output impedance is bidirectionally high. A transmission gate may be regarded as a SPST switch.

4.2.12.2 Reset

At time t_o (Figure 4-13C) the reset pulse goes high, causing TG_1 to turn on and TG_2 to turn off. The reset pulse also resets

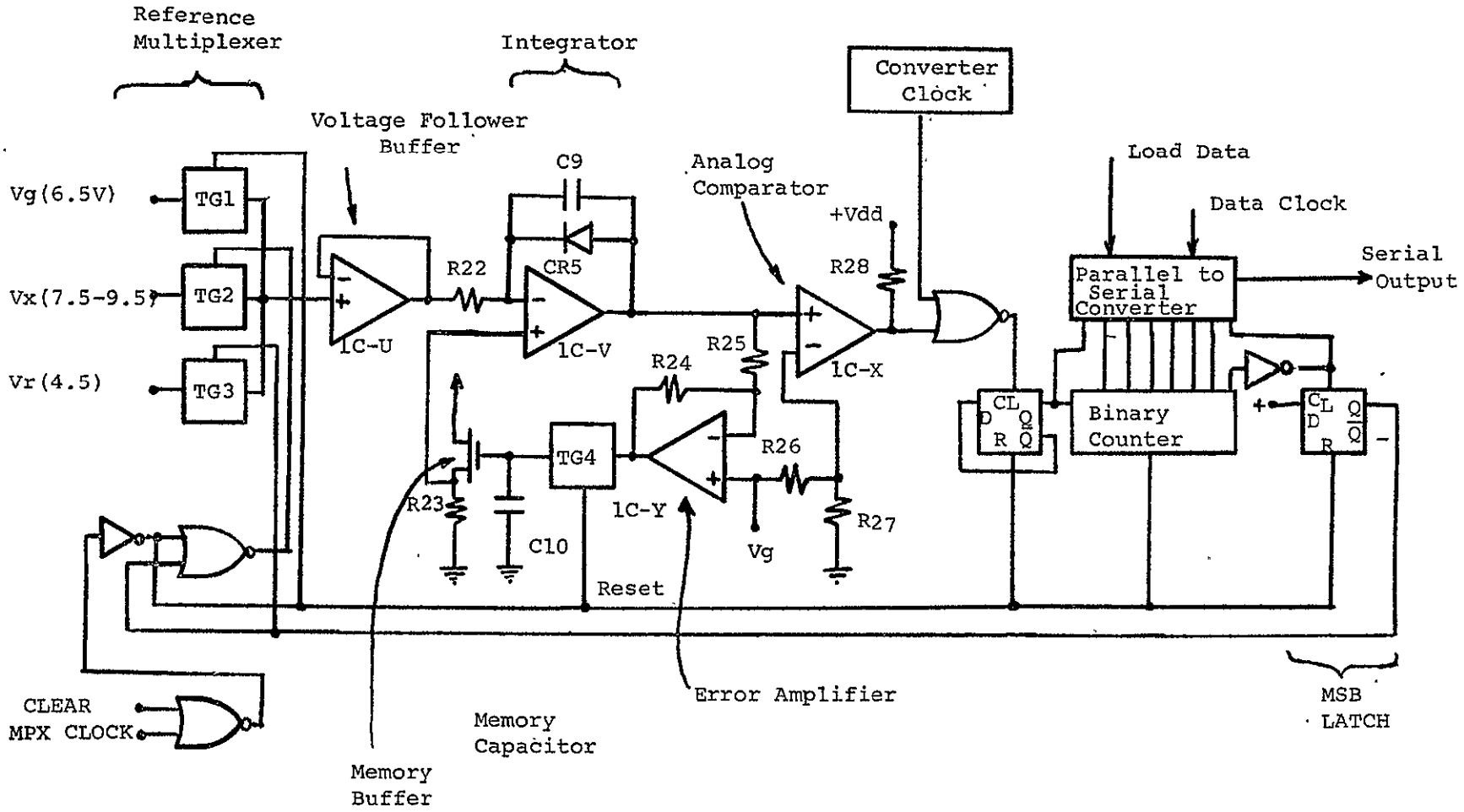


Figure 4-12. A/D Converter

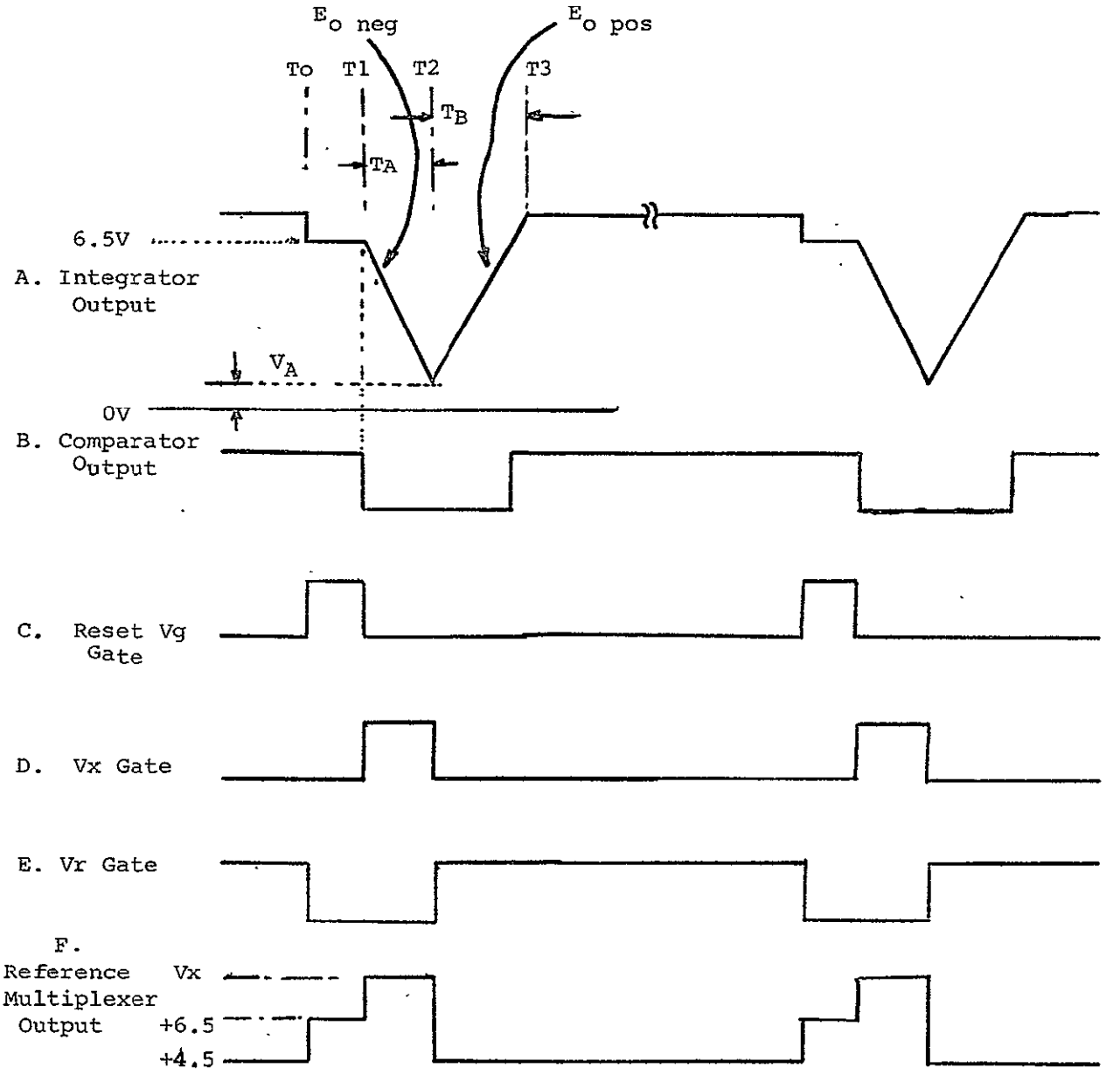


Figure 4-13. A/D Converter, Timing Diagram

the counter and D-type flip-flop latch outputs to go low. A low level on the latch output ensures TG_3 to be off. TG_4 is turned on by the reset pulse.

4.2.12.3 Offset Correction

During the reset interval, the offset correction circuit adjusts the integrator reference input (ICV-pin 3) so that the integrator output (Figure 4-13A) is the same as the integrator signal input (V_g = +6.5V).

If the integrator output is slightly higher than the reference input (V_g), the error amplifier output causes the memory capacitor C10 to discharge, bringing the integrator output back to V_g. (The buffer is a source follower.)

4.2.12.4 Integration of the Unknown (V_X)

At time T_1, the reset pulse goes off causing TG_1, TG_4 to turn off and TG_2 to turn on. The integrator signal input immediately jumps to V_X ($7.5 \leq V_X \leq 9.5$) and the integrator output generates a negative-going ramp. As soon as the ramp becomes less than the negative input of the analog comparator (which is slightly less than V_g), the output of the analog comparator becomes low (Figure 4-13B), enabling the counter control gate, allowing the counter to count the converter clock excursions. After 2^8 counter input excursions, the MSB output goes low, causing the Q output of the MSB latch flip-flop to go high (T_2).

4.2.12.5 Integration of the Reference (V_R)

When the MSB latch flip-flop goes high, TG_2 (Figure 4-13D) is turned off and TG_3 (Figure 4-13E) is turned on. The integrator signal input immediately jumps to V_R (V_R = +4.5v) (Figure 4-13F), and the integrator output begins to generate a positive-going ramp.

The ramp continues going positive until the integrator output is clamped to +7.2v. Before that time, at T_3, the integrator output passes the analog comparator negative input to cause the comparator output to go high and disable the counter input.

At this time, the digital information in the counter is ready to be sampled by the parallel-to-serial converter.

It can be seen that for greater values of the unknown (V_X), a longer time is required for the integrator output to reach the analog comparator negative reference input. This greater time allows more converter clock excursions to be counted by the counter. Therefore, for larger values of V_X, larger digital numbers are presented from the counter after conversion.

During the reset interval, the counter parallel output word is in the form 1000000. To get a parallel output word of all zeros, the A/D converter must integrate, and the counter must advance, until the MSB (most significant bit) becomes low. This will occur when the analog multiplexer input for the particular word-time is

exactly 7.5v (the lower end of the analog input range). This binary offset is used to avoid, at the analog comparator output, false gate transitions for low values of the unknown voltage (V_x).

The instantaneous output of the integrator for the negative slope (integration of V_x) is

$$\text{I.} \qquad E_{o\ neg} = V_g - \frac{V_x - V_g}{RC}\ t_A$$

where t_A is the elapsed time from t_1.

The instantaneous output of the integrator for the positive slope (Integration of Reference V_R) is

$$\text{II.} \qquad E_{o\ pos} = V_A - \frac{V_R - V_g}{RC}\ t_B$$

where t_B is the elapsed time from T_2, and V_A is the value of $E_{o\ neg}$ when $t_A = T_2 - T_1$

For the implementation of the A/D converter in the data collection platform, t_A is fixed by the number of clock excursions counted.

$t_A = 2^8 + 1\ (t_{cc})$ where t_{cc} is the converter clock period.

With V_g = +6.5V, and RC fixed, the value of V_A is dependent on the value of V_x, the unknown. I.e., the higher the value of V_x, the more negative the integrator output voltage is from V_g.

After the integration of the unknown (V_x), the reference multiplexer switches to V_R, the reference voltage, and the integrator output generates a positive slope until it reaches the comparator reference voltage (V_g). The positive slope is fixed because V_R and V_g are fixed, so at the end of the integration interval, t_b is directly related to the value of V_A. Rearranging equation II,

$$\text{III.} \quad t_b = \frac{-RC(V_g - V_A)}{V_R - V_g} \qquad (E_{o\ pos} = V_g)$$

If V_A is linearly dependent on V_x and t_b is linearly dependent on V_A, then t_b is linearly dependent on V_x.

4.2.13 Program Logic

4.2.13.1 General

The program logic consists of sequential and combinational logic providing control signals for the functional logic. The functional logic includes the multiplexor, the A/D converter, the format switch, the output gating circuitry, and the signature logic.

Table 4-3 shows the prime program logic output signals.

Immediately after the master timer initiates the warmup period, the clear line goes high to reset all digital logic and allow the A/D converter to make its offset correction.

At the end of the clear interval, the clear line goes low and the conversion-transmission sequence begins. (Figure 4-14, T=0)

TABLE 4-3. PROGRAM LOGIC OUTPUT SIGNALS

CODE		TITLE	FUNCTION	DERIVATION
Primary	A19	Load-Data	Transfers parallel data to parallel-to-serial converter	A2 delayed by A18
	A4	Data Clock	Shifts data serially from data converter	A_{og} after A2 positive transition
	Q3	MPX Clock	Resets A/D converter, advances input multiplexer	Binary counter output
	TX Enable	Transmit	Enables transmitter	Leading edge - A13 delayed by A18, trailing edge - A20 going high
	A20	End of Tx	Ends Tx-conversion cycle, returns system to quiescence	Delayed version of A12
	A16	Signature Clock	Shifts signature serially	$A_{og} \cdot$ A20
	A15	Load Signature	Transfers parallel signature to converter	Leading edge - A8, trailing edge - A17
	A10	Format Gate Control	Selects data or signature	Q17 delayed 3 Bits
	Clear	Clear	Resets all logic	
	A_{og}	System Clock	Basic transfer clock	$A_o \cdot \overline{\text{Clear}}$
	A18	Output Delay Clock	Delays "transmit" and "data" outputs to prevent trivial outputs	$1/2\ A_o \cdot 1/4\ A_o \cdot \overline{\text{Clear}}$
Secondary	A2			$A1 \cdot \overline{A_{og}}$
	A1			$\overline{Q1} \cdot Q2 \cdot \overline{Q3}$
	A13			A9 positive transition
	A9			$Q1 \cdot Q2 \cdot Q3 \cdot \overline{Q4}$
	A12			$A9 \cdot Q5 \cdot Q7$
	A8			Q7 delayed 2-1/2 Bits
	A17			Q7 delayed 3-1/2 Bits

4.2.13.2 Load Data (A19)

The binary counter IC-AF begins to count A_{og} alternations. At the end of the A/D conversion, a load-data pulse must be generated and data must begin shifting out serially to the encoder and transmitter.

One restraint on the data parallel-to-serial converter is that the first input bit will appear at the converter output synchronously with the positive edge of the clock if the load-data was high previous to the clock transition. In effect, then, the load-data pulse must overlap the positive clock transition corresponding to the first bit of the data word. A19 is generated (Figure 4-14, T1) when A18 delays A2 (D-type flip-flop 1/2 of IC-AV) which is the combination $A1 \cdot \overline{A_{og}}$. A1 is the combination $\overline{Q1} \cdot Q2 \cdot \overline{Q3}$

4.2.13.3 Data Clock (A4)

When A2 makes its first positive transition, the $\overline{Q}$ output of 1/2 of IC-AV, a D-type flip-flop, goes low enabling A4, the data clock, to follow the system clock.

4.2.13.4 Multiplex Clock (Q3)

The multiplex clock is generated directly by the binary counter. Each successive positive excursion of the multiplex clock advances the input multiplexer one step (Figure 4-14, T2). When

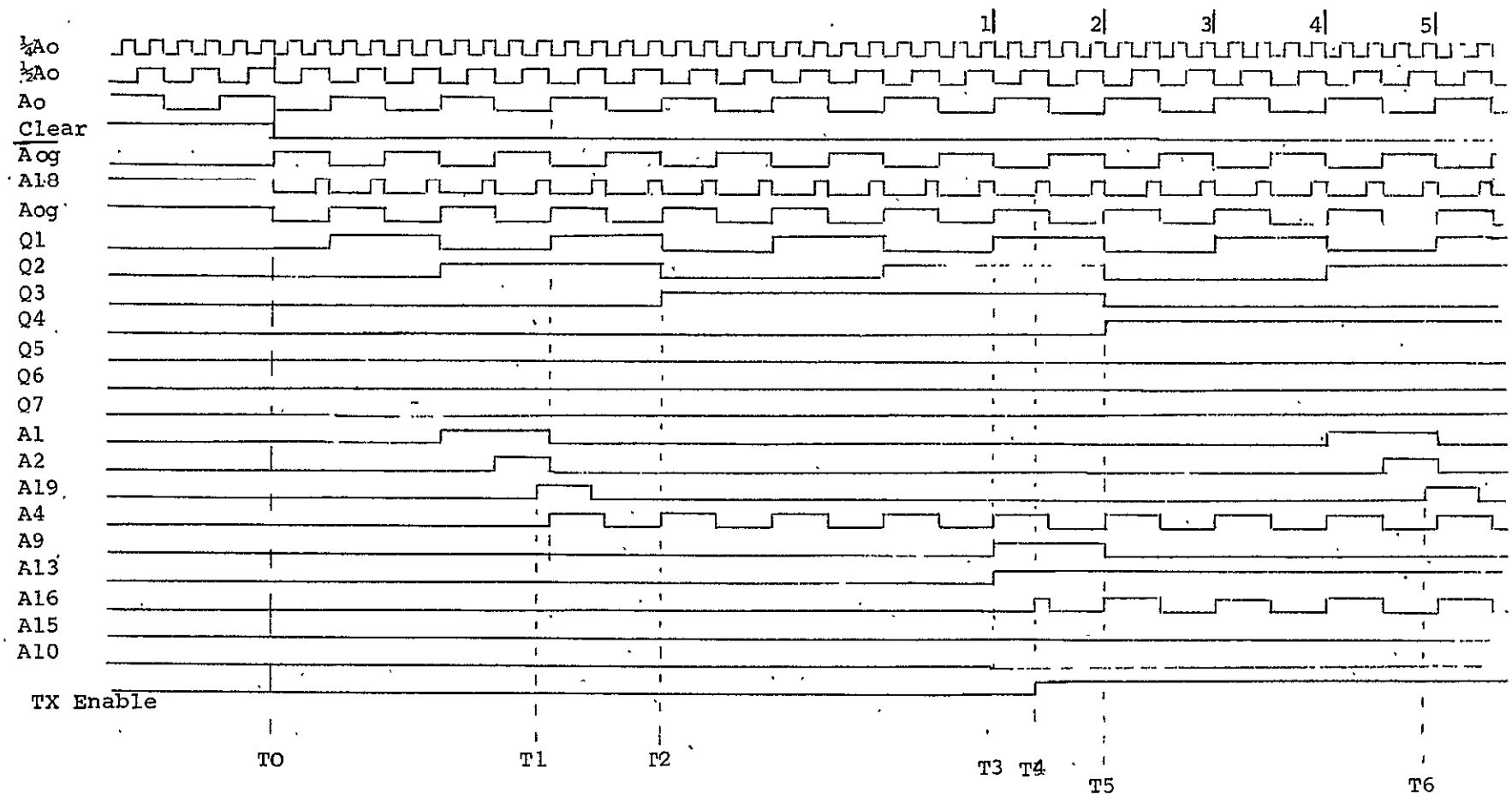


Figure 4-14. Data Collection Platform, Timing Diagram (1st 5 Bits - Post Clear)

Q3 is high (Figure 4-14, T2 to T5), the A/D converter is reset. When Q3 again goes low, the conversion process starts again.

4.2.13.5 Transmit (Tx) Enable

Due to the 5 bit delay incurred in the encoder shift register, the transmit enable signal is delayed 5 bits (Figure 4-14, T4). Tx enable is delayed additionally (less than one bit) by A18, the output delay clock. The positive edge of the Tx enable signal is coincident with the positive edge of the output delay clock (A18). A18 also delays the DATA and $\overline{\text{DATA}}$ lines, so that the first data bit is coincident with the leading edge of transmit enable.

The leading edge of Tx enable is a delayed version of the leading edge of A13. A13 is transmitted to 1/2 of the D type flip-flop IC-AK (pin 11), causing its Q output to latch high. A13 is derived when the $\overline{Q}$ output of IC-I (pin 2) is latched low. It is latched low by the positive transition of A9. A9 is the product of Q1, Q2, Q3, and $\overline{Q4}$. The output of the Tx-enable gate (IC-AE, pin 4) is forced low (Figure 4-15, T3) when A20 "end of Tx" goes high, thereby forcing Tx-enable low, ending transmission. A20 is a delayed version of A12 (Figure 4-15, T2).

In Figure 4-14, the numerals above 1/4 A_o indicate which bit of the first data word is being presented to the data output delay

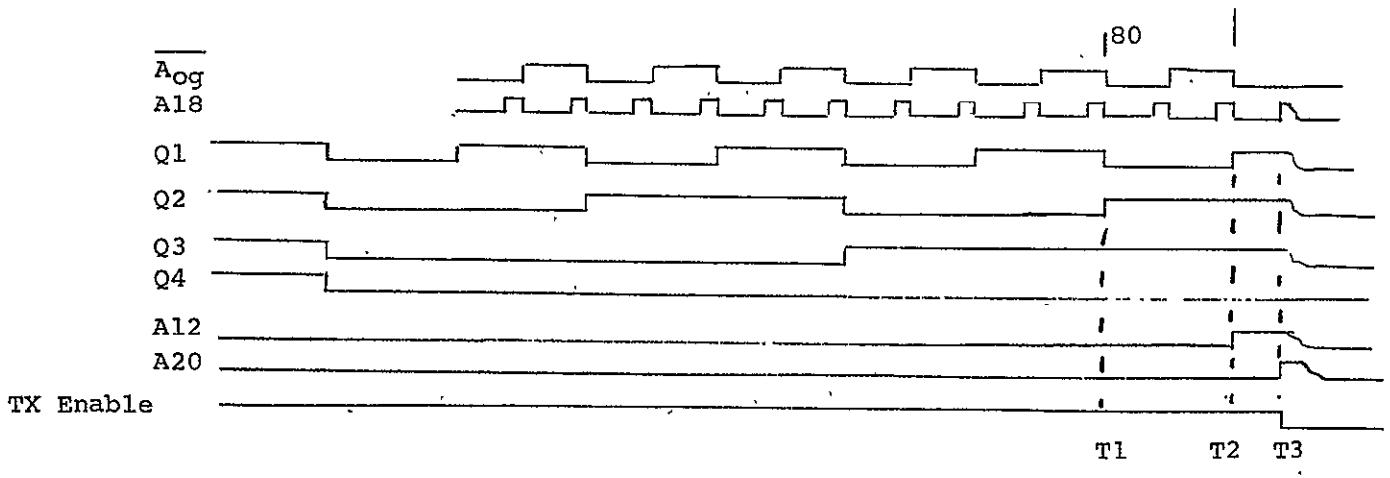


Figure 4-15. Data Collection Platform, Timing Diagram (End of Sequence)

circuit. The beginning of the LSB (Least Significant Bit) is indicated by numeral 1.

4.2.13.6 Signature Clock (A16)

The signature clock begins to function before the signature load pulse in order to clear the signature register. It is the product of A_{og} and A20. At bit-time 61 (Figure 4-16, T3) the FORMAT SWITCH connects the signature register to the encoder. Prior to that time (Figure 4-16, T2) A15, the signature load, went high. It remains high until after (Figure 4-16, T4) the next positive transition of the signature clock (coincident with the positive transition of A10). At T3, the first bit of the signature is presented to the encoder input.

4.2.13.7 Load Signature (A15) and Format Gate Control (A10)

Five D-type flip-flops, IC's G, H and 1/2 I comprise a shift register to delay the positive transition of Q7 in order to generate A15, the load signature pulse and A10, the format gate.

At the first positive transition of $\overline{A_{og}}$ after Q7 goes positive, the output of the first D flip-flop, A5 goes positive. At the third positive transition of $\overline{A_{og}}$, the output of the third D flip-flop, A8, goes positive. The complement of A8 normally forces the load signature (A15) gate (IC-K pin 4) low. When A8 goes high, the complement goes low and A15 goes high.

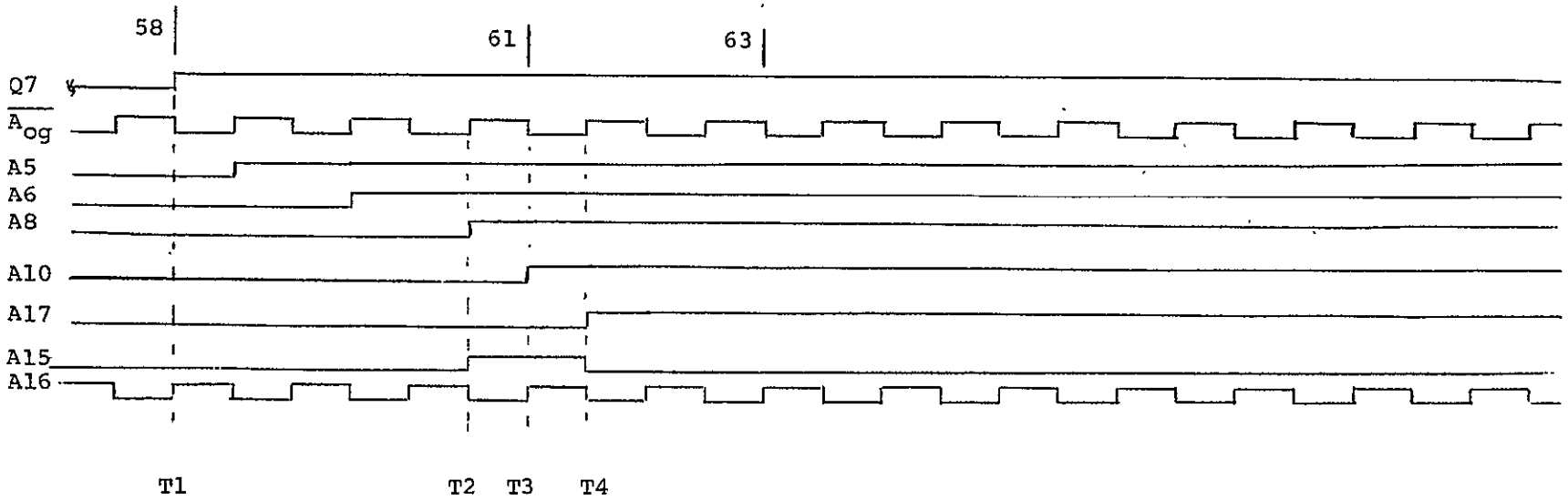


Figure 4-16. Data Collection Platform, Timing Diagram
(Bits 58-63, A10 Generation)

At the next negative transition of $\overline{A_{og}}$ (coincident with the positive transition of $\overline{A_{og}}$) the output of the fourth D flip-flop goes positive. This output is A10, the format gate control. At the next positive transition of $\overline{A_{og}}$, the output of the fifth D flip-flop (A17) goes positive, forcing A15, the load signature to zero.

SECTION 5

EQUIPMENT

5.1 MANUFACTURING AND PACKAGING TECHNIQUES

5.1.1 Logic Section

The logic section is comprised of three printed circuit boards 3 x 5 in. disposed in parallel vertical planes with the long dimension in the vertical axis (Figure 5-1).

Interboard connections are made at the top edges by means of flexible leads (Figure 5-2). To facilitate assembly and servicing, individual board layout was planned so that there would be no crossover of interboard connections.

All adjustments and test points are located close to the board edges for accessibility during operation.

The boards are double copper clad with plated-through holes to achieve intraboard connections between opposite sides of each board. Line width and space between lines is fifty mills (0.050 in.), which is more than adequate for the currents involved for circuit operation.

Optional jumper connections have been provided for the signature function and timing.

Sensor input connection points and primary power supply input are located at the bottom edges of the boards, which is also the bottom of the entire package.

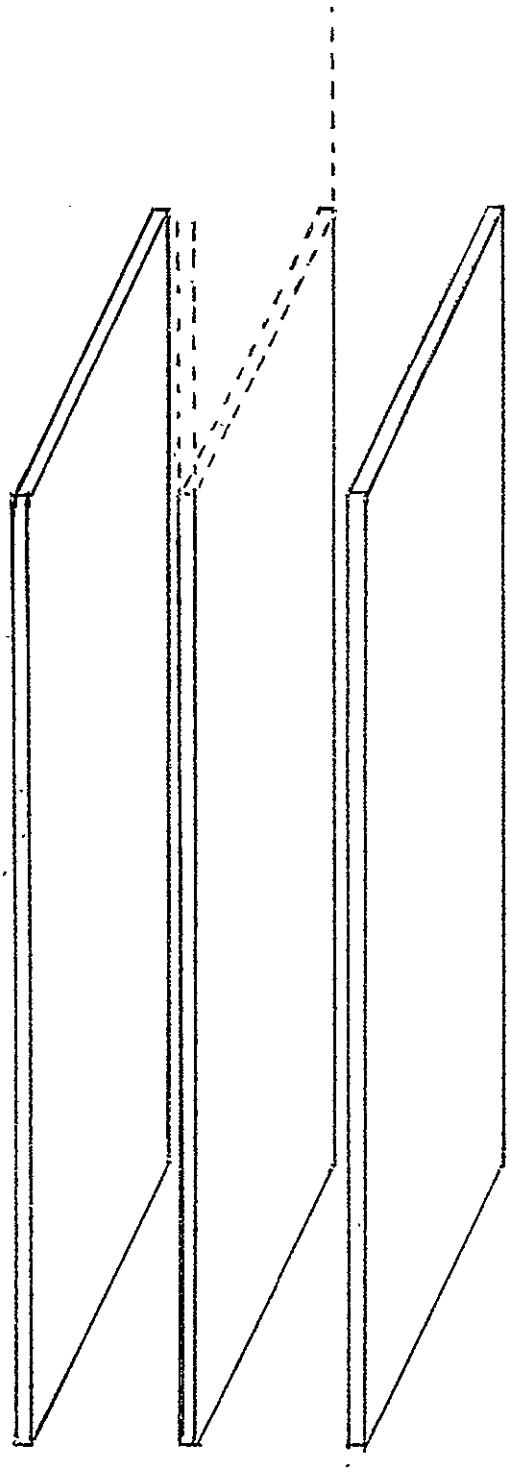


Figure 5-1. Disposition of Logic Boards

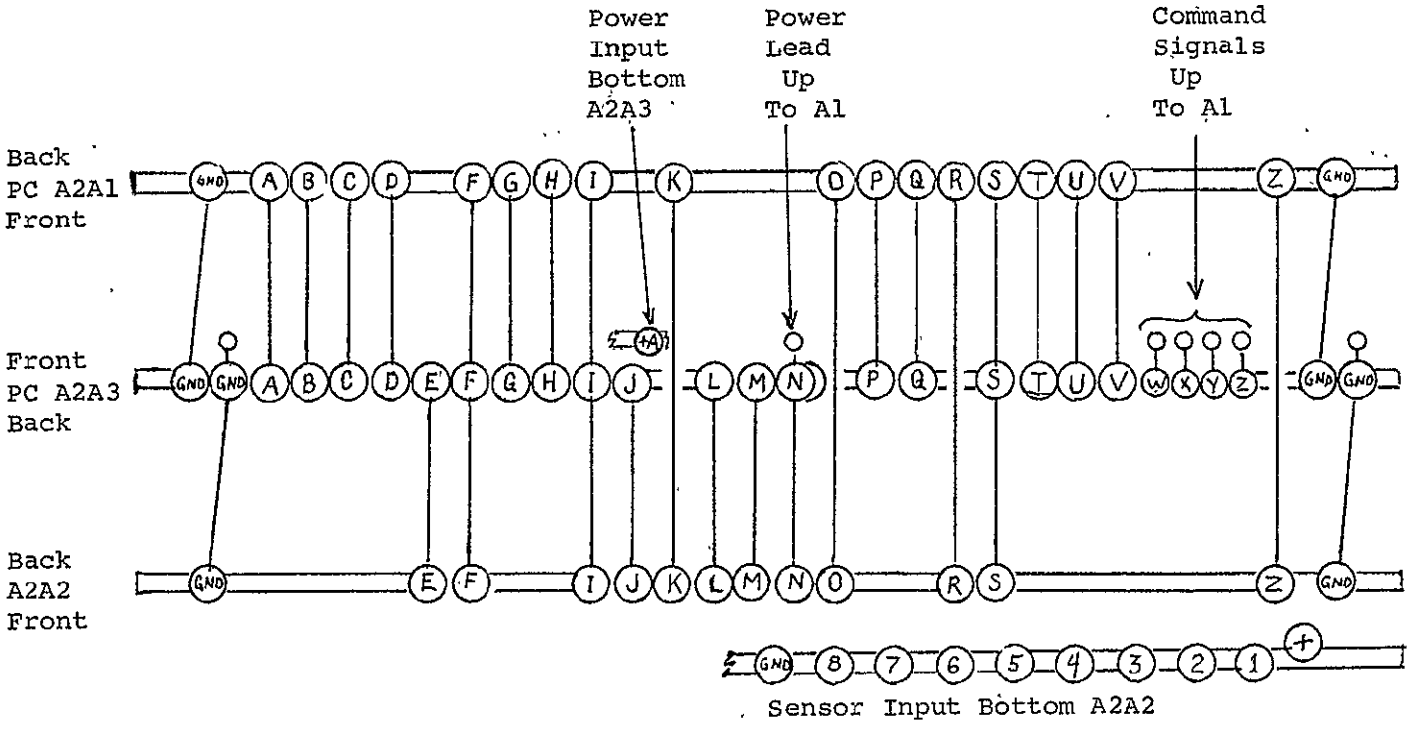


Figure 5-2. Intraboard Connections

For servicing, component replacement, and troubleshooting, the two outer logic boards may be fanned outward and upward using the interboard flexible connections or a hinge point (Figure 5-3). This will expose both sides of all three boards and make the six board surfaces accessible.

When in a closed or operating condition the boards are locked in place by means of molded foam separators (Figure 5-4). Voids have been provided in the molded foam separators to permit changing any of the optional jumper connections without altering the snug fit of the molded foam separators.

The external surfaces of the two outer boards are also foam covered to produce a foam package encasing the three logic boards.

The top of the center board is extended upward to become the main support frame for the transmitter section.

The printed boards and foam separators are applicable to both the fixed and mobile DCP. This permits a cost reduction in that a single layout of PC boards and a single mold for the foam separators is sufficient for manufacture of both types.

5.1.2 Transmitter Section

One side of the transmitter support frame is used for printed circuitry of the command signals from the logic section and power supply conductors. The opposite side is reserved as a ground plane for shielding between the various parts of the transmitter section.

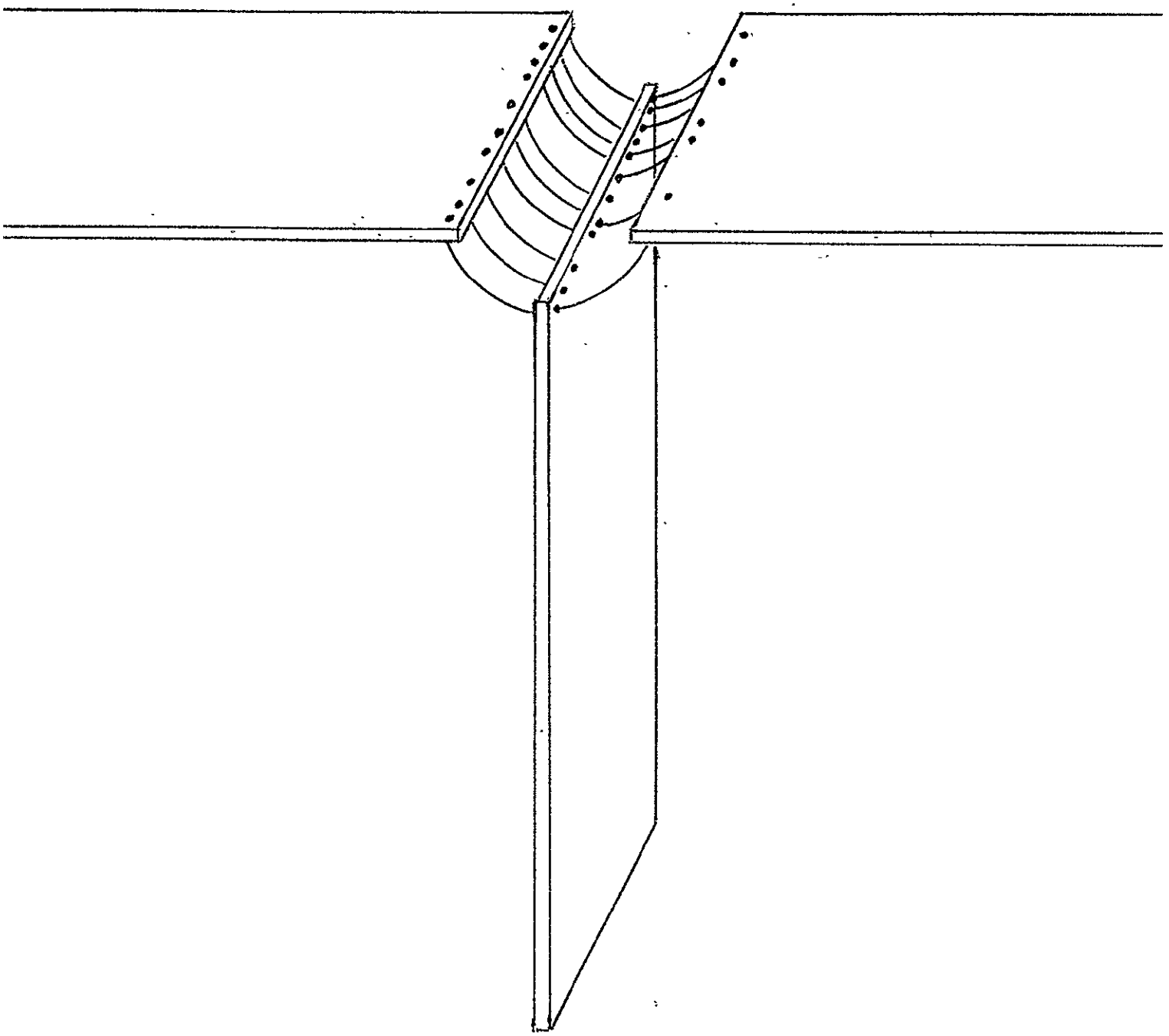


Figure 5-3. Logic Boards in Position for Servicing

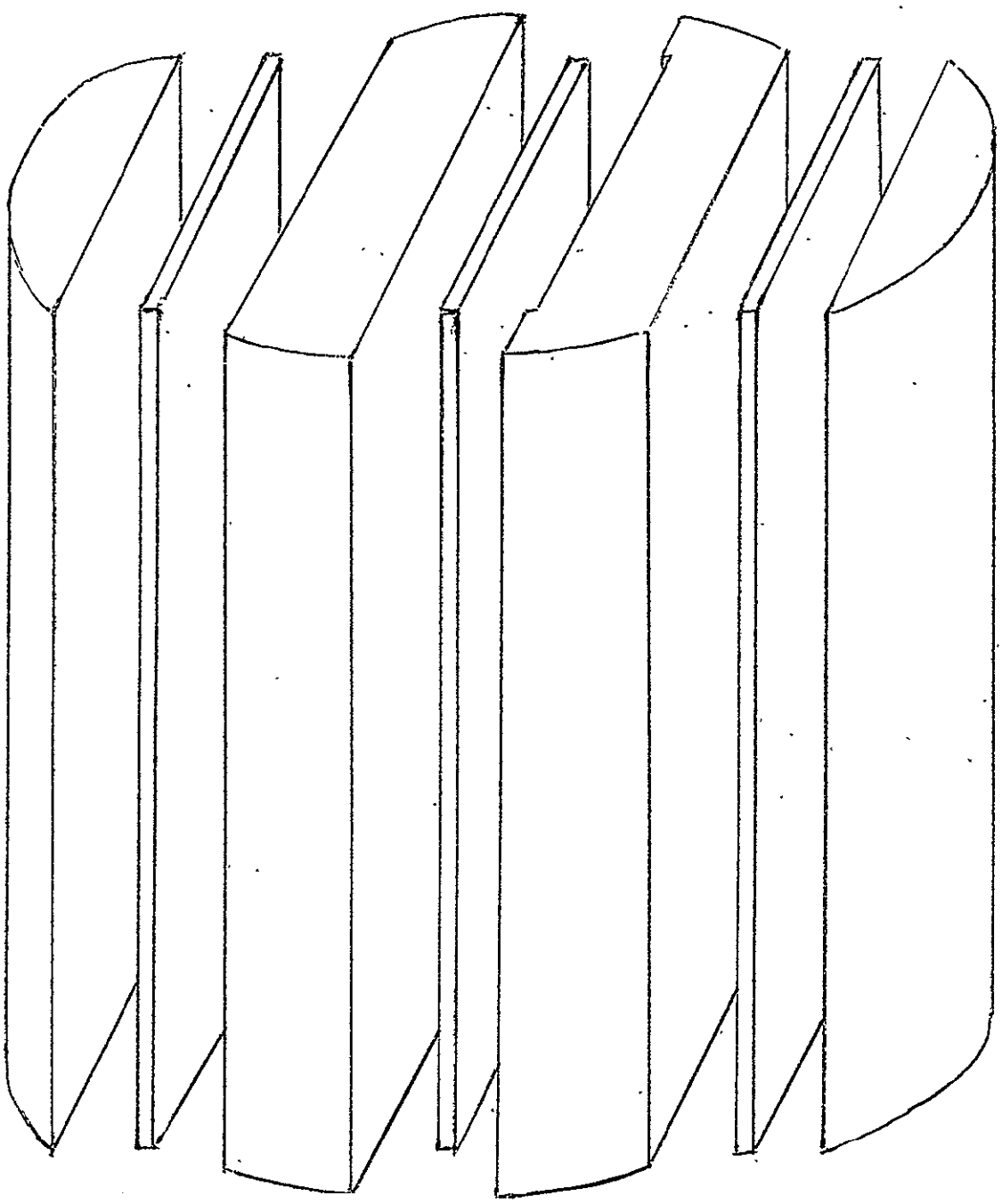


Figure 5-4. Logic Boards and Foam Separators

The multiplier and RF amplifier boards may be removed from the main frame without breaking the interconnections between them. These interconnections are located at the top edges, similar to the logic boards.

The oscillator board is shielded by a thin metallized cover.

The RF output connector is located at the top and is the main support points for attachments to the balloon harness (Figure 5-5).

The entire package is covered with a split molded foam cover (Figure 5-6). The split outer foam cover is applicable to the fixed and mobile DCP. A single mold is sufficient for manufacture of both types. The molds for the foam cover are fashioned of sheet metal, suitably braced to maintain consistency and thus ensure reproducibility of additional units.

5.2 WATERPROOF OUTER COVER

The outer split two piece foam cover could be contained within a cylindrical molded waterproof case (Figure 5-7). Optional molded support tabs may be employed for attachment of a support harness or the entire package may be supported by the antenna. The case is molded of ABS or similar material to achieve the necessary water/weatherproofing.

Figure 5-8 details the sealing of the antenna by means of a standard plastic laboratory pipe and tube connector.

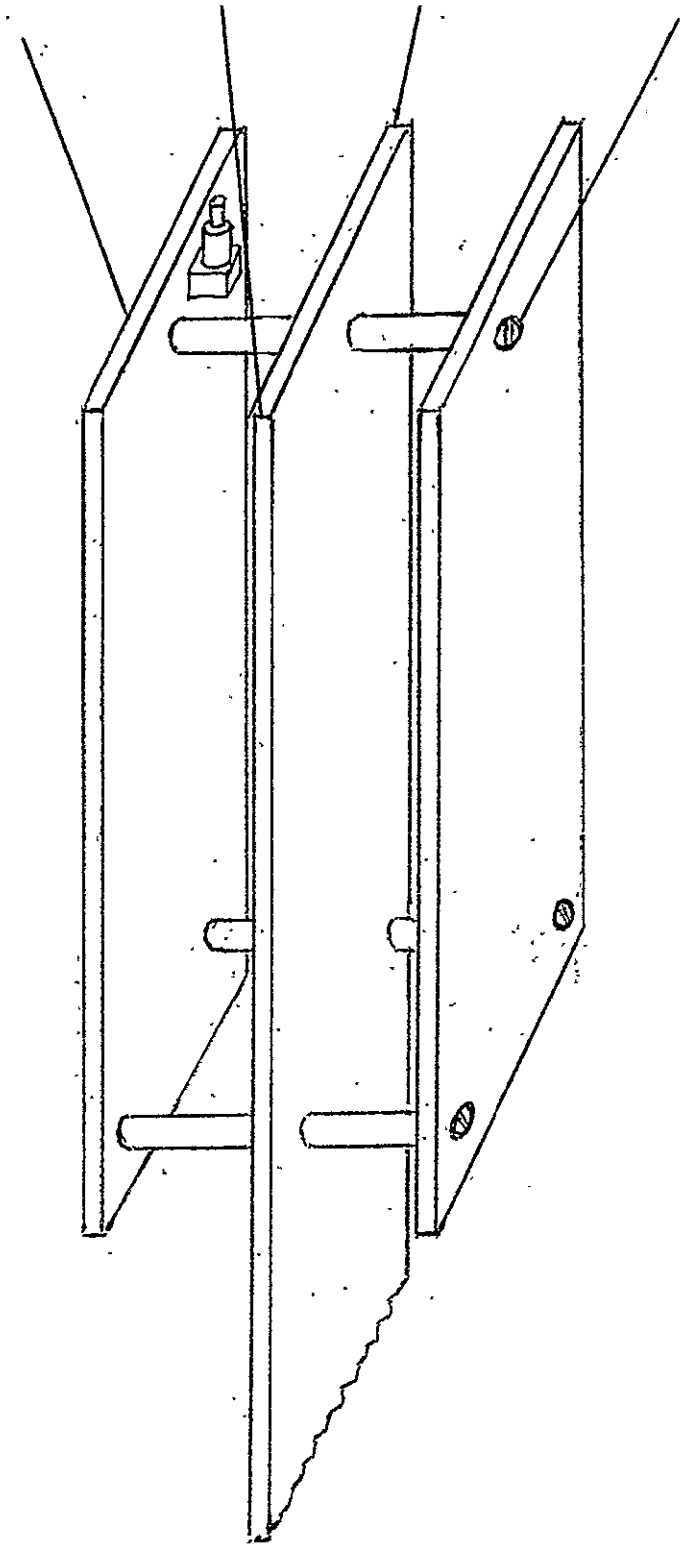


Figure 5-5. RF Boards

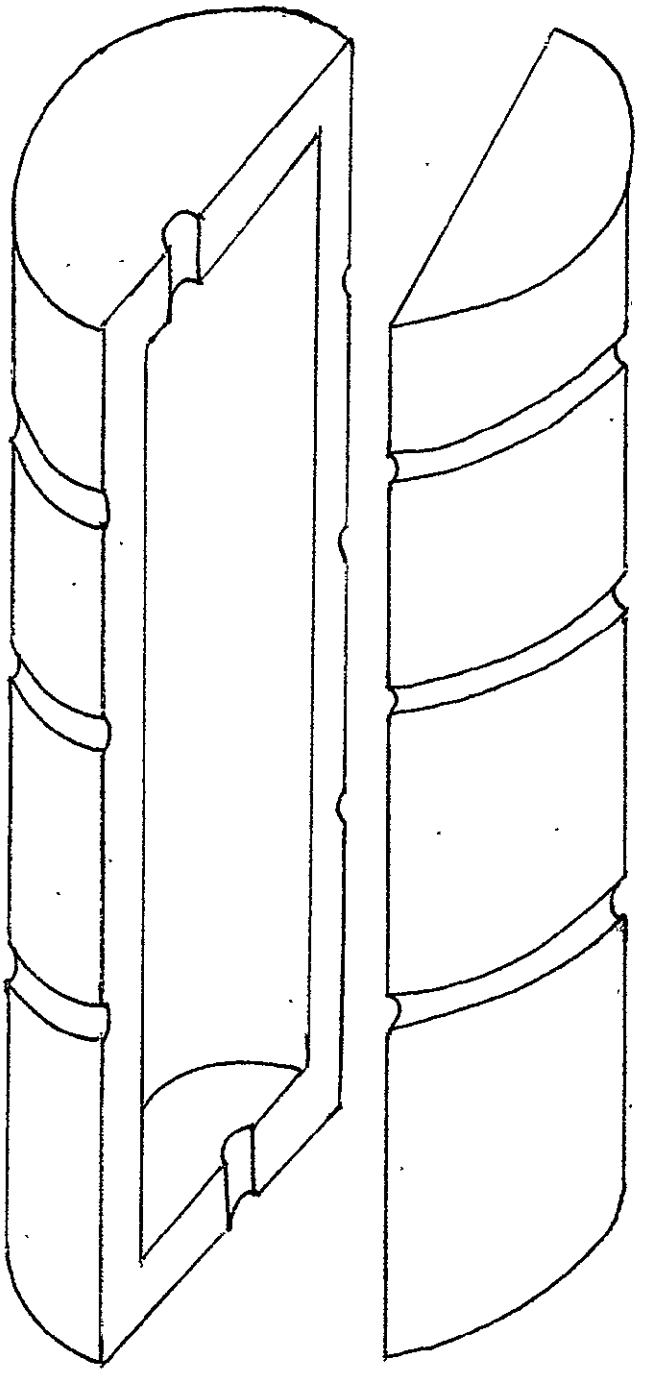


Figure 5-6. Support Covering

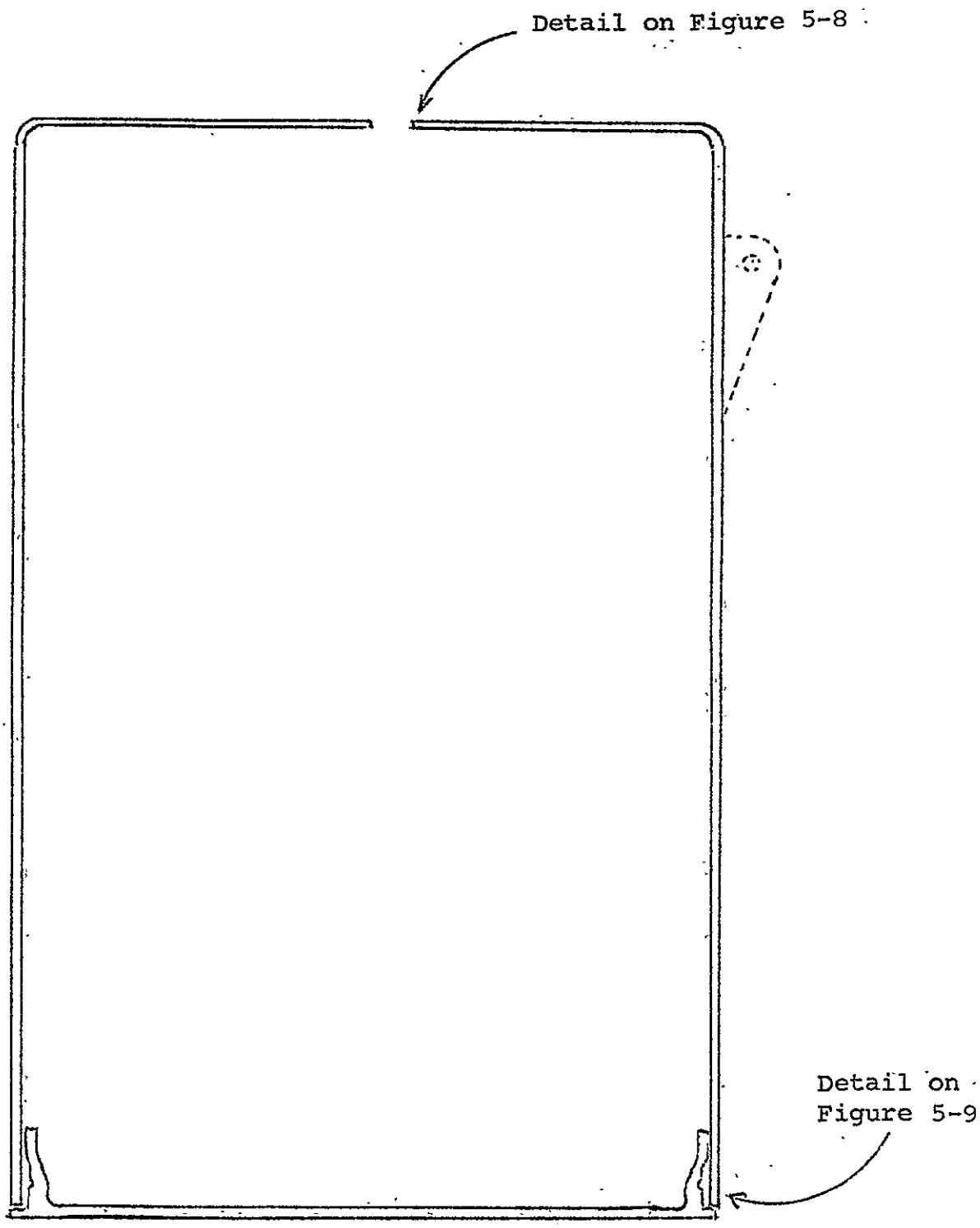


Figure 5-7. Molded Waterproof Case

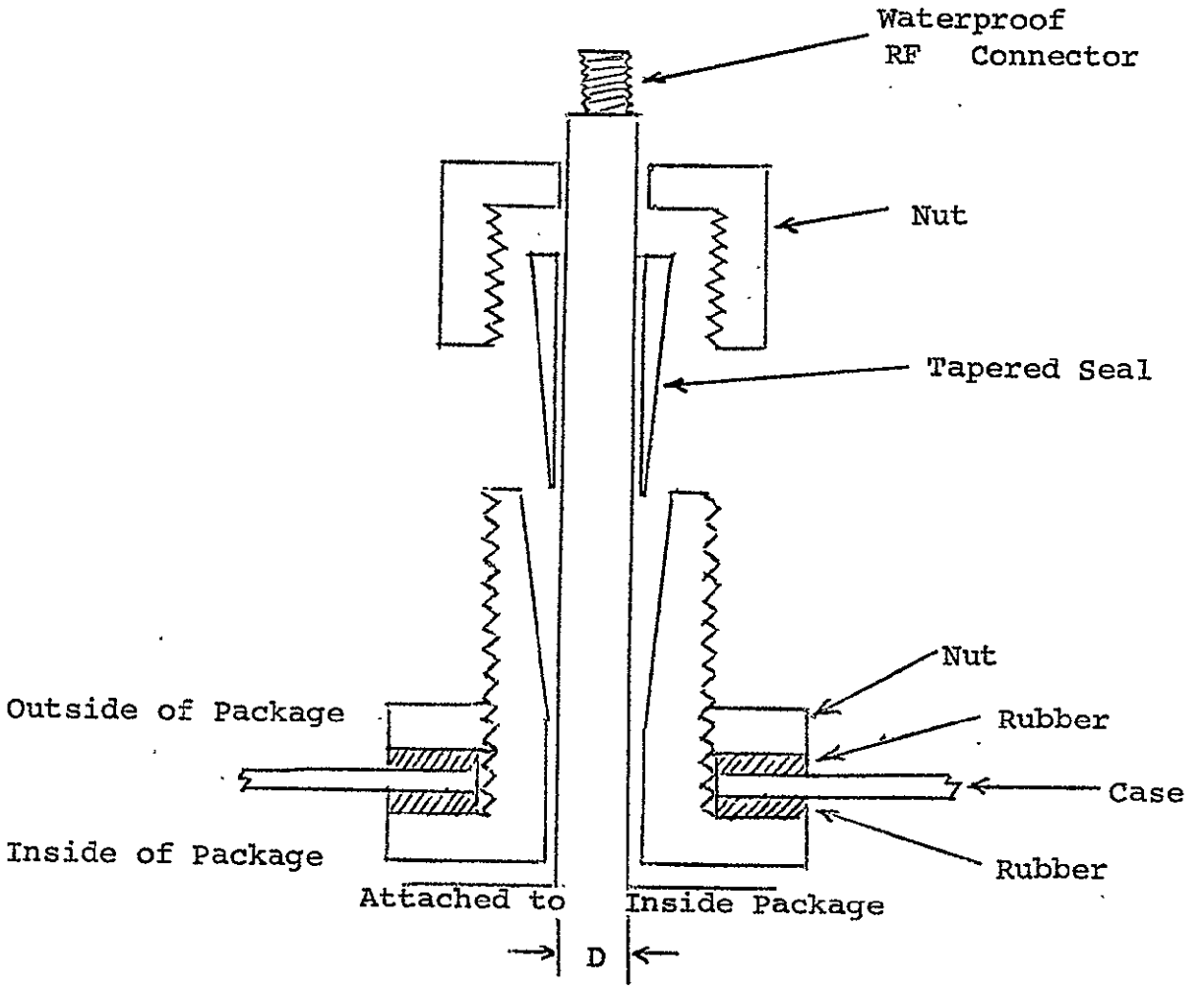


Figure 5-8. Top of Package, Waterproof Seal

Figure 5-9 details the sealing of the bottom cap to the case by means of an "O" ring and threaded coupling. The "O" ring has been placed outboard of the threads so that the threaded portion enjoys the same weather protection as the enclosed package.

The signal and power leads can be sealed by potting or with a waterproof disconnect plug external to the cap.

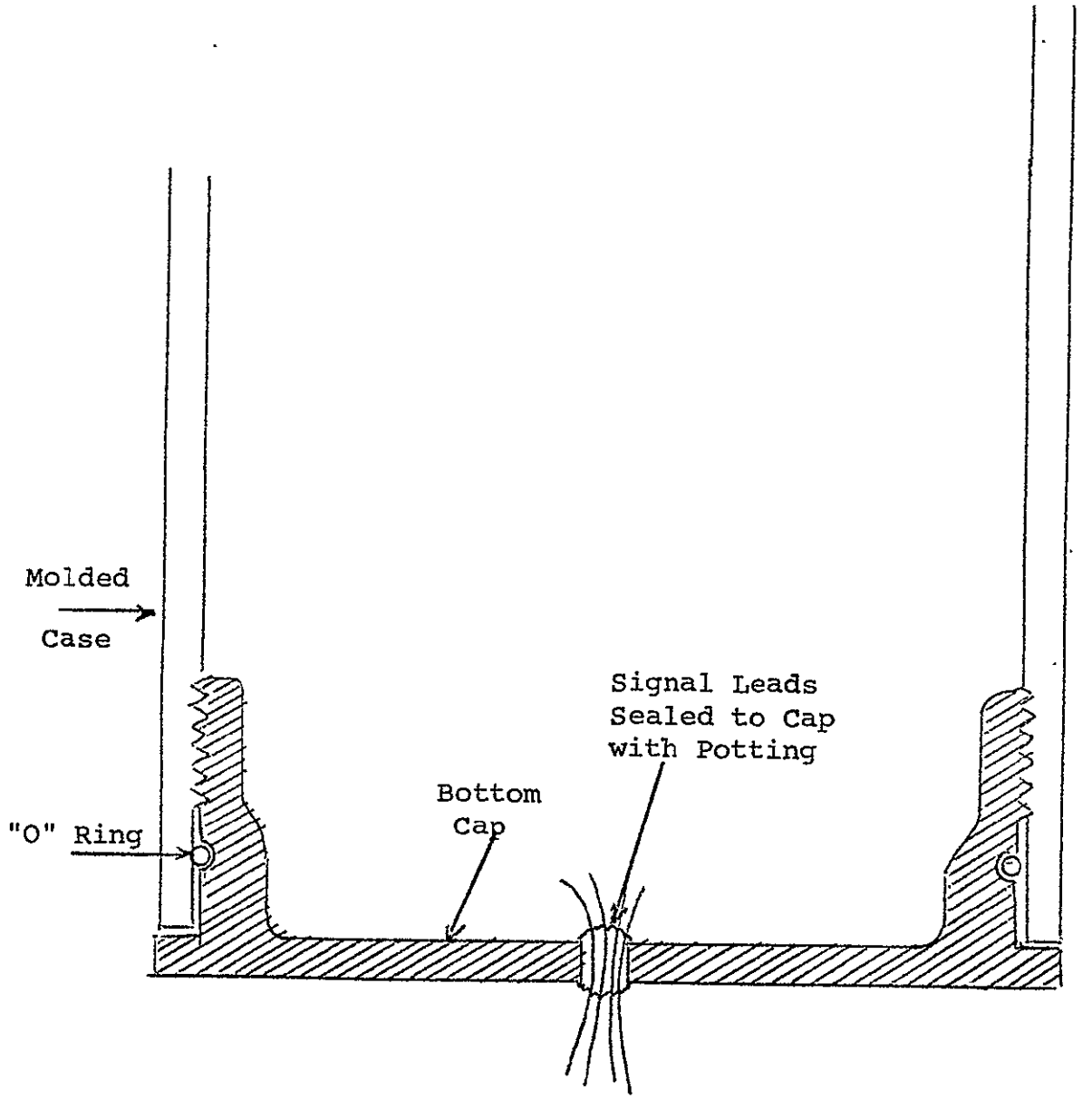


Figure 5-9. Bottom of Package, Waterproof Seal

5.3 WEIGHT

The foam has a nominal 2 lb/cu ft density and its total weight is ≈ 218 grams. The weight breakdown on the entire package for both platforms is as follows:

Logic Boards	A2A1	39.7 grams	
	A2A2	54.1	
	A2A3	53.3	
Foam Separator		41.8	188.9 grams
RF Boards	A1	40.0	
	A1A1	60.5	
	A1A2	61.5	
	A1A3	77.4	
Foam Filler		25.6	
RF Shield		10.0	275.0
Inner Package Total			463.9 grams
Outer Foam Case			150.5
Complete Package			614.4 grams

5.4 FRANGIBILITY

The foam package even when brittle from a low temperature will still retain most of its shock-absorbing qualities in addition to becoming easily fragmented. The remainder of the package has met the specified frangibility requirements as shown in Table 5-1 and Table 5-2.

TABLE 5-1. FRANGIBILITY

SPECIFICATIONS	MASS	WEIGHT/AREA		WEIGHT/LENGTH	
	Components with a Volume <1 cm^3 must have a Weight <3 grams	W/A < 2 grams/cm^2 Between >2 cm^2 < 20 cm^2		W/L <5 grams/cm for >10 cm	
Unit	Specifications Met	Total Weight / Total Area	Weight / Unit Area	Total Weight / Total Length	Weight / Unit Length
A2A1	Yes	39.7 grams / 96.77 cm^2	0.31 grams / cm^2	39.7 grams / 12.7 cm	3.2 grams / cm
A2A2	Yes	54.1 grams / 96.77 cm^2	0.56 grams / cm^2	54.1 grams / 12.7 cm	4.26 grams / cm
A2A3	Yes	53.3 grams / 96.77 cm^2	0.55 grams / cm^2	53.3 grams / 12.7 cm	4.42 grams / cm
A1	Yes	40.0 grams / 154.8 cm^2	0.259 grams / cm^2	40.0 grams / 26.32 cm	1.97 grams / cm
A1A1	Yes	60.5 grams (2 boards) / 25.8 cm^2 (each board)	2.3 grams / cm^2 1.15 grams / cm^2	60.5 grams (2 boards) / 5.08 cm But $\not>$ 10 cm (each board)	11.9 grams / cm 5.95 grams / cm
A1A2	Yes	61.5 grams / 96.77 cm^2	0.635 grams / cm^2	61.5 grams / 12.7 cm	4.92 grams / cm
A1A3	Yes	77.4 grams / 96.77 cm^2	0.8 grams / cm^2	77.4 grams / 12.7 cm	6.09 grams / cm

TABLE 5-2. WEIGHT, SIZE, AND DENSITY

	DIAMETER (in.)	LENGTH (in.)	VOLUME	WEIGHT (Grams)	DENSITY (Grams/cm^3)
Inner Package	3.5	13.5	129.89 in^3 2128.41 cm^3	464	0.22
Total Package	4.5	15.0	238.57 in^3 3910.00 cm^3	614.4	0.157

5.5 RELIABILITY AND MAINTAINABILITY

5.5.1 Reliability Prediction

A. A reliability prediction was performed per the tables of MIL-HDBK-217A using electrical stress ratios shown below and calculated at 55 degrees C.

Resistors (carbon, film and wirewound)	50 percent of rated power
Capacitors, mica and paper	40 percent of rated voltage
Capacitors, tantalum	40 to 70 percent of rated voltage
Inductors and Transformer (Hotspot)	75 percent of insulation temperature rating
Transistors, logic	65 percent of maximum junction temperature
Diodes	50 percent of rated voltage/current
Wire, Hook-up, Power Cables, etc.	50 percent of rated voltage/current

B. The four major areas for calculating the prediction were as follows:

Oscillator and Buffer	7.273
Multiplier and Modulator	9.958
RF Amplifier	5.344
Logic	70.384
TOTAL λ =	92.959×10^{-6}

The predicted MTBF is 10,700 hours for both fixed and mobile platforms.

C. The probability of successful operation of this platform for one year is given by:

$$R = e^{-\frac{t}{MTBF}}$$

Where R = Probability of Success
e = Base of Naperian Logarithmic
t = Time of One Year 8736 hr
MTBF = 10,700 hr.

$$R \cong e^{-\frac{8736}{10,700}} \cong 0.45$$

This reliability is based on the parts presently utilized in this configuration. However, with several steps of parts improvement, substantial increases in reliability are realizable. Some of these steps are discussed below.

D. Step 1 - Class B processing (MIL-STD-883) for semiconductors could raise platform MTBF to 24,100 hours with a corresponding reliability increase to R = 0.70 for a one year mission.

E. Step 2 - Replacing existing potentiometers with Hi-Rel devices could increase MTBF to almost 40,000 hours with a corresponding reliability increase to R = 0.80.

F. Step 3 - With a full Class A (MIL-STD-883) screening and burn-in program utilizing 10:1 to 20:1 improvements in failure rates, an MTBF of 100,000 hours appears possible. This would raise the probability of success to 0.92.

Any further improvements in reliability would require other techniques, primarily redundancy and crossovers which tend to negate the original specification requirement of simple, low-cost components.

5.5.2 Maintainability

Although no formal maintainability calculations were performed to determine the mean time to repair (MTTR), it is reasonable to assume that 2 hours with a 60 percent confidence level is quite feasible. The logic section has the capability of being "fanned out", which allows direct-quick troubleshooting of all components and leads on both sides of the board. The transmitter section can be easily checked for relative signal strength and continuity with standard test equipment. Replacement of components in the RF area would, in the worst case, involve board removal by unsoldering ten connection leads and three board separators held on by screws. The logic components are readily available for removal because of the board-flexing capabilities. Further improvements on the MTTR can be enhanced with receiving equipment that utilizes the inverse characteristics of the DCP. In this manner, faults can be pinpointed to the functional area in a matter of seconds.

SECTION 6

COST ANALYSIS

6.1 GENERAL

To realize where the platform complexities lie, the functional blocks of Figure 6-1 are analyzed as to their fractional cost with relation to the total platform cost. When considering units in production quantities, we shall identify both types of units as a platform. This is because the commonality factor concerned with the mobile and fixed units are such that the differential cost between them is essentially zero. Further evaluation places the functional blocks and their associated components into one of the following categories:

Category 1: Components already developed by industry that meet the requirements and are low cost.

Category 2: Components presently under development by industry that are capable of meeting the requirements and are low cost.

Category 3: Components that require further development by industry before they can meet the requirements and be low cost.

6.2 COST FACTORS

The estimates for cost are shown in Table 6-1 for the feasibility model developed for the present program.

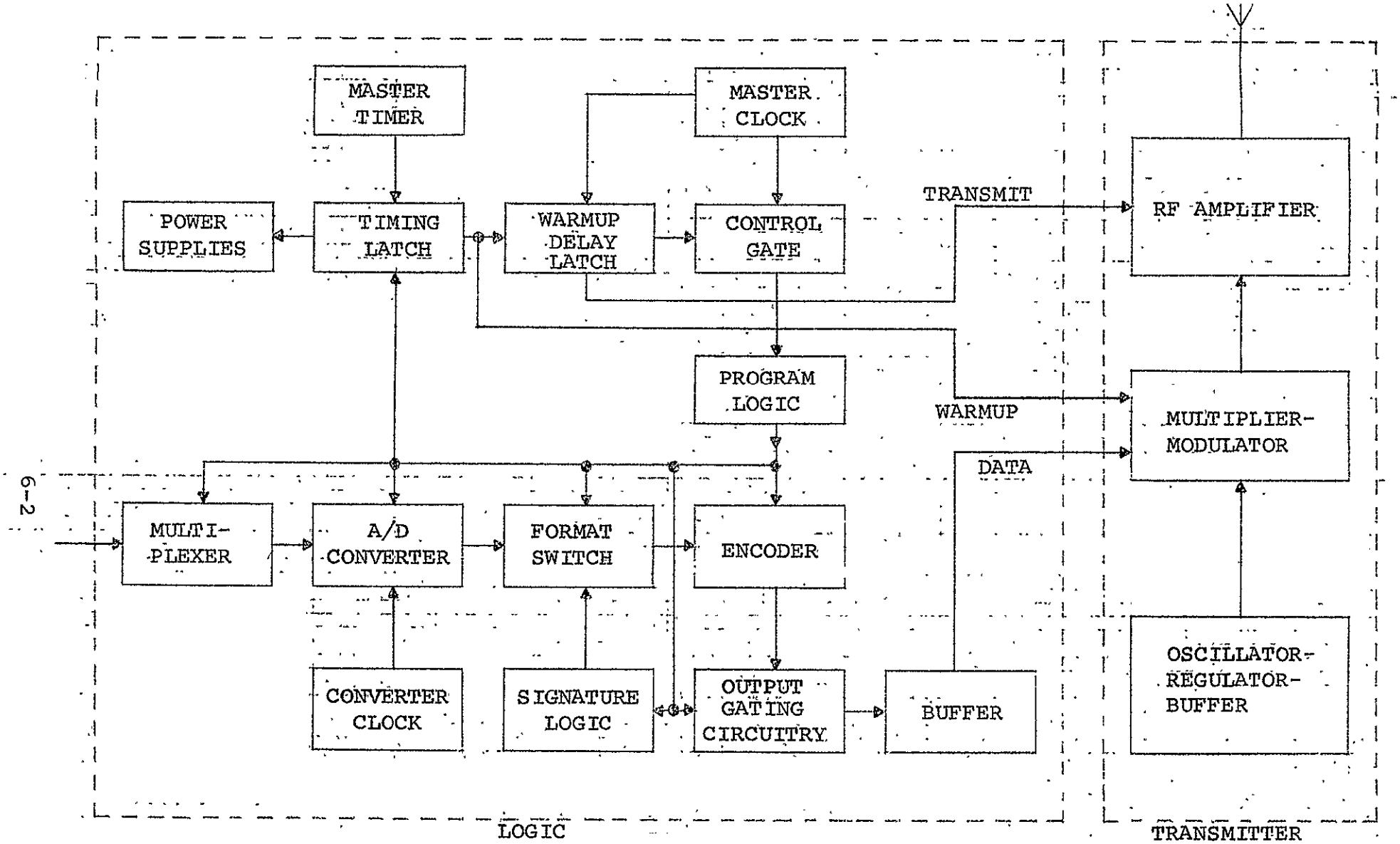


Figure 6-1. Data Collection Platform, Functional Block Diagram

TABLE 6-1. PLATFORM ESTIMATED COSTS (QUANTITY OF 100)

ITEM	FEASIBILITY MODEL (DOLLARS)
MATERIAL	400
LABOR	535
SELL PRICE	935

TABLE 6-2. PLATFORM COST EVALUATION

SECTION	PROPORTIONAL COST (PERCENT)	CATEGORY
Oscillator Assembly	35	3
Program Logic	22	1
A/D Converter (plus clock)	18	2
Functional Logic (Format Sw., Encoder, Output Gating)	10	1
Input Multiplexer and Signature Register	10	1
Miscellaneous	5	1

SECTION 7

ENVIRONMENTAL CONSIDERATION AND TRADEOFFS

In lieu of environmental testing, it will be shown that for variations in ambient temperature, the DCP's operate within the limits specified. Additionally, those areas which could lead to platform complexity, increased cost, or difference in performance from the required specifications are treated below as design tradeoffs.

7.1 TRADEOFFS OSCILLATOR-BUFFER

The stringent design requirements of the oscillator require an effort that is at the state-of-the-art. Very few tradeoffs are possible within the imposed limitations. However, if the ambient temperature variations on the oscillator section were tightened, the temperature coefficient required in the oscillator could be similarly reduced.

The only tradeoff within the oscillator-buffer subassembly is that the integrated circuit voltage regulator may be replaced by a lower cost zener diode. However, the zener diode would not provide the short circuit and over-voltage protection inherent in the IC regulator.

7.2 TRADEOFFS MULTIPLIER-MODULATOR

The design of the multipliers in the multiplier-modulator subassembly represent a tradeoff of complexity and power gain. Increased power gain can be achieved by including tunable idler circuits

in the base circuit of the multipliers. This would add another variable capacitor to each of the multipliers and thus would require adjustment during initial tuneup. This added gain can be achieved more economically in the untuned postmodulator linear amplifier. Since the operation of the platform is not dependent upon significant power gain being achieved in the multipliers, the multiplier can be tuned solely for minimum subharmonic generation This factor greatly eases the filter specification requirements.

The phase modulator in the multiplier-modulator assembly has the advantage of being relatively broadband and inexpensive. It is lower in cost and smaller than phase shifters utilizing variable capacitance or pin diodes. However, it has the disadvantage of having a relatively high insertion loss. If the multiplier-modulato subassembly were not constructed on printed circuit boards but rathe on high dielectric substrate (microelectronic form), a phase shifter could be constructed with binary varactor diodes that would have an insertion loss approximately 8 dB less than the phase shifter presently utilized. With a lower phase shift insertion loss, one stage of postmodulator amplification could be eliminated.

7.3 TRADEOFFS— RF AMPLIFIER

The TRW microelectronic broadband amplifier is the ideal approach to achieving power gain in the RF amplifier assembly.

The MX 2.5 and the MX 7.5 combined with a linear driving amplifier will fulfill the power requirements of the mobile and fixed Data Collection Platforms. A tradeoff is possible between the power output and the number of solar cells in the mobile platform. If the power output is limited by a power leveling circuit, the prime power input of the platform will be much more closely controlled, and the solar cell panels can be chosen to a lesser peak current specification.

7.4 ENVIRONMENT DESIGN CONSIDERATIONS

7.4.1 RF Portion

The transmitter of the DCP has been designed to minimize power output variations with temperature. The limiter in the oscillator loop provides several dB of compression to limit the loop gain to unity. Excess gain is thus provided to compensate for gain changes with temperature. The buffer amplifier following the oscillator loop normally operates at several dB of gain compression to maintain a constant drive to the multipliers.

The variations of gain with temperature in the multipliers is mitigated by the gain compression provided in the linear amplifier between the multipliers and the modulator. The modulator itself is very stable with temperature because of the stability of the modulator driver circuitry.

All the linear circuitry in the DCP transmitter section are self-biased in the most stable configuration possible. This limits the current, and hence the gain variations with temperature. The postmodulator linear amplifier stages combine this bias stability with a level of gain compression to limit the temperature-dependent amplitude variations to a low level. The temperature-insensitive signal thus developed would enable the final Class C stages to meet the minimum power output and efficiency requirements if parts specified over the full temperature range were utilized.

7.4.2 Logic Portion

7.4.2.1 Symbol Rate-Master Clock

When a convolutional encoder is required, the symbol rate specification is 160 symbols $\pm$0.125 percent and 1600 symbols $\pm$0.125 percent per second for the mobile and fixed platforms respectively.

Symbol rate is fixed by the master clock whose periods are 3.125 msec, and 312.5 msec nominally for the mobile and fixed platforms respectively.

Implementation of the master clock with a complimentary symmetry MOS (COS/MOS) astable multivibrator (without temperature compensation) yields the following calculated dynamic variations of the clock period for the given independent variables.

	Fixed	Mobile
Power Supply Variations (+30 mv)	±0.009%	±0.009%
Temperature Variations	-54°C to +49°C	20°C to 30°C
COS/MOS Voltage Transfer Point	±0.3%	±0.025%
Polycarbonate Capacitor	±0.25%	0%
Low Temperature Coefficient Fixed Resistor @ 50 ppm/°C	±1.0%	±0.05%
Low Temperature Coefficient Potentiometer @ 250 ppm/°C	±4.0%	±0.25%
Worst Case Variation	±5.55%	±0.325%

Implementation of the master clock using a low-cost crystal with COS/MOS circuitry would yield frequency stability within ±0.125% of initial setting for more than one year. Setting the crystal frequency to within ±0.125% of nominal is easily achieved. For a production unit then, a low cost crystal would be specified, for example, at 32 KHz, and be divided by 10 or 100 to produce the mobile and fixed clocks.

The repetition rate is fixed by the master timer whose periods are 60 ±4.5 seconds and 120 ±10 seconds respectively for the mobile and fixed platforms. Implementation of the master timer with a programmable unijunction (UJT) yields the following calculated dynamic variations of the timer period for the given independent variables.

	Fixed	Mobile
Temperature Range	-58°C to +68°C	20°C to 30°C
V_T (Offset Voltage)(0.5 to 0.75V)	+8 sec.*	Negligible**

Power dissipation for the fixed timer is 7.2 mw and power dissipation for the mobile timer is 0.2 mw. The conclusion is that the timer, as implemented in the feasibility model will suffice for both versions of the platform if the 7.2 mw dissipation in the programming resistors is at a tolerable level.

7.4.2.2 A/D Conversion

The specification limit for the A/D converter is better than 1% full scale for the fixed and mobile platforms. Conversion error takes three forms:

- Aperture Error - Aperture error is negligible because of the high sampling rate and low rate of change of the input signal.
- Quantization Error - Quantization error is a function of the number of bits of quantization. An 8-bit A/D converter can give no better than 0.39% full scale (±1/2 LSB) accuracy.
- Analog Error - Analog error sums the errors due to inaccuracies in the multiplexer, analog comparator, and offset correction circuits.

---

* R_G = 10K

** R_G = 1M

Analog error manifest in the multiplexer is temperature dependent. The offset correction and comparator inaccuracies are not significantly temperature dependent.

• Multiplexer (Analog Error) - Both the input analog and the A/D converter reference multiplexers are high-impedance-type multiplexers.

At the time when the analog input multiplexer is being sampled by the A/D converter, the output of seven channels of the input multiplexers are tied to the common output node, and likewise the outputs of V_g and V_R gates are tied to a common output node (Figure 7-1). The path from the input multiplexer to the buffer amplifier is very low, while the impedance of the off switches is relatively high.

Off channel leakage for each transmission gate at room temperature is 100 pa, while at +80°C it is 6.4×10^{-9} a. (doubles every 10°C rise). The maximum ON-impedance of a transmission gate (disregarding effects other than temperature for the time being) at 80°C is 1K. The maximum bias current for the buffer μA741 at 80°C is 0.3 μa.

Considering the OFF currents (I_{LK1}, I_{LK2}), buffer bias current (I_b), and ON resistances (R_1R_2), and referring to Figure 7-2, we derive an expression for the buffer input voltage (V_{X2});

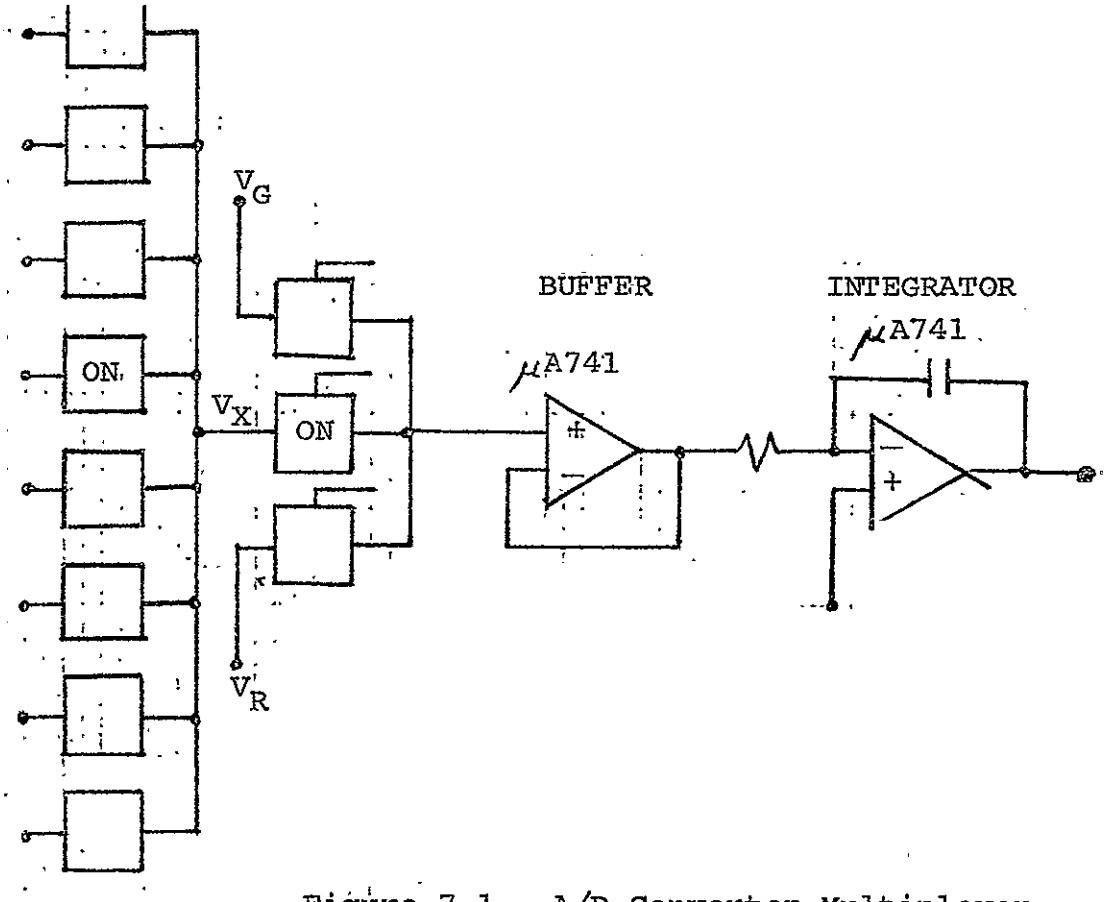


Figure 7-1. A/D Converter-Multiplexer

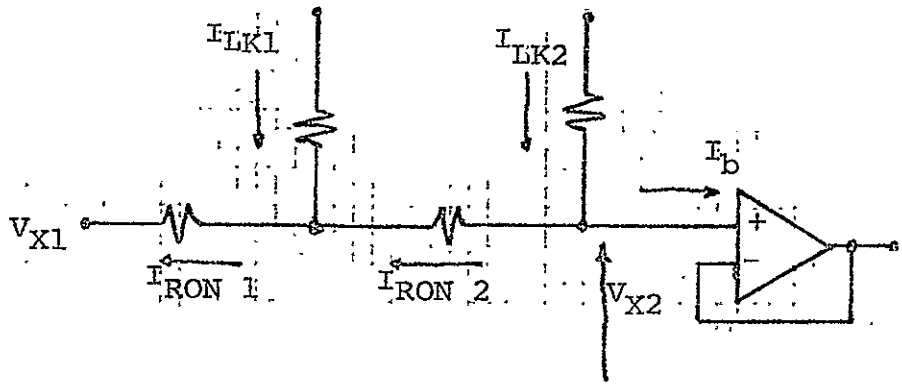


Figure 7-2. Buffer Amplifier

$$V_{X2} = V_{X1} + E_{R1} + E_{R2}$$

$$E_{R1} = I_{R1} R_1$$

$$I_{R1} = I_{LK1} + I_{R2}$$

$$I_{R2} = I_{LK2} - I_b$$

$$E_{R2} = I_{R2} R_2$$

$$I_{R2} = I_{LK2} - I_b$$

$$E_{R2} = (I_{LK2} - I_b) R_2$$

$$V_{X2} = V_{X1} + R_1 I_{LK1} + I_{LK2} (R_1 + R_2) - I_b (R_1 + R_2)$$

Substituting, we have

$$V_{X2} = 9.5 + 1K(6.4 \times 10^{-9}) + 2K(6.4 \times 10^{-9}) - 0.3\ \mu a\ (2K)$$

$$V_{X2} = 9.5 + 6.4 \times 10^{-6} + 12.8 \times 10^{-6} - 0.6 \times 10^{-3}$$

$$V_{X2} = 9.5 - 0.6\ (\times 10^{-3}) \quad \text{Q.E.D.}$$

The voltage differential from input to the buffer is 0.6 mv.

With the 2-volt input range divided into 256 quantum levels, each quantum is worth $\frac{2v}{256 \text{ levels}}$ = 7.8 mv, or 0.39 percent of full scale. A 0.6 mv error is worth 0.0245 percent of full scale.

When the A/D converter reference multiplexer has the right combination of signal, control, and supply voltages, the source-bias effect (source to substrate voltage increases the control threshold voltage because the source is not grounded as in a non-analog circuit) causes the ON resistance of the Vr gate to increase to some impedance high enough to greatly add to the multiplexer error. By lowering the P channel substrate voltage (supply voltage) the effect is negated. (The diodes CR1, CR2, and CR3 are germanium and conduct before the gate protection diodes, when the gate input goes high and thereby protects the transmission gate from possible damage due to overheating the protection diodes.

7.4.2.3 Offset Correction Error

The integrator offset correction is maintained by the 0.1 μfd capacitor C10 during the conversion interval. Assuming the capacitor will linearly discharge 66 percent (as in approximation) in the first RC interval (Figure 7-3), we determine the discharge rate to be:

$$\frac{\Delta V}{\Delta T} = \frac{V_2 - V_1}{TA}$$

$$V_2 = 0.66V$$

$$TA = RC$$

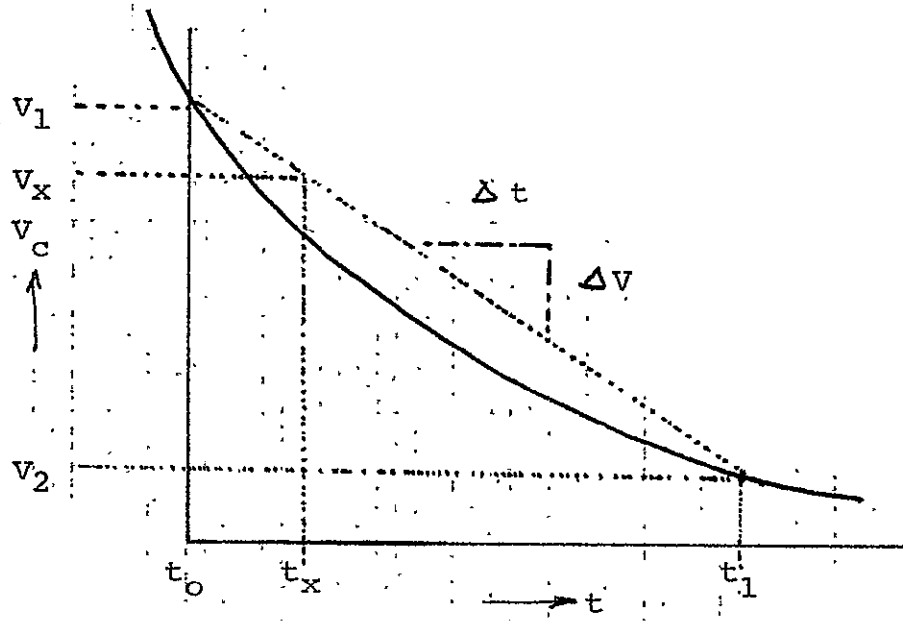


Figure 7-3. Offset Correction Discharge

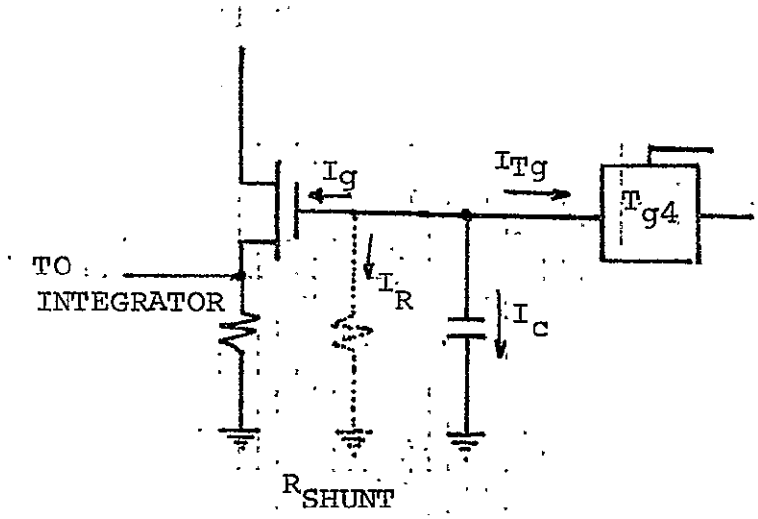


Figure 7-4. Conversion Discharge Paths

$$\frac{\Delta V}{\Delta T} = -\frac{0.34V_1}{RC} = K$$

The capacitor voltage at the end of the conversion interval (V_X), then, is

$V_X = V_1 - KT_X$ where T_X is the conversion interval period.

The capacitor has three paths of discharge; The source follower gate leakage, the capacitor leakage, and the transmission gate "OFF" leakage as illustrated in Figure 7-4. Deriving R_{shunt} we have:

$$\frac{1}{R_{shunt}} = \frac{1}{R_{gate}} + \frac{1}{R_C} + \frac{1}{R_{TG}}$$

$R_{gate} = 2.0 \times 10^9$ (with protection diode) = 2000 m ohm

$R_C = 5 \times 10^{10}$ ohm = 50,000 m ohm

$R_{TG} = \frac{12V}{6.4 \times 10\text{-}9\ a} \cong 2 \times 10^9$ ohm = 2000 m ohm

$R_{shunt} = 1000$ m ohm

Calculating V_X ; $C = 0.1\ \mu fd$ $R_C = 100$ seconds

So, $K = \frac{0.34\ (6.5)}{200} = \frac{2.2}{100} = 0.022$

$V_X = 6.5 - 0.022\ (36\ msec)$

$V_X = 6.5V - 0.792\ mv$

Therefore, the capacitor discharges approximately 1 mv during the longest conversion interval.

A 1 mv change on input represents a 0.04 percent FS error.

Analog error due to transfer nonlinearities of the integrator are cancelled when using the dual slope integration technique.

7.4.2.4 Error Summary

A/D converter errors at worst case temperature conditions are as follows (full scale):

Quantization Error		= 0.39%
Analog Multiplexer Input Error		= 0.02%
Offset Correction Error		= 0.04%
Other Errors	less than	0.10%
Total FS Error		= 0.55%

It is shown that the A/D converter described will remain within specification at the worst case temperature. The above analysis assumes a constant voltage reference supply over the temperature range. Design of a suitable reference supply is well within the state-of-the-art capabilities and is not treated here.

SECTION 8

RECOMMENDATIONS

8.1 OSCILLATOR AND RF IMPROVEMENTS

It is recommended that the entire RF assembly be implemented in microelectronic form on a high dielectric substrate to reduce the size and weight and provide the most frangible structure possible. The components in the oscillator would most likely exhibit an improved temperature coefficient when the parts are packaged in close proximity on the heat conductive substrate. The maximum temperature compensation may be thus realized.

On high dielectric substrate, untuned multipliers are economically practical because microstrip coupled-line filters can be etched on the substrate. Half-wavelength resonator filters are well suited to microstrip construction; as open circuits, they do not require ground returns through the substrate as do such quarter wavelength structures as comb-line or interdigital filters. When a short is required, any inaccuracy in its placement results in inaccurate tuning. The microstrip half-wave filters, however, need only be controlled in the outer dimensions, and thus can be accurately tuned. The filters required can be implemented within a package less than 10 inches in length. A quarter-wave resonator can also be investigated but this type of filter suffers from poor selectivity.

The high dielectric substrate will allow the construction of a phase shifter with a greatly reduced insertion loss. A $170^{\circ}(\pm 5^{\circ})$ phase shifter would be implemented with the parallel channel approach used in the development unit but with a 3-dB microstripline coupler and binary varactor diodes used for the 180° modulator. Small phase shifts could also be implemented utilizing periodically loaded microstrip lines.

It is further recommended that hybrid microelectronic linear amplifiers be utilized to increase the power level of the modulated signal to the level required by the microelectronic TRW amplifier. TRW will modify their amplifier to interface with the linear drivers. The amplifiers should be only as broadband as necessary to allow for variations in components and variations of the components with temperature. These broadband amplifiers would eliminate the need for any tuning or alignment procedures. Output power fluctuations can be limited to several tenths of a dB with the inclusion of a power leveler circuit that senses the output power and limits the gain of one of the linear stages accordingly. This constant output can be held for power supply variations as well as temperature changes. With the addition of a power leveler, the maximum power needed from the solar cells can be very closely controlled and hence the number of cells can be held to a minimum.

Two types of output filters can be implemented depending upon system requirements. A low-pass filter will provide attenuation of all frequencies above the cutoff frequency of the filter. It is also possible to implement a multiharmonic rejection filter in microstrip that will not pass the second, third, or fourth harmonic of the output signal.

8.2 LOGIC IMPROVEMENTS

It is recommended that large quantity versions of the DCP be implemented in an integrated version similar to integrated Model No. 1 (Figure 8-1). Most of the programming logic would be implemented using an ROM (Read Only Memory). The remainder of the program logic and all of the functional logic (encoder, A/D converter-digital logic, timing latches, etc.) would be implemented using the custom designed LSI integrated circuit as COS/MOS circuitry. The input multiplexer and A/D converter could remain in MSI or discrete form.

8.2.1 Implementation Using Future Developments

8.2.1.1 Digital

Most of the logic in the digital section of the DCP is ideally suited for COS/MOS integration and vice versa.

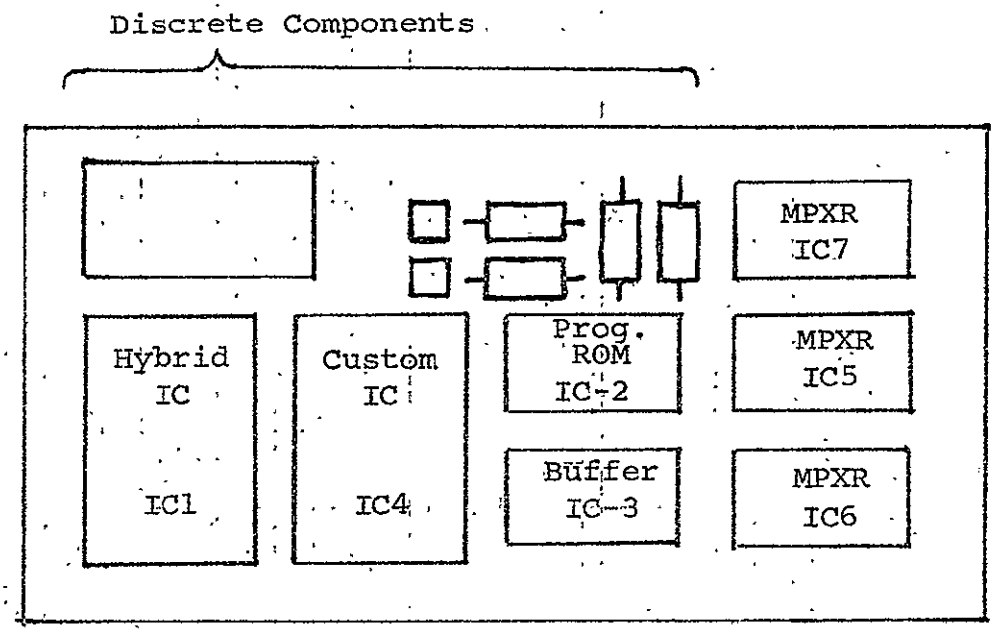


Figure 8-1. Integrated Model No. 1

Soon to be developed or released are integrated circuits (MSI) to reduce the cost of the input multiplexer by combining the function of the multiposition switch with a sequencing counter. In integrated form, the multiplexer will contain eight P-Channel MOSFET's and a ring counter to sequence the eight FET's.

8.2.1.2 Analog

Another development in the more remote future is a low cost, low power integrated version of the total A/D converter. Present problems with off-the-shelf A/D converters include excessive power dissipation, relatively high cost and large (nonfrangible) size. Presently, very low-power (microwatt) operational amplifiers are being developed in MSI form. When technology evolves enough, these operational amplifiers will be married with the rest of the A/D circuitry in monolithic form. If the performance characteristics (power and speed) are in line, a monolithic version of the A/D converter will be general enough to be practically marketed. For the near future, however, the most practical implementation of the A/D converter is a somewhat improved version of the present system.

8.2.2 Circuit Improvements to Simplify or Reduce Cost

Since the discrete components in the A/D converter comprise a large portion of platform costs, it is recommended that:

- The discrete resistors in both A/D converter and power supply circuitry be implemented by use of metal film resistors molded into 14 and 16 pin dip packages, such as the CTS resistor pack.

- The operational amplifiers IC-2, IC-3, and IC-22 be implemented using a single package with three operational amplifiers such as the RCA 3060.

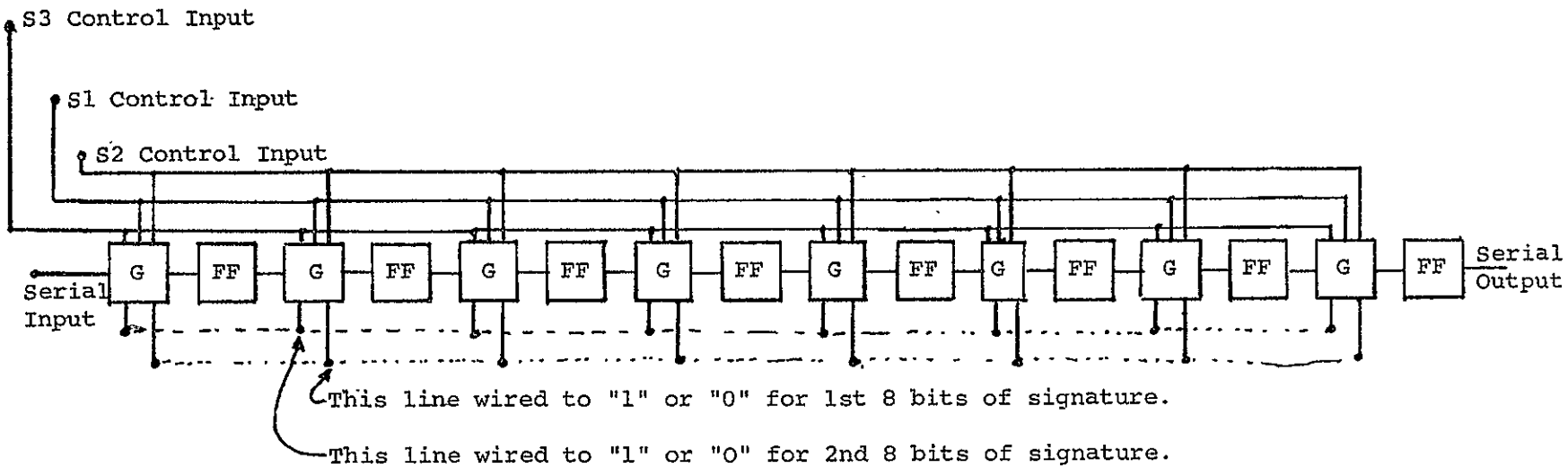
- Redesign of the reference multiplexer be attempted in order to minimize the source bias effect and minimize the parts count.

- Design effort may be expanded to include dropping the A/D converter offset correction circuitry. (This might be done by ensuring that the integrator op-amp is always in the saturated region except during the integration interval.

- If sufficient chip area remains after the design of the custom circuit, the use of an integrated timer should be considered to replace the master timer. This implementation would reduce the parts count by nine components and essentially eliminate the cost of the timer. The disadvantage, however, is that the master clock must work continuously to provide combinational timing for the DCP system. However, additional flexibility with an integrated timer is achieved because the platform

timing can be programmed externally by adjusting the counter-divide ratio. Quiescent dissipation must be considered before implementing the integrated version of the master timer.

- In considering the design of the custom IC, the signature register, 8-bit parallel-to-serial converter, and binary counter should be implemented using one 8-cell structure. With the appropriate gating, this one 8-cell structure could operate initially as a counter and upon command, after counting, serially shift the information out of the register. After the data collection interval, the third mode of the cell would allow the parallel signature inputs to be read into the register and shifted out serially. All 16 bits of the signature logic could be implemented using two parallel inputs per stage in the 8-bit counter/shifter register. (See Figure 8-2.) An 8-bit serial in-serial out shift register would be required following the multifunction converter. Serial in-serial out registers are inherently simpler than parallel in/serial out registers.
- When designing the custom integrated circuits, a mobile platform option should be implemented whose function would be to inhibit modulation during the CW interval of the mobile platform. In the present system, modulation is inhibited for the



S1	S2	S3	Function
0	0	0	Binary Counter
0	0	1	Shift Register
0	1	1	#1 Signature Preset
1	0	1	#2 Signature Preset

G: Control Gates

FF: Flip Flop Unit

(Clock Inputs Not Shown)

Figure 8-2. Multifunction Converter/Register

first five data words by connecting the data inputs to the E supply. During the conversion interval, this ensures that the A/D converter serial output is 00000000.

8.2.3 Circuit Recommendations to Improve Circuit Performance

It is recommended that:

After the above circuit improvements are made in the A/D converter, the benefits of a DC/DC converter to improve supply immunity be investigated. A DC/DC converter may provide both RF and digital sections with considerable supply immunity. Although instantaneous power dissipation would be increased due to the DC/DC converter lower efficiency, the system is turned on periodically for short intervals, therefore, the quiescent power dissipation would remain relatively constant. The average power dissipation would increase only slightly. As a battery nears the end of its useful life, it may provide for periods of 1/10 and one second, enough power to operate the data collection platform satisfactorily if supply immunity is afforded by DC/DC converter. Additionally, if the DC/DC converter were used, the analog sensor inputs would range from 0 to +2 volts if positive and negative voltages were obtained from the converter. Additionally, it is recommended that the master clock, in order to maintain the output symbol rate specification, be implemented using a low-cost crystal oscillator in conjunction with COS/MOS circuitry.

8.2.4 Serial Digital Data

The data collection platform is capable also of receiving and encoding data in serial form and modulating the transmitter. To accommodate serial information, the sensor binary output must first be converted to serial form. This can best be done as shown in Figure 8-3. The only physical change required in the DCP is to break the connection from the parallel-to-serial converter (located in the A/D converter) to the data input of the format gate.

Data is loaded into the parallel-to-serial converter exactly as the data is loaded from the A/D converter into its parallel-to-serial register. The converter does not begin to shift until the particular channel control input is high. In this way, the information in binary form is substituted directly for the analog information for the same channel. All the circuitry shown is external to the DCP and can be implemented using no more than three integrated circuits.

8.3 RECOMMENDATIONS SUMMARY

- Integrate the oscillator in microelectronic form
- Improve the transmitter section to void itself of adjustments
- Utilize automatic level control circuitry to ensure optimum operation
- Integrate the DCP for large-scale production
- Implement the digital logic in LSI form

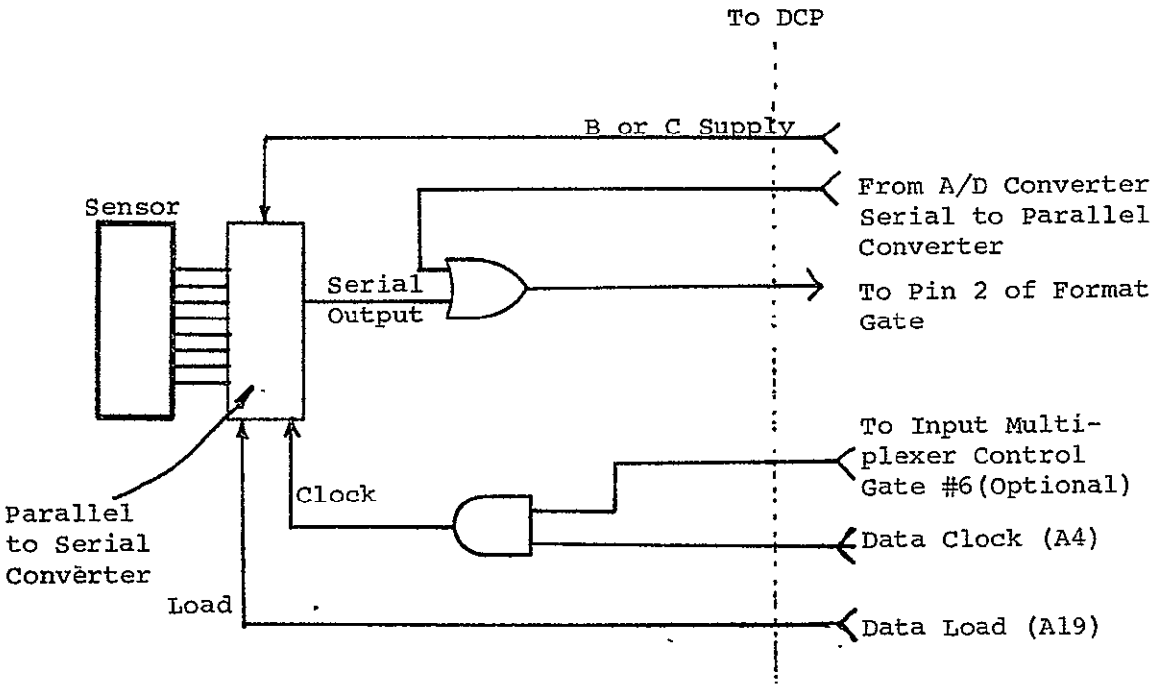


Figure 8-3. Sensor Parallel Output

- Resurvey low-current A/D converters market
- Substitute metal film resistor pack for discrete resistors
- Substitute a single low-power op amp package for the three discrete op amps used
- Redesign the A/D converter reference multiplexer
- Investigate the possibility of eliminating the offset correction circuitry
- Consider integrating the master timer
- Minimize gate count by combining functions
- Provide CW tone interval modulation inhibit
- Investigate benefits of a DC/DC converter
- Consider implementing circuitry to accept data in serial form

FUNCTIONAL PERFORMANCE TESTS

Appendix A

DATA COLLECTION PLATFORMS

Contract No. NAS5-21164

Prepared for

National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland 20771

AMERICAN ELECTRONIC LABORATORIES, INC.
Richardson Road, Colmar, Pennsylvania

TABLE OF CONTENTS

DATA COLLECTION PLATFORM

ACCEPTANCE TEST PROCEDURE

1.0 RF MODULE

1.1 Preliminary: Procedures for testing the fixed and mobile platforms are identical.

1.1.1 Connect the U.U.T. (Unit Under Test) as shown in Figure 1-1.

1.1.2 Data state W is defined to be the phase state existent when S1 is positioned such that W is grounded and V_{cc} is supplied to X. Data state X is defined to be the phase state existent when S1 is positioned such that X is grounded and V_{cc} is supplied to W.

1.1.3 The warmup mode is defined to be the mode existent when $11 \leq V \leq 13$ and S2 is open. The transmit mode is defined to be the mode existent when $11 \leq V \leq 13$ and S2 is closed.

1.1.4 The measurement of short-term (1/2 sec.) stability is made with the U.U.T. connected as shown in Figure 1-2.

1.2 Frequency

1.2.1 Open S2 and turn on supply.

1.2.2 Set supply to 12V.

1.2.3 Set S1 to data state X.

1.2.4 Connect frequency counter and set controls to measure frequency.

1.2.5 Close for 5 seconds and measure frequency.

1.2.6 Open S2.

1.2.7 Set supply to 11V.

1.2.8 Repeat 1.2.3 through 1.2.6.

1.2.9 Set supply to 13V.

1.2.10 Repeat 1.2.3 through 1.2.6.

1.3 Spurious Outputs

1.3.1 Open S2 and turn on supply.

1.3.2 Set supply to 12V.

1.3.3 Connect spectrum analyzer.

1.3.4 Set S1 to data state W.

1.3.5 Close S2 for 5 seconds and measure spurious outputs.

1.3.6 Open S2.

1.3.7 Set S1 to data state X.

1.3.8 Close S2 for 5 seconds and measure spurious outputs.

1.3.9 Open S2.

1.3.10 Set supply to 11V.

1.3.11 Repeat 1.3.4 through 1.3.9.

1.3.12 Set supply to 13V.

1.3.13 Repeat 1.3.4 through 1.3.9.

1.4 Second Harmonic

1.4.1 Open S2 and turn on supply.

1.4.2 Set supply to 12V.

1.4.3 Connect spectrum analyzer.

1.4.4 Set S1 to data state W.

1.4.5 Close S2 for 5 seconds and measure second harmonic.

1.4.6 Open S2.

1.4.7 Set S1 to data state X.

1.4.8 Close S2 for 5 seconds and measure second harmonic.

1.4.9 Open S2.

1.4.10 Set supply to 11V.

1.4.11 Repeat 1.4.4 through 1.4.9.

1.4.12 Set supply to 13V.

1.4.13 Repeat 1.4.4 through 1.4.9.

1.5 Power Output

1.5.1 Open S2 and turn on supply.

1.5.2 Set supply to 12V.

1.5.3 Null power meter and adjust range scale for greatest accuracy.

1.5.4 Set S1 to data state W.

1.5.5 Close S2 for 5 seconds and measure power output.

1.5.6 Open S2.

1.5.7 Set S1 to data state X.

1.5.8 Close S2 for 5 seconds and measure power output.

1.5.9 Open S2.

1.5.10 Set supply to 11V.

1.5.11 Repeat 1.5.4 through 1.5.9.

1.5.12 Set supply to 13V.

1.5.13 Repeat 1.5.4 through 1.5.9.

1.6 Current (Transmit)

1.6.1 Open S2 and turn on supply.

1.6.2 Set supply to 12V.

1.6.3 Set ammeter to proper range.

1.6.4 Set S1 to data state W.

1.6.5 Close S2 for 5 seconds and measure current.

1.6.6 Open S2.

1.6.7 Set S1 to data state X.

1.6.8 Close S2 for 5 seconds and measure current.

1.6.9 Open S2.

1.6.10 Set supply to 11V.

1.6.11 Repeat 1.6.4 through 1.6.9.

1.6.12 Set supply to 13V.

1.6.13 Repeat 1.6.4 through 1.6.9.

1.7 Current (Warmup)

1.7.1 Open S2 and turn on supply.

1.7.2 Set supply to 12V.

1.7.3 Set ammeter to proper range.

1.7.4 Set S1 to data state W and measure current.

1.7.5 Set S1 to data state X and measure current.

1.8 15 Minute Stability (Mobile)

.8.1 Remove top half of outer foam jacket. This provides ventilation so that the mobile platform may be run continuously. The oscillator section remains enclosed by the inner foam sections.

1.8.2 Open S2 and turn on supply.

1.8.3 Set supply to 12V.

1.8.4 Connect frequency counter and set controls to measure frequency to nearest 0.1 Hz (count period of 10 sec.).

1.8.5 Connect counter to external 1 MHz time base (HP 106B).

1.8.6 Enable printer and close S2 for the 15 minute measurement period.

NOTE: The 15 minute stability may be ascertained without removing the outer foam by closing S2 for a 1 second interval each 60 seconds and measuring the output frequency down converted to 10 Hz on a period basis. (See Figure 1-2)

1.9 Short-Term Stability

1.9.1 Connect the U.U.T. as shown in Figure 1-2.

1.9.2 Open S2 and turn on supply.

1.9.3 Set supply to 12V.

1.9.4 Set the controls on the USM-207 as follows; Function to Period BXM=10, Gate Time to 10^6/sec., Sensitivity to 0.1V, Trigger Slope to positive, Trigger Multiplier to 0.1 and Selector Switch to common.

1.9.5 Close S2 and tone frequency synthesizer so that the difference frequency at the output of the mixer is 20 Hz.

1.9.6 Enable digital printer. The period of successive 0.5 second count intervals will be recorded to the nearest 0.1 micro-second.

1.9.7 $\Delta\tau$ (τ displayed on the counter) is the 0.5 sec. stability obtained by taking the difference between successive 0.5 second measurements.

1.9.8 $$(\Delta f/f)_{rms} = (-\Delta\tau_{rms})/(\tau^2 f)$$

$\Delta f/f$ = fractional frequency stability

$\Delta\tau$ = change two successive period measurements

$\Delta\tau_{rms}$ = RMS value of 100 successive measurements of $\Delta\tau$

f = frequency of U.U.T.

1.9.9 $$\Delta\tau_{rms} = \left(\left(\sum_{n=1}^{h=100} \Delta\tau_n\right)/n\right)^{\frac{1}{2}}$$

1.10 TEST DATA SHEET

PLATFORM TYPE ☐ MOBILE ☐ FIXED

Vcc		+11V	+12V	+13V
Frequency db	X			
Spurious Outputs DB Down	X			
	W			
Second Harmonic DB Down	X			
	W			
Power Output Watts	X			
	W			
Current (Transmit) MA.	X			
	W			
Current (Warmup) MA.	X			
	W			

W: Data State W
X: Data State Y

Comments: _____

_____

_____

_____

Performed by: _____

Date _____

TEST DATA SHEET

PLATFORM TYPE [✓] MOBILE [ ] FIXED

Vcc		+11V	+12V	+13V
Frequency db Mc	X	403.100 537	403.100 552	403.100 953
Spurious Outputs DB Down	X	54 db	53 db	54 db
	W	59 db	54 db	54 db
Second Harmonic DB Down	X	55 db	55 db	55 db
	W	55 db	55 db	55 db
Power Output Watts	X	.5 W	1.06 W	1.68 W
	W	.485 W	.99 W	1.52 W
Current (Transmit) MA.	X	252 ma	352 ma	450 ma
	W	240 ma	340 ma	420
Current (Warmup) MA.	X	63 ma	72 ma	78 ma
	W	62 ma	70 ma	76 ma

W: Data State W
X: Data State Y

Comments: 15 MINUTE STABILITY: AVERAGE = 1.46 HZ, RMS = 0.870 HZ (PER MIN)

0.5 SEC. STABILITY: 2 PP/10^9

Performed by: J Fenton

Date 1-27-71

Witnessed By: K. Field 1-27-71

TEST DATA SHEET

PLATFORM TYPE ☐ MOBILE ☑ FIXED

Vcc		+11V	+12V	+13V
Frequency ~~db~~ MC.	X	402.100568	402.100172	402.100276
Spurious Outputs DB Down	X	<60	<60	<60
	W	<60	<60	<60
Second Harmonic	X	55	<60	<60
DB Down	W	55	<60	<60
Power Output	X	3.40	4.7	6.04
Watts	W	3.44	4.73	5.98
Current(Transmit)	X	1.02A	1.24A	1.51A
MA.	W	1.03A	1.26A	1.50A
Current(Warmup)	X	.09A	1.10A	150 ma
MA.	W	.09A	1.10A	150 ma

W: Data State W
X: Data State Y

Comments: ____________________

Performed by: [signature]

Date 1-28-71

[signature]

1.11 List of Required Test Equipment

(Equivalent Equipments May be Substituted)

1. Power Supply (1); Power Designs Inc., Model 2015R
2. 25 db Pad (1); EMCO A-8420N
3. Directional Coupler (2); HP778D
4. Power Meter (1); General Microwave 454A
5. Ammeter; Triplet Model 625
6. Switch S1 (1) DPDT
7. Switch S2 (1) SPST
8. Spectrum Analyzer (1); HP 851B/8551B
9. Frequency Counter (1); USM-207
10. Frequency Synthesizer; Schlumberger FSM500/FS30
11. Standard Oscillator; HP 106B
12. Driver; HP 5105A
13. AF Amplifier; 15 Hz to 200 KHz, 40 db Audio Amplifier
14. Digital Printer; HP 562A

A+ - Primer Power
GNd - Ground
W - Data
X - Data
Y - Warmup
Z - Transmit

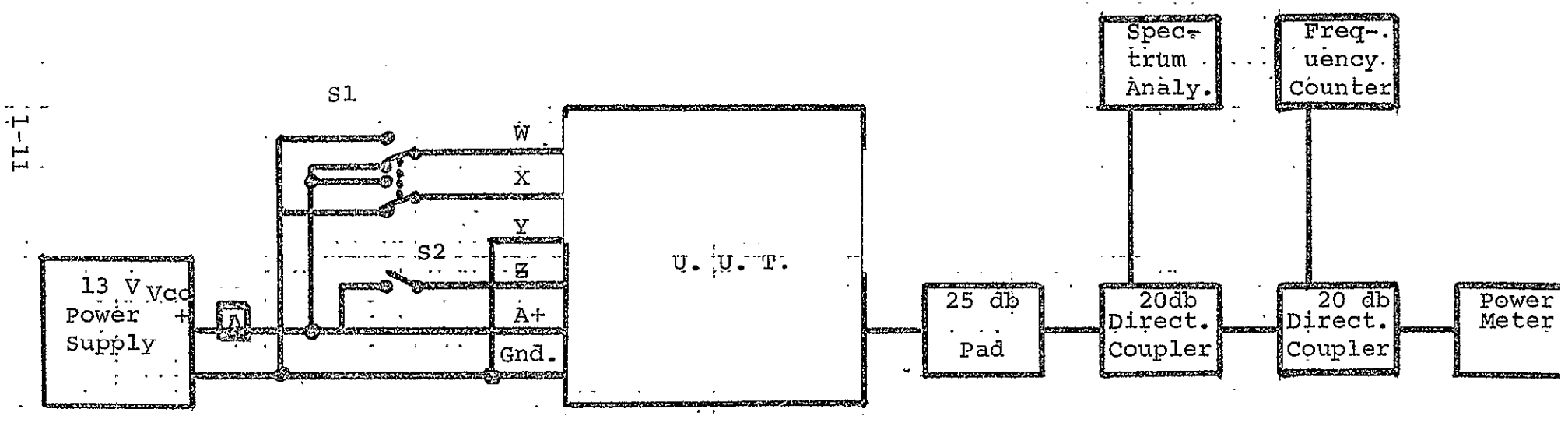


FIGURE 1-1.

RF PRELIMINARY TEST SETUP

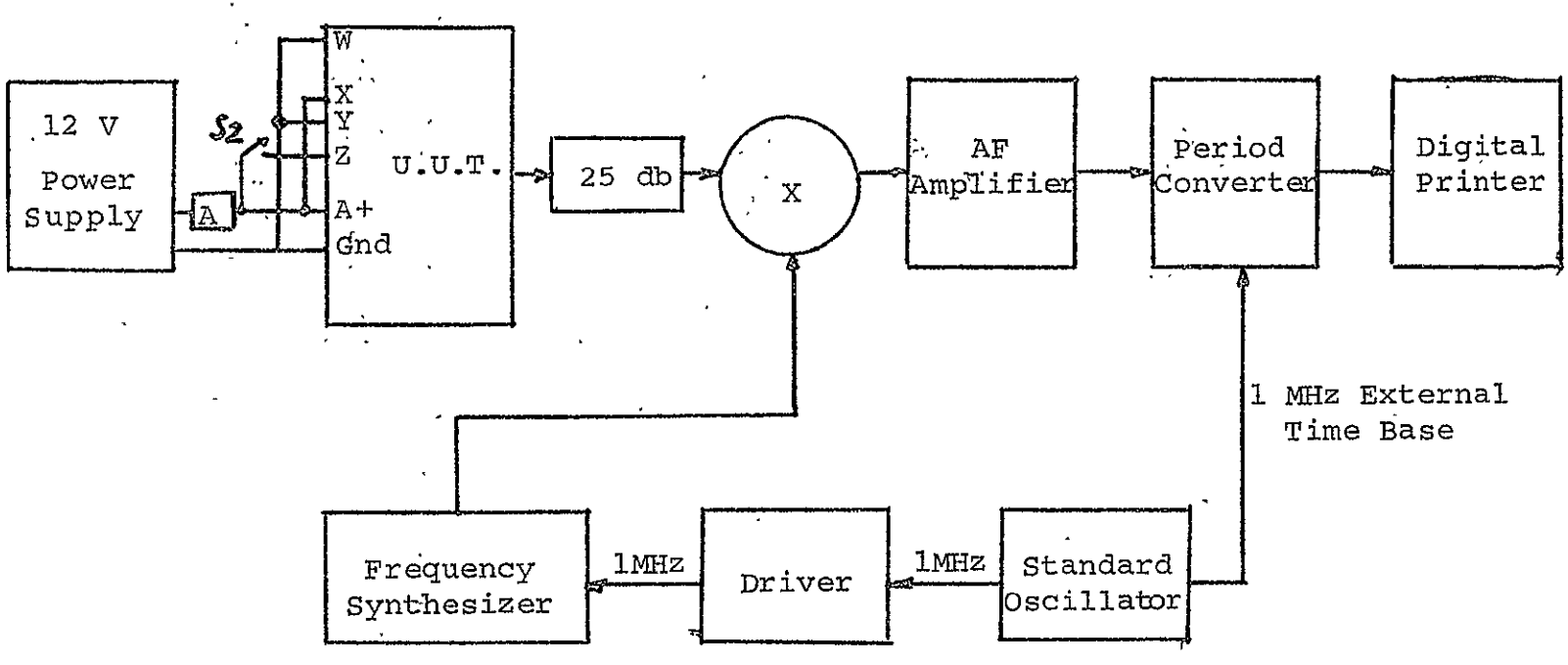


FIGURE 1-2.

RF OSCILLATOR MEASUREMENT TEST SETUP

DATA COLLECTION PLATFORM

ACCEPTANCE TEST PROCEDURE

2.0 DIGITAL SECTION

2.1 Preliminary: Procedures for testing the fixed and mobile platforms are identical.

2.1.1 Connect the U.U.T. (unit under test) as shown in Figure 2.9-1.

2.1.2 Connect the timing option input (IC-AB, Pin 1) to IC-AC, Pin 9.

2.1.3 Turn the +12 volt supply on. Turn the function generator and pulse generator on, and adjust for a 10 μsec 12 volt pulse at a one second repetition rate.

2.1.4 Record the "ON" current and the quiescent current in Table 2.8-1.

2.2 Master Timer

2.2.1 Connect the frequency counter to the U.U.T. TRANSMIT output (Pin Z) and set the controls to measure the period between positive transitions.

2.2.2 Disconnect the pulse generator output. This allows the master timer to trigger the platform independently. Take five consecutive readings and record the results in Table 2.8-1.

2.2.3 Reconnect the pulse generator output.

2.3 Master Clock Frequency

2.3.1 Set the frequency counter controls to measure the "transmit" pulse duration. Record the measurement in Table 2.8-1.

2.4 A/D Converter Measurements

2.4.1 Connect Channel A of the oscilloscope to TP5.

2.4.2 Connect Channel B to pin T (load data).

2.4.3 Adjust the oscilloscope so the leading edges of consecutive Load Data pulses are coincident with each of the first through eighth vertical graticule lines.

2.4.4 Each of the boxes from position 1 through 8 represent one word of the data format corresponding to the analog data input, with the last data channel in position no. 8. (For the mobile platform, boxes 6, 7 and 8 correspond to the three analog inputs of the mobile platform.)

2.4.5 Adjust the sensor potentiometer for 2.000 volts. Monitoring the oscilloscope, photograph the binary pattern.

2.4.6 Adjust the sensor potentiometer for 0.000 volts. Monitoring the oscilloscope, photograph the binary pattern.

2.4.7 Adjust the sensor potentiometer for some random voltage between 0.000 and 2.000 volts. Monitoring the oscilloscope, photograph the binary pattern, and record the sensor voltage.

2.4.8 From the photographed binary patterns with sensor voltages 0.000 and 2.000, ascertain that:

a. The binary word for each channel is within 1 bit of the binary word for any other channel.

b. Each channel is within 1 bit of binary zero; i.e., the three allowable conditions for any channel are

a) 00000000 (eight zeros)

b) 00000001 (seven zeros and a one)

c) 11111111 (eight ones)

2.4.9 For the photographed binary pattern with the sensor input set between 0.000 and 2.000, ascertain that the binary pattern indicates the sensor voltage within ±10 mv. Weigh each bit according to table 2.4-1.

TABLE 2.4-1.

	Bit No.	Weight
MSB	#1	1000.96 mv
	#2	500.48 mv
	#3	250.24 mv
	#4	125.12 mv
	#5	62.56 mv
	#6	31.28 mv
	#7	15.64 mv
LSB	#8	7.82 mv

2.5 Signature and Encoder

2.5.1 Ground TP5 through a 1K resistor.

2.5.2 Monitor DATA, pin W, with Channel A of the scope.

2.5.3 Monitor pin 3 of IC-B with Channel B.

2.5.4 Photograph and compare the encoded test signature with the test signature and record results in Table 1.

2.6 Final

2.6.1 Reconnect the delay timing to the proper option.

2.6.2 Remove the trigger input line from the R8, R9 junction.

2.7 List of Required Test Equipment

(Equivalent equipments may be substituted.)

1. Function Generator (1); Wavetek Model III
2. Pulse Generator (1); Data Pulse Model 101
3. Power Supply, 15 Volt, 100 ma, Adjustable (1); Power Designs Model 5015A
4. Digital Voltmeter (1); Dana Model 5500-76-E1
5. Oscilloscope (1); Tektronix Model 547
6. Frequency Counter (1); AEL USM-207
7. Preamp (1); Tektronix, Type M

2.8 TEST DATA SHEET

TABLE 2.8-1

Date _____

Performed by _____

Platform Type ☐ Mobile ☐ Fixed

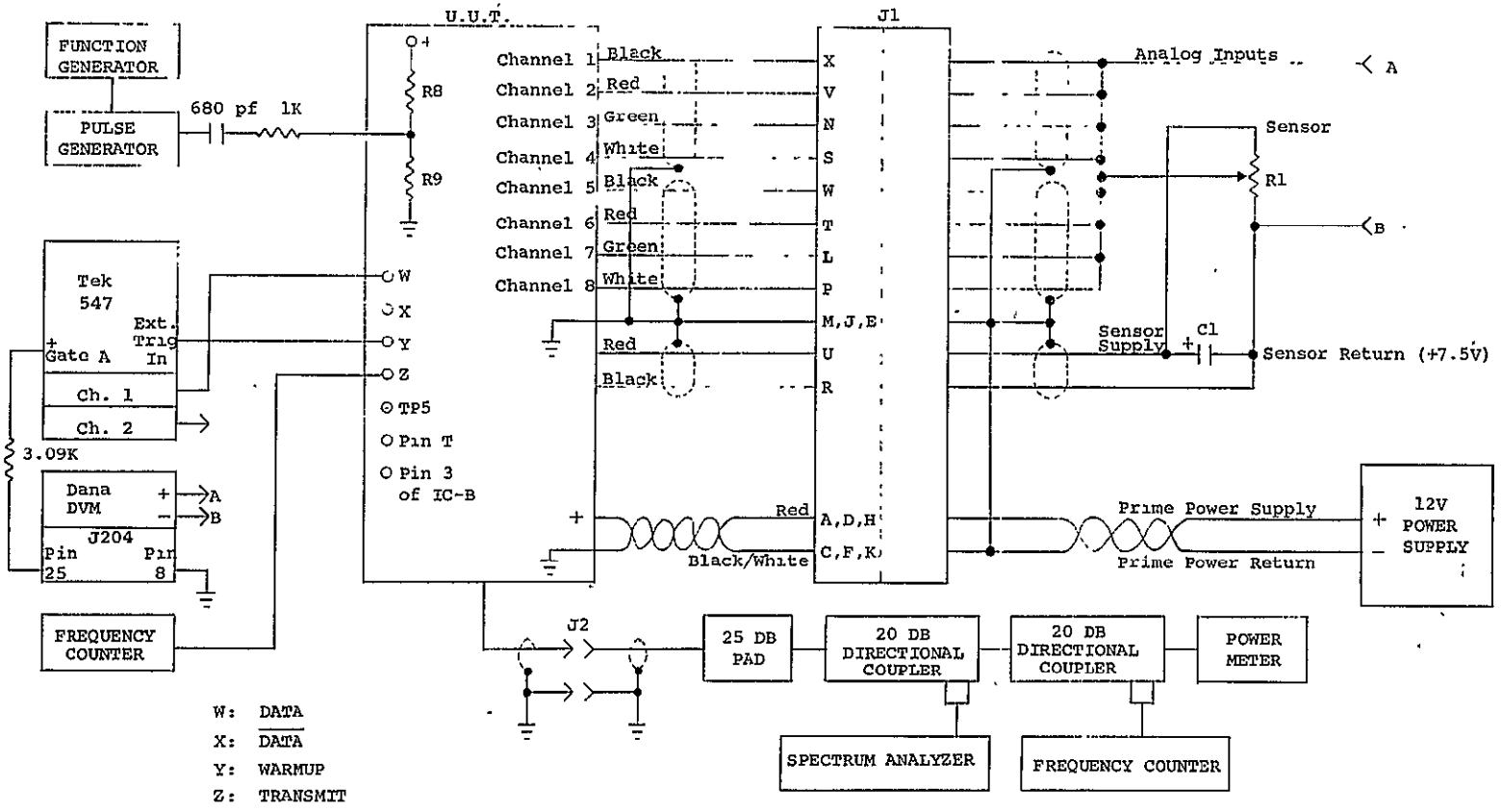
TEST PARAMETER	ACTUAL	SPECIFICATION	
		MOBILE	FIXED
2.1 On Current Quiescent Current		30 ma 0.2 ma	
2.2 Master Timer Repetition Rate	1. 2. 3. 4. 5.	60 ±4.5 sec.	120 ±10 sec.
2.3 Transmit Pulse Duration		1 ±.125 sec.	0.1 ± .0125 sec.
2.4 Binary Word for V_X = 0.000	☐ 00000001 ☐ 00000000 ☐ 11111111	Eight zeros ± 1 bit	
Binary Word for V_X = 2.000	☐ 00000001 ☐ 00000000 ☐ 11111111	Eight zeros ± 1 bit	
Binary Word for 0.000 > V_X > 2.000 V	Binary Word _____ = ____V Binary Word Equivalent =____V -Sensor Voltage ____V	= ±10 mv	

TEST DATA SHEET

TABLE 2.8-1 (Cont.)

TEST PARAMETER	ACTUAL		SPECIFICATION	
			MOBILE	FIXED
2.5 Signature and Encoder	Symbol 1	Symbol 2		

	1	0
Bit 1		
Bit 2		
Bit 3		
Bit 4		
Bit 5		
Bit 6		
Bit 7		
Bit 8		
Bit 9		
Bit 10		
Bit 11		
Bit 12		
Bit 13		
Bit 14		
Bit 15		
Bit 16		

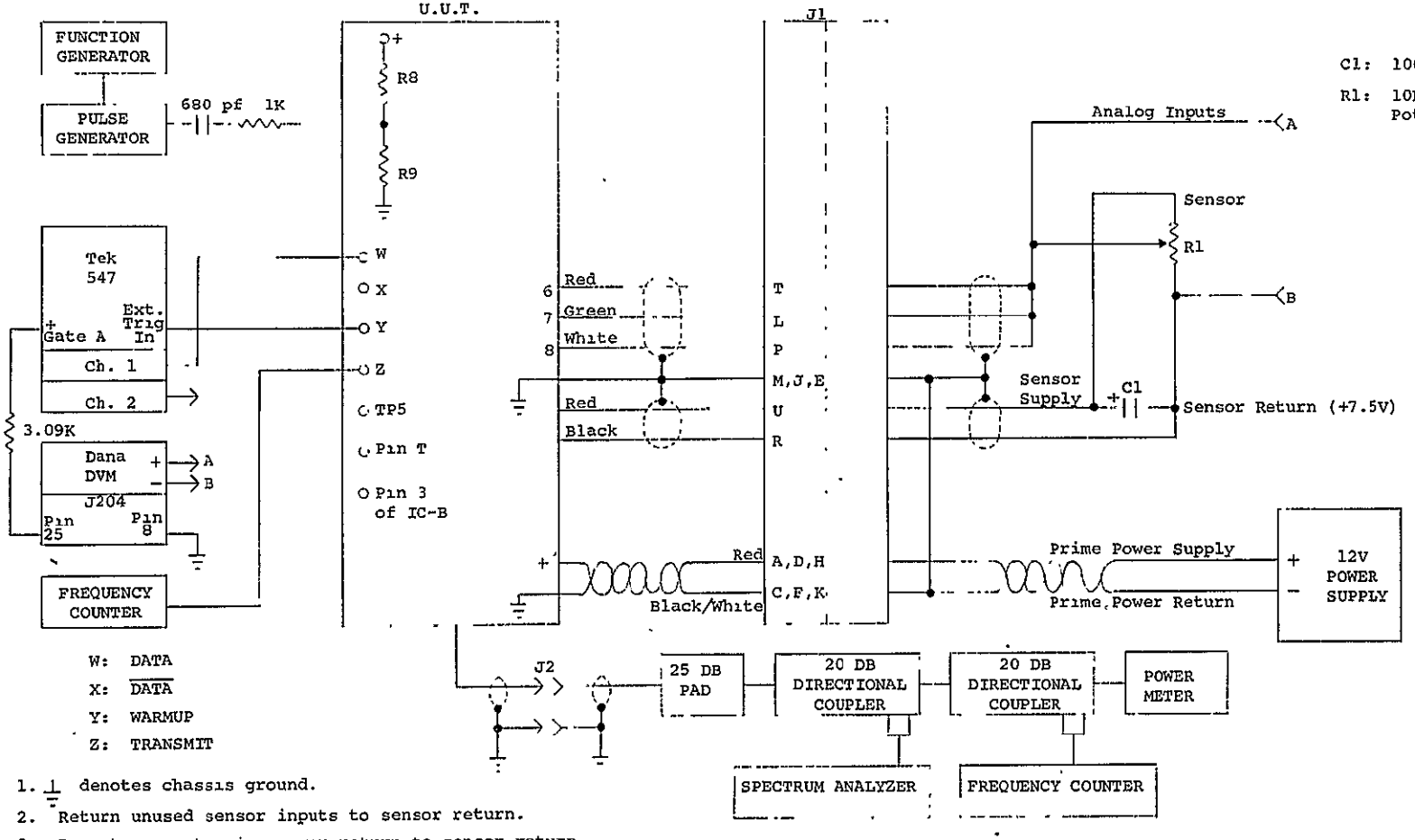


NOTE: 1. ⏚ denotes chassis ground.
2. Return unused sensor inputs to sensor return.
3. Do not connect prime power return to sensor return.
4. Channels 1 through 4 - Gray #1 jacketed cable.
5. Channels 5 through 8 - Gray #2 jacketed cable.
6. Sensor Supply - Black jacketed cable.

FIGURE 2.9.1-1

TEST INTERCONNECTING DIAGRAM

FIXED DATA COLLECTION PLATFORM



NOTE: 1. ⏚ denotes chassis ground.
2. Return unused sensor inputs to sensor return.
3. Do not connect prime power return to sensor return.
4. Channels 6, 7 and 8 - Gray jacketed cable.
5. Sensor Supply - Black jacketed cable.

FIGURE 2.9.1-2

TEST INTERCONNECTION DIAGRAM

MOBILE DATA COLLECTION PLATFORM

2.9.2 Test Data Sheet Example

Figures 2.9.2-1 through 2.9.2-7 were taken on mobile and fixed platforms during the actual acceptance tests according to the test plan as outlined in the DCP Acceptance Test Procedure.

The test data sheet example is filled in using the data from these photographs.

Figure	Sensor Voltage	Platform	Test Point
2.9.2-1	2.000 V	Fixed	TP5
2.9.2-2	0.000 V	Fixed	TP5
2.9.2-3	1.2923 V	Fixed	TP5
2.9.2.4	2.000 V	Mobile	TP5
2.9.2-5	0.000 V	Mobile	TP5
2.9.2-6	.9142 V	Mobile	TP5
2.9.2-7	---	Fixed	Pin 3 of IC-B

Photograph 2.9.2-6 shows an error in position channel 6. After the photograph 2.9.2-6 was taken, prior to shipment, analog sensor inputs were shielded to provide more immunity from electrical noise.

The anomaly has not since been observed.

Using Table 2.4-1, and photograph 2.9.2-3, we calculate the voltage indicated by the binary serial word as indicated in the photograph.

Bit	0 or 1	Weight
#1	1	1000.96 mv
#2	0	---
#3	1	250.24 mv
#4	0	---
#5	0	---
#6	1	31.28 mv
#7	1	15.64 mv
#8	0	----
Sum of Weights		1.2981 V
Sensor Voltage Input		1.2923 V

0.0068 = 6.8 mv

The error is 6.8 mv, which indicates an accuracy of better than 1%.

Refer to Figures 2.9.3 and 2.9.4 for hookup configurations for field use.

2.9.2 TEST DATA SHEET EXAMPLE

I. TEST DATA SHEET

TABLE 2.8-1

Date 1/28/11

Performed by T Lumpkin

Platform Type ☐ Mobile ☑ Fixed

TEST PARAMETER	ACTUAL	SPECIFICATION	
		MOBILE	FIXED
2.1 On Current Quiescent Current	29 ma < .2 ma	30 ma 0.2 ma	
2.2 Master Timer Repetition Rate	1. 114.1 sec 2. 114.9 sec 3. 114.9 sec 4. 114.9 sec 5. 114.9 sec	60 ±4.5 sec.	120 ±10 sec.
2.3 Transmit Pulse Duration	.0999 sec	1 ±.125 sec.	0.1 ± .0125 sec.
2.4 Binary Word for V_X = 0.000	[0] 00000001 [2] 00000000 [6] 11111111	Eight zeros ± 1 bit	
Binary Word for V_X = 2.000	[1] 00000001 [7] 00000000 [0] 11111111	Eight zeros ± 1 bit	
Binary Word for 0.000 > V_X > 2.000 V	Binary Word 10100110 = 1.2981 V Binary Word Equivalent = 1.2923 V -Sensor Voltage V 6.8m V	= ±10 mv	

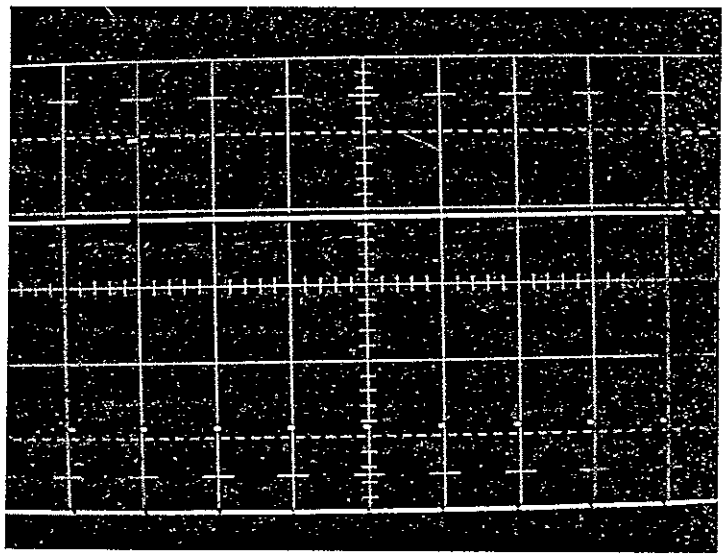
2.9.2 TEST DATA SHEET EXAMPLE

TEST DATA SHEET

TABLE 2.8-1 (Cont.)

TEST PARAMETER		ACTUAL		SPECIFICATION	
				MOBILE	FIXED
2.5 Signature and Encoder		Symbol 1	Symbol 2		
	1 / 0				
Bit 1	/ X	0	/		
Bit 2	X /	/	/		
Bit 3	/ X	/	0		
Bit 4	X /	0	/		
Bit 5	/ X	/	/		
Bit 6	/ X	0	/		
Bit 7	X /	/	0		
Bit 8	/ X	0	/		
Bit 9	/ X	/	0		
Bit 10	X /	/	0		
Bit 11	X /	/	0		
Bit 12	/ X	0	0		
Bit 13	/ X	/	/		
Bit 14	/ X	/	0		
Bit 15	/ X	/	/		
Bit 16	/ X	0	0		

Figure
2.9.2-1



TP5

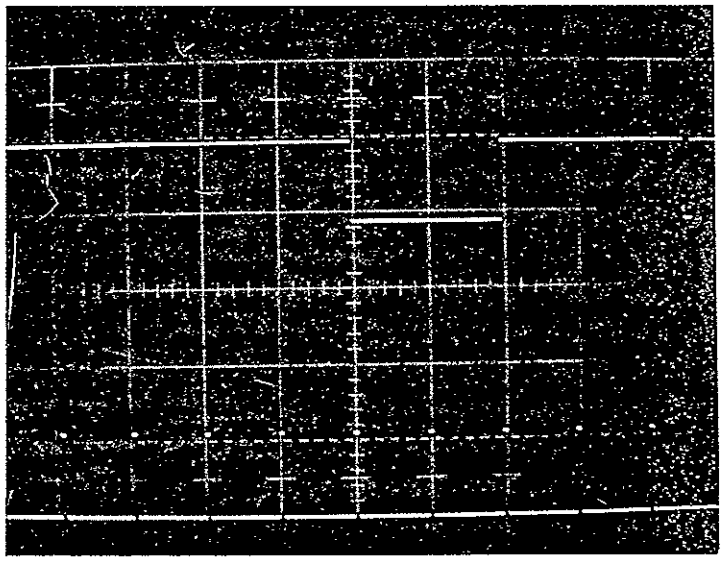
Load Data

Sensor Voltage
Input = 2.000V

Channel 1 2 3 4 5 6 7 8

Trivia

Figure
2.9.2-2



TP5

Load Data

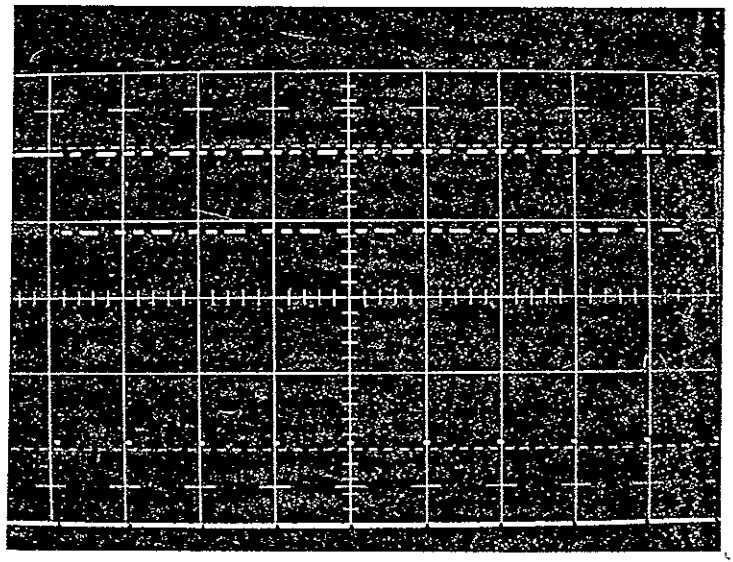
Sensor Voltage
Input = 0.000V

Channel 1 2 3 4 5 6 7 8

Trivia

FIXED
PLATFORM

Figure
2.9.2-3



TP5

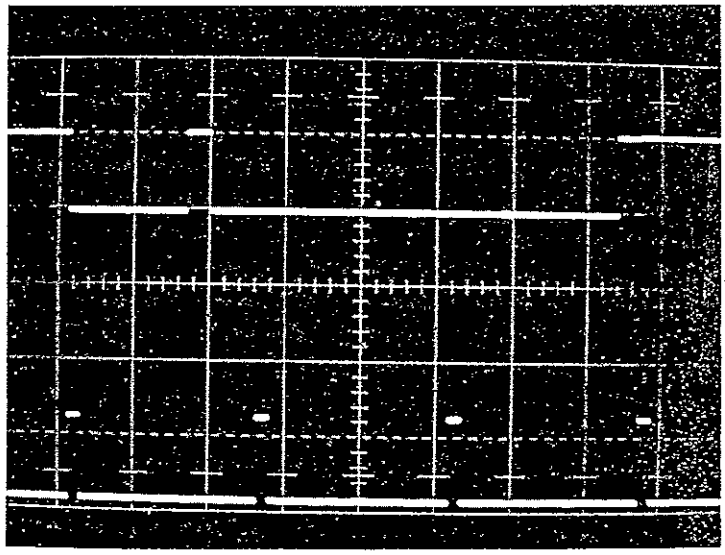
Load Data

Sensor Voltage
Input = 1.2923V

Channel 1 2 3 4 5 6 7 8

Trivia

Figure
2.9.2-4



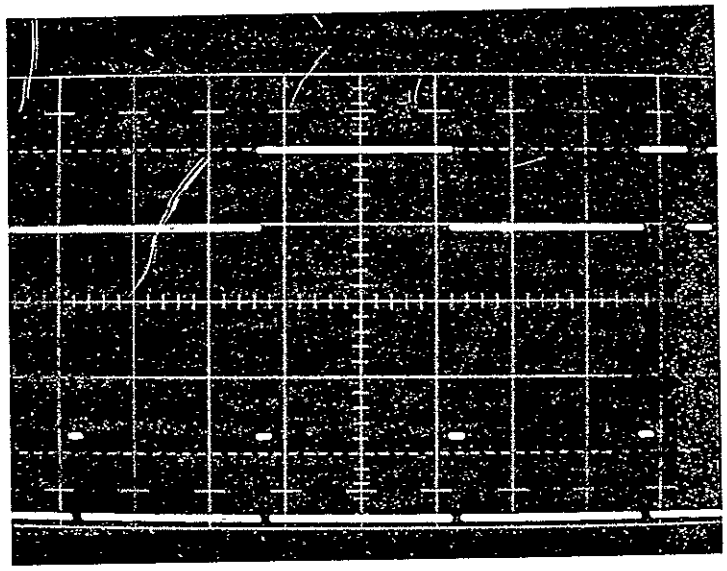
TP5

Load Data

Sensor Voltage
Input = 2.000V

Ch.6 Ch.7 Ch.8

Figure
2.9.2-5



TP5

Load Data

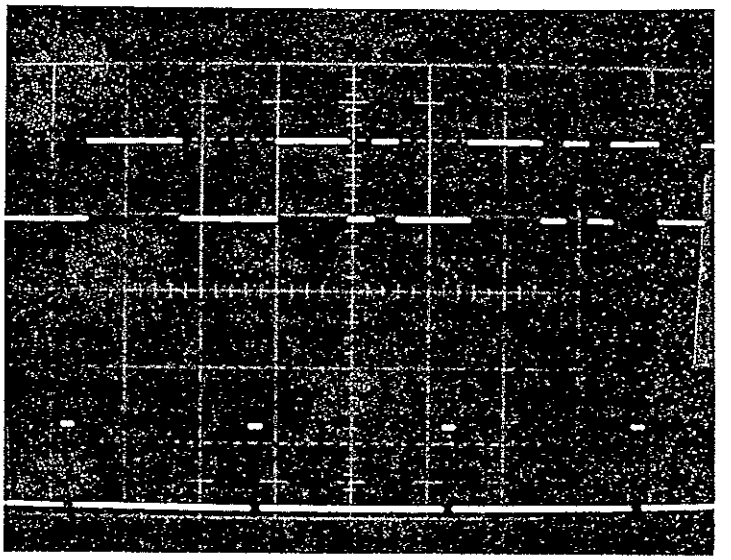
Sensor Voltage
Input = 0.000V

Ch.6 Ch.7 Ch.8

40

MOBILE
PLATFORM

Figure
2.9.2-6



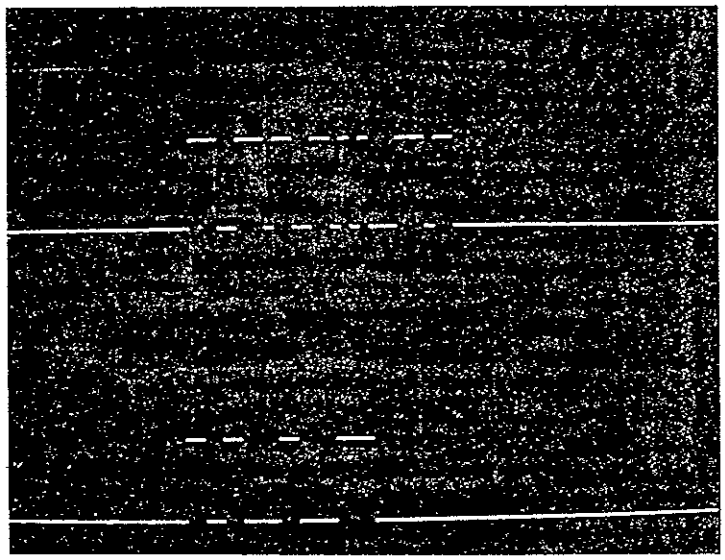
TP5

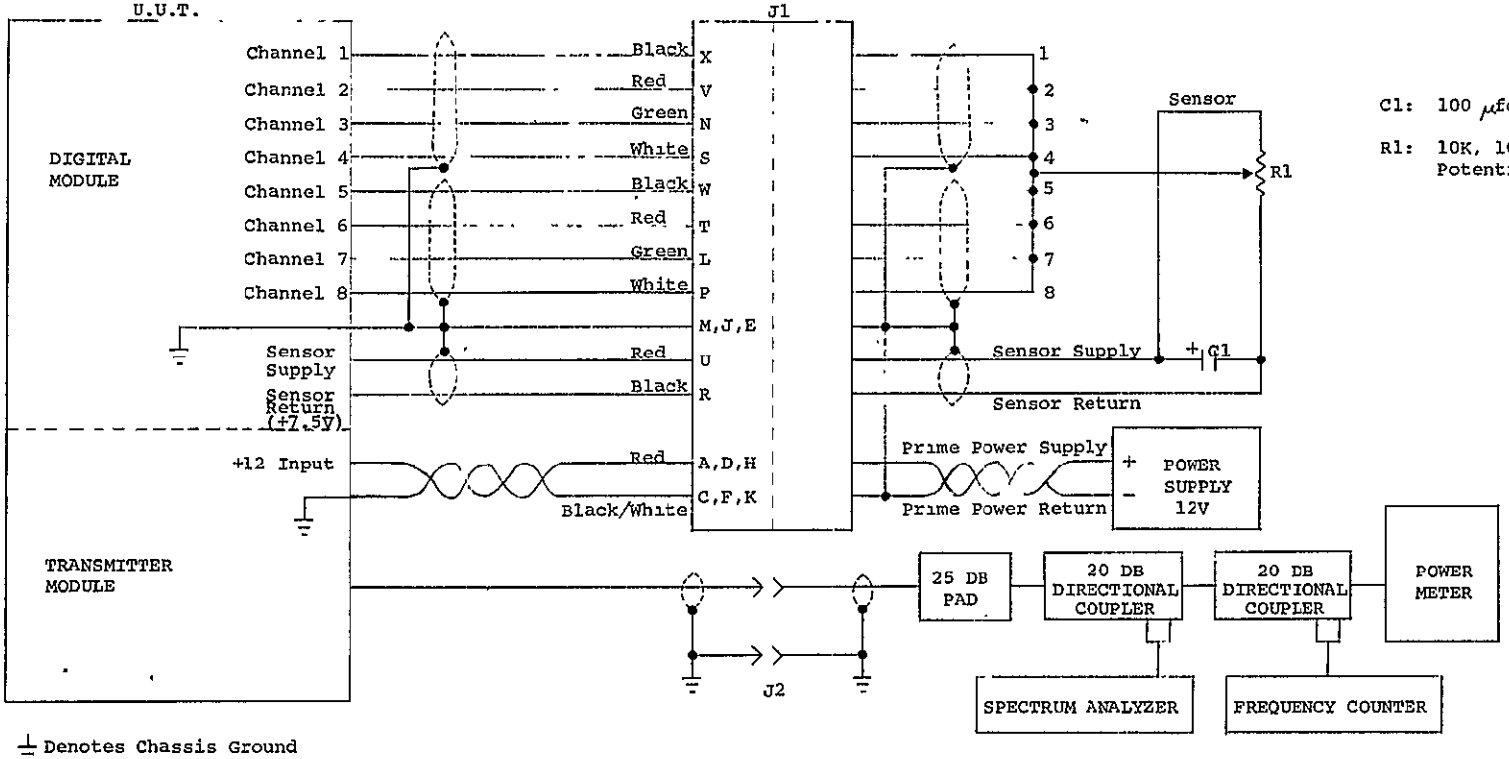
Pin T
(Load Data)

Sensor Voltage
Input = 0.9142V

Ch.6 Ch.7 Ch.8

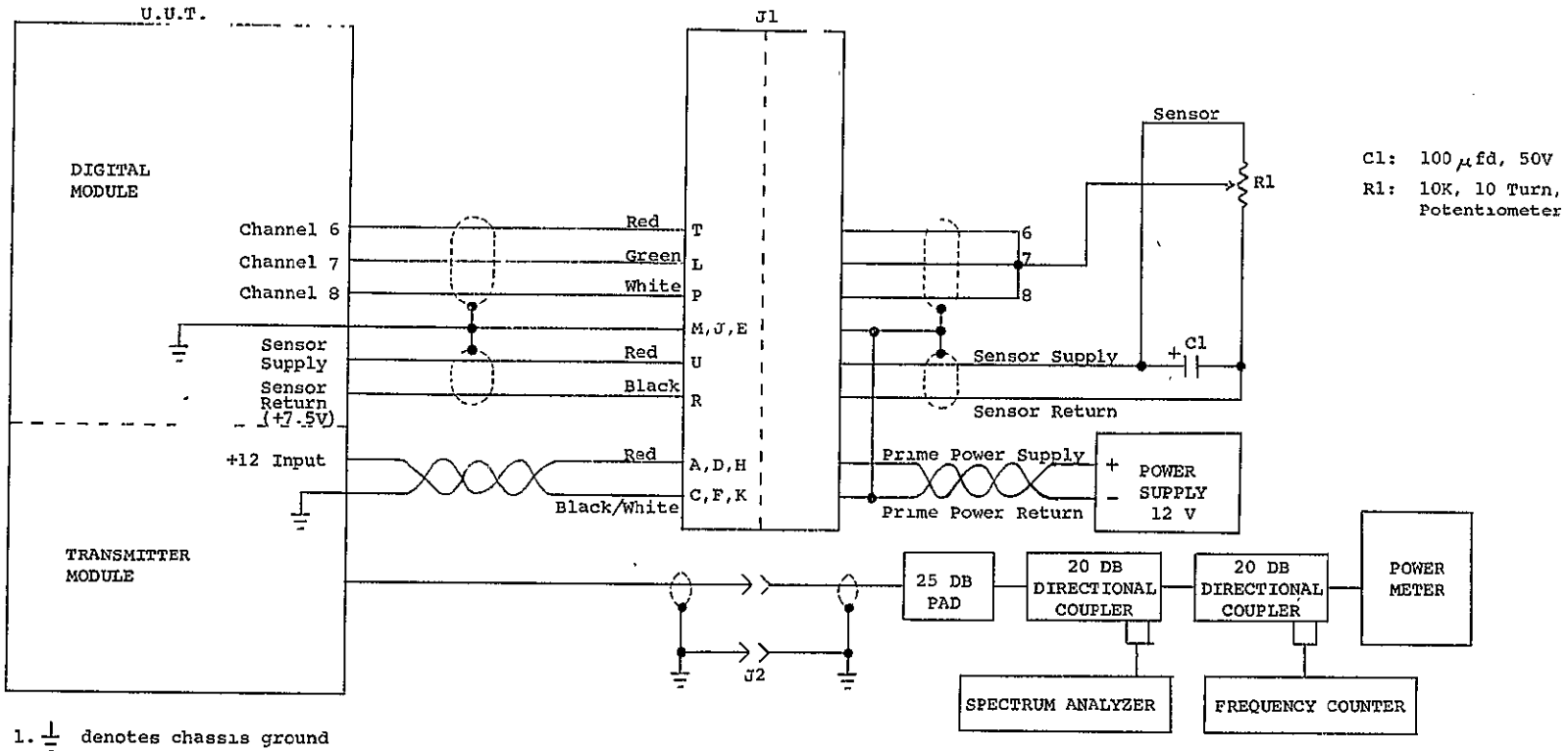
igure
.9.2-7





NOTE: 1. ⏚ Denotes Chassis Ground
2. Return unused sensor inputs to sensor return.
3. Do not connect prime power return to sensor return.
4. Channels 1 through 4 - Gray #1 jacketed cable.
Channels 5 through 8 - Gray #2 jacketed cable.
Sensor Supply - Black jacketed cable.

FIGURE 2.9.3
FIELD USE INTERCONNECTING DIAGRAM
FIXED DATA COLLECTION PLATFORM



NOTE: 1. ⏚ denotes chassis ground

2. Return unused sensor inputs to sensor return.
3. Do not connect prime power return to sensor return.
4. Channels 6, 7 and 8 - Gray jacketed cable.
   Sensor Supply - Black jacketed cable.

FIGURE 2.9.4

FIELD USE INTERCONNECTING DIAGRAM

MOBILE DATA COLLECTION PLATFORM