
# The LEON3 processor and SpaceWire Codec and their Application

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# Outline

- Enabling technologies
- LEON3-FT
- SpaceWire and RMAP
- Devices and systems
- Applications
  - BELA (DLR, Germany)
  - SIR2 (University of Bergen, Norway)
  - Prisma (SSC, Sweden)
  - ARGO (Taiwan)
  - TacSat-4
- Conclusions

# Enabling technologies

The following enabling technologies allow the development of advanced FPGA and ASIC System-on-a-Chip designs for on-board application at an unprecedented rate:

- SPARC 32-bit RISC architecture:
  - standardized instruction set portable between processor generations: e.g. ERC32, LEON2/3/4
- Debug Support Unit:
  - instruction and on-chip bus tracing
  - Debug Link UART: remote read/write
- AMBA AHB/APB on-chip buses & PnP
- SpaceWire link with RMAP

# The LEON3-FT IP core set

- The LEON3-FT is an advanced fault-tolerant 32-bit processor integer unit implementing the SPARC V8 standard instruction set
- The GRFPU-FT is a fault-tolerant IEEE-754 compliant fully pipelined floating point unit supporting single and double precision (32- and 64-bit floats) data formats
- The MMU-FT is a fault-tolerant SPARC V8 reference memory management unit with a translation look-aside buffer (TLB)
- Test silicon available since 2005 (250 nm and 180 nm)

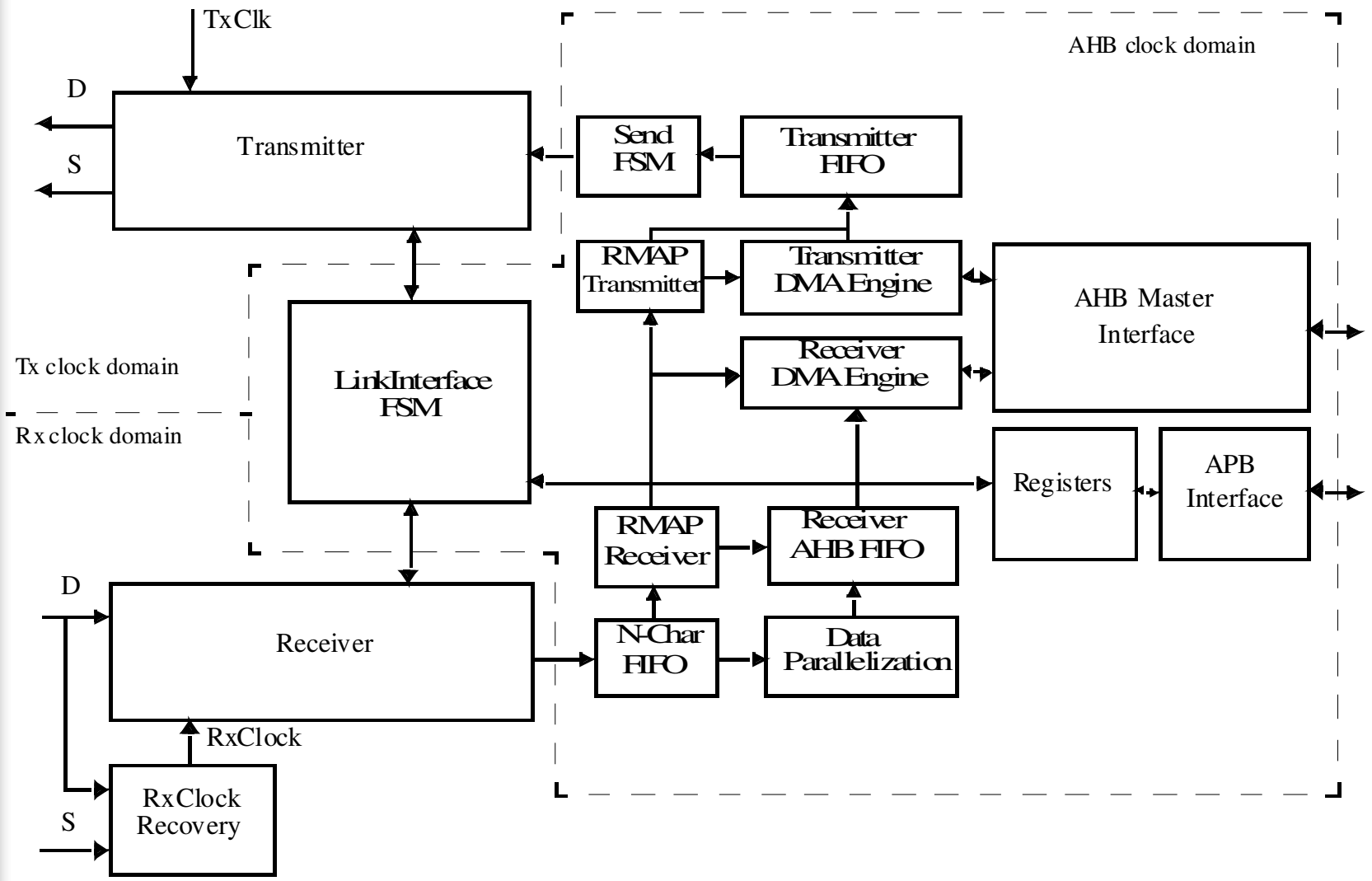
# LEON status

- LEON independently certified by Sparc International
- Verified for space use according to the stringent requirements of the European Space Agency (ESA)
- Used as reference design in the UMC low power design package
- Used as reference design by major tool vendors (Synopsis, Synplicity, Mentor, Spirit)
- Promoted by Cadence through the Open-Choice programme
- Partnership with Aldec for VHDL simulation
- Partnership with Actel for military / space applications

# SpaceWire and RMAP

- High-speed data link serial interface with Data-Strobe encoding (2 Mbit/s – 400 Mbit/s)
- Point-to-point, uses routers
- SpaceWire standard is based on IEEE-Std-1355 (DS-Link from Inmos)
- ECSS-E-50-12A standard for space
- Remote Memory Access Protocol (RMAP):
  - Allows remote read and write
  - Single byte, half-word, word or burst
  - Verified write
  - Read-modify-write
  - No support required from CPU on receiving side

# GRSPW: SpaceWire and RMAP



# GRSPW - Characteristics

- Supports AMBA AHB with high throughput
- Supports full RMAP
- Fault-tolerant version /w memory protection
- Portable between technologies and tools: Xilinx, Actel and ASIC
- Small footprint on Actel (Companion Core)
- RTEMS and VxWorks drivers available

| Core configuration | RTAX2000S-1 | ASIC |
|---|---|---|
| GRSPW | 2,800 / 2 / 40 / 100 | 10,000 gates |
| GRSPW + RMAP | 3,600 / 2 / 40 / 100 | 15,000 gates |
| GRSPW-FT | 2,900 / 4 / 40 / 100 | 11,000 gates |
| GRSPW-FT + RMAP | 3,700 / 4 / 40 / 100 | 16,000 gates |

# Devices and Deliverables

- Devices
  - LEON3-RTAX – Actel FPGA
  - GR701 - Companion Chip – Actel FPGA
  - UT699RH – Aeroflex
  - GR-RASTA – Xilinx FPGA based prototyping
- Different type of deliverables to customers:
  - LEON3FT / GRLIB-FT VHDL/EDIF netlists
  - LEON3FT-RTAX programming files
  - LEON3FT-RTAX devices

# LEON3-RTAX, Actel RTAX2000S

LEON3-RTAX is a LEON3-FT implemented using Actel RTAX2000S FPGA devices

Characteristics:

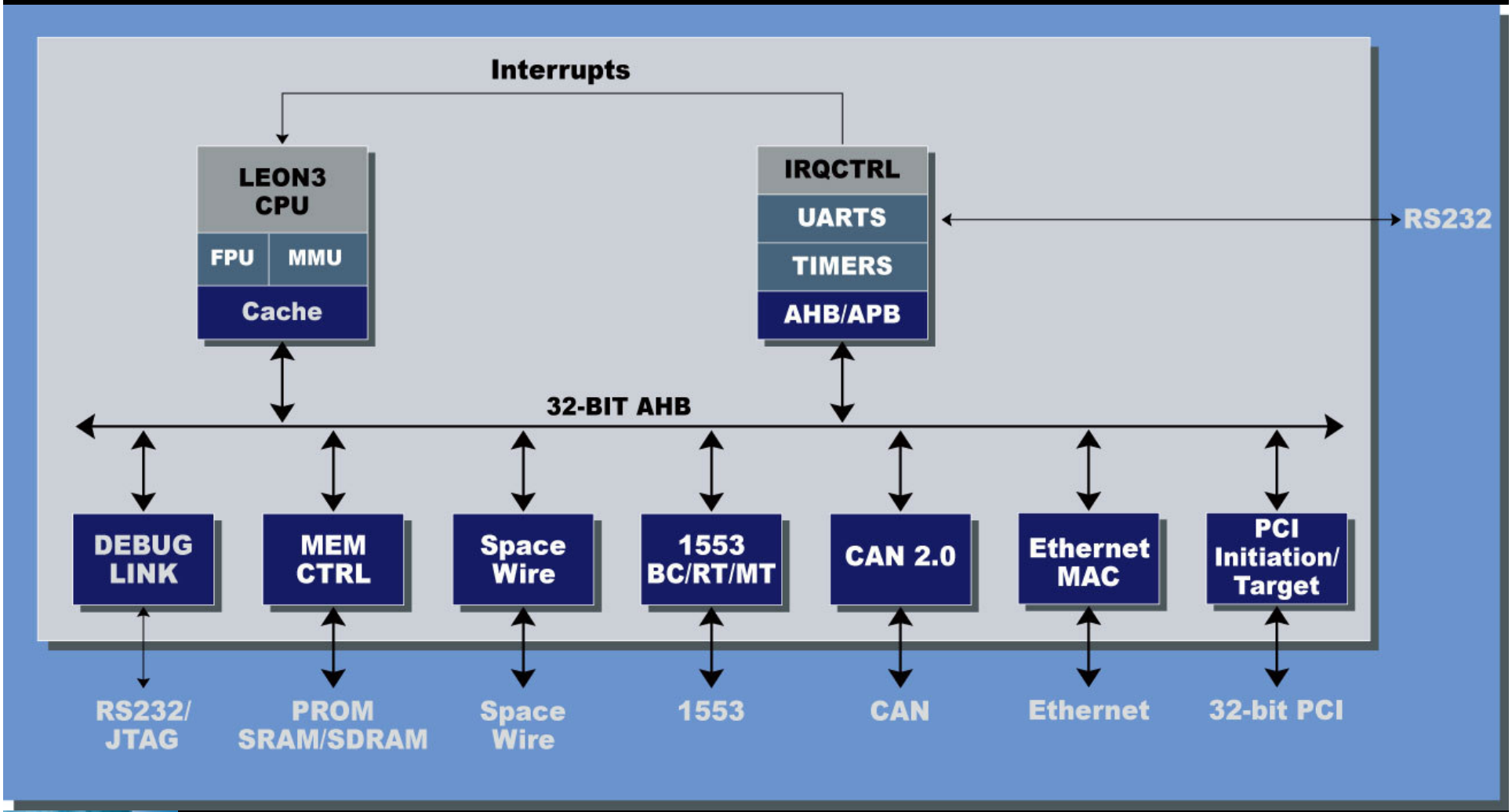
- Actel RTAX2000S -1
- CCGA624 or CQFP352
- 20-25 MHz system frequency, 33 MHz PCI
- Up to 100 MBPS SpaceWire

Delivery:

- Programmed component
- Programming file
- Individual IP core netlists (supports Actel Libero design flow)
- Prototyping using commercial FBG896 parts with adapter

Several systems already shipped

# LEON3-RTAX, Architecture



# LEON3-RTAX, Configurations

| Configuration name | Instrument Controller-1 | Instrument Controller-2 | Spacecraft Controller-1 | Spacecraft Controller-2 | Spacecraft Controller-3 | Spacecraft Controller-4 |
|---|---|---|---|---|---|---|
| Configuration ID (CID) | 1 | 2 | 3 | 4 | 5 | 6 |
| LEON3FT Integer Unit | Yes | Yes | Yes | Yes | Yes | Yes |
| Hardware multiply&divide | | | | | | Yes |
| Power down mode | | | | | | Yes |
| Memory Management Unit | | | | | | Yes |
| Floating Point Unit | Yes | Yes | Yes | | | |
| Debug Support Unit | Yes | Yes | Yes | Yes | Yes | Yes |
| UART Debug Link | Yes | Yes | Yes | Yes | Yes | Yes |
| JTAG Debug Link | | | | | Yes | |
| On-Chip Memory | 4 kbytes | | 2 kbytes | | | |
| 1553 RT | 1 | | | | | |
| 1553 BC/RT/MT | | | 2 | | | |
| SpaceWire | | 2 | | 3 | 2 | |
| CAN 2.0B | 1 | | | | 1 | |
| PCI Initiator/Target/Arbit. | | | | | | Yes |
| Ethernet MAC | | | | | | Yes |
| Memory Controller | Yes | Yes | Yes | Yes | Yes | Yes |
| SDRAM Support | | | | Yes | Yes | Yes |
| Standard peripherals | Yes | Yes | Yes | Yes | Yes | Yes |
| Package | CQFP352 | CQFP352 | CQFP352 | CCGA624 | CCGA624 | CCGA624 |

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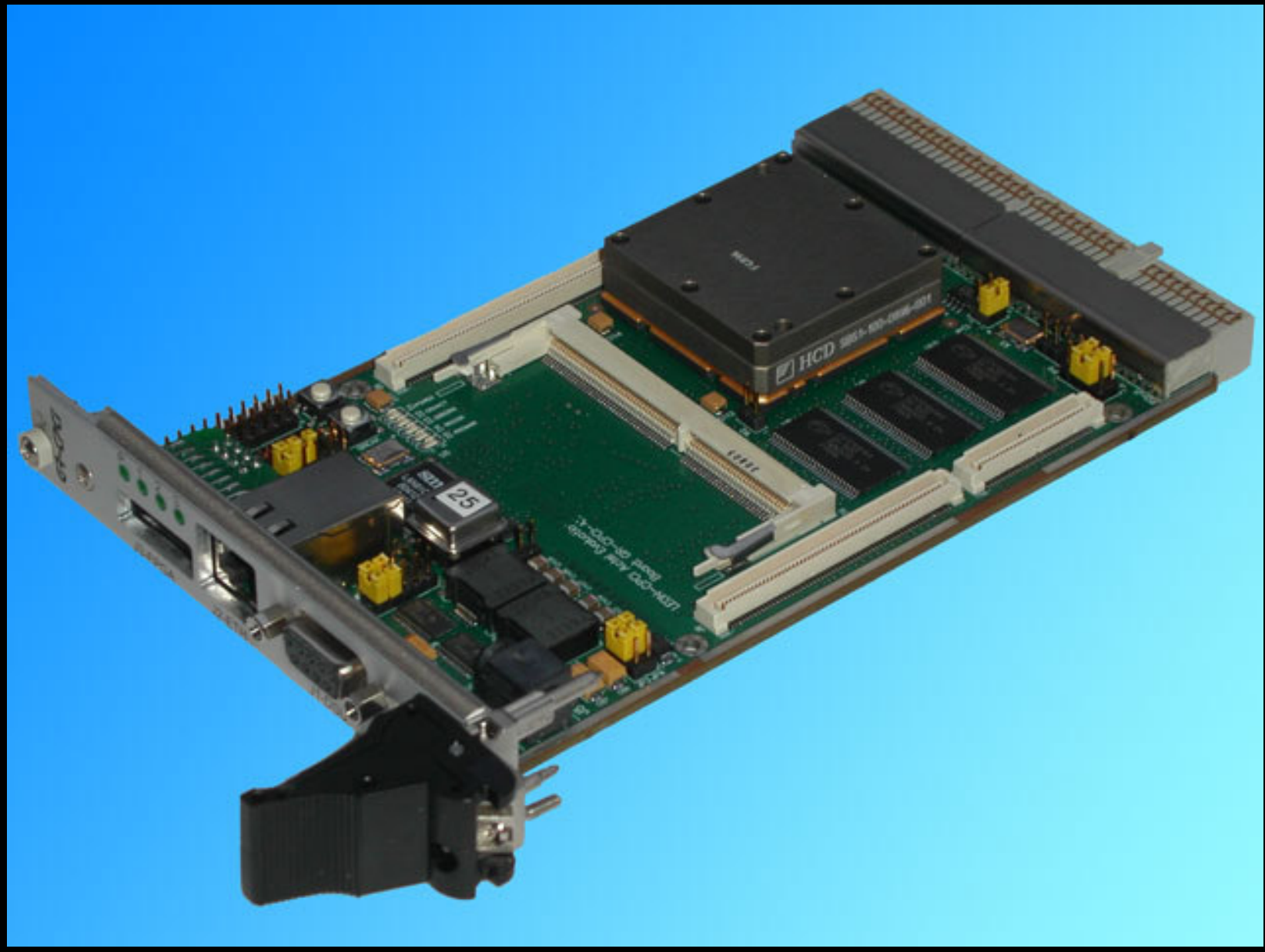
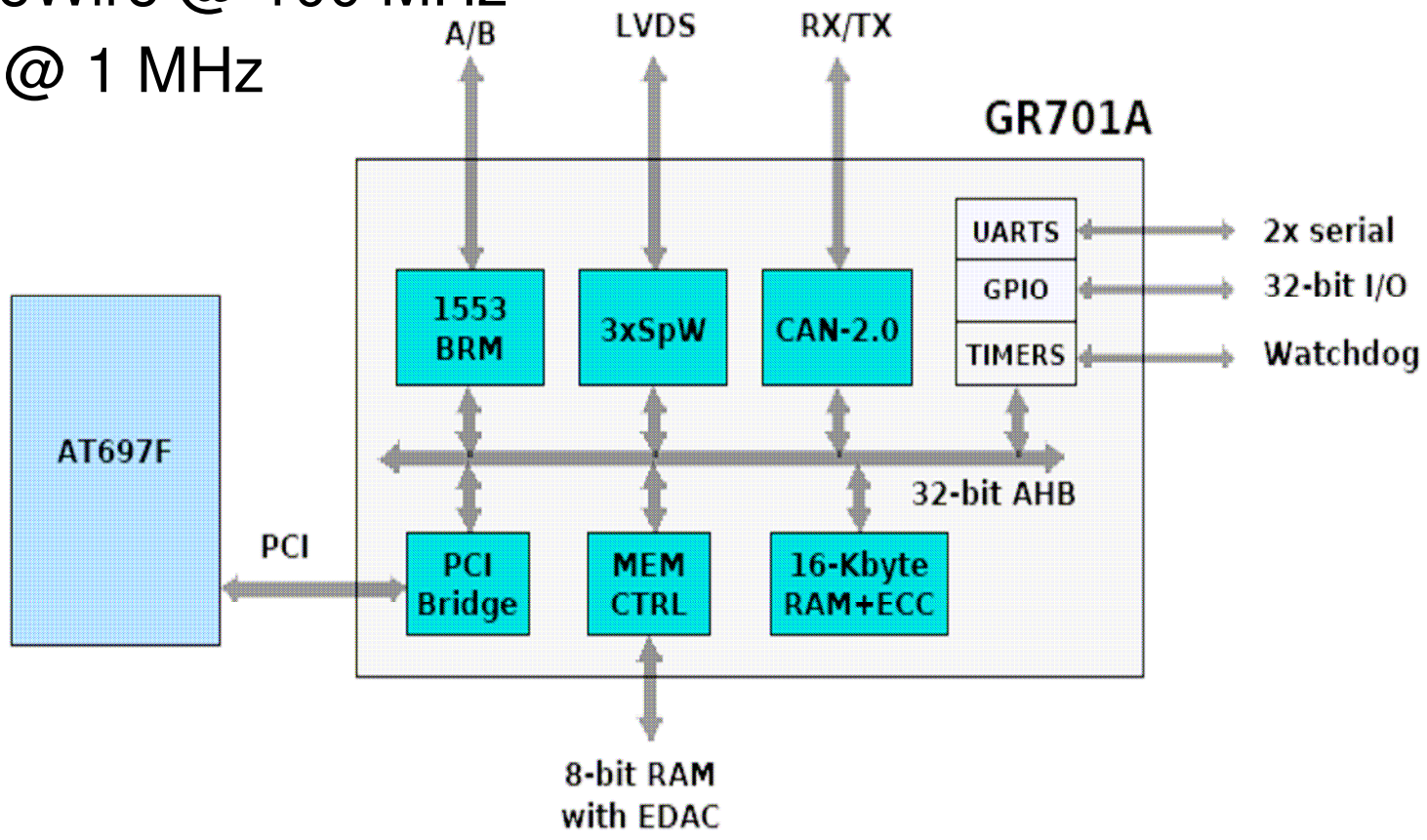
# LEON3-RTAX, GR-CPCI-AX2000



# GR701 - Companion Chip

PCI based companion chip implemented on RTAX2000S:

- PCI @ 33 MHz (Actel)
- 1553 @ 24 MHz (Actel)
- SpaceWire @ 100 MHz
- CAN @ 1 MHz



# GRESB - Ethernet SpaceWire Bridge

Ethernet to SpaceWire bridge (with CAN 2.0)

Supports multiple links, routing and RMAP

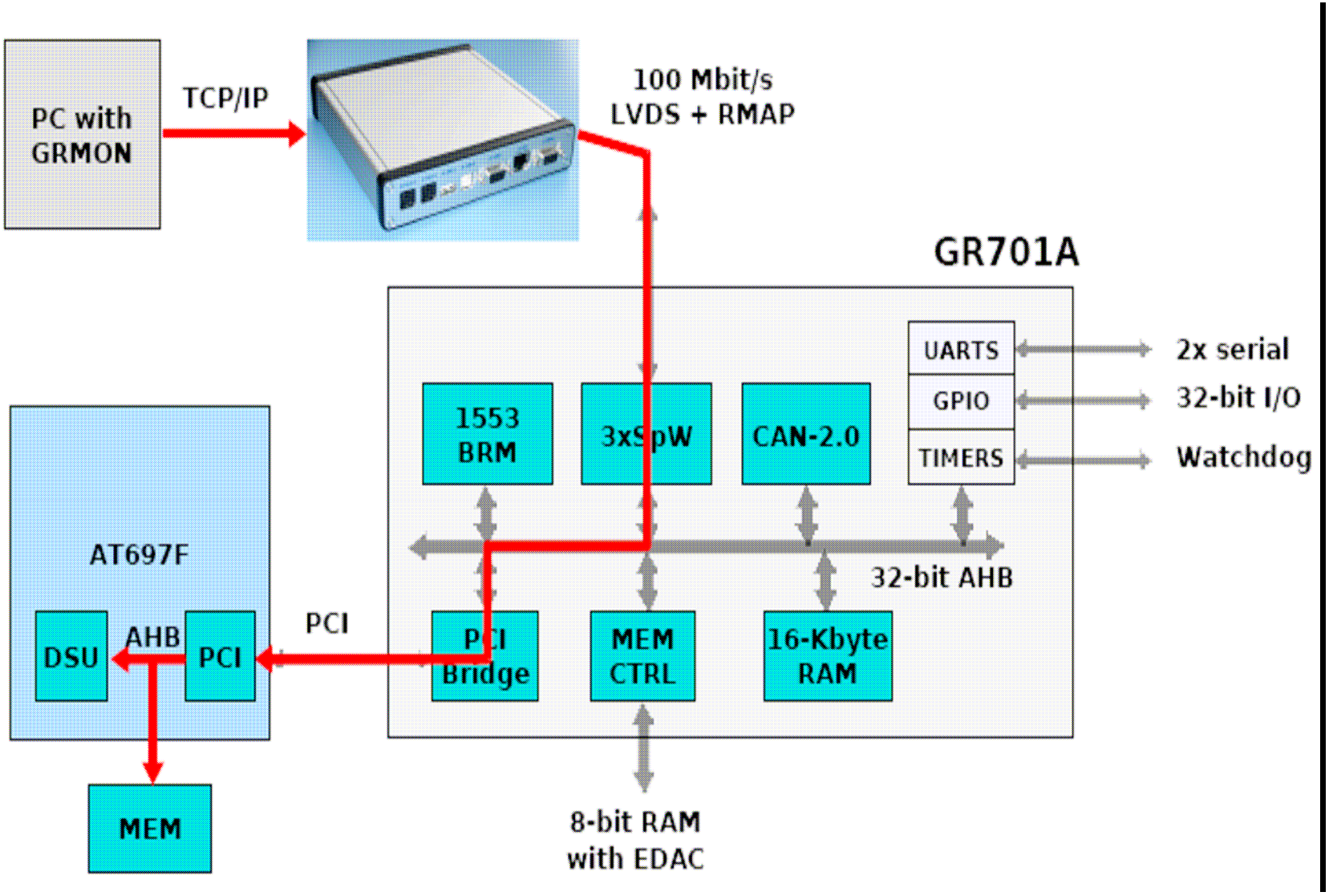
IP tunnelling and web interface

Xilinx Spartan-3 FPGA

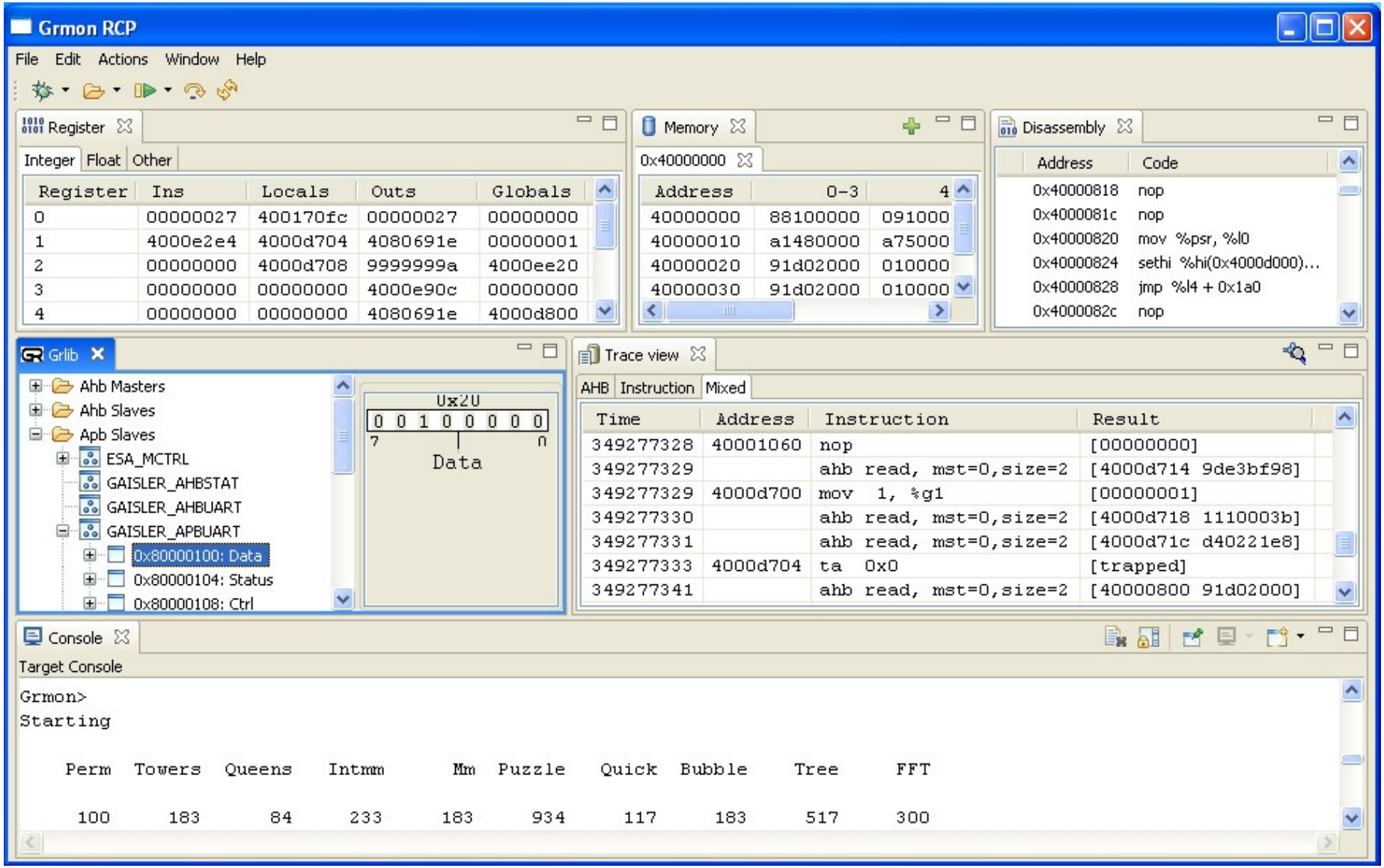
LEON3 inside

Linux based

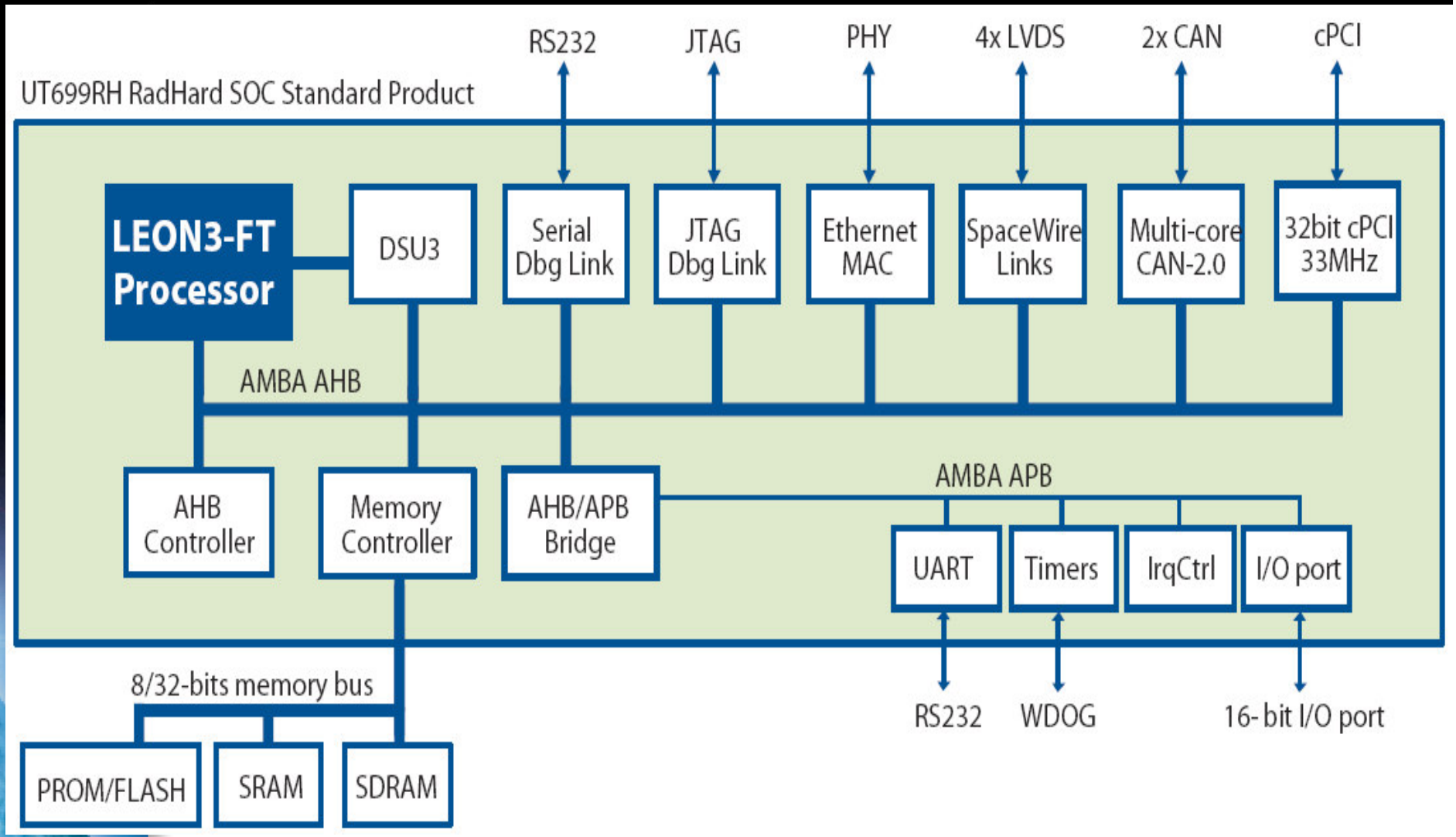
# Debugging with GR701



# GRMON – debug monitor



# Aeroflex UT699RH



# GR-RASTA LEON2/3 Development System

The *GR-RASTA LEON2/3 Development System* is a PCI based set of processor and interface boards aimed towards the development of avionics.

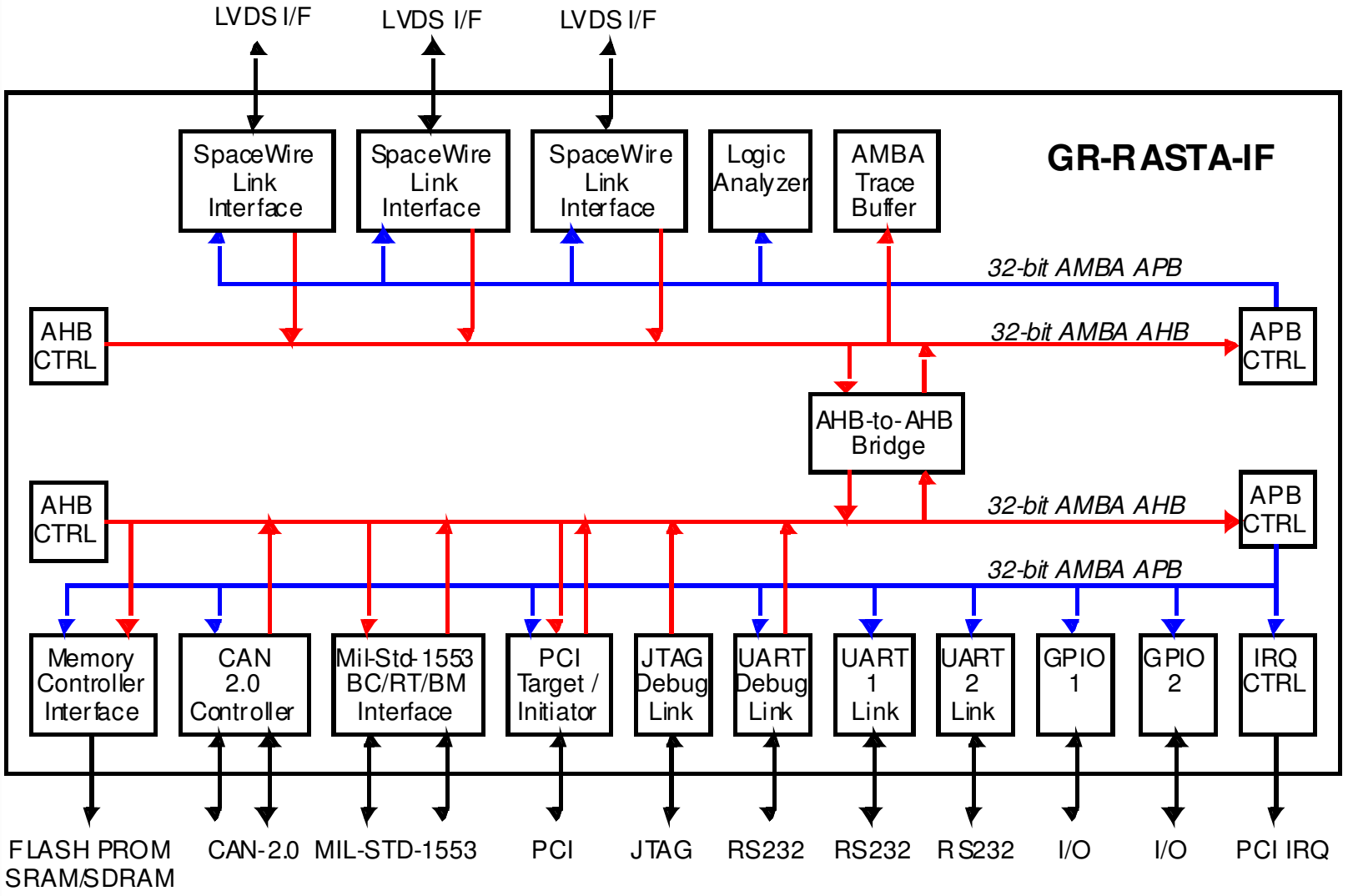
A rich variety of compact PCI boards provides a large number of variations:

- Processors: LEON3, LEON2, AT697, SPW-RTC
- Buses: SpaceWire, Mil-Std-1553, CAN, Ethernet
- Peripherals: PCI, UART, JTAG, GPIO, Timers
- Memories: SRAM, SDRAM, FLASH PROM
- Spacecraft communication: CCSDS/ECSS TM/TC

Boards support ASIC, Actel and Xilinx FPGAs

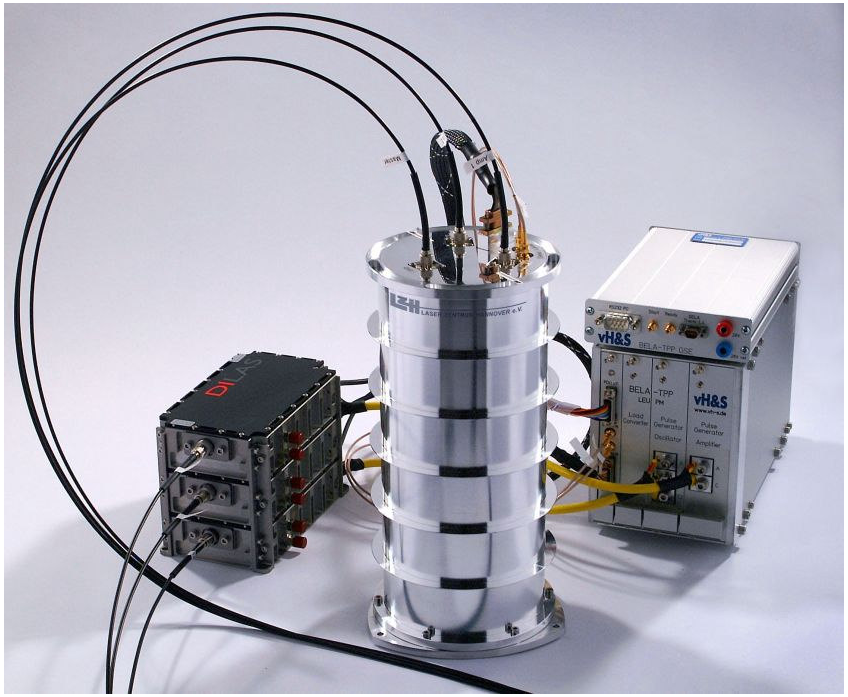
# GR-RASTA CPCI Crate

# GR-RASTA Interface Board



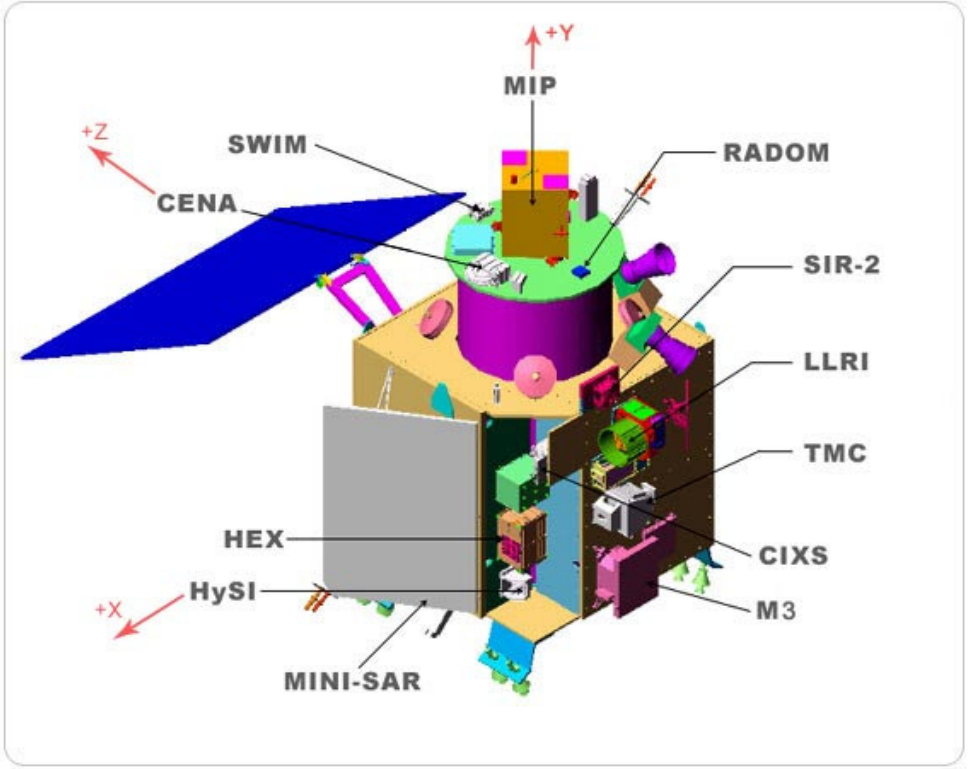
# Applications - BELA

- Bepi-Colombo Laser Altimeter (BELA)
- DLR (Germany)
- LEON3-FT delivered as VHDL netlist
- Bepi-Colombo, ESA's mission to Mercury
- Mercury Planetary Orbiter (MPO)
- Launch 2013
- In orbit 2019 -

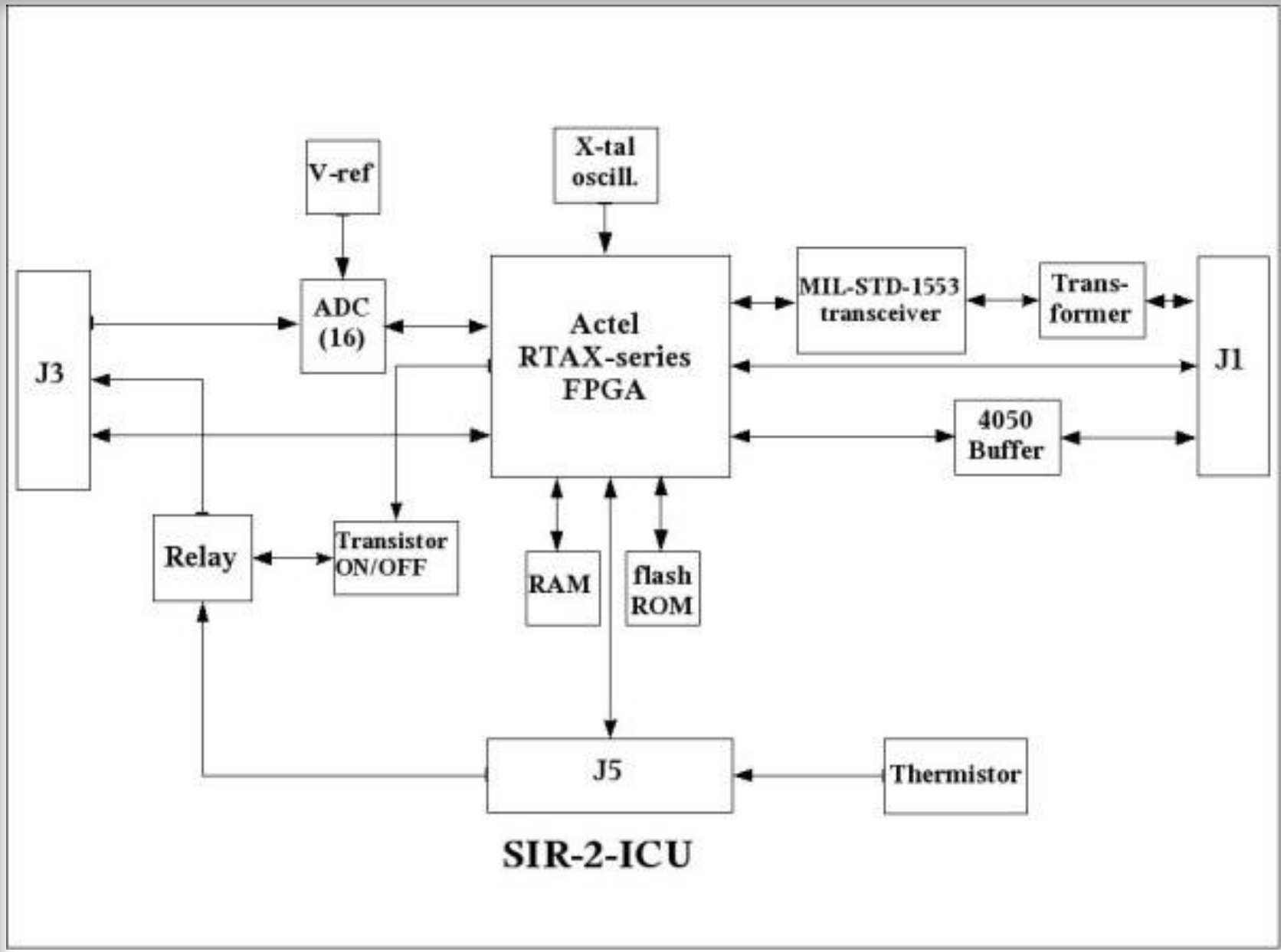


# Applications – SIR2

- SIR-2 instrument is a highly compact, monolithic grating, near infrared spectrometer
- Chandrayaan-1, India's mission to the moon
- University of Bergen, Norway
- LEON3-FT delivered as VHDL netlist
- MIL-STD-1553B wrapper for ACTEL core
- GRLIB used
- Launch 2008



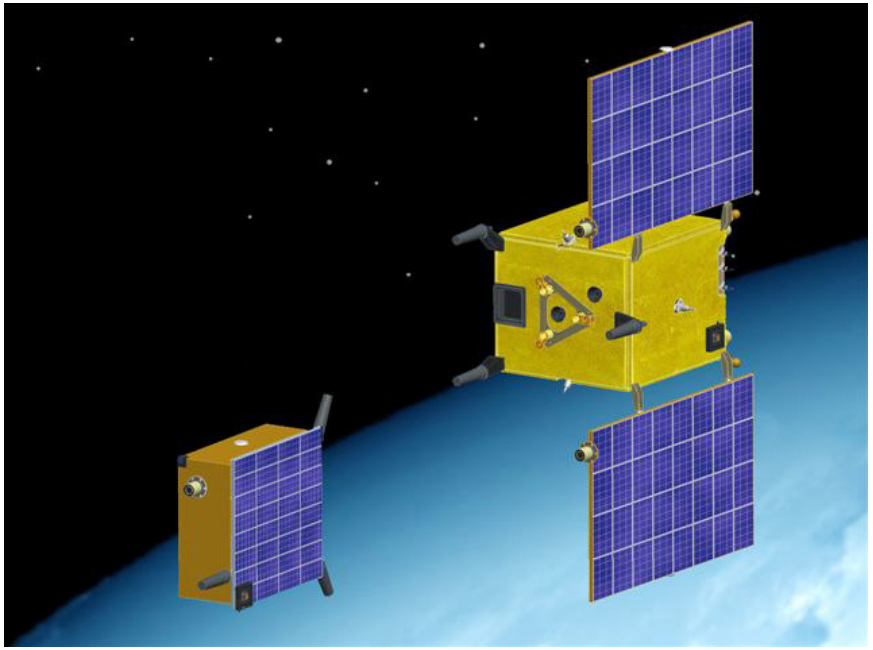
# Applications – SIR2



# Applications - PRISMA

Swedish/German technology mission to demonstrate different technologies and guidance/navigation strategies for Rendezvous and Formation Flying in space.

- Autonomous formation flying
- Homing
- Rendezvous
- Proximity Operations
- Final Approach
- Recede Operation
- Launch 2009



# Applications - PRISMA

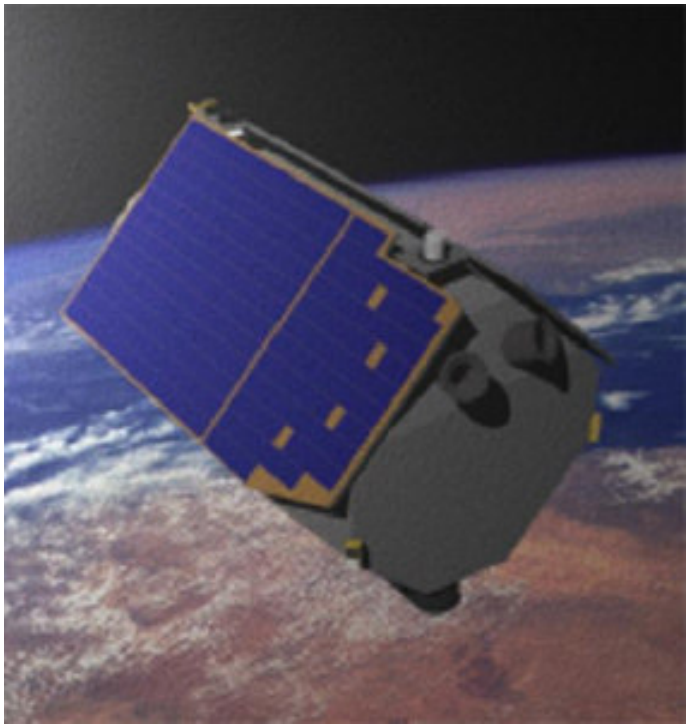
- Spacecraft control computer based on standard LEON3-RTAX design

- LEON3-FT delivered as a VHDL netlist
- GRLIB based design
- Customer added own IP cores
- Gaisler Research developed AMBA interface:
  - SpaceWire interface, single port
  - CAN interface, redundant ports
- 24 MHz system frequency (due to CAN)

- RTAX2000S parts to be programmed shortly

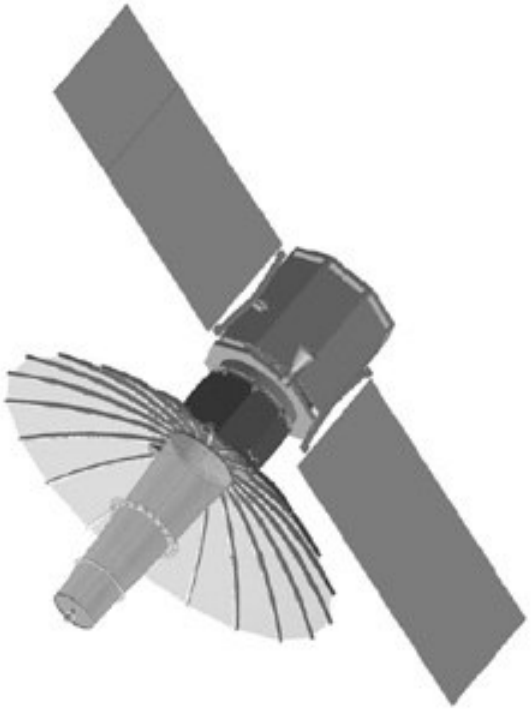
# Applications - ARGO

- ARGO, Remote Sensing mission
- Taiwan National Space Organization (NSPO)
- Spacecraft control computer based on standard LEON3-RTAX design:
  - SpaceWire links
  - Std peripherals
- ACER Inc. (Taiwan)
- Carlo Gavazzi Space (I)
- RapidEye constellation
- Launch 2009



# Applications – TacSat-4

- Operationally Responsive Space (ORS)
- TacSat-4 SpaceWire link has two nodes:
  - Payload Data Handler (PDH) on spacecraft bus
  - Universal Interface Electronics (UIE) on payload
  - Connected by SpaceWire cables
- The UIE employ the Gaisler Research LEON3 processor and SpaceWire core in an Actel RTAX2000S FPGA
- Jaffe et al. ISC 2007



# Applications – Others

- LEON3-RTAX :
  - Assurance Technology Corporation (US)
  - Syderal SA (Switzerland)
  - Tubitak Uzay (Turkey)
  - INTA – INTAμSat (Spain) (tentative)
- LEON3 / LEON3-FT:
  - EADS Astrium (France)
  - Ball Aerospace (US)
  - Microsat Systems Inc (US)
  - Orbital Research Inc (US)
  - General Dynamics AIS (US)
  - Zarlink Semiconductor (Canada)
  - Vineyard Technologies (US)

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# Conclusions

- By embracing the enabling technologies presented, several powerful system-on-a-chip designs have been developed in a short period of time.
- The key factors have been efficient implementation of truly re-usable IP cores, such as the GRSPW SpaceWire codec, which have been designed with interoperability and portability in mind from the start.
- This has resulted in sophisticated flight products that are being shipped to customers right now.