GR716

Microcontroller for Embedded Space Application

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2019 CAN IN SPACE WORKSHOP

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GR716 – LEON3FT Microcontroller

Microcontroller Introduction

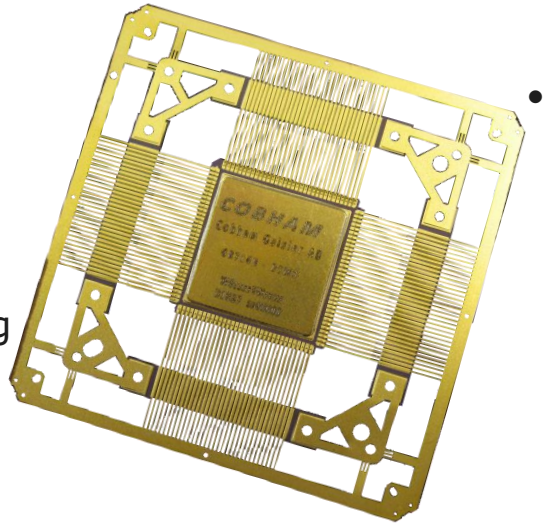
Description

The GR716 features a fault-tolerant LEON3 SPARC V8 processor, communication interfaces and on-chip ADC, DAC, Power-on-Reset, Oscillator, Brown-out detection, LVDS transceivers, regulators to support for single 3.3V supply, ideally suited for space and other high-rel applications

Applications

Support for many different standard interfaces makes the GR716 microcontroller is ideally fit for handling supervision and control in a satellite, such as

- propulsion system control
- sensor bus control
- robotics applications control
- simple motor control
- mechanism control
- power control
- particle detector instrumentation
- radiation environment monitoring
- thermal control
- antenna pointing control
- remote terminal unit control
- simple instrument control



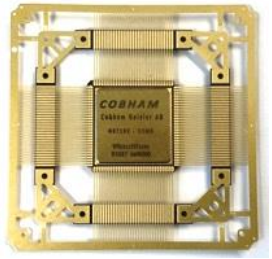
Specifications

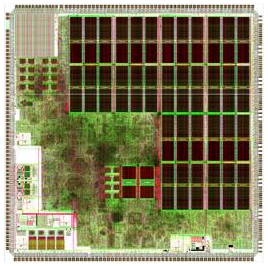
- System frequency up-to 50 MHz
- SpaceWire links up-to 100 Mbps
- CQFP132 hermetically sealed ceramic package
- Total Ionizing Dose (TID) up to 100 krad (Si, functional)
- Single-Event Latch-Up (SEL) to LET_{TH} > 118 MeV-cm^{2}mg
- Single-Event Upset (SEU) below 10^{-6} bit error rate and day in space environment
- Support for single 3.3V supply

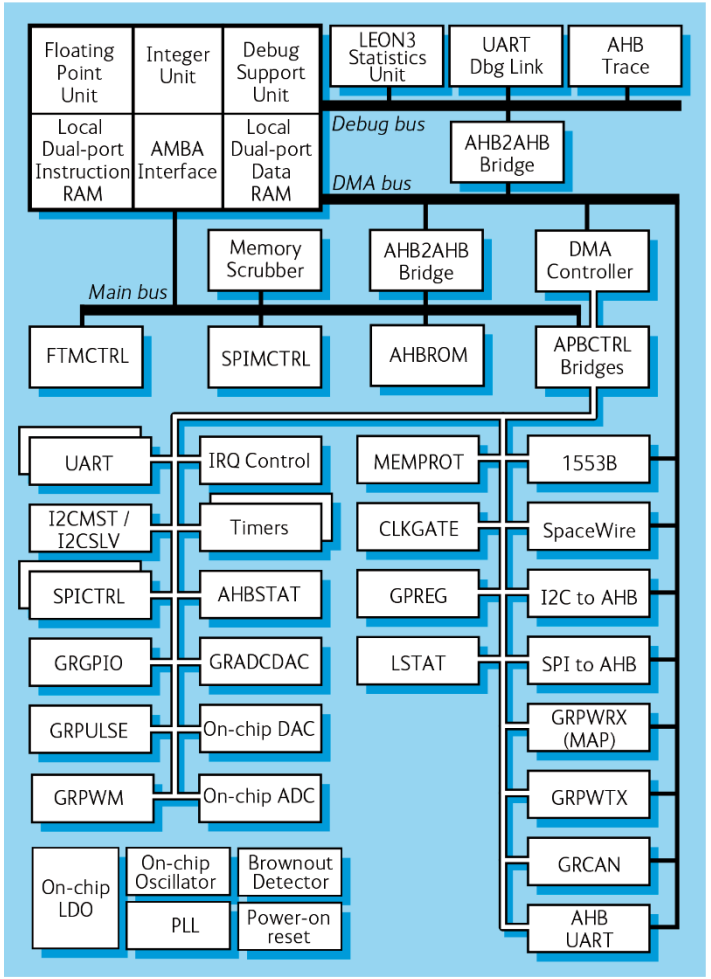
GR716 – LEON3FT Microcontroller

Microcontroller Features

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, 50 MHz
  - LEON-REX - 16-bit instructions for improved code density
  - Floating Point Unit
  - 192KiB on-chip instruction and data memory
  - Memory protection units
  - Non-intrusive advanced on-chip debug support unit
- External EDAC memory: 8-bit PROM/SRAM, SPI, I2C
- SpaceWire interface with time distribution support, 100 Mbps
- MIL-STD-1553B interface
- 2x **CAN** 2.0B controller interface
- PacketWire with CRC acceleration support
- Programmable PWM interface
- SPI with SPI-for-Space protocols
- UARTs, I2C, GPIO, Timers with Watchdog
- Dual ADC 11bits @ 200Ksps, 4 differential or 8 single ended
- DAC 12bits @ 3Msps, 4 channels
- Mixed General purpose inputs and outputs
- Power-on-Reset and Brown-out-detection
- Temperature sensor, Integrated PLL
- On-chip regulator for 3.3V single supply
- 132 pin QFP, 24 mm x 24 mm







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Processor Performance

- On-chip SRAM w/ Dual Port, EADC and Scrubbing, Radiation Tolerant
  - 192 KiB Instruction and Data – User defined mix of instruction vs data
- Integrated Floating Point Unit
  - IEEE-754 compliant floating-point unit, supporting both single and double precision operands
- Memory Protection Unit
  - 8 zones and individual access control of peripherals
- System Clock frequency: 50MHz
  - Dynamic reconfiguration of system clock for low power
- System Benchmark
  - Dryshtone: 0.93 Dhrystone / MHz
  - Whetstone: 0.43 Whetstone / MHz
  - CoreMark: 2.21 CoreMark / MHz
  - EDAC, Scrubbing, DMA transfers and debug are non-intrusive and do not affect performance

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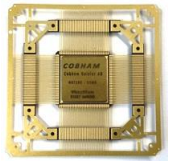

Processor	**Processor core**	LEON3FT
	Architecture	SPARC V8 w. V8e subset
	RISC type	32bit
	Instruction set	SPARC V8(e), LEON REX
	Pipeline stages	7
	Tightly coupled memory	192 KiB
	FPU	IEEE-754
	MPU	yes
	Mul/Div	Mul/Div
	Peripheral DMA	multi-channel
	Interrupt handling	deterministic
	Performance counters	yes
	Debug unit	yes
	Embeded trace buffer	yes
	Processor MHz	50
Performance	**Dhrystone / MHz**	0.93
	Whetstone / MHz	0.43
	CoreMark / MHz	2.21

** Dhrystone Performance: Compiler Versions and Ground Rules application note is available at https://www.gaisler.com/index.php/information/app-tech-notes*

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Typical Power Consumtption @ Nominal temp and voltage conditions

- Standby
  - Current consumption direct after boot has finished (Waiting remote boot)
- CoreMark
  - Highest measured current consumption while running CoreMark (All code is executed from internal memory protected by EDAC)
- Whetstone
  - Highest measured current consumption while running Whetstone (All code is executed from internal memory protected by EDAC)
- CAN / SRAM / RTEMS
  - Highest measured current consumption while receiving and transmitting on the CAN bus.
  - RTEMS operating systems and drivers are executed from external SRAM

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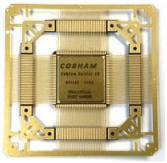


Mode	Supply Mode	Frequency	1.8V Supply	3.3V Supply
Standby	Dual Supply	10MHz	18mA	10mA
	Single Supply	10MHz	-	34mA
	Dual Supply	25MHz	58mA	11mA
	Single Supply	25MHz	-	75mA
CoreMark	Dual Supply	10MHz	36mA	10mA
	Single Supply	10MHz	-	52mA
	Dual Supply	25MHz	104mA	11mA
	Single Supply	25MHz	-	121mA
WhetStone	Dual Supply	10MHz	34mA	10mA
	Single Supply	10MHz	-	48mA
	Dual Supply	25MHz	97mA	11mA
	Single Supply	25MHz	-	117mA
RTEMS/CAN	Dual Supply	10MHz	35mA	15mA
	Single Supply	10MHz	-	56mA
	Dual Supply	25MHz	78mA	20mA
	Single Supply	25MHz	-	104mA

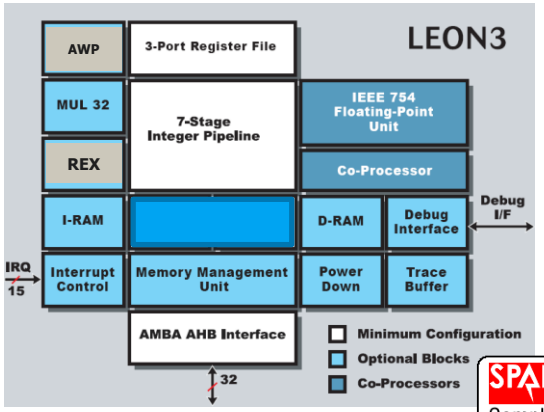
** Values represents maximum measured current consumption in mode or test*
*** Values are an average of 128 sample averaging with 532us between samples*

GR716 – LEON3FT Microcontroller

Key features – processor and memory

Processor core

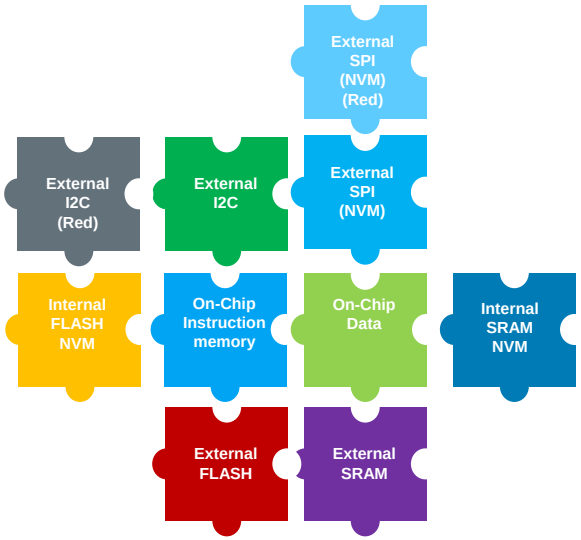
- Fault-tolerant SPARC V8 processor with 31 register windows and support 16-bit instruction operation (REX)
- Double precision IEEE-754 floating point unit
- Memory protection units with 8 zones and individual access control of peripherals
- Advanced on-chip debug support unit with trace buffers and statistics
- Deterministic software execution and non-intrusive debugging
- Fast context switching (PWRPSR, AWP, register partitioning, SVT, MVT)
- Interrupt zero jitter delay



Fault-tolerant SPARC V8 processor

Memory support

- 192KiB EDAC protected tightly coupled memory with single cycle access from processor and ATOMIC bit operations
- Dedicated SPI Memory interface with boot ROM capability and EDAC
- I2C memory interface with boot ROM capability
- 8-bit SRAM/ROM I/F with support up to 16MiB ROM and 256MiB SRAM
- Scrubber with programmable scrub rate for all embedded memories and external PROM/SRAM and SPI memories
- Redundant boot memory (PROM/SRAM/SPI/I2C/NVRAM)
- Application software container for checking software integrity using CRC
- Boot from internal SRAM, external PROM/FLASH/SRAM/SPI/I2C memory



Support of many variety of memory types

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Boot options

- Remote boot (no software or external memory required)
  - UART
  - SpaceWire RMAP
  - SPI / SPI4SPACE
  - I2C
- Internal Boot PROM supported boot (configures the I/0s):
  - External PROM/SRAM
  - External SPI Memory
  - Embedded NVRAM/PROM/SRAM in package (future option)
  - External I2C PROM
- Direct boot (bypass internal boot prom)
  - External PROM/SRAM
  - External SPI Memory
  - Embedded NVRAM/PROM/SRAM in package (future option)

Select Boot option via external pins

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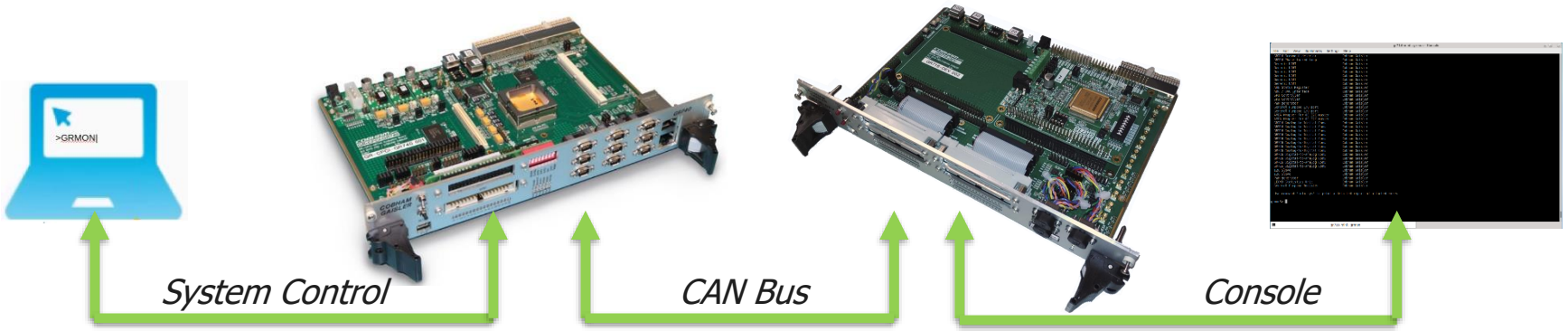
Boot via CAN

- Boot over CAN is supported via small boot software
  - Remote read and write commands access to all register memory locations
  - Support processor restart at arbitrary location
- Demonstration software based upon drivers and software included in the free GR716 software environment available for download at www.gaisler.com
- Demonstration software is demonstrated using software simulator TSIM-GR716 and in real-world allowing a GR740 Quad-Core LEON4 Processor to access to full memory space in GR716 for uploading software.



For a demonstration please visit Cobham Gaisler's exhibition stand

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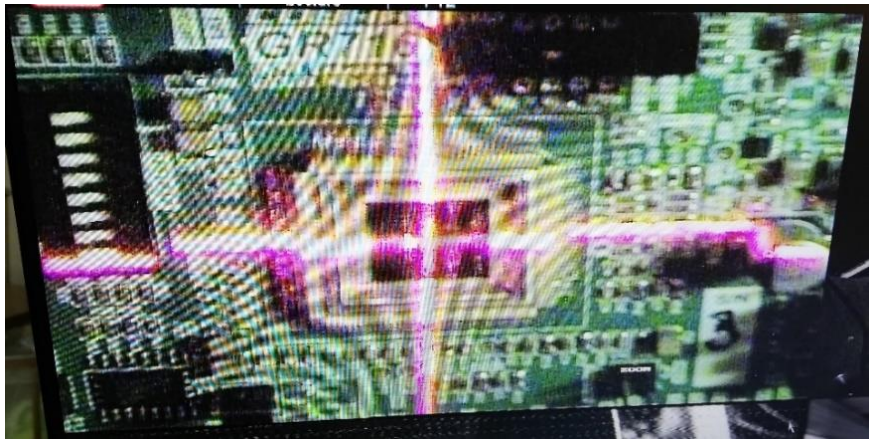
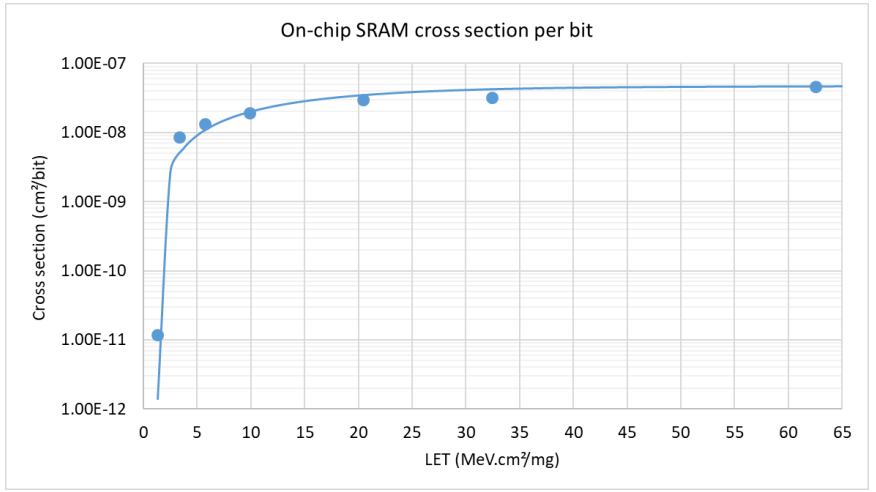
Radiation hardening - Ready for Space

- Processor register file
  - 32+7 BCH EDAC + bit-interleaving + bit-spacing
- On-chip instruction and data memories
  - 32+7 BCH EDAC + bit-interleaving
  - Independent programmable periodic scrubber for instruction and data memories
- External memory interfaces
  - 8-bit external PROM/SRAM interface with 32+7 BCH EDAC protection
  - Programmable periodic scrubber for PROM/SRAM and SPI memories
  - Redundant memory boot capability
- System and Configuration register
  - General – RHBD (IMEC DARE180U)
  - PLL and IOs configuration registers – RHBD + 32+7 BCH EDAC
- Analog hardware blocks
  - General – RHBD (IMEC DARE180U)





** The results presented are from the first silicon and they do not represent the final silicon*
*** Results in agreement with the data known from the IMEC DARE180U library and 100% of all upsets were corrected during heavy Ion test*

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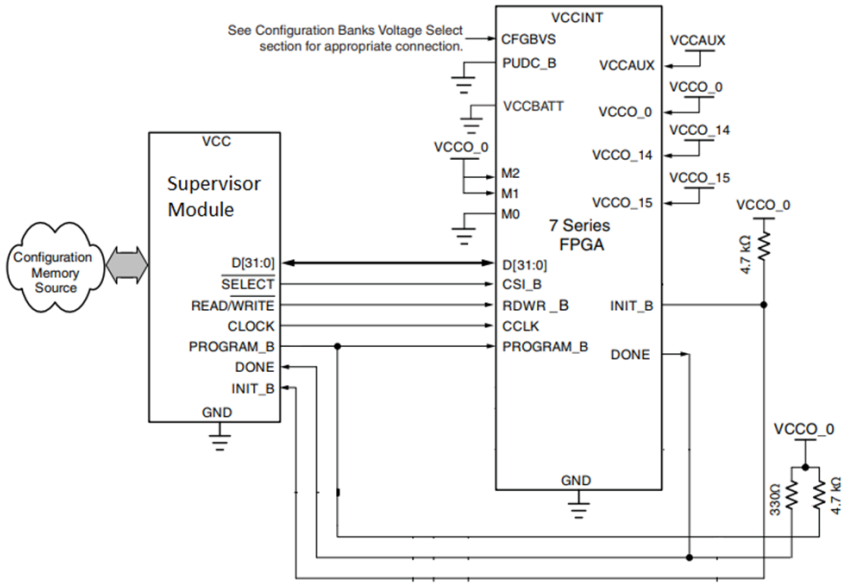
Flight Model

- GR716 is currently available in engineering samples
- Re-spin of the die is planned for tapeout the end of 2019
- Support for CAN-FD (**GRCANFD**)
- Programmable timing for analog multiplexing and conversion
- Additional ADC Sample&Hold circuits to support motor control
- LVDS with fail-safe and cold-spare
- SpaceWire routing capabilities
- FPGA supervisor core (**GRSCRUB**)
  - Compatible with Xilinx FPGAs
  - SelectMap interface
  - Programming
  - Scrubbing
  - Blind or readback
  - Full or partial
  - CRC, ECC, or Full Frame Check (FFC)



FPGA supervisor example
Adapted from Xilinx UG470

Flight devices planned to be available end of 2020

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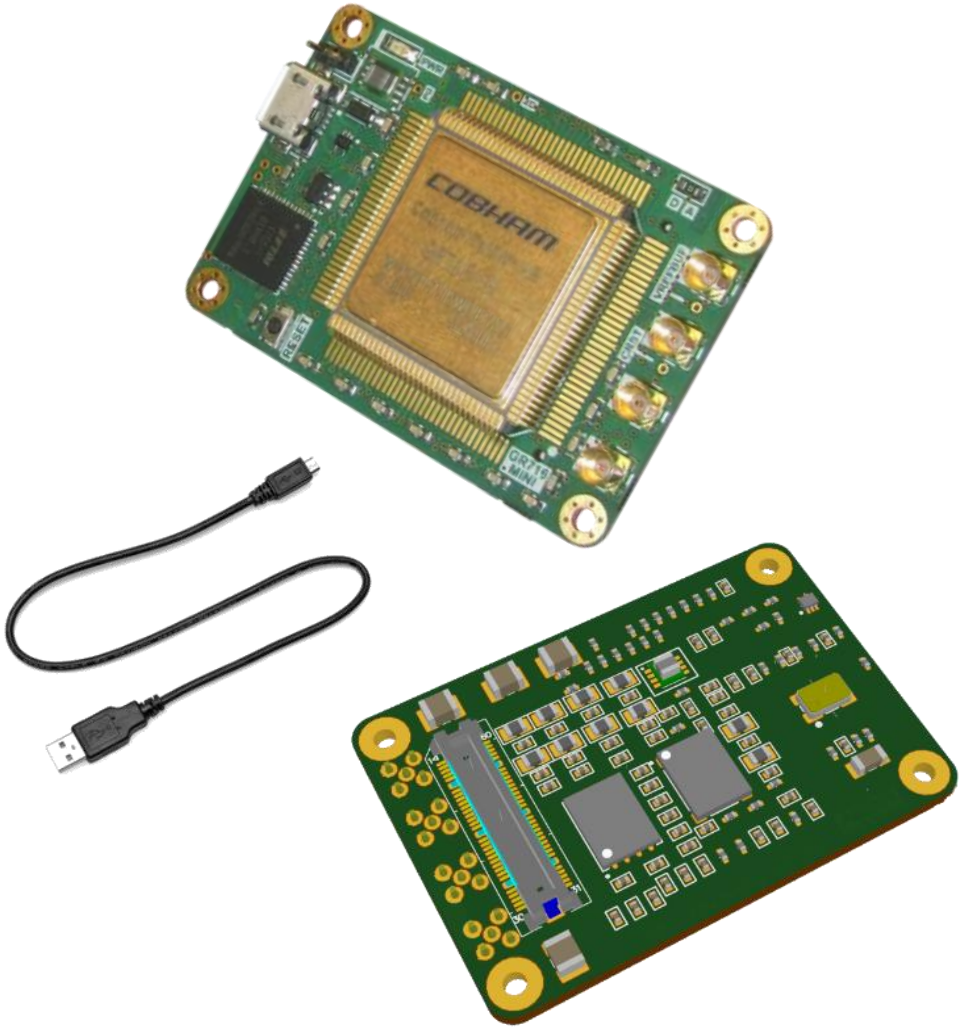
Evaluation Boards

- Design for evaluation board:
  - GR716 microcontroller
  - SPI Flash PROM (32 MiB)
  - SRAM (2 MiB)
  - FTDI USB interface
    - GRMON3 debug I/F via Debug UART
    - 2x UART interfaces, 1x I2C interface
    - control of reset, configuration pins etc.
    - power supply
  - 4x MMCX (micro-miniature coaxial):
    - 2x ADC, 2x DAC
  - miniature 80 pin mezzanine connector:
    - addition ADC, DAC, LVDS, GPIO, etc.
  - Oscillator
  - LED for power indication etc.
  - 50mm x 35mm (37.5% of a credit card)
- Shipped with:
  - free GRMON3 GUI (limited) download
  - free compilers, OS, tools downloads
  - USB cable (debug and power)



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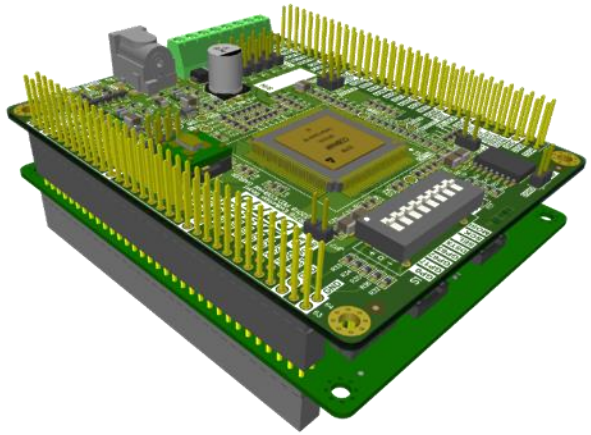
Development Board

- Design for development board:
  - GR716 microcontroller
  - SPI Flash PROM (32 MiB)
  - PCI104 style stackable headers (2 x 64 pin) for interfaces
    - measurement points on all GPIO/interface signals for monitoring/debug
    - interface to user defined modules (memory, digital I/F, analog I/F)
    - interface to cPCI mother board in 6U rack or box format
  - Debug UART /IF
  - LVDS in/out (3+3 pairs) for 1x SpW or x SPI for Space
  - GPIO (64 pins)
    - digital I/O
    - external memory I/F
    - 6x UART
    - Mil-Std-1553B, PacketWire, CAN, I2C, 3x SPI, 16x PWM out
    - 8x analog in, 4x analog out, external ADC/ADC interface
    - 1x SpaceWire, 1x TDP
  - Socketed oscillator (5–25MHz)
  - DIP-switch for bootstrap options
  - Powered from external supply (range 5V to 12V)
  - Single supply operation or individual supplies
  - 80mm x 100mm format

GR716 Standalone Board



Stack multiple boards via PC104 connector

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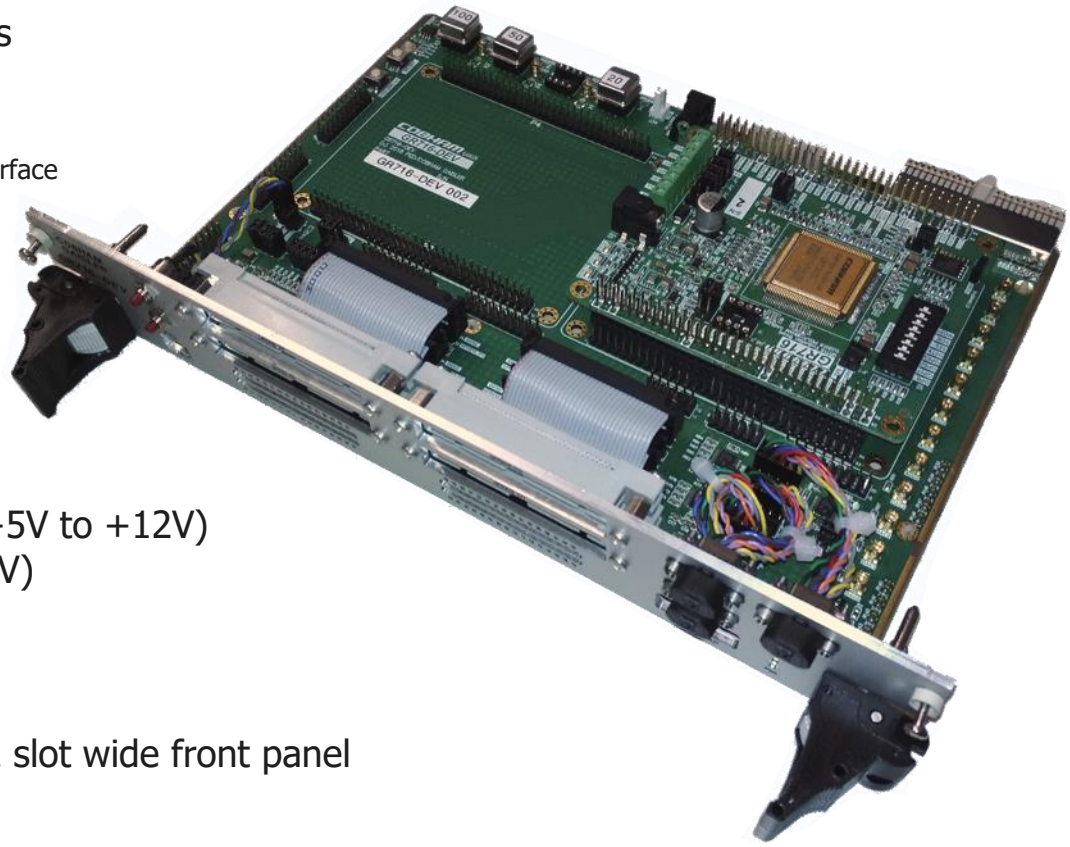
GR-CPCI-GR716-DEV – GR716 interface development board

- Design for interface application board:
  - GR716-BOARD engineering board in dedicated slot
    - Multiple slots for possibility to attach multiple GR716 engineering boards
  - Expansion slot for memory or user defined functions (e.g. SRAM, ADC/DAC)
  - Socketed oscillators for system, SpaceWire, Mil-Std-1553B and PWM clocks
  - Configuration of front panel functions
  - Front panel interfaces
    - MDM9S for fixed SpW (LVDS) interface
    - MDM9S for configurable SpW/SPI4S (LVDS) interface
    - GPIO (64 pins on standard 0.1" connectors)
    - LED indicators (64) for GPIO pins
    - DIP switch for bootstrap options
    - Reset and DSU Break push-button switches
    - LEDs for power and reset status
    - FTDI USB interface
      - GRMON3 debug I/F via Debug UART
      - 2x UART interfaces, 1x I2C interface
  - Power from external supply (range +5V to +12V) or via cPCI backplane connector (+5V)
  - Expansion through accessory boards
    - 6x UARTs using GR-CPCI-6U-UART
    - CAN, Mil-Std-1553B, SPI using GR-CPCI-GR740
  - 233mm x 160mm, 6U cPCI format, 2 slot wide front panel



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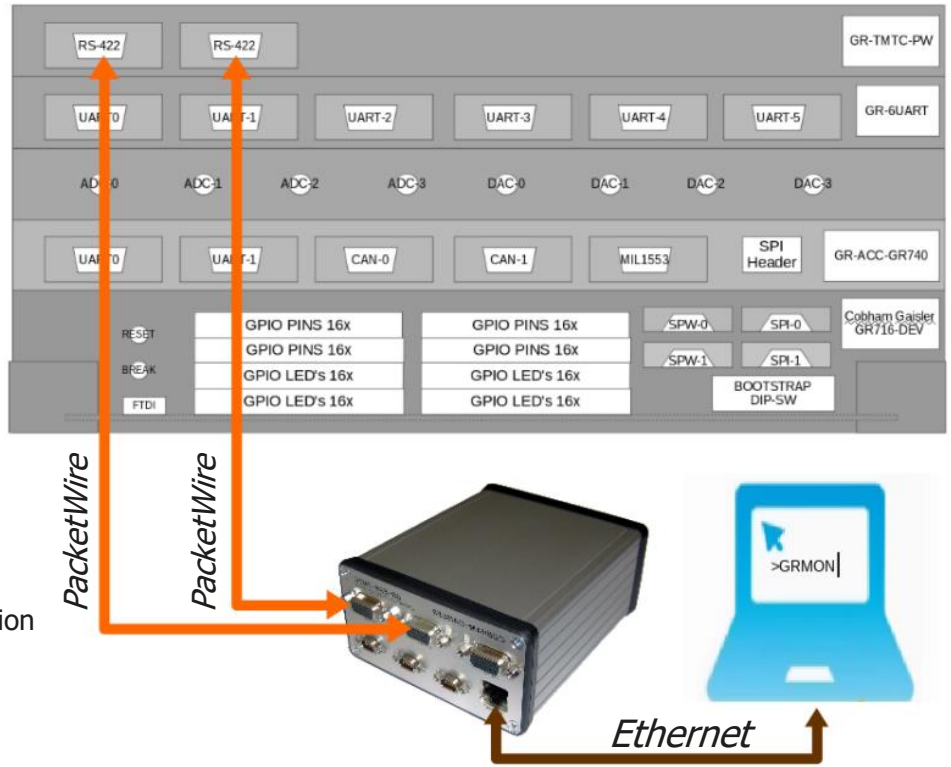
Build your application

- Build your application via available interface boards
- Compatible boards possible to direct connect and use from Cobham Gaisler:
  - GR-ACC-6U-6UART
    - Extend number of UARTs in the system
  - GR-ACC-GR740
    - Dual CAN 2.0 transceiver, Dual MIL-1553B interface and SPI interface
  - GR-CPCI-CAN
    - Dual CAN 2.0 transceiver
  - GR-TMTC-PW (6U)
    - RX/TX PacketWire interface
  - SPI4S Test Board
    - Reference board for SPI for Space demonstration
  - Analog Front end
    - Easy connection of external ADC and DAC

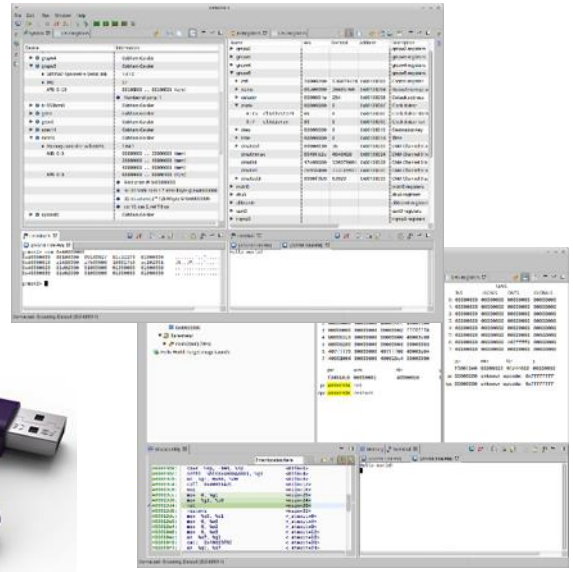


- Use Configuration Board to avoid driver contamination
  - Possible to fit mezzanine board on the development board to avoid erroneous configuration of the IOs

GR716 – LEON3FT Microcontroller

Software development environment

- BCC2 Development Environment
  - GCC 7.2.0 or CLANG 8
    - Performance increase with '*link time optimization*'
    - CLANG 8 to be released in 2019
  - GR716 BSP Support build in
    - GR716 features and IO Device drivers
- GRMON3 Debugger
  - Graphical User Interface (GUI) based on Eclipse TCF (Target Communication Framework) platform
  - GRMON displays HW/SW state in GUI without GDB in-between
- TSIM3 Software Simulator
  - GR716 features and IO device Support



GR716 – LEON3FT Microcontroller

BCC2 for GR716

- Bare metal toolchain for LEON processors
  - C/C++ cross compilers, both GCC and LLVM/Clang
  - C/C++ standard libraries
  - Open source with permissive licenses
- Support for GR716
  - Basic support for the GR716 architecture
    - Memory map, interrupts, capabilities
    - Linker scripts
    - ROM resident images
  - Support for GR716 features
    - REX
    - Single Vector Traps
    - Can generate chip specific instructions
  - Device drivers for GR716 I/O cores
    - SpaceWire, CAN, SPI, 1553, GPIO etc.
  - Flat mode, staying in one register window
    - Can reduce jitter
    - Can be used with register window partitioning
  - Optional C runtime with even smaller footprint: -qnano

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BCC2 for GR716 - Adjusting to different profiles

Property	Performance	Footprint	IRQ Response time
Soft mul/div	-	-	+
Soft float	-	-	+
Flat mode	*	-	+
Single Vector Trapping	-	+	-
Smaller runtime: -qnano		+	~
More register windows	+	~	~
IRQ jitter reduction	-	~	-
REX		+	
Optimize for size	-	+	~

Effects in general for the given metric:

+	better	*	Varies
-	worse		
~	marginal		

GR716 – LEON3FT Microcontroller

TSIM3 GR716 Simulator development

- Already used in daily internal testing
  - All boot possibilities
  - Load and run from local memory or external RAM (SPI-PROM, FLASH, SRAM)
  - External interfaces
    - SpaceWire, CAN, SPI, GPIO, etc.
  - Many of the new GR716 features in place
- TSIM GR716 release in 2019 June
  - In between TSIM2 and TSIM3
    - GR716 does not need all new features of TSIM3
  - User model API available
    - Not in final TSIM3 form

TSIM

```
$ /tsim-leon3 -gr716 ./coremark.elf
tsim> run

TSIM/LEON3 SPARC simulator, version tsim3-dev-ad71c1e55f1cee67 (internal version)

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For latest updates, go to http://www.gaisler.com/
Comments or bug-reports to support@gaisler.com

Number of CPUs: 1
register windows: 31
system frequency: 50.000 MHz
using 64-bit time
Allocated 128 KiB LOCAL ICACHE RAM memory at 0x31000000
Allocated 64 KiB LOCAL DCACHE RAM memory at 0x30000000
allocated 4096 KiB SRAM memory, in 1 bank
allocated 2048 KiB ROM memory
allocated 16384 KiB SPIM ROM memory
allocated 16384 KiB SPIM ROM memory
section: .text, addr: 0x31000000, size 78032 bytes
section: .rodata, addr: 0x30000000, size 3088 bytes
section: .data, addr: 0x30000c10, size 1584 bytes
read 475 symbols
tsim> run
 starting at 0x31000000
2K performance run parameters for coremark.
CoreMark Size    : 666
Total ticks      : 18529354
Total time (secs): 18.529354
Iterations/Sec   : 107.936844
Iterations       : 2000
Compiler version : GCC7.2.0
Compiler flags   : -O2 -qnano -qsvt -qbsp=gr716 -mcpu=leon3
Memory location  : Static
seedcrc          : 0xe9f5
[0]crclist       : 0xe714
[0]crcmatrix     : 0x1fd7
[0]crcstate      : 0x8e3a
[0]crcfinal      : 0x4983
Correct operation validated. See readme.txt for run and reporting rules.
CoreMark 1.0 : 107.936844 / GCC7.2.0 -O3 -qnano -qsvt -flto -qbsp=gr716 -mcpu=leon3  / S

 Program exited normally.

tsim>
```

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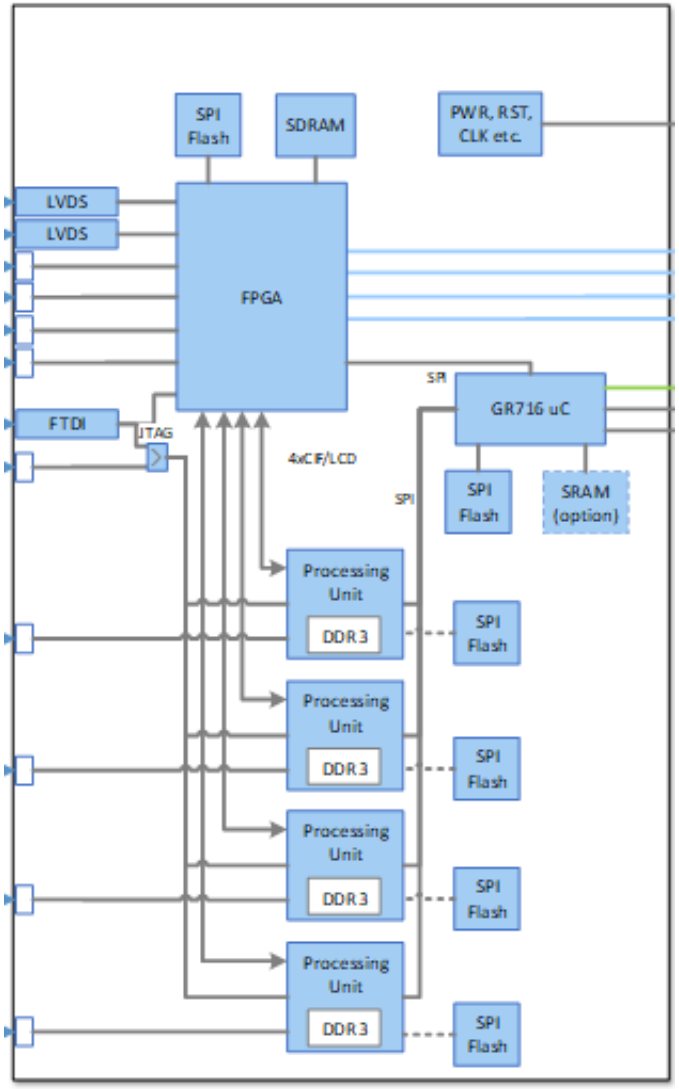
User Scenarios – COTS Supervisor

- European Space Agency activity - "High Performance Compute Board - An FPGA Accelerated DSP Payload Data Processor Board"
- GR716 will supervise four cutting-edge AI processing COTS devices coupled with a high-capacity FPGA in order to provide a board that supports state-of-the-art computer vision implementations
- Board architecture to be presented at the Space Computing Conference in July 2019



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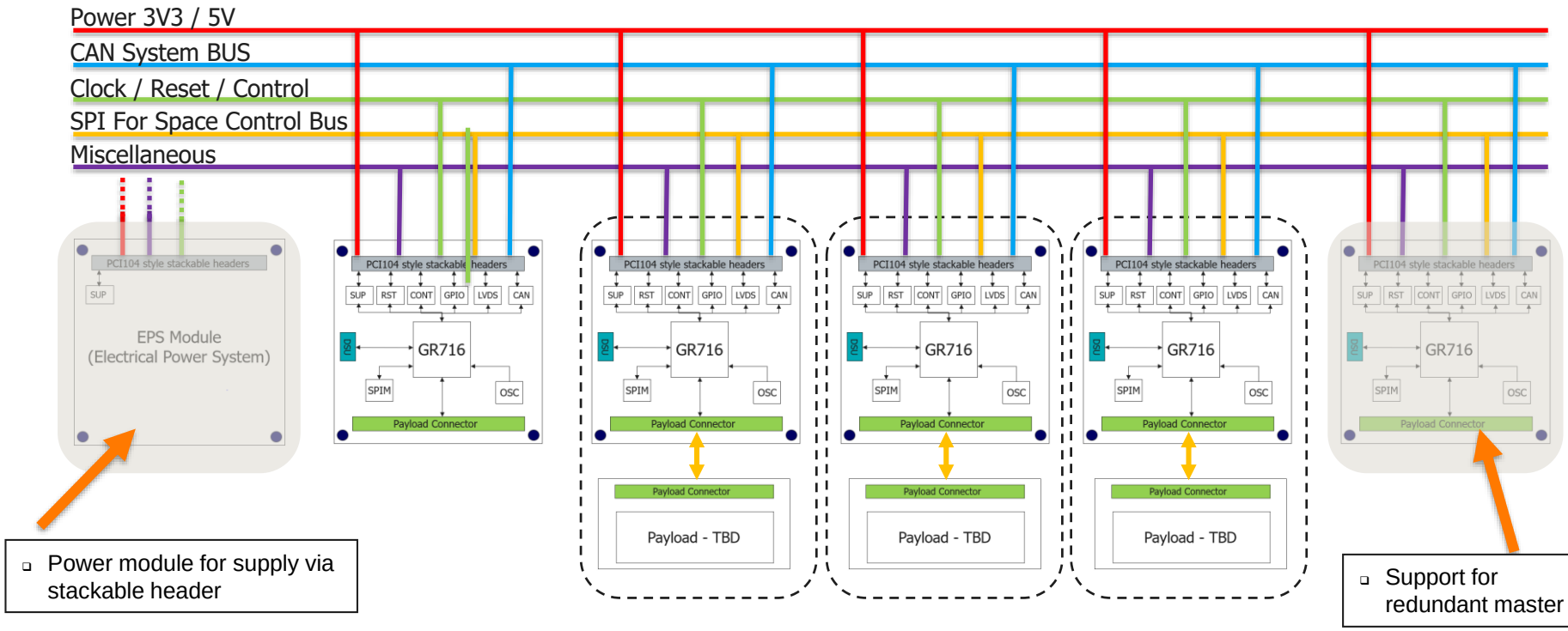
User Scenarios – Small Satellite payload boards

- Concept configuration for Small Satellites:
  - Redundant master support and support for up-to 4 payloads in hardware
  - CAN is selected as main system and payload bus
  - SPI-For-Space is used for software download and control.
    - Supports redundancy via one or multiple master



GR716 – LEON3FT Microcontroller

Conclusion

- TBD

GR716

Microcontroller for Embedded Space Application

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THANK YOU!

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