AXP15060 Datasheet

PMIC for multi-core high-performance system

Revision 0.1

2018.04.10

Version History

Version	Modify Time	Description
V 0.1	2018.04.10	Initial version

Declaration

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Catalog

1. Overview

AXP15060 is a highly integrated power management IC targeting at applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for multi-core processors to meet the complex and accurate requirements of power control.

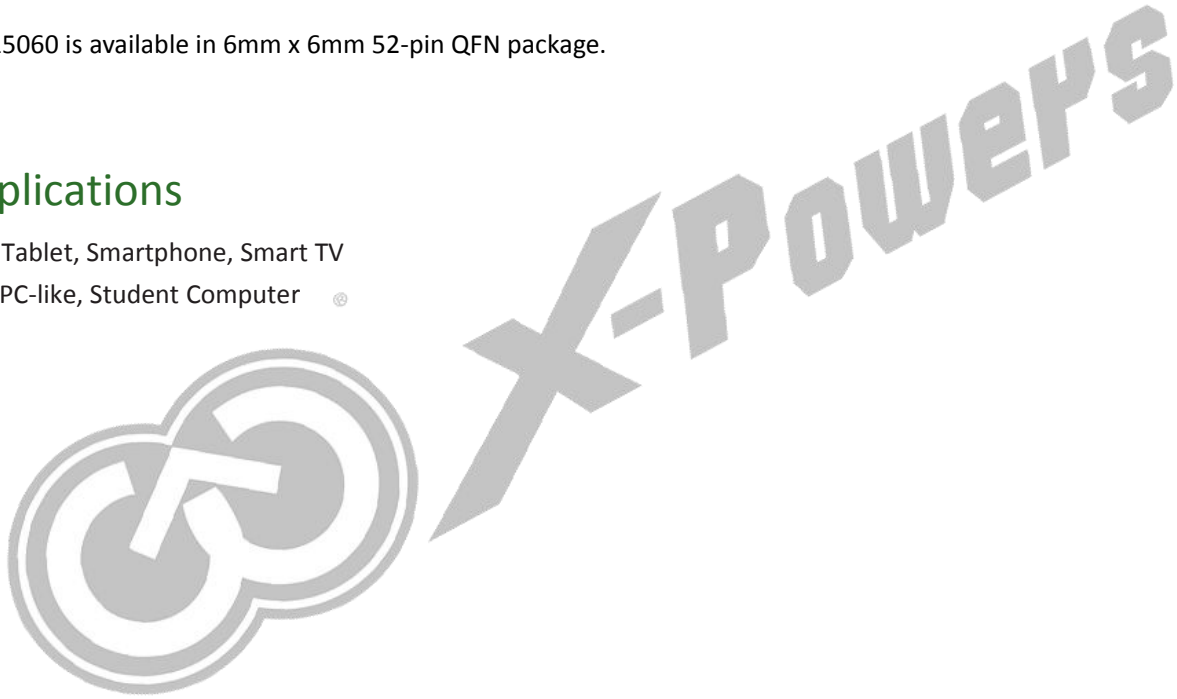
AXP15060 supports 23 channel power outputs(including 6 channel DCDC).To ensure the security and stability of the power system, AXP15060 integrates protection circuits such as over-voltage protection(OVP), under-voltage protection(UVP) and over-temperature protection(OTP).

AXP15060 provides a fast interface(Two Wire Serial Interface, TWSI) for system to dynamically adjust output voltages, enable power outputs and configure interrupt condition.

AXP15060 is available in 6mm x 6mm 52-pin QFN package.

Applications

- VR, Tablet, Smartphone, Smart TV
- UMPC-like, Student Computer



2. Feature

- 6 DCDCs
  DCDC1: 1.5~3.4V, 0.1V/step, IMAX=2A
  DCDC2: 0.5~1.2V, 10mV/step, 1.22~1.54V, 20mV/step, IMAX=3.5A, DVM
  DCDC3: 0.5~1.2V, 10mV/step, 1.22~1.54V, 20mV/step, IMAX=3.5A, DVM
  DCDC4: 0.5~1.2V, 10mV/step, 1.22~1.54V, 20mV/step, IMAX=2.5A, DVM
  DCDC5: 0.8~1.12V, 10mV/step, 1.14~1.84V, 20mV/step, IMAX=2.5A, DVM
  DCDC6: 0.5~3.4V, 0.1V/step, IMAX=2.5A
  DCDC2 &DCDC3 can be set to dual-phase; DCDC4 & DCDC6 can be set to dual-phase.
  DVM(Dynamic Voltage scaling Management) ramp rate: 1step/15.625us and 1step/31.250us.

- 16 LDOs, 1 Switch
  RTCLDO: 1.8V/3.3V,for RTC power, 100mA, always enable, input is ALDOIN
  ALDO1: 0.7~3.3V, 0.1V/step, IMAX=600mA, input is ALDOIN
  ALDO2: 0.7~3.3V, 0.1V/step, IMAX=300mA, input is ALDOIN
  ALDO3: 0.7~3.3V, 0.1V/step, IMAX=200mA, input is ALDOIN
  ALDO4:0.7~3.3V, 0.1V/step, IMAX=300mA, input is ALDOIN
  ALDO5: 0.7~3.3V, 0.1V/step, IMAX=300mA, input is ALDOIN

  BLDO1: 0.7~3.3V, 0.1V/step, IMAX=300mA, input is BLDOIN
  BLDO2: 0.7~3.3V, 0.1V/step, IMAX=500mA, input is BLDOIN
  BLDO3: 0.7~3.3V, 0.1V/step, IMAX=300mA, input is BLDOIN
  BLDO4: 0.7~3.3V, 0.1V/step, IMAX=400mA, input is BLDOIN
  BLDO5: 0.7~3.3V, 0.1V/step, IMAX=600mA, input is BLDOIN.

  CLDO1: 0.7~3.3V, 0.1V/step, IMAX=200mA, input is CLDOIN
  CLDO2: 0.7~3.3V, 0.1V/step, IMAX=200mA, input is CLDOIN
  CLDO3: 0.7~3.3V, 0.1V/step, IMAX=300mA, input is CLDOIN
  CLDO4: 0.7~4.2V, 0.1V/step, IMAX=200mA, input is CLDOIN

  LDO: for CPUs, NMOS LDO, V_{DDR}/2(source /sink), 0.7~1.4V, 50mV/step, IMAX=200mA, input is DCDC5.
  Switch: 0.1ohm switch, input is DCDC1, IMAX=1A, soft turn on.

- Two wire serial interface (SCK/SDA) supporting standard mode (100KHz) and quick mode (400KHz), the slave address is 0x36(7 bits)
- Internal temperature sensor and protection
- Monitor DCDCs output voltage, send interrupt and over temperature protection
- Customization for start up sequence and default voltage
- QFN6*6-52P-EP-0.4Pitch

3. Typical Application

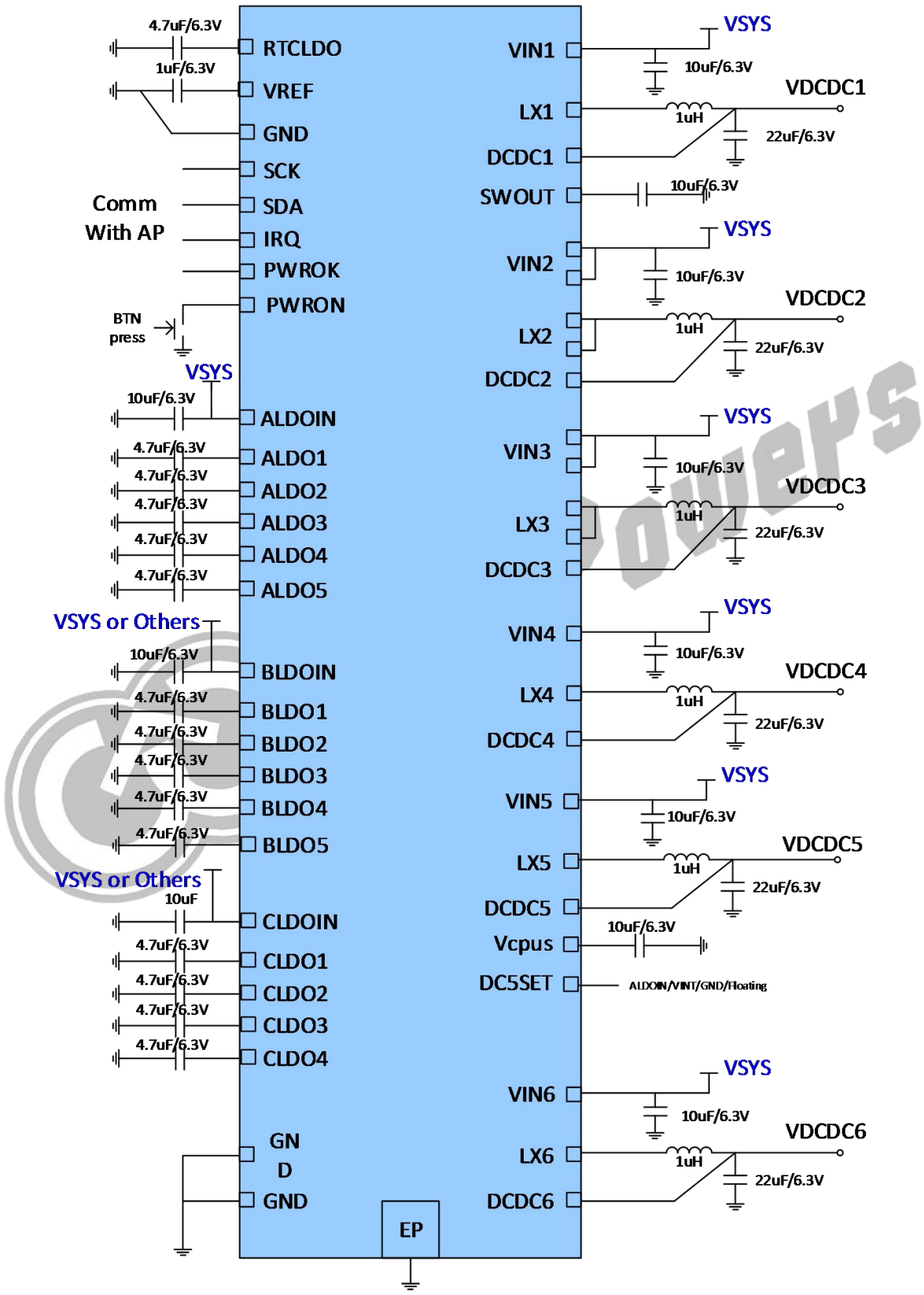


Figure 3-1 AXP15060 Typical Application

4. Pin Map

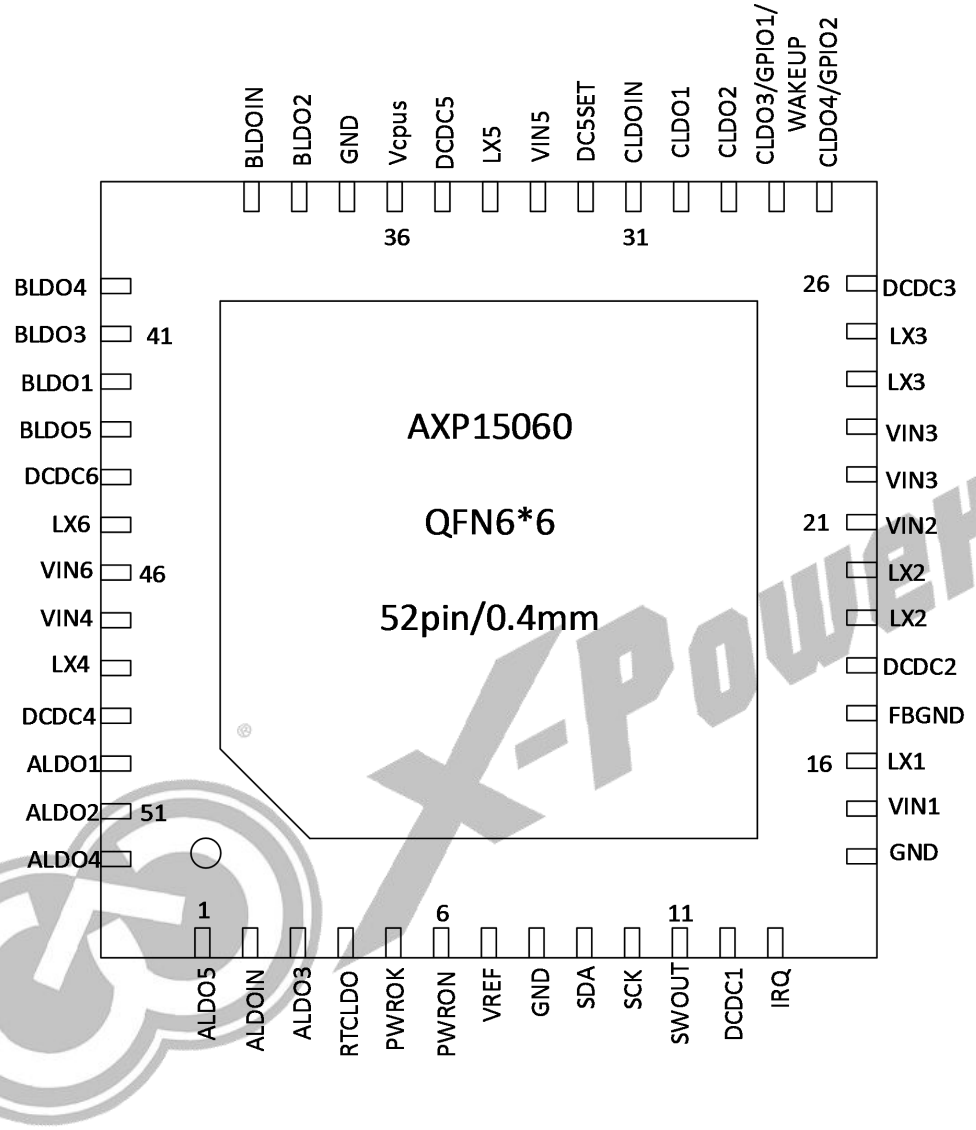


Figure 4-1 AXP15060 Pin Map

5. Pin List

NO.	Name	Type	Condition	Description
1	ALDO5	PO		Output pin of ALDO5
2	ALDOIN	PI		ALDO input source and internal analog power
3	ALDO3	PO		Output pin of ALDO5
4	RTCLDO	PO		RTC power output
5	PWROK	DO		Power good indication output
6	PWRON	IO		Power On-Off key input， Internal 100k pull up to VINT
7	VREF	AIO		Internal reference voltage
8	GND	G		GND for internal analog circuit
9	SDA	DIO		Data pin for serial interface, need a 2.2KΩ Pull High.
10	SCK	DI		Clock pin for serial interface, need a 2.2KΩ Pull High.
11	SWOUT	PO		DCDC1 Switch output pin
12	DCDC1	PI		DCDC1 feedback pin and Switch input source
13	IRQ	PIO		IRQ output
14	GND	G		GND for internal analog circuit
15	VIN1	PI		DCDC1 input source
16	LX1	PIO		Inductor pin for DCDC1
17	FBGND	AI		GND for DCDC2FB 1.DCDC2 remote feedback signal GND, line connect to the DCDC2 loading GND. 2.If not used, just be floating.
18	DCDC2	AI		DCDC2 feedback pin
19、20	LX2	PIO		Inductor pin for DCDC2
21	VIN2	PI		DCDC2 input source
22、23	VIN3	PI		DCDC3 input source
24、25	LX3	PIO		Inductor pin for DCDC3
26	DCDC3	AI		DCDC3 feedback pin
27	CLDO4/GPIO2	PO/GPIO	REG 2CH[2:0]	Output pin of CLDO4 or GPIO2 configured by REG 2CH
28	CLDO3/GPIO1 /WAKEUP	PO/GPIO	REG 2BH[6:5]	Output pin of CLDO3 or GPIO1 or WAKEUP input pin configured by REG 2BH
29	CLDO2	PO		Output pin of CLDO2
30	CLDO1	PO		Output pin of CLDO1
31	CLDOIN	PI		CLDO input source
32	DC5SET	AI		Setting DCDC5 Output Voltage
33	VIN5	PI		DCDC5 input source
34	LX5	PIO		Inductor pin for DCDC5
35	DCDC5	PI		DCDC5 feedback pin and CPUSLDO input source
36	VCPUS	PO		Output pin of CPUSLDO
37	GND	G		GND for internal analog circuit

38	BLDO2	PO		Output pin of BLDO2
39	BLDOIN	PI		BLDO input source
40	BLDO4	PO		Output pin of BLDO4
41	BLDO3	PO		Output pin of BLDO3
42	BLDO1	PO		Output pin of BLDO1
43	BLDO5	PO		Output pin of BLDO5
44	DCDC6	AI		DCDC6 feedback pin
45	LX6	PIO		Inductor pin for DCDC6
46	VIN6	PI		DCDC6 input source
47	VIN4	PI		DCDC4 input source
48	LX4	PIO		Inductor pin for DCDC4
49	DCDC4	AI		DCDC4 feedback pin
50	ALDO1	PO		Output pin of ALDO1 and RTC input source
51	ALDO2	PO		Output pin of ALDO2
52	ALDO4	PO		Output pin of ALDO4
EP	EP	PG		Exposed Pad, need to be connected to system ground

6. Absolute Ratings

Table 6-1 Absolute ratings

SYMBOL	DESCRIPTION	VALUE	UNITS
ALDOIN/BLDOIN/CLDOIN /VIN1/VIN2/VIN3/VIN4/ VIN5/VIN6	Input Voltage	-0.3 ~ 7.5	V
Ta	Operating Temperature Range	-40~85	℃
T_J	Junction Temperature Range	-40 ~ 125	℃
Ts	Storage Temperature Range	-40 ~150	℃
T_{LEAD}	Maximum Soldering Temperature (at leads，10sec)	300	℃
V_{ESD}	Maximum ESD stress voltage，Human Body Model	>2000	V

7. Electrical Characteristics

V_{IN} =5V, T_A= 25℃

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
PMIC Under Voltage						
V_{OFF}	PMIC Under Voltage Power off		2.6		3.0	V
Off Mode Current						
I_{OFF}	OFF Mode Current	ALDOIN=5V		30		μA
Logic						
V_{IL}	Logic Low Input Voltage			0.3		V
V_{IH}	Logic High Input Voltage			1.2		V
TWSI						
V_{CC}	Input Supply Voltage			3.3		V
ADDRESS	TWSI Slave Address (7 bits)			0x36		
f_{SCK}	Clock Operating Frequency			400		kHZ
t_f	Clock Data Fall Time	2.2Kohm Pull High		60		ns
t_r	Clock Data Rise Time	2.2Kohm Pull High		100		ns
DCDC						
f_{OSC}	Oscillator Frequency	Default		3		MHz
DCDC1						
V_{IN1}	VIN1 Input Voltage		V_{OFF}		5.5	V
I_{VIN1}	Input Current	PFM Mode I_{DC1OUT} =0		50		μA
I_{DC1OUT}	Available Output Current			2000		mA
V_{DC1OUT}	Output Voltage Range		1.5		3.4	V
V_{DC1_STEP}	Output Voltage Step			100		mV/step
V_{DC1_RIPPLE}	Output Voltage Ripple	PFM Mode	-30		+30	mV
		PWM Mode	-10		+10	mV
V_{DC1_ACC}	Output Voltage Accuracy	PFM, V_{DC1OUT}<=1V	-20		+40	mV
		PFM, V_{DC1OUT}>1V	-2%		+4%	
		PWM, V_{DC1OUT}<=1V	-30		+30	mV
		PWM, V_{DC1OUT}>1V	-3%		+3%	
V_{DC1_OVP}	Over Voltage Protection			120%* V_{DC1OUT}		V
V_{DC1_UVP}	Under Voltage Protection			85%* V_{DC1OUT}		V
DCDC2						
V_{IN2}	VIN2 Input Voltage		V_{OFF}		5.5	V
I_{VIN2}	Input Current	PFM Mode I_{DC2OUT} =0		50		μA
I_{DC2OUT}	Available Output Current			3500		mA
V_{DC2OUT}	Output Voltage Range		0.5		1.54	V

V_{DC2_STEP}	Output Voltage Step	V_{DC2OUT}=0.5~1.2V			10		mV/step
		V_{DC2OUT}=1.22~1.54V			20		mV/step
V_{DC2_RIPPLE}	Output Voltage Ripple	PFM Mode		-30		+30	mV
		PWM Mode		-10		+10	mV
V_{DC2_ACC}	Output Voltage Accuracy	PFM	V_{DC2OUT}<=1V	-20		+40	mV
			V_{DC2OUT}>1V	-2%		+4%	
		PWM	V_{DC2OUT}<=1V	-30		+30	mV
			V_{DC2OUT}>1V	-3%		+3%	
V_{DC2_OVP}	Over Voltage Protection				130%* V_{DC2OUT}		V
V_{DC2_UVP}	Under Voltage Protection				85%* V_{DC2OUT}		V
DCDC3							
V_{IN3}	VIN3 Input Voltage			V_{OFF}		5.5	V
I_{VIN3}	Input Current	PFM Mode I_{DC3OUT} =0			50		uA
I_{DC3OUT}	Available Output Current				3500		mA
V_{DC3OUT}	Output Voltage Range			0.5		1.54	V
V_{DC3_STEP}	Output Voltage Step	V_{DC3OUT}=0.5~1.2V			10		mV/step
		V_{DC3OUT}=1.22~1.54V			20		mV/step
V_{DC3_RIPPLE}	Output Voltage Ripple	PFM Mode		-30		+30	mV
		PWM Mode		-10		+10	mV
V_{DC3_ACC}	Output Voltage Accuracy	PFM	V_{DC3OUT}<=1V	-20		+40	mV
			V_{DC3OUT}>1V	-2%		+4%	
		PWM	V_{DC3OUT}<=1V	-30		+30	mV
			V_{DC3OUT}>1V	-3%		+3%	
V_{DC3_OVP}	Over Voltage Protection				130%* V_{DC3OUT}		V
V_{DC3_UVP}	Under Voltage Protection				85%* V_{DC3OUT}		V
DCDC4							
V_{IN4}	VIN4 Input Voltage			V_{OFF}		5.5	V
I_{VIN4}	Input Current	PFM Mode I_{DC3OUT} =0			50		uA
I_{DC4OUT}	Available Output Current				2500		mA
V_{DC4OUT}	Output Voltage Range			0.5		1.54	V
V_{DC4_STEP}	Output Voltage Step	V_{DC4OUT}=0.5~1.2V			10		mV/step
		V_{DC4OUT}=1.22~1.54V			20		mV/step
V_{DC4_RIPPLE}	Output Voltage Ripple	PFM Mode		-30		+30	mV
		PWM Mode		-10		+10	mV
V_{DC4_ACC}	Output Voltage Accuracy	PFM	V_{DC4OUT}<=1V	-20		+40	mV

			V_{DC4OUT}>1V	-2%		+4%	
		PWM	V_{DC4OUT}<=1V	-30		+30	mV
			V_{DC4OUT}>1V	-3%		+3%	
V_{DC4_OVP}	Over Voltage Protection				130%* V_{DC4OUT}		V
V_{DC4_UVP}	Under Voltage Protection				85%* V_{DC4OUT}		V
DCDC5							
V_{IN5}	VIN5 Input Voltage			V_{OFF}		5.5	V
I_{VIN5}	Input Current	PFM Mode I_{DC3OUT} =0			50		uA
I_{DC5OUT}	Available Output Current				2500		mA
V_{DC5OUT}	Output Voltage Range			0.8		1.84	V
V_{DC5_STEP}	Output Voltage Step	V_{DC5OUT}=0.8~1.12V			10		mV/step
		V_{DC5OUT}=1.14~1.84V			20		mV/step
V_{DC5_RIPPLE}	Output Voltage Ripple	PFM Mode		-30		+30	mV
		PWM Mode		-10		+10	mV
V_{DC5_ACC}	Output Voltage Accuracy	PFM	V_{DC5OUT}<=1V	-20		+40	mV
			V_{DC5OUT}>1V	-2%		+4%	
		PWM	V_{DC5OUT}<=1V	-30		+30	mV
			V_{DC5OUT}>1V	-3%		+3%	
V_{DC5_OVP}	Over Voltage Protection				130%* V_{DC5OUT}		V
V_{DC5_UVP}	Under Voltage Protection				85%* V_{DC5OUT}		V
DCDC6							
V_{IN6}	VIN6 Input Voltage			V_{OFF}		5.5	V
I_{VIN6}	Input Current	PFM Mode I_{DC3OUT} =0			50		uA
I_{DC6OUT}	Available Output Current				2500		mA
V_{DC6OUT}	Output Voltage Range			0.5		3.4	V
V_{DC6_STEP}	Output Voltage Step				100		mV/step
V_{DC6_RIPPLE}	Output Voltage Ripple	PFM Mode		-30		+30	mV
		PWM Mode		-10		+10	mV
V_{DC6_ACC}	Output Voltage Accuracy	PFM	V_{DC6OUT}<=1V	-20		+40	mV
			V_{DC6OUT}>1V	-2%		+4%	
		PWM	V_{DC6OUT}<=1V	-30		+30	mV
			V_{DC6OUT}>1V	-3%		+3%	
V_{DC6_OVP}	Over Voltage Protection	V_{DC6OUT}<1.5V			130%* V_{DC6OUT}		V
		V_{DC6OUT}<1.5V			120%*		

				V_{DC6OUT}		
V_{DC6_UVP}	Under Voltage Protection			85%* V_{DC6OUT}		V
RTCLDO						
V_{RTCLDO}	Output Voltage	I_{RTC_VCC}=1mA	-1%	1.8 3.0	1%	V
I_{RTCLDO}	Output Current			100		mA
ALDO						
V_{ALDOIN}	ALDOIN Input Voltage		V_{OFF}		5.5	V
ALDO1						
V_{ALDO1}	Output Voltage Range	I_{ALDO1}=1mA	0.7		3.3	V
V_{ALDO1_STEP}	Output Voltage Step			100		mV/step
V_{ALDO1_ACC}	Output Voltage Accuracy			±1%		
I_{ALDO1}	Output Current			600		mA
I_Q	Quiescent Current			120		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{ALDO1}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
ALDO2						
V_{ALDO2}	Output Voltage Range	I_{ALDO2}=1mA	0.7		3.3	V
V_{ALDO2_STEP}	Output Voltage Step			100		mV/step
V_{ALDO2_ACC}	Output Voltage Accuracy			±1%		
I_{ALDO2}	Output Current			300		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{ALDO2}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
ALDO3						
V_{ALDO3}	Output Voltage Range	I_{ALDO3}=1mA	0.7		3.3	V
V_{ALDO3_STEP}	Output Voltage Step			100		mV/step
V_{ALDO3_ACC}	Output Voltage Accuracy			±1%		
I_{ALDO3}	Output Current			200		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{ALDO3}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
ALDO4						
V_{ALDO4}	Output Voltage Range	I_{ALDO4}=1mA	0.7		3.3	V
V_{ALDO4_STEP}	Output Voltage Step			100		mV/step
V_{ALDO4_ACC}	Output Voltage Accuracy			±1%		

I_{ALDO4}	Output Current			300		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{ALDO4}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
ALDO5						
V_{ALDO5}	Output Voltage Range	I_{ALDO5}=1mA	0.7		3.3	V
V_{ALDO5_STEP}	Output Voltage Step			100		mV/step
V_{ALDO5_ACC}	Output Voltage Accuracy			±1%		
I_{ALDO5}	Output Current			300		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{ALDO5}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
BLDO						
V_{BLDOIN}	BLDOIN Input Voltage		V_{OFF}		5.5	V
BLDO1						
V_{BLDO1}	Output Voltage Range	I_{BLDO1}=1mA	0.7		3.3	V
V_{BLDO1_STEP}	Output Voltage Step			100		mV/step
V_{BLDO1_ACC}	Output Voltage Accuracy			±1%		
I_{BLDO1}	Output Current			300		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{BLDO1}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
BLDO2						
V_{BLDO2}	Output Voltage Range	I_{BLDO2}=1mA	0.7		3.3	V
V_{BLDO2_STEP}	Output Voltage Step			100		mV/step
V_{BLDO2_ACC}	Output Voltage Accuracy			±1%		
I_{BLDO2}	Output Current			500		mA
I_Q	Quiescent Current			80		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{BLDO2}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
BLDO3						
V_{BLDO3}	Output Voltage Range	I_{BLDO3}=1mA	0.7		3.3	V
V_{BLDO3_STEP}	Output Voltage Step			100		mV/step
V_{BLDO3_ACC}	Output Voltage Accuracy			±1%		
I_{BLDO3}	Output Current			300		mA

I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{BLDO3}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
BLDO4						
V_{BLDO4}	Output Voltage Range	I_{BLDO4}=1mA	0.7		3.3	V
V_{BLDO4_STEP}	Output Voltage Step			100		mV/step
V_{BLDO4_ACC}	Output Voltage Accuracy			±1%		
I_{BLDO4}	Output Current			400		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{BLDO4}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
BLDO5						
V_{BLDO5}	Output Voltage Range	I_{BLDO5}=1mA	0.7		3.3	V
V_{BLDO5_STEP}	Output Voltage Step			100		mV/step
V_{BLDO5_ACC}	Output Voltage Accuracy			±1%		
I_{BLDO5}	Output Current			600		mA
I_Q	Quiescent Current			90		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{BLDO5}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
CLDO						
V_{CLDOIN}	CLDOIN Input Voltage		V_{OFF}		5.5	V
CLDO1						
V_{CLDO1}	Output Voltage Range	I_{CLDO1}=1mA	0.7		3.3	V
V_{CLDO1_STEP}	Output Voltage Step			100		mV/step
V_{CLDO1_ACC}	Output Voltage Accuracy			±1%		
I_{CLDO1}	Output Current			200		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{CLDO1}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
CLDO2						
V_{CLDO2}	Output Voltage Range	I_{CLDO2}=1mA	0.7		3.3	V
V_{CLDO2_STEP}	Output Voltage Step			100		mV/step
V_{CLDO2_ACC}	Output Voltage Accuracy			±1%		
I_{CLDO2}	Output Current			200		mA
I_Q	Quiescent Current			70		μA

PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{CLDO2}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
CLDO3						
V_{CLDO3}	Output Voltage Range	I_{CLDO3}=1mA	0.7		3.3	V
V_{CLDO3_STEP}	Output Voltage Step			100		mV/step
V_{CLDO3_ACC}	Output Voltage Accuracy			±1%		
I_{CLDO3}	Output Current			300		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{CLDO3}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
CLDO4						
V_{CLDO4}	Output Voltage Range	I_{CLDO4}=1mA	0.7		4.2	V
V_{CLDO4_STEP}	Output Voltage Step			100		mV/step
V_{CLDO4_ACC}	Output Voltage Accuracy			±1%		
I_{CLDO4}	Output Current			200		mA
I_Q	Quiescent Current			70		μA
PSRR	Power Supply Rejection Ratio	V_{in}=3.7V, I_{CLDO4}=10mA, 1KHz		70		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
CPUSLDO						
V_{CPUS}	Output Voltage	As reference of V_{DDR}		V_{DDR}/2		
		As General Purpose LDO, I_{CPUS}=1mA	0.7		1.4	V
V_{CPUS_STEP}	Output Voltage Step	As General Purpose LDO		50		mV/step
V_{CPUS_ACC}	Output Voltage Accuracy			±1%		
I_{CPUS}	Output Current	As reference of V_{DDR}		30		mA
		As General Purpose LDO		200		mA
I_Q	Quiescent Current	As General Purpose LDO		70		μA
PSRR	Power Supply Rejection Ratio	V_{DC5OUT}=1.84V, I_{CPUS}=10mA, 1KHz		60		dB
e_N	Output Noise,0-80KHz			40		μV_{RMS}
SWOUT						
R_{SWOUT}	Internal Ideal Resistance	PIN to PIN		100		mΩ

8. Block Diagram

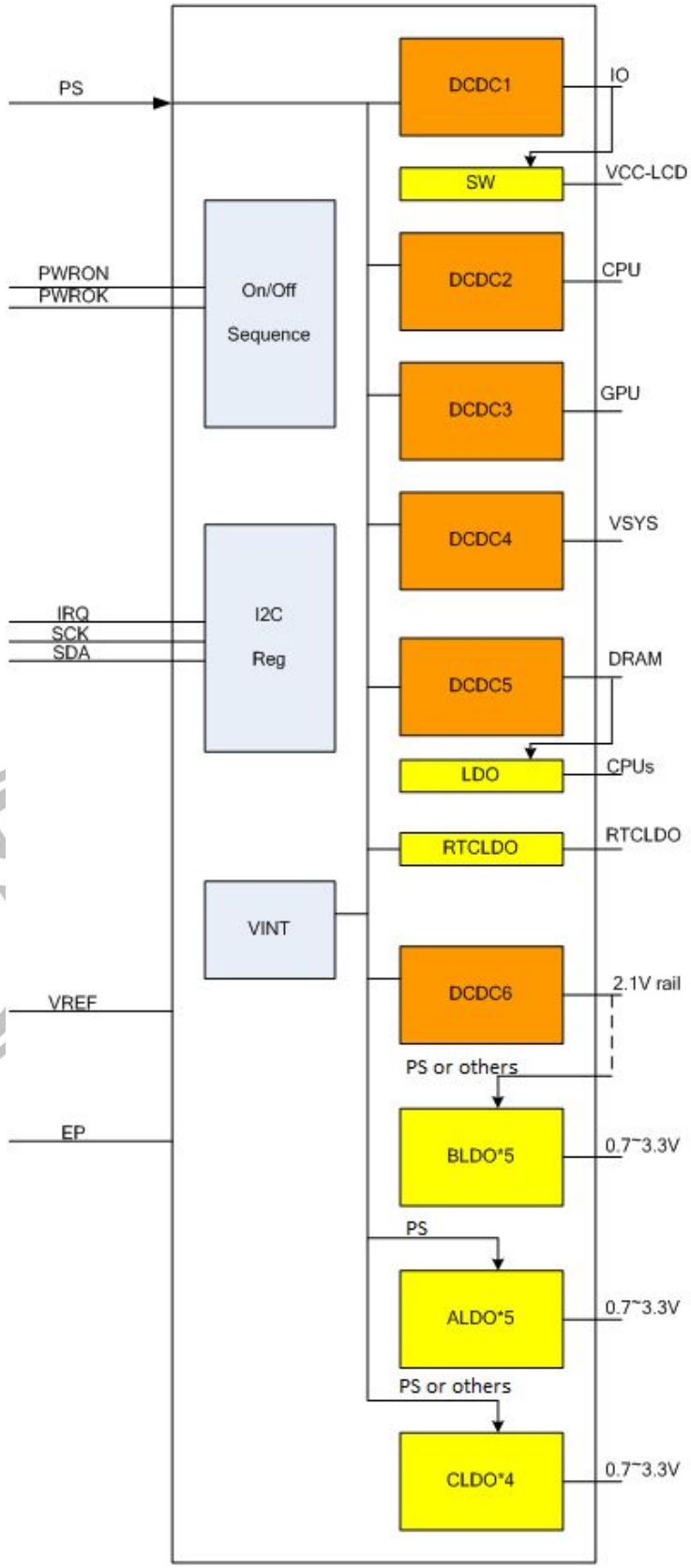


Figure 8-1. Block Diagram

9. Control and Operation

When AXP15060 is powered on, SCK/SDA pin of TWSI (two wire serial interface) will be pulled up to IO Power and then Host can adjust and monitor AXP15060 with rich feedback information.

Remarks: “Host” here refers to system processor.

9.1 Power On/Off & Reset

PMIC has power off and power on status. When at off state, all voltage outputs are turned off except RTCLDO and VREF. At this time, the total power consumption is typically 30uA.

Power on-off Key (POK)

EN/PWRON pin can be configured as PWRON pin or EN pin by customization. The default is PWRON pin. The Power on-off Key (POK) can be connected between PWRON pin and GND of AXP15060. AXP15060 can automatically identify the four status(Long-press ,Short-press ,Negative edge, Positive edge) and then correspond respectively.

Power on

1.When EN/PWRON pin is configured as PWRON pin, power on sources include:
(1).POK. AXP15060 can be powered on by pressing and holding POK for a period of time that longer than “ONLEVEL”.
(2).ALDOINGOOD low go high. The function can be configured by customization.
(3).IRQ Low level. When REG1FH[7]=1 and IRQ pin is low level for more than 16ms, AXP15060 will be powered on

2.When EN/PWRON pin is used as EN pin , AXP15060 can be powered on by EN pin from low go high(0.6V).

After power on, DC-DC and LDO will be soft booted in preset timing sequence.

Power Off

1.When EN/PWRON pin is configured as PWRON pin, power off sources include:
(1).POK. AXP15060 can be powered off by pressing and holding POK for a period of time that longer than “OFFLEVEL”. The function can be configured by REG36H[3] and REG36H[2] decides whether the PMIC auto turns on or not when it shuts down after OFFLEVEL POK.
(2).Write “1” to REG32H[7] .
(3).ALDOINGOOD high go low. When ALDOIN<VOFF or ALDOIN>5.8V, AXP15060 will be powered off. The default of VOFF is 2.6V which can be configured by REG1FH[5:3].
(4).The output voltage of DCDC is 15% lower than the setting value. The function can be configured by REG1EH[6:1].
(5).The output voltage of DCDC is much larger than their setting. The function can be configured by REG1EH[0].
(6).Die temperature is over the warning level2(125℃)。The function can be configured by REG32H[1].

Sleep and wakeup

When the running system needs to enter Sleep mode, Maybe one or several power outputs should be disabled or changed to other voltage. Wakeup can be initiated by the following sources:

1.Software wakeup (REG31H[5] is set to 1)

2.POK negative edge IRQ(EN/PWRON pin is configured as PWRON pin and REG41H[3] is set to 1)

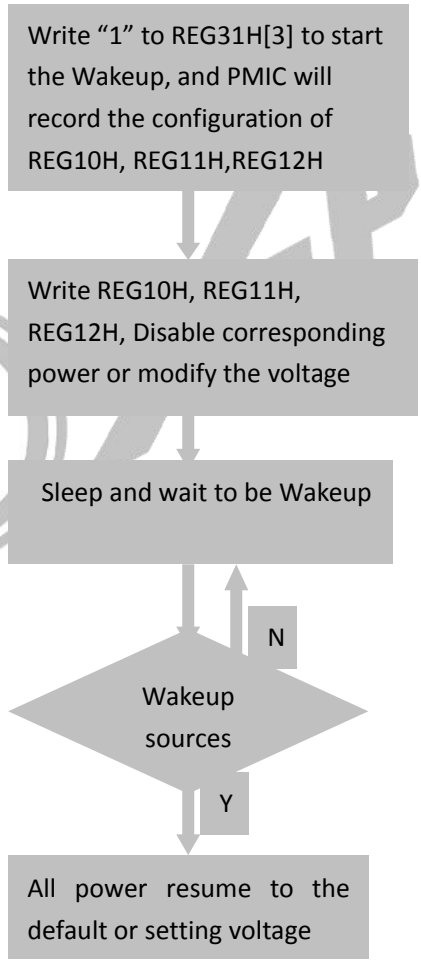
3.POK long press IRQ(EN/PWRON pin is configured as PWRON pin and REG41H[0] is set to 1)

4.IRQ pin wakeup(REG1FH[7]=1 and IRQ pin is low level for more than 16ms)

5.Wakeup pin input(REG2BH[6:5]=11 and the active level is detected; the active level can be configured by REG2BH[7])

These sources will make the all PMIC power outputs resume to the default voltage or the setting voltage, which is configured by REG31H[6], and all shutdown powers will resume by the startup sequence.

See the control process under sleep and wakeup modes as below:



Reset

The PMIC has system reset and power on reset.

- System reset

System reset means the registers will be reset when PMIC is powered on. When at system reset state, all voltage

outputs are turned off except RTCLDO and VREF. There are two ways of system reset.

(1).PWROK drive low.

The PWROK pin can be used as the reset signal of application system. During AXP15060 startup, PWROK outputs low level, which will be pulled up to startup the system after output voltage reaches the regulated value.

When application system works normally, If the PWROK pin is driven low by external key or other reasons, the PMIC will be restarted. The function can be configured by REG32H[4].

(2).Write "1" to REG32H[6] to restart the PMIC.

- Power on reset

Power on reset means the registers will be reset when PMIC is powered up. When at power on reset state, all voltage outputs are turned off including RTCLDO and VREF.

9.2 Multi-Power Outputs

The following table has listed the multi-power outputs and their functions of AXP15060.

Output Path	Type	Default Voltage	Startup Sequence	Application Suggestion	Load Capacity(Max)
DCDC1	BUCK	3.3V	2	IO/USB	2000mA
DCDC2	BUCK	0.9V	2	CPU	3500mA
DCDC3	BUCK	0.9V	1	GPU	3500mA
DCDC4	BUCK	0.9V	1	SYS	2000mA
DCDC5	BUCK	1.1V/DC5SET	1	DDR	2000mA
DCDC6	BUCK	OFF	OFF	LDO	2000mA
ALDO1	LDO	OFF	OFF	N/A	600mA
ALDO2	LDO	1.8V	2	N/A	300mA
ALDO3	LDO	1.8V	2	N/A	200mA
ALDO4	LDO	3.3V	2	N/A	300mA
ALDO5	LDO	2.5V	1	N/A	300mA
BLDO1	LDO	OFF	OFF	N/A	300mA
BLDO2	LDO	OFF	OFF	N/A	500mA
BLDO3	LDO	OFF	OFF	N/A	300mA
BLDO4	LDO	OFF	OFF	N/A	400mA
BLDO5	LDO	1.8V	2	N/A	600mA
CLDO1	LDO	OFF	OFF	N/A	200mA
CLDO2	LDO	3.3V	2	N/A	200mA
CLDO3	LDO	OFF	OFF	N/A	300mA
CLDO4	LDO	OFF	OFF	N/A	200mA
VCPUS	LDO	0.9V	1	CPUs/Reference of DDR	200mA
RTC-LDO	LDO	1.8V	Always on	RTC	100mA
DC1SW	Switch	OFF	OFF	N/A	1000mA

AXP15060 includes six synchronous step-down DCDCs, sixteen LDOs and one switch. The work frequency of DC-DC is 3MHz. External small inductors and capacitors can be connected. In addition, 6-ch DCDCs can be set in fixed PWM mode or auto mode (automatically switchable according to the load). See register REG1BH.

DCDC2/3/4/5 has DVM enable option. In DVM mode, when there is a change in the output voltage, DCDC will change to the new targeted value step by step. It supports two kinds of DVM slope:1step/15.625us and 1step/31.250us. The slope can be chosen by REG1AH[5].

DCDC2 and DCDC3 as well as DCDC4 and DCDC6 can be configured as dual phase DCDC to meet the high current requirement. When DCDC2/3 and DCDC4/6 are working as dual phase DCDC, the parameter setting is only controlled by the registers of DCDC2 and DCDC4.

DCDC5 voltage configuration is depended on the DC5SET pin and customization. When the DC5SET pin is connected to 1.8V, the default output is 1.5V. When a resistor(Rs) is connected between the DC5SET pin and GND, the default output is 1.1V. When DC5SET pin is connected to GND, the default output is 1.2V. When the DC5SET pin is floating, the default output is depended on customization.

DC5SET	GND	1.8V	Rs (20K~200K)	floating
Default voltage of DCDC5	1.2V	1.5V	1.1V	Customization，default is 1.36V

AXP15060 can configure the default voltage, the startup sequence and other control of all power output.
Startup sequence:The startup sequence has eight levels from 0 to 7. When the sequence is 0, it means the output is booted at the first step. When the sequence code is 1, it means the output is booted at the second step. When the sequence is 7, it means the output is not booted.
Default voltage setting: The default voltage of each channel can be set to each step within the output range.

9.3 Multi-Function Pin Description

EN/PWRON

EN/PWRON can be configured as EN pin or PWRON PIN by customization. When it is configured as PWRON pin, a Power on-off Key (POK) can be connected between PWRON pin and GND. When it is configured as EN pin, it can be used for dial switch.

CLDO4/GPIO2

It can be configured as LDO or GPIO. Please refer to REG2CH[2:0] Instruction for details.

CLDO3/GPIO1/WAKEUP

It can be configured as LDO or GPIO or WAKEUP pin. Please refer to REG2BH[6:5] Instruction for details.

9.4 Interrupt

PMIC Interrupt Controller monitors the trigger events such as over voltage, PWRON pin signal, over temperature and so on. When the events occur and their IRQ enable bits are set to 1 (Refer to registers REG40H and REG41H), corresponding IRQ status will be set to 1 (Refer to registers REG48H and REG49H), and IRQ pin (open drain) will be pulled down. When host detects triggered IRQ signal, host will scan through the IRQ Status registers and respond accordingly. Meanwhile, Host will reset the IRQ status by writing “1” to status bit.

The input edge IRQ of GPIO will only function when CLDO3/GPIO1/WAKEUP and CLDO4/GPIO2 are set as GPIO.

Bit	IRQ	DESCRIPTION
REG48_[7]	IRQ1	DCDC6 under voltage
REG48_[6]	IRQ2	DCDC5 under voltage
REG48_[5]	IRQ3	DCDC4 under voltage
REG48_[4]	IRQ4	DCDC3 under voltage
REG48_[3]	IRQ5	DCDC2 under voltage
REG48_[2]	IRQ6	DCDC1 under voltage
REG48_[1]	IRQ7	IC temperature over level2
REG48_[0]	IRQ8	IC temperature over level1
REG49_[5]	IRQ9	GPIO2 IRQ
REG49_[4]	IRQ10	POK positive edge
REG49_[3]	IRQ11	POK negative edge
REG49_[2]	IRQ12	GPIO1 IRQ
REG49_[1]	IRQ13	POK short press
REG49_[0]	IRQ14	POK long press

10. Register

10.1 Register List

Address	Description	R/W	Default
00	Power ON Source	R	
04-07	4 data buffers	R/W	00H
10	on-off control1	R/W	37H
11	on-off control2	R/W	62H
12	on-off control3	R/W	18H
13	DCDC1 Voltage control	R/W	12H
14	DCDC2 Voltage control	R/W	3CH
15	DCDC3 Voltage control	R/W	3CH
16	DCDC4 Voltage control	R/W	00H
17	DCDC5 Voltage control	R/W	2CH
18	DCDC6 Voltage control	R/W	06H
19	ALDO1 Voltage control	R/W	00H
1A	DCDC mode control1	R/W	00H
1B	DCDC mode control2	R/W	00H
1E	output monitor control & off discharge	R/W	81H
1F	IRQ & PWROK & Voff setting	R/W	07H
20	ALDO2 Voltage control	R/W	17H
21	ALDO3 Voltage control	R/W	00H
22	ALDO4 Voltage control	R/W	00H
23	ALDO5 Voltage control	R/W	00H
24	BLDO1 Voltage control	R/W	0BH
25	BLDO2 Voltage control	R/W	0BH
26	BLDO3 Voltage control	R/W	00H
27	BLDO4 Voltage control	R/W	00H
28	BLDO5 Voltage control	R/W	00H
29	CLDO1 Voltage control	R/W	00H
2A	CLDO2 Voltage control	R/W	04H
2B	CLDO3 voltage control & CLDO3/GPIO1/Wakeup control	R/W	1AH
2C	CLDO4/GPIO2 control	R/W	00H
2D	CLDO4 Voltage control	R/W	00H
2E	CPUSLDO Voltage control	R/W	00H
31	power wakeup CTRL	R/W	00H
32	power disable & power down sequence	R/W	24H
36	POK setting	R/W	59H
40	IRQ Enable1	R/W	03H

Address	Description	R/W	Default
41	IRQ Enable2	R/W	03H
48	IRQ Status1	R/W	00H
49	IRQ Status2	R/W	00H

10.2 Register Description

REG 00：Power ON source indication

Reset：system reset

Bit	Description	R/W
7-6	Reserved	R
5	Startup by ALDOINGOOD from L go H when EN is High	R
4	Startup by EN from L go H when ALDOINGOOD is High	R
3	Startup by IRQ pin	R
2	Startup by PWRON Press	R
1	Reserved	R
0	Startup by ALDOIN from L go H	R

REG 04-07：4 Data Buffers

Default：00H

Reset：Power on reset

REG 10：Output power on-off control 1

Default：37H

Reset：system reset

Bit	Description		R/W	Default
7-6	Reserved		RW	0
5	DCDC-6 on-off control	0-off; 1-on	RW	1
4	DCDC-5 on-off control	0-off; 1-on	RW	1
3	DCDC-4 on-off control	0-off; 1-on	RW	0
2	DCDC-3 on-off control	0-off; 1-on	RW	1
1	DCDC-2 on-off control	0-off; 1-on	RW	1
0	DCDC-1 on-off control	0-off; 1-on	RW	1

REG 11：Output power on-off control 2

Default：62H

Reset：system reset

Bit	Description		R/W	Default
7	BLDO3 on-off control	0-off; 1-on	RW	0
6	BLDO2 on-off control	0-off; 1-on	RW	1
5	BLDO1 on-off control	0-off; 1-on	RW	1
4	ALDO5 on-off control	0-off; 1-on	RW	0

3	ALDO4 on-off control	0-off; 1-on	RW	0
2	ALDO3 on-off control	0-off; 1-on	RW	0
1	ALDO2 on-off control	0-off; 1-on	RW	1
0	ALDO1 on-off control	0-off; 1-on	RW	0

REG 12：Output power on-off control 3

Default：18H

Reset：system reset

Bit	Description		R/W	Default
7	Switch on-off control	0-off; 1-on	RW	0
6	CPUSLDO on-off control	0-off; 1-on	RW	0
5	CLDO4 on-off control	0-off; 1-on	RW	0
4	CLDO3 on-off control	0-off; 1-on	RW	1
3	CLDO2 on-off control	0-off; 1-on	RW	1
2	CLDO1 on-off control	0-off; 1-on	RW	0
1	BLDO5 on-off control	0-off; 1-on	RW	0
0	BLDO4 on-off control	0-off; 1-on	RW	0

REG 13：DC/DC 1 voltage control

Default：12H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	DCDC-1 voltage setting bit4-0, default is 3.3V: 1.5~3.4V，100mV/step，20steps	RW	10010

REG 14：DC/DC 2 voltage control

Default：3CH

Reset：system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC-2 voltage setting bit6-0, default is 1.1V: 0.5~1.2V，10mV/step，71steps 1.22~1.54V，20mV/step，17steps	RW	0111100

REG 15：DC/DC 3 voltage control

Default：3CH

Reset：system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC-3 voltage setting bit6-0, default is 1.1V: 0.5~1.2V，10mV/step，71steps 1.22~1.54V，20mV/step，17steps	RW	0111100

REG 16：DC/DC 4 voltage control

Default：00H

Reset：system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC-4 voltage setting bit6-0, default is 0.5V: 0.5~1.2V，10mV/step，71steps 1.22~1.54V，20mV/step，17steps	RW	0000000

REG 17：DC/DC 5 voltage control

Default：2CH

Reset：system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC-5 voltage setting bit6-0, default is 1.36V: 0.8~1.12V，10mV/step，33steps 1.14~1.84V，20mV/step，36steps	RW	0101100

REG 18：DC/DC 6 voltage control

Default：06H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	DCDC-6 voltage setting bit4-0, default is 1.1V: 0.5~3.4V，100mV/step，30steps	RW	00110

REG 19：ALDO1 voltage control

Default：00H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	ALDO1 voltage setting bit4-0, default is 0.7V: 0.7~3.3V，100mV/step，27steps	RW	00000

REG 1A：DCDC mode control 1

Default：00H

Reset：system reset

Bit	Description		R/W	Default
7	DCDC 4&6 poly-phase control 0：no poly-phase；　　1：poly-phase		RW	0
6	DCDC 2&3 poly-phase control 0：no poly-phase；　　1：poly-phase		RW	0
5	DCDC DVM voltage ramp control	0：1step/15.625us	RW	0

		1：1step/31.250us		
4	Reserved		RW	0
3	DCDC-5 DVM on-off control	0：disable 1：enable	RW	0
2	DCDC-4 DVM on-off control		RW	0
1	DCDC-3 DVM on-off control		RW	0
0	DCDC-2 DVM on-off control		RW	0

REG 1B：DCDC mode control 2

Default：00H

Reset：system reset

Bit	Description		R/W	Default
7-6	Reserved		RW	0
5	DCDC-6 PFM/PWM control	0：auto switch 1：always PWM	RW	0
4	DCDC-5 PFM/PWM control		RW	0
3	DCDC-4 PFM/PWM control		RW	0
2	DCDC-3 PFM/PWM control		RW	0
1	DCDC-2 PFM/PWM control		RW	0
0	DCDC-1 PFM/PWM control		RW	0

REG 1E：Output monitor control & Discharge

Default：81H

Reset：Power on reset

Bit	Description	R/W	Default
7	Internal off-Discharge enable for Buck & LDO & SWITCH 0: disable 1: enable	RW	1
6	DCDC-6 85% low voltage turn off PMIC function 0: disable 1: enable	RW	0
5	DCDC-5 85% low voltage turn off PMIC function 0: disable 1: enable	RW	0
4	DCDC-4 85% low voltage turn off PMIC function 0: disable 1: enable	RW	0
3	DCDC-3 85% low voltage turn off PMIC function 0: disable 1: enable	RW	0
2	DCDC-2 85% low voltage turn off PMIC function 0: disable 1: enable	RW	0
1	DCDC-1 85% low voltage turn off PMIC function 0: disable 1: enable	RW	0
0	If voltage of DCDC is over 120%(130%) than their setting， the PMIC shutdown or not.（OVP） 0: not shutdown 1: shutdown	RW	1

REG 1F：IRQ & PWROK & VOFF setting

Default：07H

Reset：Power on reset

Bit	Description	R/W	Default
7	IRQ pin turn on or wakeup AXP15060 function enable. 0: disable 1: enable	RW	0
6	Reserved	RW	0
5-3	VOFF setting bit2-0: 2.6~3.3V，0.1V/step，8steps	RW	000
2	Enable for 4ms delay when PMIC power off normally 0：disable 1：enable	RW	1
1-0	Delay time between PWROK signal and power good time 00：8ms；01：16ms；10：32ms；11：64ms	RW	11

REG 20：ALDO2 voltage control

Default：17H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	ALDO2 voltage setting bit4-0, default is 3.0V: 0.7~3.3V，100mV/step，27steps	RW	10111

REG 21：ALDO3 voltage control

Default：00H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	ALDO3 voltage setting bit4-0, default is 0.7V: 0.7~3.3V，100mV/step，27steps	RW	00000

REG 22：ALDO4 voltage control

Default：00H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	ALDO4 voltage setting bit4-0, default is 0.7V: 0.7~3.3V，100mV/step，27steps	RW	00000

REG 23：ALDO5 voltage control

Default：00H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	ALDO5 voltage setting bit4-0, default is 0.7V: 0.7~3.3V，100mV/step，27steps	RW	00000

REG 24：BLDO1 voltage control

Default：0BH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	BLDO1 voltage setting bit4-0, default is 1.8V: 0.7~3.3V，100mV/step，27steps	RW	01011

REG 25：BLDO2 voltage control

Default：0BH

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	BLDO2 voltage setting bit4-0, default is 1.8V: 0.7~3.3V，100mV/step，27steps	RW	01011

REG 26：BLDO3 voltage control

Default：00H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	BLDO3 voltage setting bit4-0, default is 0.7V: 0.7~3.3V，100mV/step，27steps	RW	00000

REG 27：BLDO4 voltage control

Default：00H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	BLDO4 voltage setting bit4-0, default is 0.7V: 0.7~3.3V，100mV/step，27steps	RW	00000

REG 28：BLDO5 voltage control

Default：00H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	BLDO5 voltage setting bit4-0, default is 0.7V: 0.7~3.3V，100mV/step，27steps	RW	00000

REG 29：CLDO1 voltage control

Default：00H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	CLDO1 voltage setting bit4-0, default is 0.7V: 0.7~3.3V，100mV/step，27steps	RW	00000

REG 2A：CLDO2 voltage control

Default：04H

Reset：system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	CLDO2 voltage setting bit4-0, default is 1.1V: 0.7~3.3V，100mV/step，27steps	RW	00100

REG 2B：CLDO3 voltage control & CLDO3 /GPIO1/Wakeup control

Default：1AH

Reset：system reset

Bit	Description	R/W	Default
7	When REG2B[6:5]= 11, the active level: 0: low active 1: high active	RW	0
6-5	CLDO3/GPIO1/Wakeup pin function control: 00: CLDO3 01: GPIO1, Output low 10: GPIO1, Output high, high level set by REG2B[4:0],1.25V~3.3V 11: Wakeup, Input, threshold voltage is 1.2V	RW	00
4-0	CLDO3 voltage setting(GPIO1 high level) bit4-0, default is 3.3V: 0.7~3.3V, 100mV/step, 27steps	RW	11010

REG 2C：CLDO4/GPIO2

Default：00H

Reset：bit[2] power on reset, others system reset

Bit	Description	R/W	Default
7-4	Reserved	RW	0
3	When REG2C[2:0]=011, the GPIO2 input edge trigger IRQ setting 0: the negative edge 1: high positive edge	RW	0
2-0	CLDO4/GPIO2 pin function control: 000: CLDO4 001: GPIO2, Output low 010: GPIO2, Output high，high level set by REG2D[5:0], 1.25V~3.3V 011: GPIO2, Input, threshold voltage is 1.2V 100~101: Reserved 110~111: floating	RW	000

REG 2D：CLDO4 voltage control

Default：00H

Reset：system reset

Bit	Description	R/W	Default
7-6	Reserved	RW	0
5-0	CLDO4 voltage setting (GPIO2 high level) bit5-0, default is 0.7V: 0.7~4.2V, 100mV/step, 36steps	RW	000000

REG 2E：CPUSLDO voltage control

Default：00H

Reset：system reset

Bit	Description	R/W	Default
7-4	Reserved	RW	0
3-0	CPUSLDO voltage setting bit3-0, default is 0.7V: 0.7~1.4V, 50mV/step, 15steps; Vddr/2，0b'1111.	RW	0000

REG 31：Power wakeup CTRL

Default：00H

Reset：bit[3] is System reset，the others is Power on reset

Bit	Description	R/W	Default
7	PWROK drive low or not when Power wake up and REG31[3]=1. 0: not drive low 1: drive low in wake up period	RW	0
6	Voltage recovery control when AXP15060 wakeup 0: recovery to the default 1: Do nothing to the voltage	RW	0
5	Soft Power wakeup, write 1 to this bit, the output power will be wake up, and this bit will clear itself	RW	0
4	Control bit for IRQ output and wake up trigger when reg31[3] is 1 0 : IRQ pin is masked and IRQ can wake up AXP15060 1 : IRQ pin is normal and IRQ can not wake up AXP15060	RW	0
3	Enable bit for the function that output power be waked up by REG31_[5]、POKNIRQ、POKLIRQ、or IRQ pin is Low. 0: Wakeup function Off 1: Wakeup function On It self-clear after wakeup	RW	0
2-0	Reserved	RW	0

REG 32：Power disable & Power down sequence

Default：24H

Reset：bit [7:6] is System reset，the others is Power on reset

Bit	Description	R/W	Default
7	Power disable control. Write 1 to this bit will power off the PMIC，and this bit	RW	0

	will clear itself		
6	Host restart the PMIC and clear itself	RW	0
5	Enable for PMIC to monitor the status of PWROK pin to judge whether PMIC starts up normally 0: disable 1: enable	RW	1
4	Enable for restart the PMIC by PWROK drive low 0: disable 1: enable	RW	0
3	Output power down sequence control 0: at the same time 1: the reverse of the start up sequence	RW	0
2	Die temperature detect enable 0 : disable 1: enable	RW	1
1	The PMIC shut down or not when die temperature is over the warning level 2 0: not shutdown 1: shutdown	RW	0
0	Enable for 16s POK shut the PMIC 0: disable 1: enable	RW	0

REG 36：POK setting

Default：59H

Reset：bit3 is System reset，the others is Power on reset

Bit	Description	R/W	Default
7-6	ONLEVEL setting 00: 128ms 01: 1s 10: 2s 11: 3s	RW	01
5-4	IRQLEVEL setting 00: 1s 01: 1.5s 10: 2s 11: 2.5s	RW	01
3	Enable bit for the function which will shut down the PMIC when POK is larger than OFFLEVEL 0: disable 1: enable	RW	1
2	The PMIC auto turn on or not when it shut down after OFFLEVEL POK 0: not turn on 1: auto turn on	RW	0
1-0	OFFLEVEL setting 00: 4s 01: 6s 10: 8s 11: 10s	RW	01

REG 40：IRQ Enable1

Default：03H

Reset：System reset

Bit	Description	R/W	Default
7	Voltage of DCDC-6 is under 85% of setting IRQ enable	RW	0
6	Voltage of DCDC-5 is under 85% of setting IRQ enable	RW	0
5	Voltage of DCDC-4 is under 85% of setting IRQ enable	RW	0
4	Voltage of DCDC-3 is under 85% of setting IRQ enable	RW	0
3	Voltage of DCDC-2 is under 85% of setting IRQ enable	RW	0
2	Voltage of DCDC-1 is under 85% of setting IRQ enable	RW	0

1	Die temperature is over the warning level 2 IRQ enable	RW	1
0	Die temperature is over the warning level 1 IRQ enable	RW	1

REG 41：IRQ Enable2

Default：03H

Reset：System reset

Bit	Description	R/W	Default
7-6	Reserved	RW	0
5	GPIO2 IRQ enable	RW	0
4	POKPIRQ enable	RW	0
3	POKNIRQ enable	RW	0
2	GPIO1 IRQ enable	RW	0
1	POKSIRQ enable	RW	1
0	POKLIRQ enable	RW	1

REG 48：IRQ Status1

Default：00H

Reset：System reset

Bit	Description	R/W	Default
7	Voltage of DCDC-6 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0
6	Voltage of DCDC-5 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0
5	Voltage of DCDC-4 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0
4	Voltage of DCDC-3 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0
3	Voltage of DCDC-2 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0
2	Voltage of DCDC-1 is under 85% of setting，write 1 to this bit or the output rise to normal will clear it	RW	0
1	Die temperature is over the warning level 2 Write 1 to it or temperature drop to level 2 will clear it	RW	0
0	Die temperature is over the warning level 1 Write 1 to it or temperature drop to level 1 will clear it	RW	0

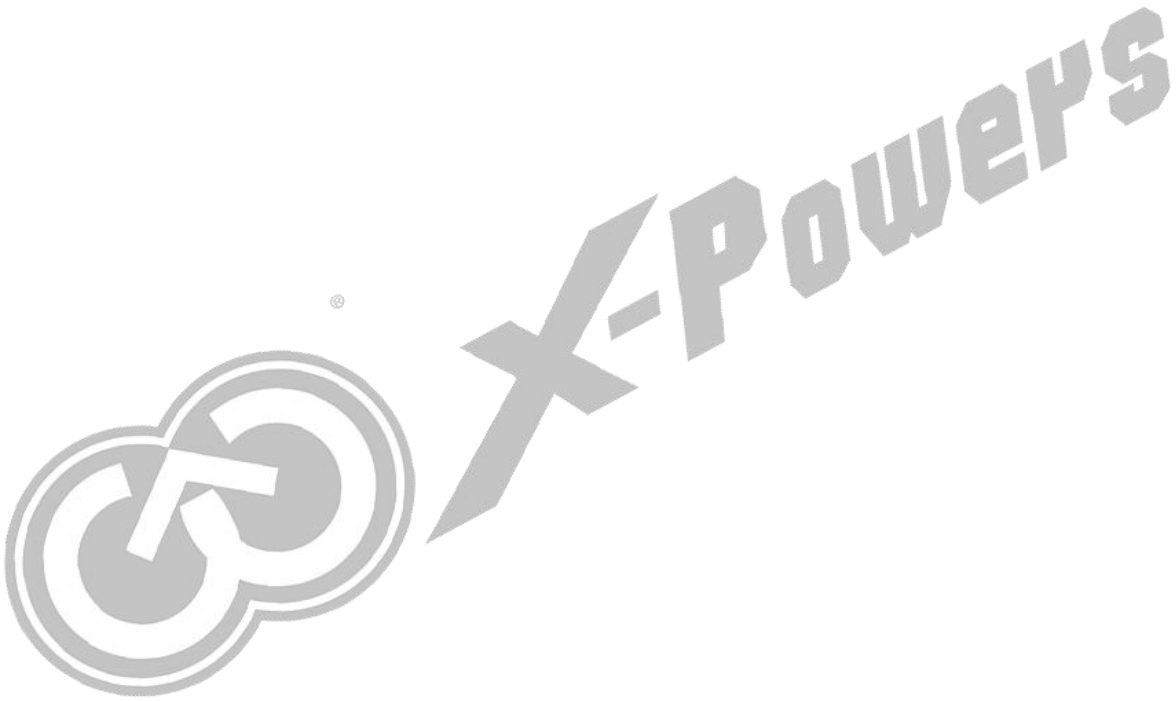
REG 49：IRQ Status2

Default：00H

Reset：System reset

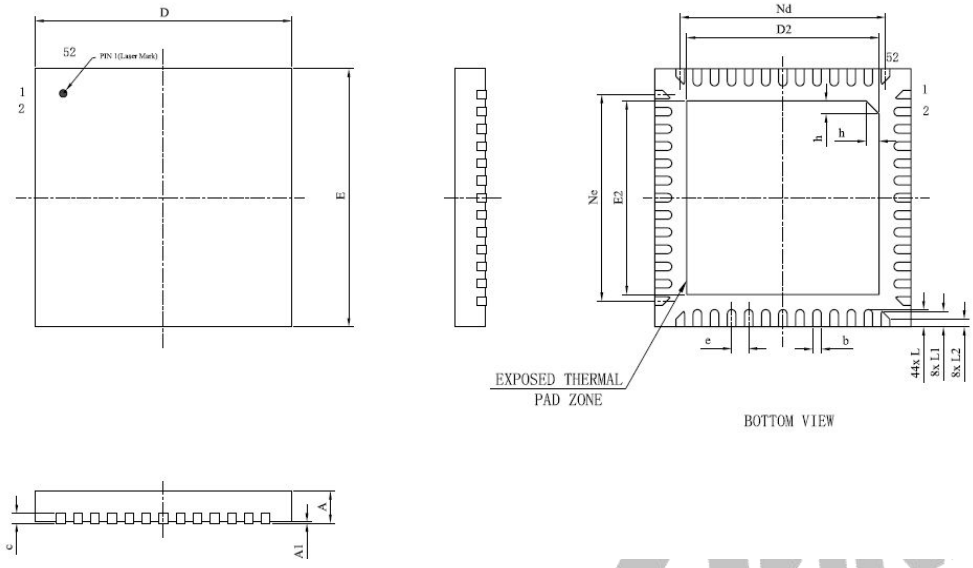
Bit	Description	R/W	Default
7-6	Reserved	RW	0
5	GPIO2 IRQ, write 1 to it will clear it	RW	0
4	POKPIRQ,write 1 to it will clear it	RW	0

3	POKNIRQ,write 1 to it will clear it	RW	0
2	GPIO1 IRQ,write 1 to it will clear it	RW	0
1	POKSIRQ,write 1 to it will clear it	RW	0
0	POKLIRQ,write 1 to it will clear it	RW	0



11. Package

AXP15060 package is QFN6*6, 52-pin.

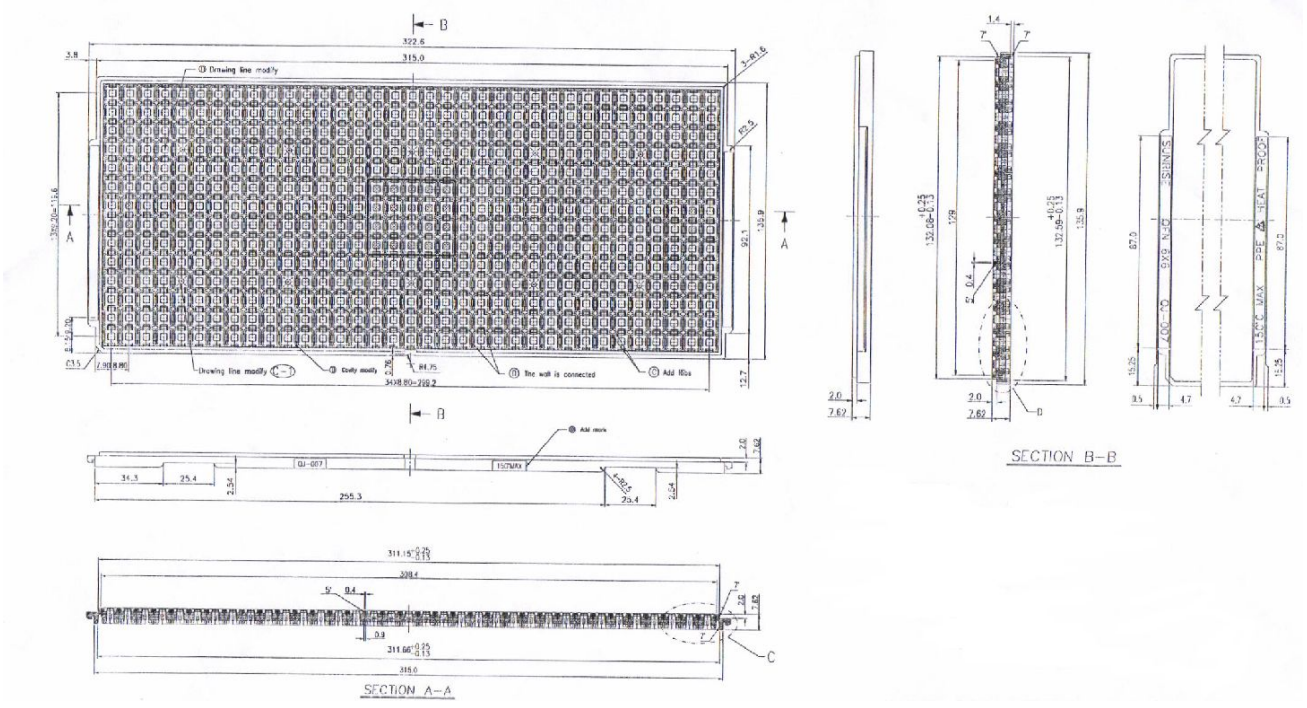


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.35	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
L/F载体尺寸 (mil)	185*185		

Marking information:

The first five stand for LOT, as long as the first five number is same, then the lot is same. The six and seven stand for IC version, the last four is related to package information.

Tray Information:



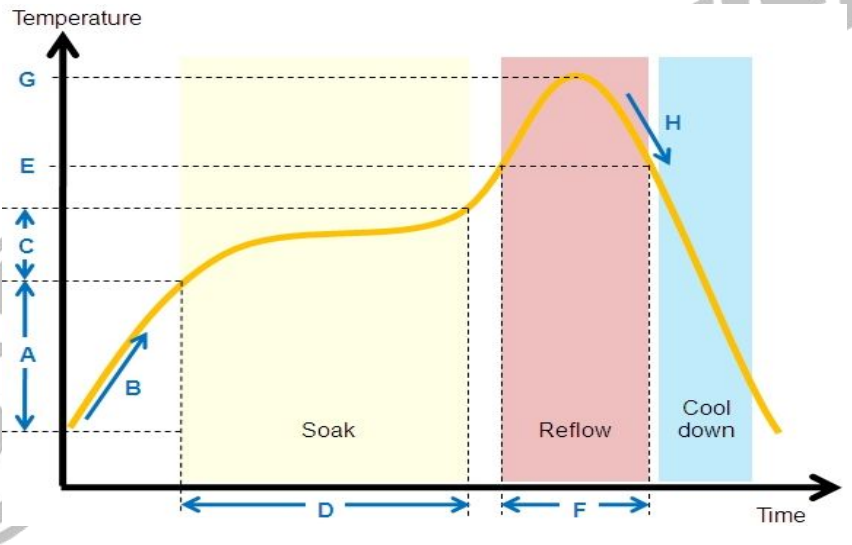
Tray Package Information:

Item	Color	Size
Aluminum foil bags	Silvery white	540mm x 300mm x 0.14mm
Pearl cotton cushion(Vacuum bag)	White	12mm x 680mm x 185mm
Pearl cotton cushion (The Gap between vacuum bag and inside box)	White	Left-Right:12mm x 180mm x 85mm Front-Back:12mm x 350mm x 70mm
Inside Box	White	396mm x 196mm x 96mm
Outside Box	White	420mm x 410mm x 320mm

Order Information:

Type	Quantity	Part Number
Tray	490pcs/Tray 10trays/Package	AXP15060

Mounting Conditions:



	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25℃ -> 150℃
B	Preheat ramp up rate	1.5~2.5 ℃/sec
C	Soak temperature range	150℃ -> 190℃
D	Soak time	80~110 sec
E	Liquidus temperature	217℃
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250℃
H	Cool down temperature rate	≤4℃/sec