Cinterion® ALAS5V

Hardware Interface Description

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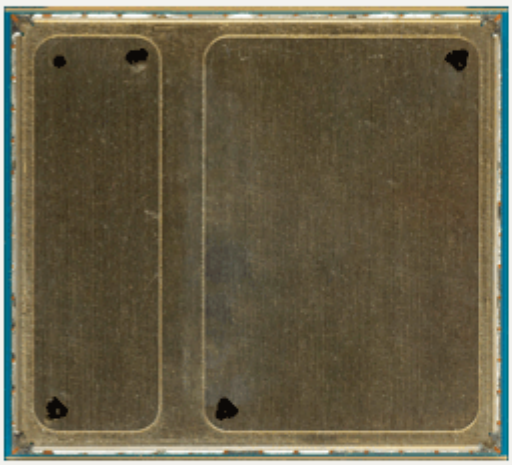

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1 Introduction

This document[1] describes the hardware of the Cinterion® ALAS5V module. It helps you quickly retrieve interface specifications, electrical and mechanical details and information on the requirements to be considered for integrating further components.

1.1 Product Variants

This document applies to the following Gemalto M2M modules:
- Cinterion® ALAS5V-W
- Cinterion® ALAS5V-CN
- Cinterion® ALAS5V-E
- Cinterion® ALAS5V-US

Where necessary a note is made to differentiate between the various product variants and releases.

1. The document is effective only if listed in the appropriate Release Notes as part of the technical documentation delivered with your Gemalto M2M product.

1.2 Key Features at a Glance

Feature	Implementation
General	
Frequency bands	Note: Not all of the frequency bands (and 3GPP technologies) mentioned throughout this document are supported by every ALAS5V product variant. Please refer to Section 1.2.1 for an overview of the frequency bands supported by each ALAS5V product variant.
GSM class	Small MS
Output power (according to Release 99)	GSM/GPRS/UMTS: Class 4 (+33dBm ±2dB) for EGSM850 and EGSM900 Class 1 (+30dBm ±2dB) for GSM1800 and GSM1900 Class E2 (+27dBm ± 3dB) for GSM 850 8-PSK and GSM 900 8-PSK Class E2 (+26dBm +3 /-4dB) for GSM 1800 8-PSK and GSM 1900 8-PSK Class 3 (+24dBm +1/-3dB) for all supported WCDMA FDD bands
Output power (according to Release 4)	TD-SCDMA: Class 2 (+24dBm +1/-3dB) for TD-SCDMA 1900 (Bd39) and TD-SCDMA 2000 (Bd34)
Output power (according to Release 8)	LTE (FDD): Class 3 (+23dBm ±2dB) for all supported LTE FDD bands LTE (TDD): Class 3 (+23dBm ±2dB) for all supported LTE TDD bands
Power supply	$3.3V \leq V_{BATT+} \leq 4.2V$
Operating temperature (board temperature)	Normal operation: -30°C to +85°C Restricted operation: -40°C to +95°C
Physical	Dimensions: 40mm x 36mm x 3mm Weight: 8.8g
RoHS	All hardware components fully compliant with EU RoHS Directive
LTE features	
3GPP Release 13	Down- and Uplink carrier aggregation (CA) to increase bandwidth, and thereby increase bitrate: • Maximum aggregated bandwidth: 80MHz • Maximum number of component carriers: 2 • Inter-band FDD • Intra-band FDD, TDD, contiguous, non-contiguous • Supported inter- and intra-band CA configurations: See Section 1.2.2 CAT 6 supported DL 300Mbps, UL 50Mbps 2x2 MIMO in DL direction
HSPA features	
3GPP Release 8	UE CAT. 14, 24 DC-HSPA+ – DL 42Mbps HSUPA – UL 5.76Mbps Compressed mode (CM) supported according to 3GPP TS25.212

Feature	Implementation
UMTS features	
3GPP Release 8	PS data rate – 384 kbps DL / 384 kbps UL
TD-SCDMA features	
3GPP Release 4	2.8 Mbps DL / 2.2Mbps UL
GSM / GPRS / EGPRS features	
Data transfer	GPRS: • Multislot Class 12 • Mobile Station Class B • Coding Scheme 1 – 4 EGPRS: • Multislot Class 12 • EDGE E2 power class for 8 PSK • Downlink coding schemes – CS 1-4, MCS 1-9 • Uplink coding schemes – CS 1-4, MCS 1-9 • SRB loopback and test mode B • 8-bit, 11-bit RACH • 1 phase/2 phase access procedures • Link adaptation and IR • NACC, extended UL TBF • Mobile Station Class B
SMS	Point-to-point MT and MO, Cell broadcast, Text and PDU mode
Software	
AT commands	Hayes, 3GPP TS 27.007 and 27.005, and proprietary Gemalto M2M commands
SIM Application Toolkit	SAT Release 99, letter classes b, c, e with BIP and RunAT support
Firmware update	Firmware update supported
GNSS Features	
Protocol	NMEA
Modes	Standalone GNSS (GPS, GLONASS, Beidou, Galileo) Integrated gpsOne 9HT support (GPS, GLONASS, Beidou, Galileo) QZSS and SBAS support
General	Power saving modes DC feed bridge and control of power supply for active antenna via GPIO
Interfaces	
Module interface	Surface mount device with solderable connection pads (SMT application interface). Land grid array (LGA) technology ensures high solder joint reliability and provides the possibility to use an optional module mounting socket. For more information on how to integrate SMT modules see also [3]. This application note comprises chapters on module mounting and application layout issues as well as on additional SMT application development equipment.

Feature	Implementation
Antenna	50Ω. GSM/UMTS/LTE main antenna, LTE Diversity/MIMO antenna, (active/passive) GNSS antenna
USB	USB 2.0 High Speed (480Mbit/s) device interface or USB 3.0 Super Speed (5Gbit/s) device interface
Serial interface	ASC0: • 8-wire (plus GND line) interface unbalanced, asynchronous • Fixed baud rates from 115,200 to 921,600bps • Supports RTS0/CTS0 hardware flow control Linux controlled only: ASC1: • 4-wire, unbalanced asynchronous interface • Fixed baud rates: 115,200bps to 921,60bps • Supports RTS1/CTS1 hardware flow control ASC2: 2-wire, unbalanced asynchronous interface at RXD2 and TXD2 lines used for tracing and debugging purposes (optional)
UICC interface	2 UICC interfaces (switchable) Supported chip cards: UICC/SIM/USIM 2.85V, 1.8V
I^2C interface	1 I^2C interface
Audio	2 digital interfaces (I^2S) - first DAI reserved for future use
Power on/off, Reset	
Power on/off	Switch-on by hardware signal IGT Switch-off by AT command (AT^SMSO) or IGT (option) Automatic switch-off in case of critical temperature or voltage conditions
Reset	Orderly shutdown and reset by AT command
Emergency-off	Emergency-off by hardware signal EMERG_OFF
Special Features	
Antenna	SAIC (Single Antenna Interference Cancellation) / DARP (Downlink Advanced Receiver Performance) Rx Diversity (receiver type 3i - 64-QAM) / MIMO
GPIO	15 I/O pins of the application interface programmable as GPIO. GPIO1 can be configured as dead reckoning synchronization signal. Programming can be done via AT commands.
Emergency call handling (not for -US variant)	EU eCall 3GPP Release 10 compliant (modem) ERA compliant (modem and GNSS)
ADC inputs	Analog-to-Digital Converter with four unbalanced analog inputs for (external) antenna diagnosis
JTAG	JTAG interface for debug purposes
eMMC	Linux controlled: Embedded Multi-Media Card interface
PCIe	Linux controlled: PCIe interface
Evaluation kit	
Evaluation module	ALAS5V module soldered onto a dedicated PCB.

1.2.1 Supported Frequency Bands

The following table lists the supported frequency bands for each of the ALAS5V product variants mentioned in Section 1.1. Supported CA configurations can be found in Section 1.2.2.

Table 1: Supported frequency bands for each product variant

Band	ALAS5V-W	ALAS5V-CN	ALAS5V-E	ALAS5V-US
GSM/GPRS/EDGE				
850MHz	x			x
900MHz	x	x	x	x
1800MHz	x	x	x	x
1900MHz	x			x
UMTS/HSPA				
Bd.I (2100MHz)	x	x	x	
Bd.II (1900MHz)				x
Bd.III (1800MHz)	x	x	x	
Bd.IV (1700MHz)				x
Bd.V (850MHz)	x			x
Bd.VI (850MHz)	x			
Bd.VIII (900MHz)	x	x	x	
Bd.XIX (850MHz)	x			
TD-SCDMA				
Bd.34 (2000MHz)		x		
Bd.39 (1900MHz)		x		
LTE-FDD				
Bd.1 (2100MHz)	x	x	x	
Bd.2 (1900MHz)				x
Bd.3 (1800MHz)	x	x	x	
Bd.4 (1700MHz)				x
Bd.5 (850MHz)	x			x
Bd.7 (2600MHz)	x	x	x	
Bd.8 (900MHz)	x	x	x	
Bd.12 (700MHz)				x
Bd.18 (850MHz)	x			
Bd.19 (850MHz)	x			
Bd.20 (800MHz)	x		x	
Bd.26 (850MHz)	x			
Bd.28 (700MHz)	x		x	
Bd.66 (1700MHz)				x

Table 1: Supported frequency bands for each product variant

Band	ALAS5V-W	ALAS5V-CN	ALAS5V-E	ALAS5V-US
LTE-TDD				
Bd.38 (2600MHz)	x	x		
Bd.39 (1900MHz)	x	x		
Bd.40 (2300MHz)	x	x		
Bd.41 (2600MHz)[1]	x	x		

1. **Note:** Out of the 3GPP specified frequency range for LTE Band 41, only that part which is used in China and Japan (2545MHz to 2655MHz) is supported by ALAS5V. For the US market LTE Band 41 is disabled by software.

1.2.2 Supported CA Configurations

The following table lists the supported CA configurations (aka supported band combinations) for each of the ALAS5V product variants mentioned in Section 1.1.

Table 2: Supported CA configurations

Downlink CA	Bandwidth combination set	Product variant (ALAS5V-...)
Intra-band continuous		
CA_1C	0, 1	E, W, CN
CA_2C	0	US
CA_3C	0	E, W, CN
CA_5B	0, 1	US, W
CA_7B	0	E, US, W, CN
CA_7C	0, 1, 2	E, US, W, CN
CA_8B	0	W
CA_12B	0	US
CA_38C	0	W, CN
CA_39C	0	W, CN
CA_40C	0, 1	W, CN
CA_41C	0, 1, 2, 3	CN
CA_66B	0	US
CA_66C	0	US
Intra-band non-continuous		
CA_2A-2A	0	US
CA_3A-3A	0, 1, 2	E, W, CN
CA_4A-4A	0, 1	US
CA_7A-7A	0, 1, 2, 3	E, US, W, CN
CA_40A-40A	0, 1	W, CN
CA_41A-41A	0, 1	CN
CA_66A-66A	0	US
CA_66A-66B	0	US

Table 2: Supported CA configurations

Downlink CA	Bandwidth combination set	Product variant (ALAS5V-...)
Inter-band (two bands)		
CA_1A-5A	0, 1	W
CA_1A-8A	0, 1, 2	E, W, CN
CA_1A-18A	0, 1	W
CA_1A-19A	0	W
CA_1A-20A	0	E, W
CA_1A-26A	0, 1	W
CA_1A-28A	0, 1	E, W
CA_2A-5A	0, 1	US
CA_2A-5B	0	US
CA_2A-12A	0, 1, 2	US
CA_2A-12B	0	US
CA_2A-28A	0	US
CA_2A-29A	0, 1, 2	US
CA_3A-5A	0, 1, 2, 3,4	W
CA_3A-8A	0, 1, 2, 3	E, W, CN
CA_3A-19A	0	W
CA_3A-20A	0, 1	E, W
CA_3A-26A	0, 1	W
CA_3A-28A	0, 1	E, W
CA_3C-8A	0	CN
CA_4A-5A	0, 1	US
CA_4A-12A	0, 1, 2, 3, 4, 5	US
CA_4A-12B	0	US
CA_4A-28A	0	US
CA_4A-29A	0, 1, 2	US
CA_5A-7A	0, 1	US, W
CA_5A-30A	0	US
CA_5A-40A	0, 1	W
CA_5B-30A	0	US
CA_5A-66A	0	US
CA_5A-66B	0	US
CA_5B-66A	0	US
CA_7A-8A	0, 1, 2	E, W, CN
CA_7A-12A	0	US
CA_7A-20A	0, 1	E, W
CA_7A-28A	0, 1	E, US, W
CA_7B-28A	0	E, US, W
CA_8A-40A	0, 1	W, CN
CA_8A-41A	0, 1	CN
CA_12A-30A	0	US
CA_12A-66A	0, 1, 2, 3, 4, 5	US

Table 2: Supported CA configurations

Downlink CA	Bandwidth combination set	Product variant (ALAS5V-...)
CA_20A-38A	0	W
CA_20A-40A	0	W
CA_28A-40A	0	W
CA_29A-66A	0	US

1.3 ALAS5V System Overview

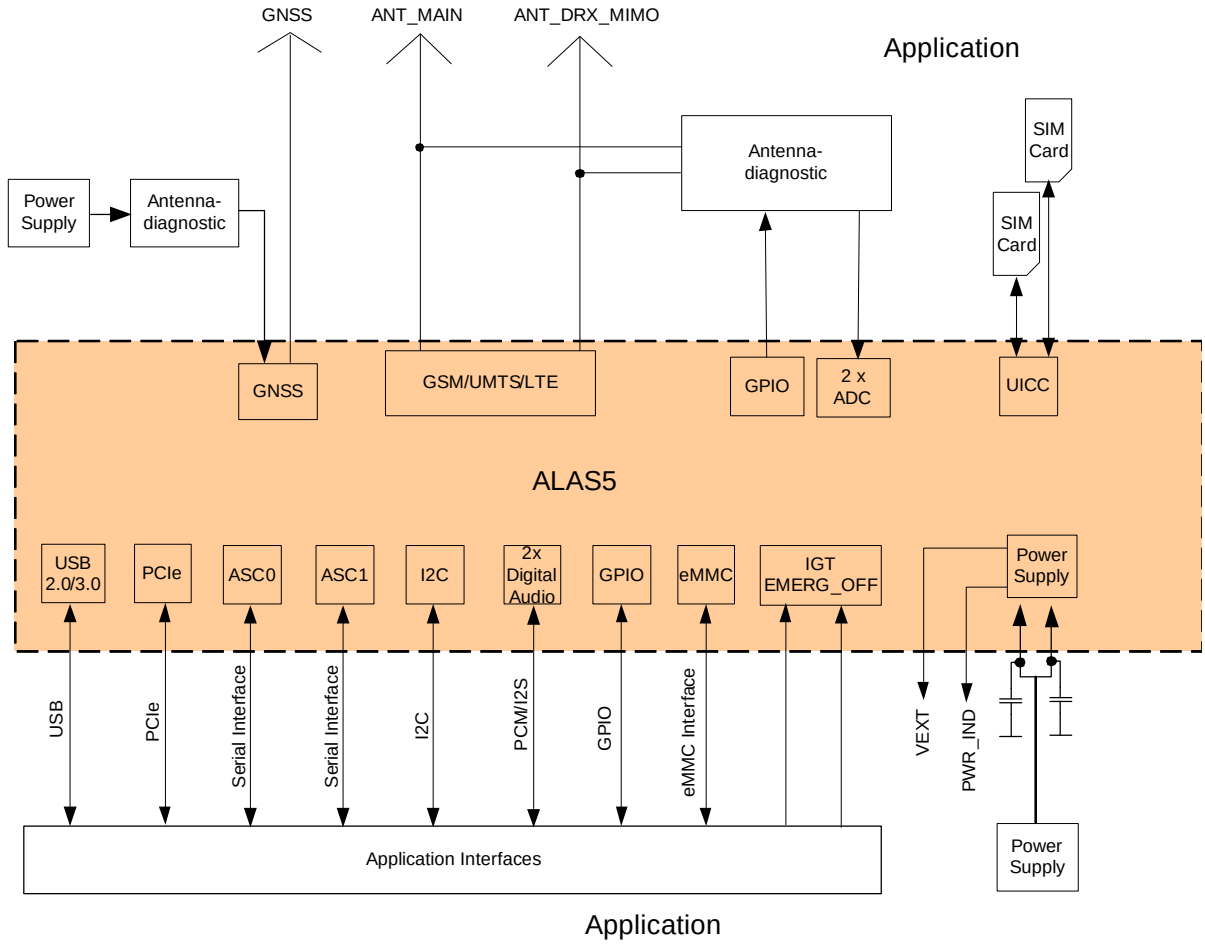


Figure 1: ALAS5V system overview

1.4 Circuit Concept

Figure 2 shows a block diagram of the ALAS5V module and illustrates the major functional components:

Baseband block:
- GSM/UMTS/LTE controller/transceiver/power supply
- NAND/LPDDR2 memory devices
- Application interface (SMT with connecting pads)

RF section:
- RF transceiver
- RF power amplifier/frontend
- RF filter
- GNSS receiver/Front end
- Antenna pad

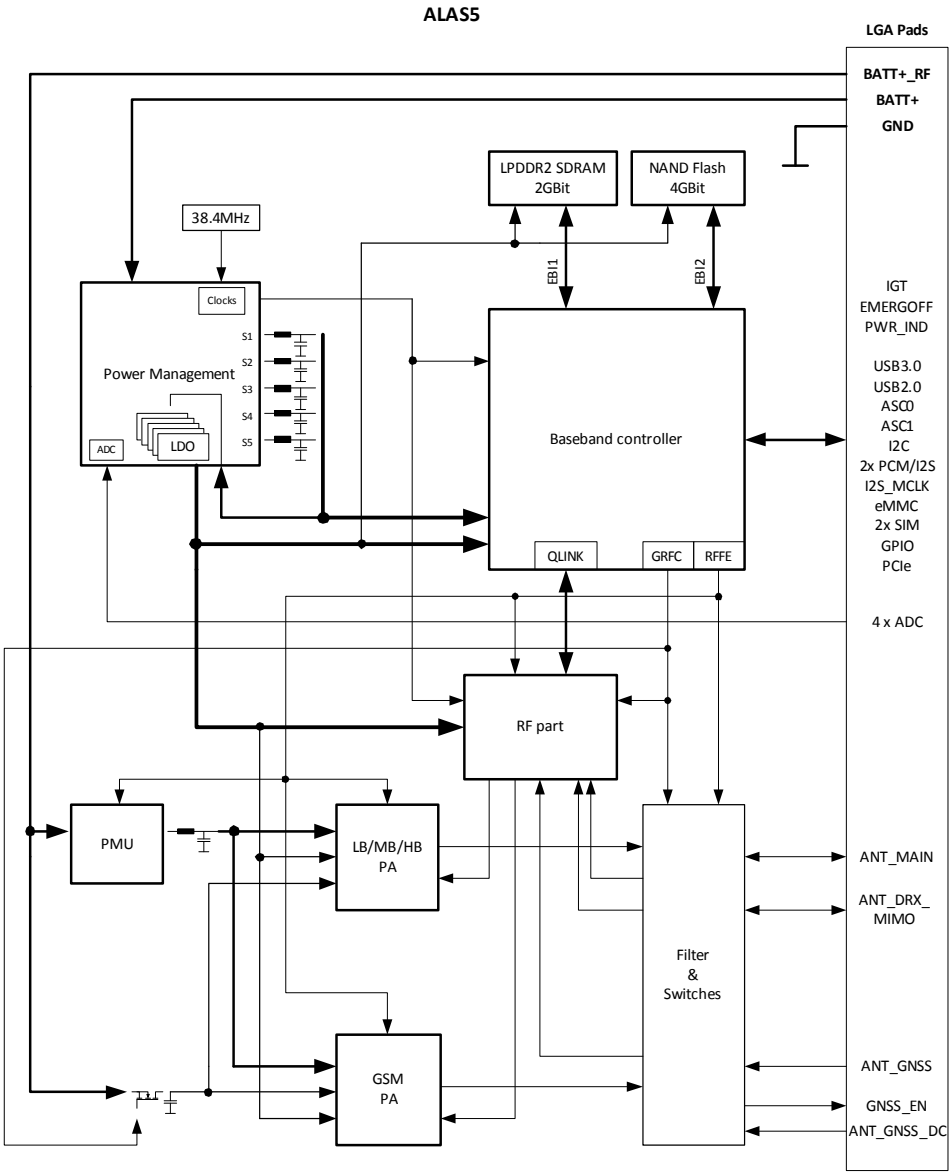


Figure 2: ALAS5V block diagram

2 Interface Characteristics

ALAS5V is equipped with an SMT application interface that connects to the external application. The SMT application interface incorporates the various application interfaces as well as the RF antenna interface.

2.1 Application Interface

2.1.1 Pad Assignment

The SMT application interface on the ALAS5V provides connecting pads to integrate the module into external applications. Table 3 lists the pads' assignments. Figure 3 (bottom view) and Figure 4 (top view) show the connecting pads' numbering plan.

Please note that a number of connecting pads are marked as reserved for future use (rfu) and further qualified as either (<name>), (dnu), (GND) or (nc):

- Pads marked as "rfu" and qualified as "<name>" (signal name) may be soldered and could be connected to an external application compliant to the signals' electrical characteristics as described in Table 4.
- Pads marked "rfu" and qualified as "dnu" (do not use) may be soldered but should not be connected to an external application.
- Pads marked "rfu" and qualified as "GND" (ground) are assigned to ground with ALAS5V modules, but may have different assignments with future Gemalto M2M products using the same pad layout.
- Pads marked "rfu" and qualified as "nc" (not connected) are internally not connected with ALAS5V modules, but may be soldered and arbitrarily be connected to external ground.

Also note that some pads are marked with a circle (◯). These pads have a round shape for improved impedance control.

Gemalto strongly recommends to solder all connecting pads for mechanical stability and heat dissipation.

Also, Gemalto strongly recommends to provide test points for certain signal lines to and from the module while developing SMT applications – for debug and/or test purposes during the manufacturing process. In this way it is possible to detect soldering problems. Please refer to [3] for more information on test points and how to implement them. The signal lines for which test points should be provided for are marked as "Test point required" or "Test point recommended" in Section 2.1.2: Table 4 describing signal characteristics.

Table 3: Overview: Pad assignments

Pad No.	Signal Name	Pad No.	Signal Name	Pad No.	Signal Name
A2	GND	E15	rfu (dnu)	M5	GND
A5	GND	E16	rfu (dnu)	M6	GND
A6	GND	E17	rfu (dnu)	M7	GPIO17
A7	rfu (dnu)	E18	VEXT	M8	JTAG_WD_DISABLE
A8	GND	E19	rfu (dnu)	M9	I2CDAT1
A9	GND	E20	BATT+	M10	I2CCLK1
A10	GND	F2	ANT_DRX_MIMO	M11	rfu (dnu)
A11	rfu (dnu)	F3	GND	M12	rfu (dnu)
A12	GND	F4	GND	M13	EMMC_D6
A13	GND	F5	GND	M14	EMMC_D1
A14	GND	F6	rfu (dnu)	M15	GPIO22
A15	ANT_GNSS	F7	rfu (dnu)	M16	USB_DP
A16	GND	F8	rfu (nc)	M17	USB_DN
A17	ANT_GNSS_DC	F14	rfu (nc)	M18	CCCLK2
A20	GND	F15	GND	M19	CCCLK1
B4	rfu (dnu)	F16	EMERG_OFF	M20	GPIO8 (Interrupt)
B5	GND	F17	DSR0	N3	GND
B6	GND	F18	RXD0	N4	GND
B7	GND	F19	DTR0	N5	GND
B8	GND	F20	BATT+	N6	GND
B9	GND	G2	GND	N7	FSC2
B10	GND	G3	GND	N8	DOUT2
B11	GND	G4	GND	N9	DIN2
B12	GND	G5	GND	N10	BCLK2
B13	GND	G6	rfu (dnu)	N11	GND
B14	GND	G16	GND	N12	EMMC_D4
B15	GND	G17	GND	N13	EMMC_D5
B16	GND	G18	DCD0 / Download	N14	EMMC_D2
B17	GND	G19	CTS0	N15	EMMC_D0
B18	rfu (dnu)	G20	RTS0	N16	GND
C2	GND	H2	GND	N17	GND
C4	GND	H3	GND	N18	CCIN2
C5	GND	H4	GND	N19	CCIN1
C6	GND	H5	GND	P2	GND
C7	GND	H6	GND	P4	BATT+_RF
C8	GND	H16	USB_SSTX_P	P5	BATT+_RF
C9	GND	H17	USB_SSTX_N	P6	GPIO5 (Interrupt)
C10	GND	H18	GPIO6 (Interrupt)	P7	rfu (DIN1)
C11	GND	H19	TXD0	P8	rfu (DOUT1)
C12	GND	H20	rfu (BATT_ID)	P9	rfu (BCLK1)
C13	GND	J2	GND	P10	rfu (FSC1)
C14	GND	J3	GND	P11	MCLK
C15	GND	J4	GND	P12	EMMC_D7
C16	GND	J5	GND	P13	EMMC_CMD
C17	GPIO3 (Interrupt)	J6	rfu (dnu)	P14	EMMC_D3
C18	JTAG_TCK	J16	GND	P15	EMMC_CLK
C20	GND	J17	GND	P16	PCIE_CLK_P
D3	GND	J18	CCIO2	P17	PCIE_CLK_N
D4	GND	J19	CCIO1	P18	VUSB_IN
D5	GND	J20	RING0	P20	GND
D6	GND	K2	GND	R5	PWR_IND
D7	rfu (dnu)	K3	GND	R6	RTS1
D8	ADC4_IN	K4	GND	R7	CTS1
D9	ADC5_IN	K5	GND	R8	TXD1
D10	ADC1_IN	K6	rfu (dnu)	R9	RXD1
D11	ADC2_IN	K16	USB_SSRX_P	R10	PCIE_HOST_WAKE
D12	GPIO11	K17	USB_SSRX_N	R11	PCIE_HOST_RST
D13	GNSS_EN	K18	CCRST2	R12	GND
D14	JTAG_TMS	K19	CCVCC1	R13	GND
D15	JTAG_TRST	K20	rfu (dnu)	R14	PCIE_CLK_REQ
D16	JTAG_TDI	L2	ANT_MAIN	R15	GND
D17	JTAG_SRST	L3	GND	R16	GND
D18	JTAG_TDO	L4	GND	R17	GPIO16 (Interrupt)
D19	IGT	L5	GND	T2	GND
E2	GND	L6	rfu (dnu)	T5	rfu (dnu)
E3	GND	L7	EMMC_DETECT	T6	rfu (dnu)
E4	GND	L8	rfu (nc)	T7	FwSwap
E5	GND	L14	rfu (nc)	T8	TXD2
E6	GND	L15	EMMC_PWR	T9	GPIO15
E7	rfu (dnu)	L16	GND	T10	RXD2
E8	GPIO1/ DR_SYNC	L17	GND	T11	GND
E9	GPIO7 (Interrupt)	L18	CCVCC2	T12	PCIE_RX_P
E10	GPIO14	L19	CCRST1	T13	PCIE_RX_N
E11	GPIO13	L20	GPIO4	T14	GND
E12	GPIO12	M2	GND	T15	PCIE_TX_P
E13	JTAG_PS_HOLD	M3	GND	T16	PCIE_TX_N
E14	rfu (dnu)	M4	GND	T17	GND
				T20	GND

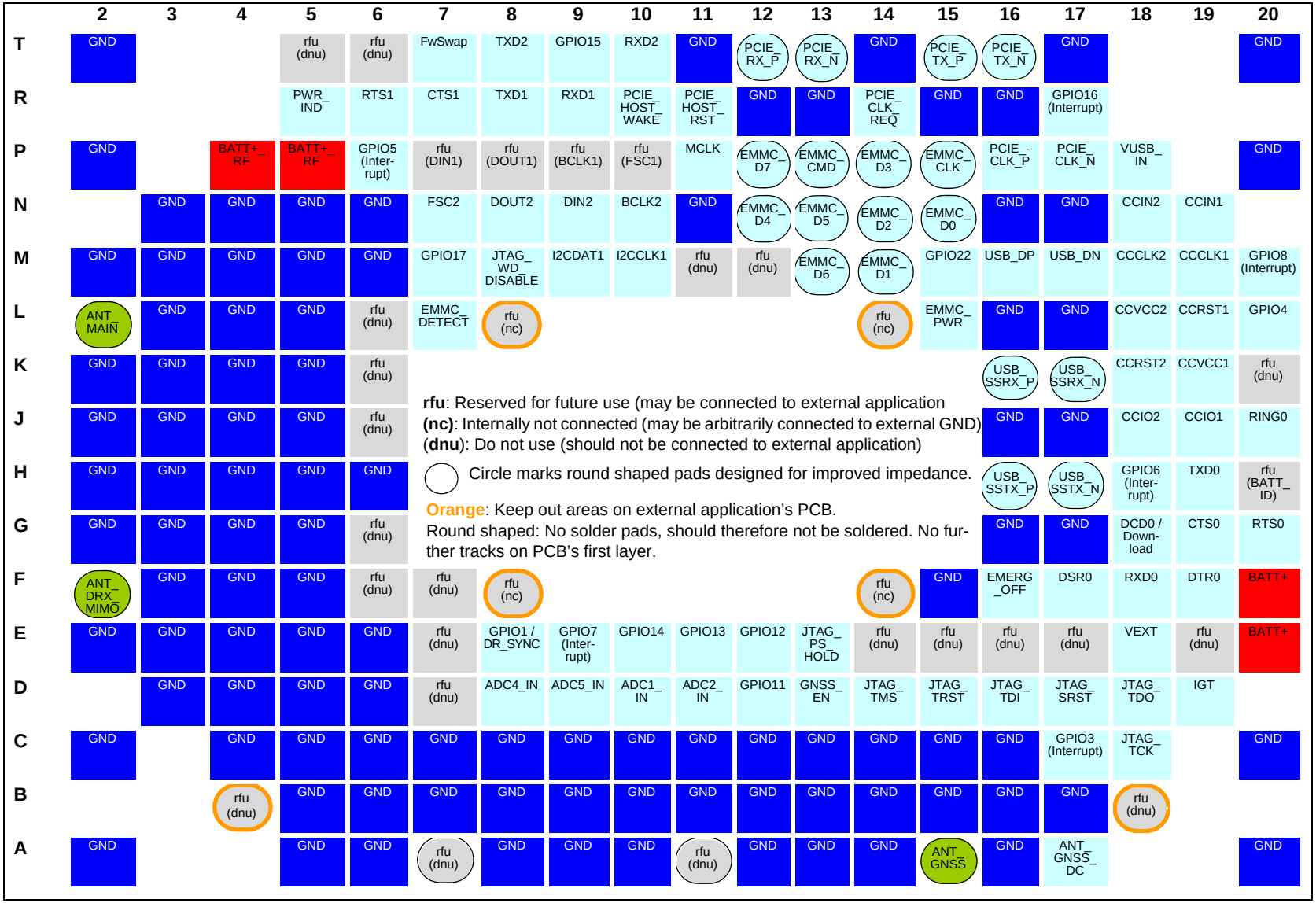


Figure 3: ALAS5V bottom view: Pad assignments

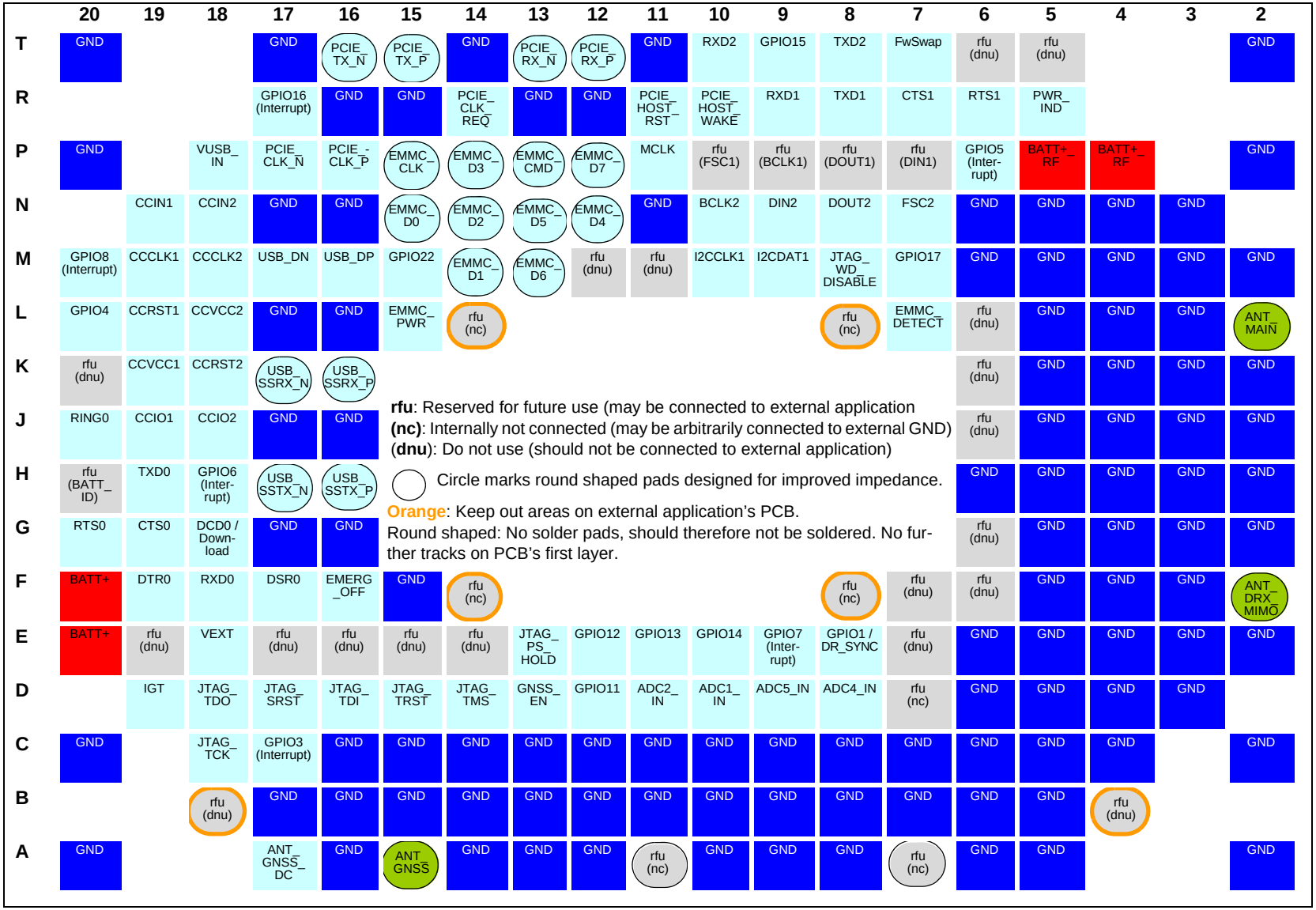


Figure 4: ALAS5V top view: Pad assignments

2.1.2 Signal Properties

Please note that the reference voltages listed in Table 4 are the values measured directly on the ALAS5V module. They do not apply to the accessories connected.

Table 4: Signal description

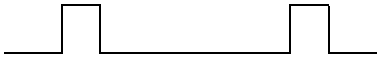
Function	Signal name	IO	Signal form and level	Comment
Power supply	BATT+ BATT+_RF	I	$V_I$max = 4.2V $V_I$min = 3.3V (on board)  n Tx = n x 577µs peak current every 4.615ms Imax = see Table 25 WCDMA TX continuous current Imax = see Table 25 LTE TX continuous current Imax = see Table 25	Supply voltage lines for general power management and the RF power amplifier. Lines of BATT+/BATT+_RF and GND respectively must be connected in parallel for supply purposes because higher peak currents may occur. Minimum voltage must not fall below 3.3V including drop, ripple, spikes.
	GND		Ground	Application Ground
External supply voltage	VEXT	O	$C_L$max = 1µF V_O = 1.80V -2.4%, +2% Normal operation: $I_O$max = -50mA SLEEP mode operation: $I_O$max = -1mA	VEXT may be used for application circuits. If unused keep line open. Test point recommended. The external digital logic must not cause any spikes or glitches on voltage VEXT. Do not exceed $I_O$max in any operation mode.
Supply voltage for active GNSS antenna (Input)	ANT_GNSS_DC	I	$V_I$max = 5V Imax = 50mA	If unused connect to GND. The input current must be limited to 50mA (antenna short circuit protection).
External GNSS supply voltage enable (output)	GNSS_EN	O	V_{OL}max = 0.45V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.30V at I = -2mA V_{OH}nom = 1.65V at I = -100µA V_{OH}max = 1.84V	Enable signal for an external voltage regulator (intended for active GNSS antenna, high=active). No external pull-up allowed during startup until the module has been secured in factory.

Table 4: Signal description

Function	Signal name	IO	Signal form and level	Comment
Ignition	IGT	I	R_{PU} ≈ 200kΩ V_{OH}max = 1.84V V_{IH}max =2.00V V_{IH}min = 1.30V V_{IL}max = 0.50V Low impulse width > 100ms	This signal switches the module on. It is required to drive this line low by an open drain or open collector driver connected to GND. Test point recommended.
Emer-gency off	EMERG_ OFF	I	R_{PU} ≈ 40kΩ V_{OH}max = 1.84V V_{IH}max = 2.00V V_{IH}min = 1.30V V_{IL}max = *0.50V* ~~|___|~~ low impulse width up to 2000ms (as long as PWR_IND stays low)	It is required to drive this line low by an open drain or open collector driver connected to GND until the module finally switches off. If unused keep line open. Test point recommended. Note that a low impulse of more than 2000ms will reset the module's RTC.
Firmware switch	FwSwap	I	V_{IL}max = 0.50V V_{IH}min = 1.30V V_{IH}max = 2.0V I_{IHPD} = 27.5µA…97.5µA I_{ILPU} = -27.5µA…-97.5µA $I_{High\text{-}Z\ max}$= ±1µA	Input during the startup phase: If FwSwap's state is High, a switch to the possible other, and currently not active firm-ware image is triggered. Test point required.
SIM card detection	CCIN1	I	R_{PU} ≈ 24kΩ to VEXT V_{OH}max=1.84V V_{IH}min = 1.25V at -25µA V_{IH}max= 2.0V V_{IL}max = 0.35V at -60µA	CCIN = Low means SIM card inserted. If SIM card holder does not support CCINx, connect to GND. CCIN2: External pull-up required - for details please refer to Section 2.1.7. If 2nd SIM interface not used, keep line open.
	CCIN2	I	V_{IL} (max) = 0.5V V_{IH} (min) = 1.30V V_{IH} (max) = 2.0V $I_{High\text{-}Z}$ (max) = ±1µA	

Table 4: Signal description

Function	Signal name	IO	Signal form and level	Comment
2.85V SIM card interfaces	CCRST1 CCRST2	O	V_{OL}max = 0.4V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 2.2V at I = -2mA V_{OH}nom = 2.65V at I = -100µA V_{OH}max = 2.91V	Maximum cable length or copper track should be not longer than 100mm to SIM card holder. CCIO2: External 10kW pull-up required - for details please refer to Section 2.1.7. If unused keep lines open.
	CCCLK1 CCCLK2			
	CCIO1 CCIO2	I/O	R_{PU} = 6.7..8.5kΩ V_{IL}max = 0.55V V_{IH}min = 2.35V V_{IH}max = 3.05V V_{OL}max = 0.4V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 2.35V at I ≥ -45µA V_{OH}max = 2.91V	
	CCVCC1 CCVCC2	O	$V_O$min = 2.75V $V_O$typ =2.85V $V_O$max = 2.91V $I_O$max = -50mA	
1.8V SIM card interface	CCRST1 CCRST2	O	V_{OL}max = 0.4V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.40V at I = -2mA V_{OH}min = 1.65V at I = -100µA V_{OH}max = 1.84V	Maximum cable length or copper track should be not longer than 100mm to SIM card holder. CCIO2: External 10kW pull-up required - for details please refer to Section 2.1.7. If unused keep lines open.
	CCCLK1 CCCLK2			
	CCIO1 CCIO2	I/O	R_{PU} = 6.7..8.5kΩ V_{IL}max = 0.30V V_{IH}min = 1.30V V_{IH}max = 1.84V V_{OL}max = 0.4V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.40V at I ≥ -50µA V_{OH}max = 1.84V	
	CCVCC1 CCVCC2	O	$V_O$min = 1.74V $V_O$typ = 1.80V $V_O$max = 1.84V $I_O$max = -50mA	
SIM interface shut-down	BATT_ID	I	External pull up to VEXT and pull down resistor within battery case required. R_{PU} = 100kΩ, R_{PD} = 10kΩ	Reserved for future use. Connect line to GND.
Serial Modem Interface ASC0	RXD0	O	V_{OL}max = 0.45V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.30V at I = -2mA V_{OH}nom = 1.65V at I = -100µA V_{OH}max = 1.84V	Test points recommended for TXD0, RXD0, DCD0, RTS0, and CTS0. If DCD0 is driven low during startup-phase, module enters Download Mode (see Section 4.2.2) If unused keep line open.
	CTS0	O		
	DSR0	O		
	RING0	O		
	DCD0	I/O		
	TXD0	I	V_{IL}max = 0.50V V_{IH}min = 1.30V V_{IH}max = 2.0V I_{IHPD} = 27.5µA…97.5µA I_{ILPU} = -27.5µA…-97.5µA $I_{High\text{-}Z\ max}$= ±1µA	
	RTS0	I		
	DTR0	I		

Table 4: Signal description

Function	Signal name	IO	Signal form and level	Comment
Serial Modem Interface ASC1	RXD1	O	V_{OL}max = 0.45V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.30V at I = -2mA V_{OH}nom = 1.65V at I = -100µA V_{OH}max = 1.84V	Test points recommended for RXD1, TXD1, CTS1, RTS1. If unused keep line open.
	CTS1	O		
	TXD1	I	V_{IL}max = 0.50V V_{IH}min = 1.30V V_{IH}max = 2.0V I_{IHPD} = 27.5µA…97.5µA I_{ILPU} = -27.5µA…-97.5µA $I_{High\text{-}Z\ max}$= ±1µA	
	RTS1	I		
Serial Debug Interface ASC2 (Gemalto internal)	RXD2	O	V_{OL}max = 0.45V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.30V at I = -2mA V_{OH}nom = 1.65V at I = -100µA V_{OH}max = 1.84V	No external pull-up / pull-down resistors allowed. Test points required. If unused keep line open.
	TXD2	I	V_{IL}max = 0.50V V_{IH}min = 1.30V V_{IH}max = 2.0V I_{IHPD} = 27.5µA…97.5µA I_{ILPU} = -27.5µA…-97.5µA $I_{High\text{-}Z\ max}$= ±1µA	
Power indicator	PWR_IND	O	V_{IH}max = 5.5V V_{OL}max = 0.45V at Imax = 2mA	PWR_IND (Power Indicator) notifies the module's on/off state. PWR_IND is an open collector that needs to be connected to an external pull-up resistor. Low state of the open collector indicates that the module is on. Vice versa, high level notifies the Power Down mode. Therefore, the signal may be used to enable external voltage regulators that supply an external logic for communication with the module, e.g. level converters. Test point recommended.

Table 4: Signal description

Function	Signal name	IO	Signal form and level	Comment
USB	VUSB_IN	I	V_{IN}min = 3.0V V_{IN}max = 5.75V $I_I$max = 100µA Cin=1µF	USB detection. Test point recommended.
	USB_DN	I/O	Full and High speed signal (differential) characteristics according to USB 2.0 specification.	If unused keep lines open. Test point recommended. USB High Speed mode operation requires a differential impedance of 90Ω.
	USB_DP	I/O		
	USB_ SSRX_N	I	Super Speed signal (differential) Rx characteristics according USB 3.0 specification.	If unused keep lines open. USB Super Speed mode operation requires a differential impedance of 90Ω.
	USB_ SSRX_P	I		
	USB_ SSTX_N	O	Super Speed signal (differential) Tx characteristics according USB 3.0 specification.	
	USB_ SSTX_P	O		
Digital audio interface (PCM/I^2S)	DIN2	I	V_{OL}max = 0.45V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.30V at I = -2mA V_{OH}nom = 1.65V at I = -100µA V_{OH}max = 1.84V V_{IL}max = 0.50V V_{IH}min = 1.30V V_{IH}max = 2.0V I_{IHPD} = 27.5µA…97.5µA I_{ILPU} = -27.5µA…-97.5µA $I_{High\text{-}Z\ max}$= ±1µA	Digital audio interface configurable as PCM or I^2S interface. If unused keep lines open. First digital audio interface (DIN1, BCLK1, FSC1, and DOUT1) reserved for future use.
	BCLK2	I/O		
	FSC2	I/O		
	DOUT2	O		
	MCLK	O	V_{OL}max = 0.45V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.30V at I = -2mA V_{OH}nom = 1.65V at I = -100µA V_{OH}max = 1.84V fo = TBD. MHz	For I^2S: Master clock output Test point recommended in case I^2S interface is not used.

Table 4: Signal description

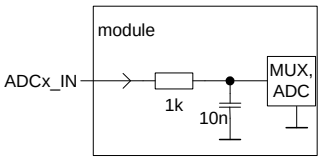
Function	Signal name	IO	Signal form and level	Comment
GPIO interface	GPIO1, GPIO3...8, GPIO11...17, GPIO22	I/O	V_{OL}max = 0.45V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.30V at I = -2mA V_{OH}nom = 1.65V at I = -100µA V_{OH}max = 1.84V V_{IL}max = 0.50V V_{IH}min = 1.30V V_{IH}max = 2.0V I_{IHPD} = 27.5µA…97.5µA I_{ILPU} = -27.5µA…-97.5µA $I_{High\text{-}Z\ max}$= ±1µA	GPIO3, GPIO5...GPIO7, GPIO8, and GPIO16 are interrupt enabled. They can be used to for instance wake up the module (see Section 2.1.12). Following functions can be configured for GPIOs using AT commands: GPIO1 --> DR_SYNC There is a 2.2k decoupling resistor between GPIO17 and JTAG_WD_DISABLE. Test points recommended for GPIO1, GPIO3. If unused keep lines open. However, GPIO7 and GPIO17, must be low during module startup until the module has been secured in factory.
1PPS interface	GPIO1 (DR_SYNC)	O	Clock signal with 1 pulse per second, frequency 1Hz, accuracy +/- 5ms	If the feature is enabled (see Chapter 3).
ADC interface	ADC1_IN, ADC2_IN, ADC4_IN, ADC5_IN	I	Full specification compliance range V_{Imin}>=0.10V V_{Imax}<=1.70V R_I ≈ 10MΩ Resolution: 14 Bit Accuracy: < ±2mV ADC conversion time t (max) = 550µs at 4.8MHz sample clock	If unused keep line open. Prepared for general purpose and antenna diagnostic use. 

Table 4: Signal description

Function	Signal name	IO	Signal form and level	Comment
PCIe	PCIE_RX_N	I	According to PCI Express Specification, Revision 2.0/2.1 (one lane, 5 GBit/s)	
	PCIE_RX_P			
	PCIE_TX_N	O		
	PCIE_TX_P			
	PCIE_CLK_N	I/O		
	PCIE_CLK_P			
	PCIE_-CLK_REQ	IO	V_{OL}max = 0.45V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.30V at I = -2mA V_{OH}nom = 1.65V at I = -100µA V_{OH}max = 1.84V V_{IL}max = 0.50V V_{IH}min = 1.30V V_{IH}max = 2.0V I_{IHPD} = 27.5µA…97.5µA I_{ILPU} = -27.5µA…-97.5µA $I_{High\text{-}Z\ max}$= ±1µA	Additional PCIe control signals
	PCIE_HOST_RST	O		
	PCIE_HOST_WAKE	I		
I^2C interface	I2CDAT1	I/O	V_{IL}max = 1.30V V_{IH}min = 0.50V V_{IH}max = 2.0V V_{OL}max = 0.3V at I = 3mA V_{OH}max = 1.84V I_{ILPU} = -27.5µA…-97.5µA	Open Drain Output (internal pull up) External pull up resistors required. Maximum load 510 Ohm.
	I2CCLK1	O		
JTAG interface	JTAG_SRST	I	V_{OL}max = 0.45V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.30V at I = -2mA V_{OH}nom = 1.65V at I = -100µA V_{OH}max = 1.84V V_{IL}max = 0.50V V_{IH}min = 1.30V V_{IH}max = 2.0V I_{IHPD} = 27.5µA…97.5µA I_{ILPU} = -27.5µA…-97.5µA $I_{High\text{-}Z\ max}$= ±1µA	Debug interface. Test point recommended for all JTAG lines.
	JTAG_TCK			
	JTAG_TDI			
	JTAG_TMS			
	JTAG_TRST			
	JTAG_TDO	O		
	JTAG_WD_-DISABLE	I	V_{IL}max = 0.3V at -100µA V_{IH}min = 1.50V at 100µA V_{IH}max = 2.0V	High during reset and start-up does disable the watch-dog timer (jumper to VEXT). There is a 2k2Ohm decoupling resistor between JTAG_WD_DISABLE and GPIO17.
	JTAG_PS_HOLD	I	V_{IH}min = 1.65V at 680µA V_{IL}max = 0.20V at 680µA V_{OH}max = 1.84V V_{OH}min = 1.30V at 150µA V_{OL}max = 0.5V at -200µA	High holds the power supply during debugging (jumper to VEXT).

Table 4: Signal description

Function	Signal name	IO	Signal form and level	Comment
eMMC interface	EMMC_ DETECT	I	V_{OL}max = 0.45V at I = 2mA V_{OL}nom = 0.1V at I = 100µA V_{OH}min = 1.30V at I = -2mA V_{OH}nom = 1.65V at I = -100µA V_{OH}max = 1.84V V_{IL}max = 0.50V V_{IH}min = 1.30V V_{IH}max = 2.0V I_{IHPD} = 27.5µA…97.5µA I_{ILPU} = -27.5µA…-97.5µA $I_{High\text{-}Z\ max}$= ±1µA	eMMC
	EMMC_PWR	O	$V_{OUT\ (nom)}$ = 2.95V / 1.8V $I_{OUT\ (max)}$ = 150mA	
1.8V eMMC	EMMC_CLK	O	V_{OL}max = 0.45V at rated drive strength V_{OH}min = 1.40V at rated drive strength V_{OH}max = 1.84V V_{IL}max = 0.58V at rated drive strength V_{IH}min = 1.27V at rated drive strength V_{IH}max = 2.0V $I_{High\text{-}Z\ max}$= ±5µA	
	EMMC_CMD	O		
	EMMC_D[0...7]	I/O		
2.95V eMMC	EMMC_CLK	O	V_{OL}max = 0.36V at rated drive strength V_{OH}min = 2.05V at rated drive strength V_{OH}max = 2.91V V_{IL}max = 0.68V at rated drive strength V_{IH}min = 1.82V at rated drive strength V_{IH}max = 3.05V $I_{High\text{-}Z\ max}$= ±10µA	
	EMMC_CMD	O		
	EMMC_D[0...7]	I/O		

2.1.2.1 Absolute Maximum Ratings

The absolute maximum ratings stated in Table 5 are stress ratings under any conditions. Stresses beyond any of these limits will cause permanent damage to ALAS5V.

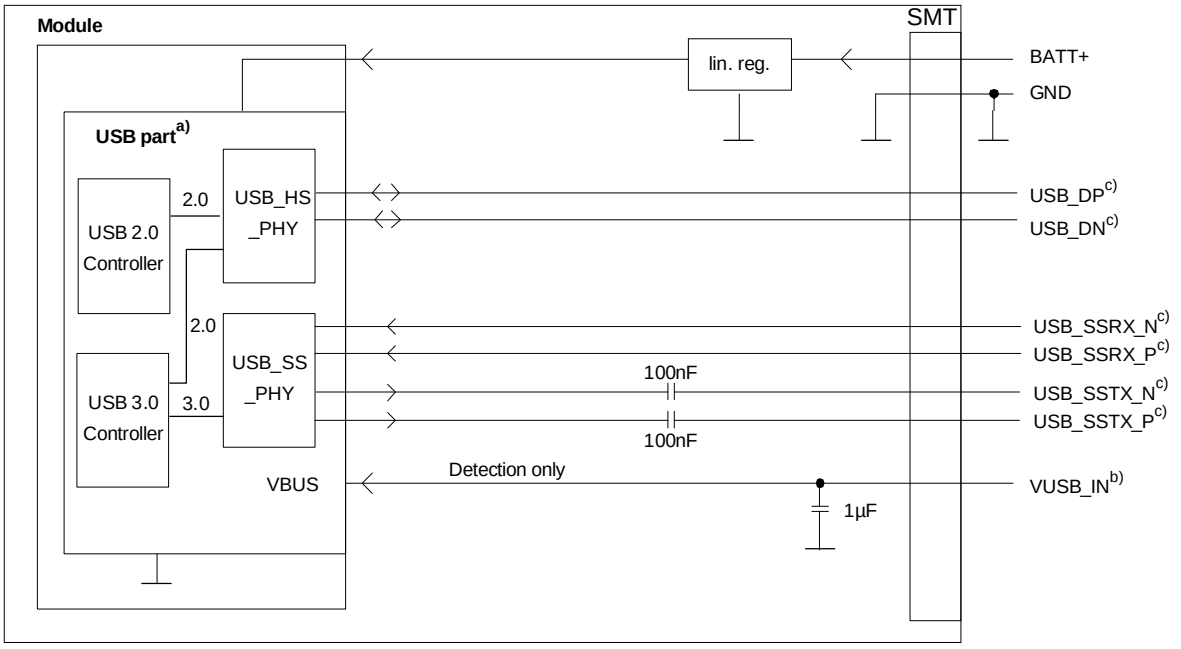
Table 5: Absolute maximum ratings (TBD.)

Parameter	Min	Max	Unit
Supply voltage BATT+	-0.3	+5.5	V
Voltage at all digital lines in Power Down mode (except VEXT)	-0.3	+0.5	V
Voltage at VEXT in Power Down mode	-0.3	+0.3	V
Voltage at digital lines in normal operation	-0.3	+2.3	V
Voltage at UICC interface, CCVCC 1.8V in normal operation	-0.3	+2.3	V
Voltage at UICC interface, CCVCC 3.0V in normal operation	-0.3	+3.4	V
Voltage at ADC lines if the module is powered by BATT+	-0.5	V_{BATT+}+0.5V	V
Voltage at ADC lines if the module is not powered	-0.5	+0.5	V
VEXT maximum current shorted to GND		-600	mA
VUSB_IN	-0.3	5.75	V
USB 3.0 data lines	-0.3	+1.4	V
USB 2.0 data lines	-0.3	+3.6	V
PCIe data and clock lines	-0.3	+1.4	V
PCIe control lines	-0.3	2.1	V
Voltage at PWR_IND line	-0.5	5.5	V
PWR_IND input current if PWR_IND= low		2	mA
Voltage at following signals: IGT, EMERG_OFF	-0.3	2.1	V

2.1.3 USB Interface

ALAS5V supports a USB 3.0 Super Speed (5Gbps) device interface, and alternatively a USB 2.0 device interface that is High Speed compatible. The USB interface is primarily intended for use as command and data interface, and for downloading firmware.

The USB host is responsible for supplying the VUSB_IN line. This line is for voltage detection only. The USB part (driver and transceiver) is supplied by means of BATT+. This is because ALAS5V is designed as a self-powered device compliant with the “Universal Serial Bus Specification Revision 3.0”[1].



a) All serial (including R_S) and pull-up resistors for data lines are implemented .

b) Since VUSB_IN is used for detection only it is recommended not to add any further blocking capacitors on the VUSB_IN line.

c) If the USB interface is operated with super or high speeds, it is recommended to take special care routing the data lines. Application layout should implement a differential impedance of 90 ohms for proper signal integrity .

Figure 5: USB circuit

To properly connect the module's USB interface to the external application, a USB 3.0 or 2.0 compatible connector and cable or hardware design is required. For further guidelines on implementing the external application’s USB 3.0 or 2.0 interface see [4] and [5]. For more information on the USB related signals see Table 4. Furthermore, the USB modem driver distributed with ALAS5V needs to be installed.

While a USB connection is active, the module will never switch into SLEEP mode. Only if the USB interface is in Suspended state or Detached (i.e., VUSB_IN = 0) is the module able to switch into SLEEP mode thereby saving power[2].

1. The specification is ready for download on http://www.usb.org/developers/docs/
2. Please note that if the USB interface is employed, and a USB cable is connected, there should also be a terminal program linked to the USB port in order to receive and process the initial SYSSTART URC after module startup. Otherwise, the SYSSTART URC remains pending in the USB driver's output buffer and this unprocessed data prevents the module from power saving.

2.1.4 Serial Interface ASC0

ALAS5V offers an 8-wire (plus GND) unbalanced, asynchronous modem interface ASC0 conforming to ITU-T V.24 protocol DCE signaling. The electrical characteristics do not comply with ITU-T V.28. The significant levels are 0V (for low data bit or active state) and 1.8V (for high data bit or inactive state). For electrical characteristics please refer to Table 4.

ALAS5V is designed for use as a DCE. Based on the conventions for DCE-DTE connections it communicates with the customer application (DTE) using the following signals:
- Port TXD @ application sends data to the module's TXD0 signal line
- Port RXD @ application receives data from the module's RXD0 signal line

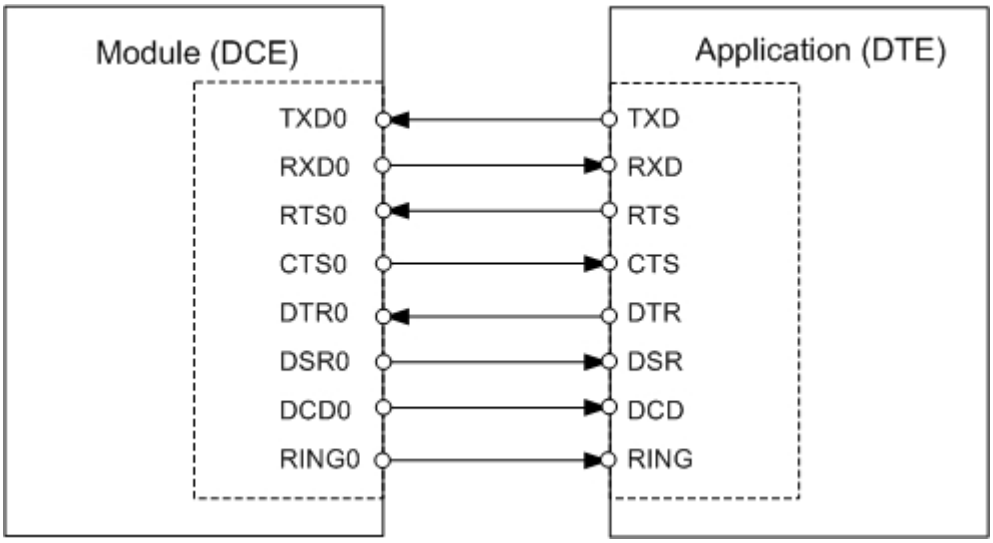


Figure 6: Serial interface ASC0

Features:
- Includes the data lines TXD0 and RXD0, the status lines RTS0 and CTS0, and the modem control lines DTR0, DSR0, DCD0 and RING0.
- Configured for 8 data bits, no parity and 1 stop bit.
- ASC0 can be operated at fixed bit rates from 115,200 to 921,600bps.
- Supports RTS0/CTS0 hardware flow control.

Note: If the ASC0 serial interface is the application's only interface, it is suggested to connect test points on the USB signal lines as a potential tracing possibility.

Table 6: DCE-DTE wiring of ASC0

V.24 circuit	DCE		DTE	
	Line function	Signal direction	Line function	Signal direction
103	TXD0	Input	TXD	Output
104	RXD0	Output	RXD	Input
105	RTS0	Input	RTS	Output
106	CTS0	Output	CTS	Input
108/2	DTR0	Input	DTR	Output
107	DSR0	Output	DSR	Input
109	DCD0	Output	DCD	Input
125	RING0	Output	RING	Input

2.1.5 Serial Interface ASC1

ALAS5V provides a 4-wire unbalanced, asynchronous modem interface ASC1 conforming to ITU-T V.24 protocol DCE signaling. The electrical characteristics do not comply with ITU-T V.28. The significant levels are 0V (for low data bit or active state) and 1.8V (for high data bit or inactive state). For electrical characteristics please refer to Table 3.

ALAS5V is designed for use as a DCE. Based on the conventions for DCE-DTE connections it communicates with the customer application (DTE) using the following signals:
- Port TXD @ application sends data to module's TXD1 signal line
- Port RXD @ application receives data from the module's RXD1 signal line

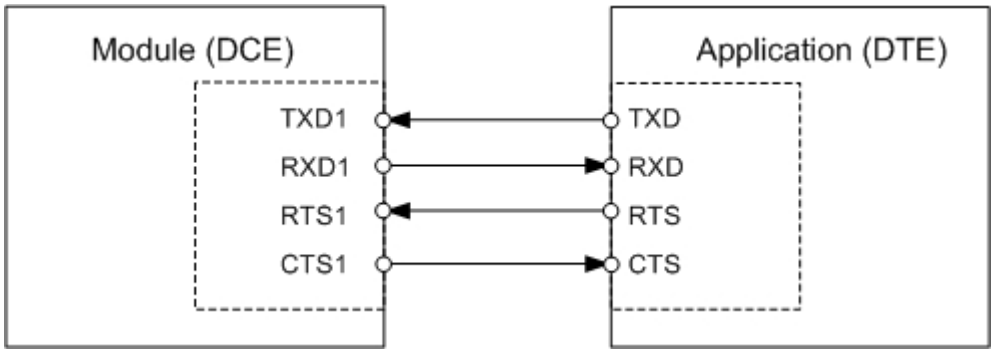


Figure 7: Serial interface ASC1

Features
- Includes only the data lines TXD1 and RXD1 plus RTS1 and CTS1 for hardware handshake.
- On ASC1 no RING line is available.
- Configured for 8 data bits, no parity and 1 or 2 stop bits.
- ASC1 can be operated at fixed bit rates from 115,200 bps to 921,600 bps.
- Supports RTS1/CTS1 hardware flow.
- Linux controlled only.

2.1.6 Inter-Integrated Circuit Interface

ALAS5V provides an Inter-Integrated Circuit (I^2C) interface. I^2C is a serial, 8-bit oriented data transfer bus for bit rates up to 400kbps in Fast mode. It consists of two lines, the serial data line I2CDAT and the serial clock line I2CCLK. The module acts as a single master device, e.g. the clock I2CCLK is driven by the module. I2CDAT is a bi-directional line. Each device connected to the bus is software addressable by a unique 7-bit address, and simple master/slave relationships exist at all times. The module operates as master-transmitter or as master-receiver. The customer application transmits or receives data only on request of the module.

The applications' I^2C interface can be powered via the VEXT line of ALAS5V. If connected to the VEXT line, the I^2C interface will properly shut down when the module enters the Power Down mode.

In the application I2CDAT and I2CCLK lines need to be connected to a positive supply voltage (e.g., VEXT) via a pull-up resistor. For electrical characteristics please refer to Table 4.

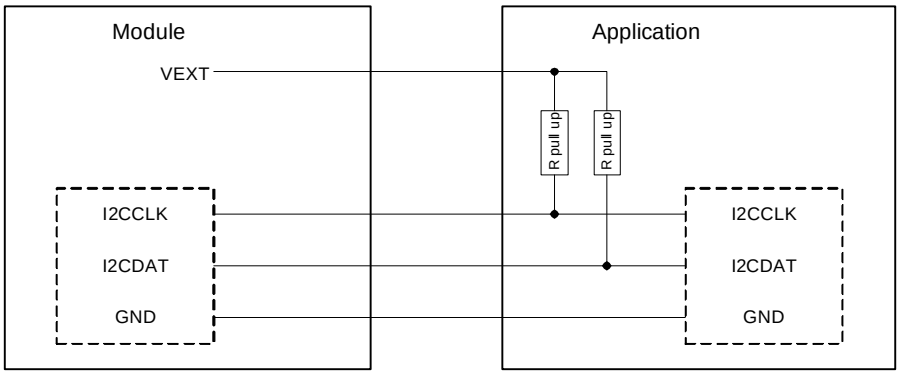


Figure 8: I^2C interface connected to VEXT

Note: Good care should be taken when creating the PCB layout of the host application: The traces of I2CCLK and I2CDAT should be equal in length and as short as possible.

2.1.7 UICC/SIM/USIM Interface

ALAS5V has two UICC/SIM/USIM interfaces compatible with the 3GPP 31.102 and ETSI 102 221. These are wired to the host interface in order to be connected to an external SIM card holder. Five pads on the SMT application interface are reserved for each of the two SIM interfaces.

The UICC/SIM/USIM interface supports 2.85V and 1.8V SIM cards. Please refer to Table 4 for electrical specifications of the UICC/SIM/USIM interface lines depending on whether a 2.85V or 1.8V SIM card is used.

The CCINx signal serves to detect whether a tray (with SIM card) is present in the card holder. Using the CCINx signal is mandatory for compliance with the GSM 11.11 recommendation if the mechanical design of the host application allows the user to remove the SIM card during operation. To take advantage of this feature, an appropriate SIM card detect switch is required on the card holder. For example, this is true for the model supplied by Molex, which has been tested to operate with ALAS5V and is part of the Gemalto M2M reference equipment submitted for type approval. See Chapter 8 for Molex ordering numbers.

Table 7: Signals of the SIM interface (SMT application interface)

Signal	Description
GND	Ground connection for SIM interfaces. Optionally a separate SIM ground line may be used to improve EMC.
CCCLK1 CCCLK2	Chipcard clock line for 1st and 2nd SIM interface.
CCVCC1 CCVCC2	SIM supply voltage line for 1st and 2nd SIM interface.
CCIO1 CCIO2	Serial data line for 1st and 2nd SIM interface, input and output.
CCRST1 CCRST2	Chipcard reset line for 1st and 2nd SIM interface.
CCIN1 CCIN2	Input on the baseband processor for detecting a SIM card tray in the holder. If the SIM is removed during operation the SIM interface is shut down immediately to prevent destruction of the SIM. The CCINx signal is active low. The CCINx signal is mandatory for applications that allow the user to remove the SIM card during operation. The CCINx signal is solely intended for use with a SIM card. It must not be used for any other purposes. Failure to comply with this requirement may invalidate the type approval of ALAS5V.

Note: No guarantee can be given, nor any liability accepted, if loss of data is encountered after removing the SIM card during operation. Also, no guarantee can be given for properly initializing any SIM card that the user inserts after having removed the SIM card during operation. In this case, the application must restart ALAS5V.

By default, only the 1st SIM interface is available and can be used. Using the AT command AT^SCFG="SIM/CS" it is possible to switch between the two SIM interfaces. Command settings are non-volatile - for details see [1].

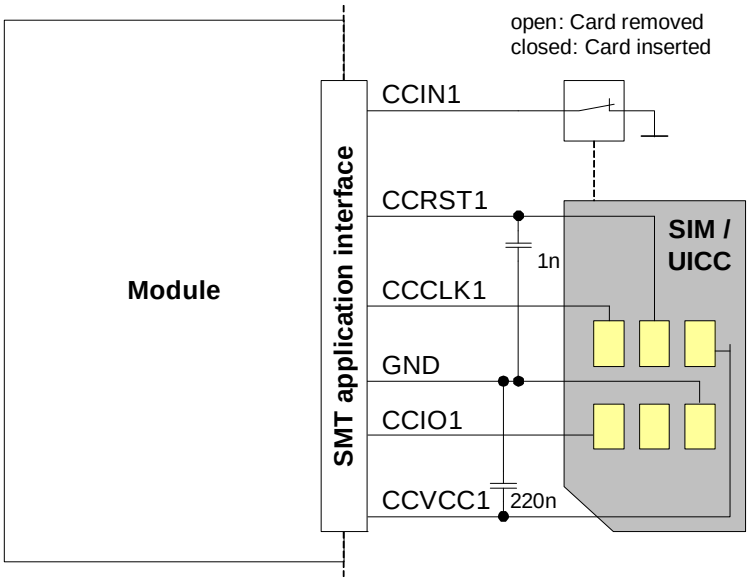


Figure 9: First UICC/SIM/USIM interface

The total cable length between the SMT application interface pads on ALAS5V and the pads of the external SIM card holder must not exceed 100mm in order to meet the specifications of 3GPP TS 51.010-1 and to satisfy the requirements of EMC compliance.

To avoid possible cross-talk from the CCCLKx signal to the CCIOx signal be careful that both lines are not placed closely next to each other. A useful approach is using the GND line to shield the CCIOx line from the CCCLKx line.

An example for an optimized ESD protection for the SIM interface is shown in Section 2.1.8.

Note: Figure 9 shows how to connect a SIM card holder to the first SIM interface. With the second SIM interface some internally integrated components on the SIM circuit will have to be externally integrated as shown for the second SIM interface in Figure 10. The external components at CCIN2 should be populated as close as possible to the signal's SMT pad

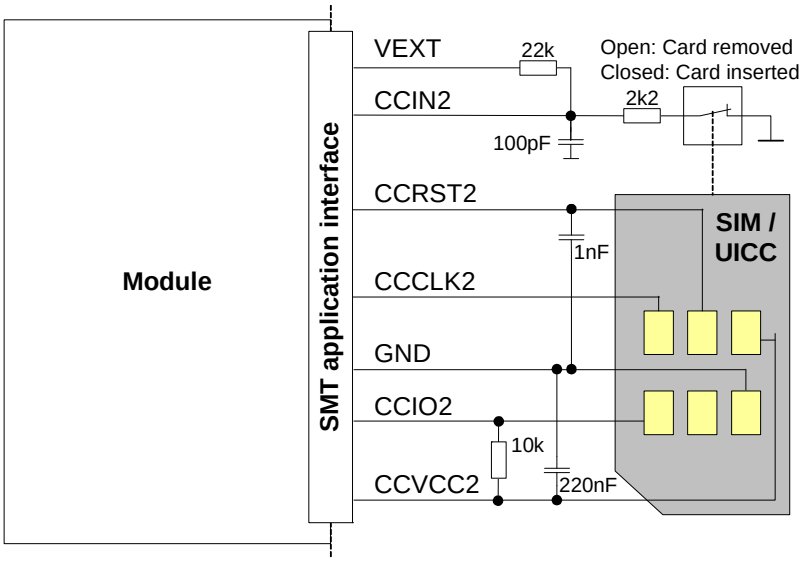


Figure 10: Second UICC/SIM/USIM interface

2.1.8 Enhanced ESD Protection for SIM Interfaces

To optimize ESD protection for the SIM interfaces it is possible to add ESD diodes to the interface lines of the first and second SIM interface as shown in the example given in Figure 11.

The example was designed to meet ESD protection according ETSI EN 301 489-1/7: Contact discharge: ± 4kV, air discharge: ± 8kV.

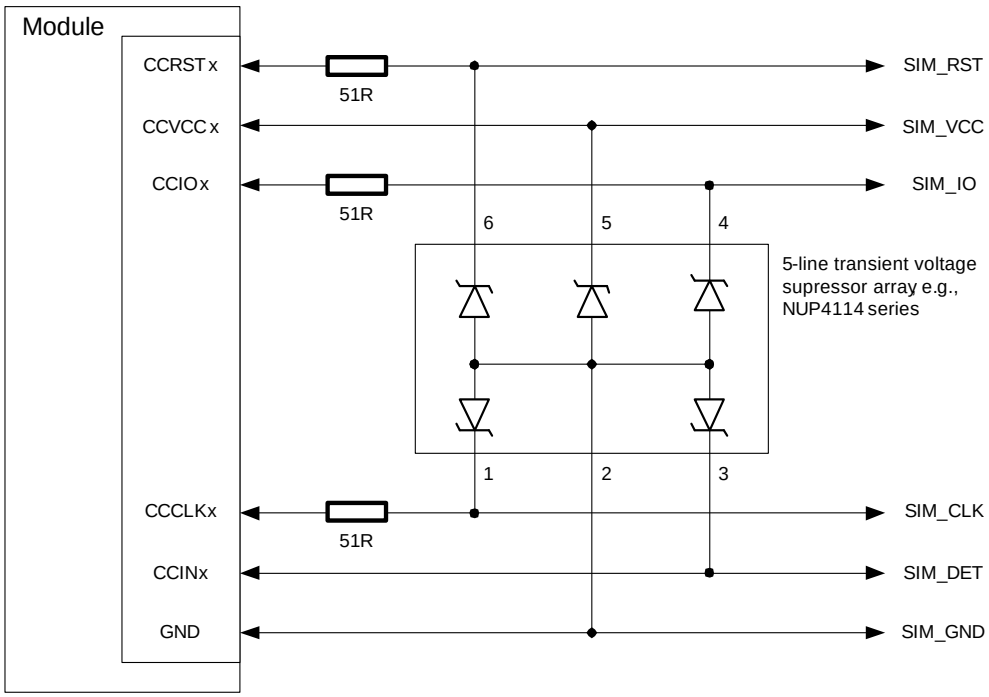


Figure 11: SIM interfaces - enhanced ESD protection

2.1.9 Digital Audio Interface

ALAS5V has two digital audio interfaces (DAIs) that can be employed as inter pulse code modulation (PCM) or Inter-IC Sound (I^2S) interface. Default setting is pulse code modulation. Please note that the first DAI is reserved for future use.

2.1.9.1 Pulse Code Modulation Interface (PCM)

ALAS5V's PCM interface can be used to connect audio devices capable of pulse code modulation. The PCM functionality is limited to the use of wideband codecs with 16kHz sample rate only. The PCM interface runs at 16 kHz sample rate (62.5µs frame length), while the signal processing maintains this rate in a wideband AMR call or samples automatically down to 8kHz in a narrowband call. Therefore, the PCM sample rate is independent of the audio bandwidth of the call.

The PCM interface has the following implementation:
- Master mode
- Short frame synchronization
- 16kHz/8kHz sample rate
- 4096/1024/512/256 kHz bit clock at 16kHz sample rate
- 2048/512/256/128 kHz bit clock at 8kHz sample rate

Table 8 lists the available PCM interface signals.

Table 8: Overview of PCM pin functions

Signal name	Signal direction: Master	Description
DOUT2	O	PCM Data from ALAS5V to external codec
DIN2	I	PCM Data from external codec to ALAS5V
FSC2	O	Frame synchronization signal to external codec
BCLK2	O	Bit clock to external codec. Note: If the BCLK2 signal is permanently provided (AT^SAIC parameter <clk_mode> = 0), the module will no longer enter its power save (SLEEP) state.

Note: PCM data is always formatted as 16-bit uncompressed two’s complement. Also, all PCM data and frame synchronization signals are written to the PCM bus on the rising clock edge and read on the falling edge.

The timing of a PCM short frame is shown in Figure 12.

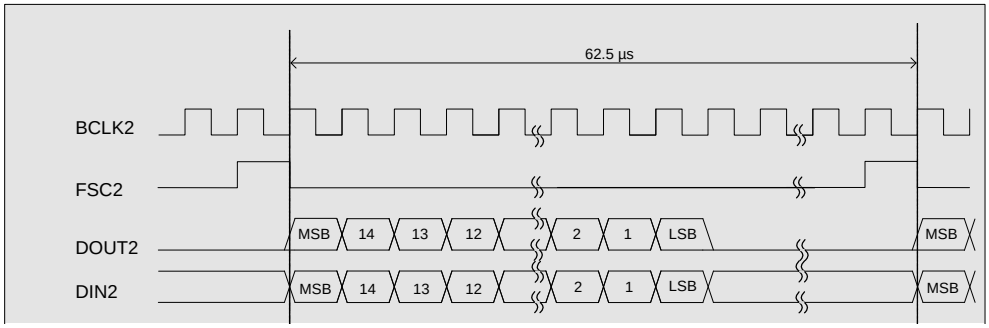


Figure 12: PCM timing short frame (master, 4096KHz, 16kHz sample rate)

2.1.9.2 Inter-IC Sound Interface

The Inter-IC Sound Interface is a standardized bidirectional I²S based digital audio interface for transmission of mono voice signals for telephony services.

An activation of the I²S line is possible only out of call and out of tone presentation. The I²S properties and capabilities comply with the requirements layed out in the Phillips I2S Bus Specifications, revised June 5, 1996.

The I²S interface has the following characteristics:
- Bit clock mode: Master, optional master clock output
- Sampling rate: 8KHz (narrowband), 16KHz (wideband)
- 256kHz bit clock at 8kHz sample rate
- 512kHz bit clock at 16kHz sample rate
- Frame length: 32 bit stereo voice signal (16 bit word length)
- Optional Master clock: 2048KHz (8KHz sample rate) or 4096KHz (16KHz sample rate)

Table 9 lists the available I²S interface signals, Figure 13 shows the I²S timing.

Table 9: Overview of I²S pin functions

Signal name on SMT application interface	Signal configuration inactive	Signal direction: Master	Description
DOUT2	PD	O	I²S data from ALAS5V to external codec
DIN2	PD	I	I²S data from external codec to ALAS5V
FSC2	PD	O	Frame synchronization signal to/from external codec Word alignment (WS)
BCLK2	PD	O	Bit clock to external codec. Note: If the BCLK2 signal is permanently provided (AT^SAIC parameter <clk_mode> = 0), the module will no longer enter its power save (SLEEP) state.
MCLK	PD	O	I²S Master to supply external codecs without PLL.

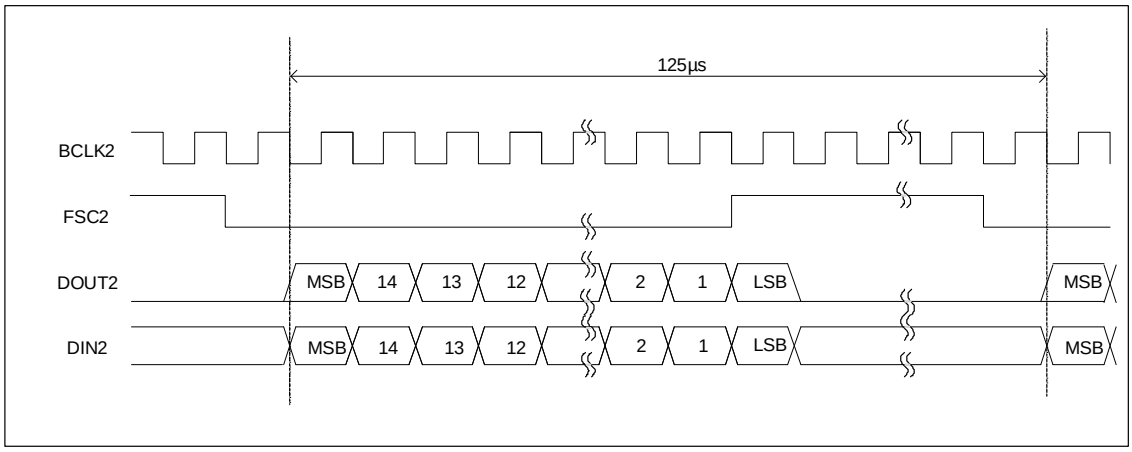


Figure 13: I²S timing (master mode)

2.1.10 Analog-to-Digital Converter (ADC)

ALAS5V provides four unbalanced ADC input lines: ADC[1-2...4-5]_IN. They can be used to measure four independent, externally connected DC voltages in the range of 0.1V to 1.7V. As described in Section 2.2.4 and Section 5.2 they can be used especially for antenna diagnosing.

The AT^SRADC command can be employed to select the ADC line, set the measurement mode and read out the measurement results.

2.1.11 RTC Backup

The internal Real Time Clock of ALAS5V is supplied from a separate voltage regulator in the power supply component which is also active when ALAS5V is in Power Down mode and BATT+ is available.

An alarm function is provided that allows to wake up ALAS5V. When the alarm time is reached the module wakes up into normal operating mode (default), or to the functionality level that was valid before power down. For example, if the module was in Airplane mode before power down, the module will wake up without logging on to the GSM/UMTS/LTE network.

2.1.12 GPIO Interface

ALAS5V has 15 GPIOs for external hardware devices. Each GPIO can be configured for use as input or output. All settings are AT command controlled.

The IO port driver has to be opened before using and configuring GPIOs. Before changing the configuration of a GPIO pin (e.g. input to output) the pin has to be closed. If the GPIO pins are not configured or the pins/driver were closed, the GPIO pins are high-Z with pull down resistor. If a GPIO is configured to input, the pin has high-Z without pull resistor.

If ALAS5V is in power save (SLEEP) mode a level state transition at GPIO3, GPIO5, GPIO6, GPIO7, GPIO8, or GPIO16 will wake up the module, if such a GPIO was configured as input using AT^SCPIN. To query the level state the AT^SCPOL command may be used. For details on the mentioned AT commands please see [1].

Table 10 shows GPIO lines with possible alternative functionalities, and comments on these optional assignments.

Table 10: GPIO lines and possible alternative assignment

GPIOs / Alternative signal names	Description of possible alternative signals
GPIO1 / DR_SYNC	DR_SYNC. GPIO1 can also be configured as DR_SYNC line, i.e., a one pulse per second (1PPS) output for external dead reckoning applications. For more information see Chapter 3.

2.1.13 Control Signals

2.1.13.1 PWR_IND Signal

PWR_IND notifies the on/off state of the module. High state of PWR_IND indicates that the module is switched off. The state of PWR_IND immediately changes to low when IGT is pulled low. For state detection an external pull-up resistor is required.

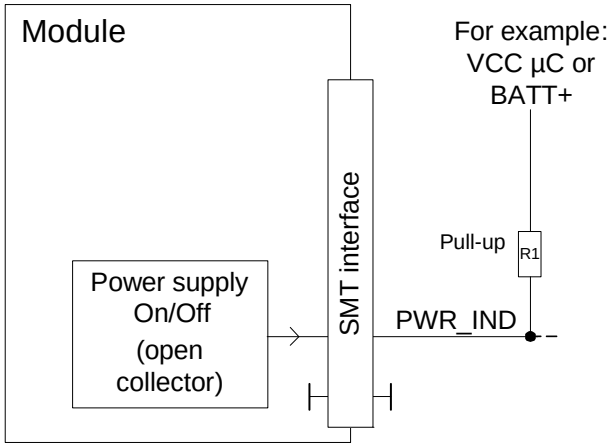


Figure 14: PWR_IND signal

2.1.13.2 Remote Wakeup

If no call, data or message transfer is in progress, the external host application may shut down its own module interfaces or other components in order to save power. If a call, data, or other request (URC) arrives, the external application can be notified of this event and be woken up again by a state transition of a configurable remote wakeup line. Available as remote wakeup lines are some GPIO signals (recommended is GPIO4). Please refer to [1]: AT^SCFG: "RemoteWakeUp/..." for details on how to configure these lines for defined wakeup events on specified device interfaces. Possible states are listed in Table 11.

If no line is specifically configured as remote wakeup signal, the remote USB suspend and resume mechanism as specified in the “Universal Serial Bus Specification Revision 2.0” applies for the USB interface (see Section 2.1.3). Possible states for the remote wakeup GPIO lines are listed in Table 11.

Table 11: Remote wakeup lines

Signal	I/O/P	Description
GPIOx	O	Inactive to active high transition: 0 = No wake up request 1 = The host shall wake up

2.1.13.3 Firmware Swap

The firmware swap signal FwSwap allows to toggle between two firmware images that may be available on the module. Setting the FwSwap line to high during the module’s startup phase triggers the firmware swap. The signal may for instance be used as a fallback or backup solution in case a possible firmware update is not successful.

Please connect this signal to the external application and implement a test point.

2.1.14 JTAG Interface

For test purposes, e.g., 8D reporting without re-soldering the module from the external application.

2.1.15 eMMC Interface

ALAS5V has an eMMC interface that can be used for development and test purposes, e.g., to write crash dumps from the module's FFS to eMMC. To connect an eMMC a separate, additional power supply is required as described in Section 2.1.15.1.

2.1.15.1 eMMC Power Supply

An eMMC requires two separate power supplies normally named VCC (3V3) and VCCQ (3V3 / 1V8). ALAS5V however, provides only a single power supply pad for eMMC, i.e., the EMMC_PWR pad. Therefore, an additional external power supply for the eMMC is necessary, and can for instance be provided through a voltage regulator enabled with the EMMC_PWR line.

A sample connecting circuit is shown in Figure 15. Note that with ALAS5V the EMMC_PWR line switches from 2.95V to 1.8V during eMMC operation.

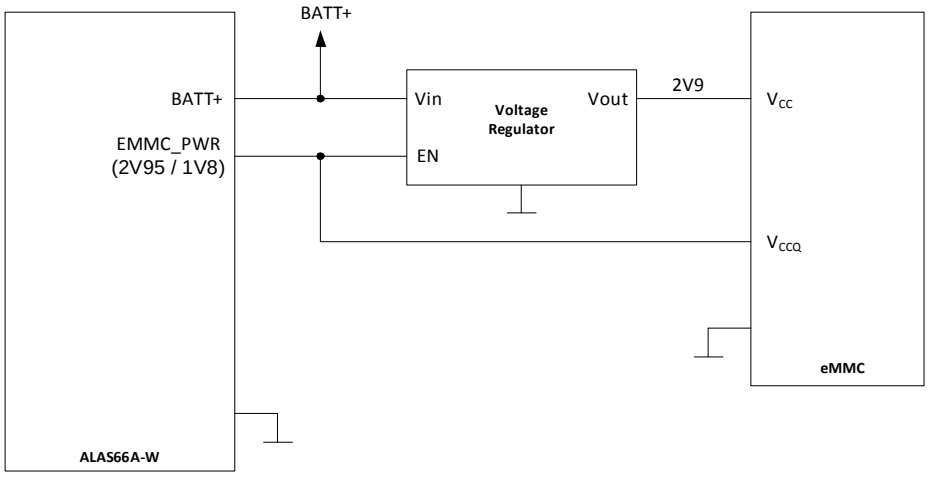


Figure 15: eMMC power supply

2.2 GSM/UMTS/LTE Antenna Interface

The ALAS5V GSM/UMTS/LTE antenna interface comprises a GSM/UMTS/LTEmain antenna as well as a UMTS/LTE Rx diversity/MIMO antenna to improve signal reliability and quality[1]. The interface has an impedance of 50Ω. ALAS5V is capable of sustaining a total mismatch at the antenna interface without any damage, even when transmitting at maximum RF power.

The external antennas must be matched properly to achieve best performance regarding radiated power, modulation accuracy and harmonic suppression. Matching networks are not included on the ALAS5V PCB and should be placed in the host application, if the antenna does not have an impedance of 50Ω.

Regarding the return loss ALAS5V provides the following values in the active band:

Table 12: Return loss in the active band

State of module	Return loss of module	Recommended return loss of application
Receive	≥ 8dB	≥ 12dB
Transmit	Undefined mismatch	≥ 12dB

1. By delivery default the UMTS/LTE Rx diversity/MIMO antenna is configured as available for the module since its usage is mandatory for LTE. Please refer to [1] for details on how to configure antenna settings.

2.2.1 Antenna Interface Specifications

Table 13: RF Antenna interface GSM/UMTS/LTE (at operating temperature range[1])

Parameter	Conditions	Min.	Typical	Max.	Unit
LTE connectivity	Band 1, 2, 3, 4, 5, 7, 8, 12, 18, 19, 20, 26, 28, 38, 39, 40, 41, 66				
Receiver Input Sensitivity @ ARP (ch. bandwidth 5MHz; 4 antenna combined, TRX1, TRX2, RX3, RX4))	LTE 2100 Band 1	-102	-107		dBm
	LTE 1900 Band 2	-100	-106		dBm
	LTE 1800 Band 3	-99	-107		dBm
	LTE 1700 Band 4	-102	-107		dBm
	LTE 850 Band 5	-97.3	-108		dBm
	LTE 2600 Band 7	-100	-106		dBm
	LTE 900 Band 8	-96.3	-107		dBm
	LTE 700 Band 12	-96.3	-106		dBm
	LTE 850 Band 18	-96.8	-108		dBm
	LTE 850 Band 19	-96.8	-108		dBm
	LTE 800 Band 20	-99	-108		dBm
	LTE 850 Band 26	-96.8	-108		dBm
	LTE 700 Band 28	-97.8	-108		dBm
	LTE 2600 Band 38	-99.3	-106		dBm
	LTE 1900 Band 39	-102	-108		dBm
	LTE 2300 Band 40	-102	-105		dBm
	LTE 2300 Band 41	-100	-107		dBm
	LTE 2600 Band 66	-101.5	-107		dBm
RF Power @ ARP with 50Ω Load	LTE 2100 Band 1	+21	+23	+25	dBm
	LTE 1900 Band 2	+21	+23	+25	dBm
	LTE 1800 Band 3	+21	+23	+25	dBm
	LTE 1700 Band 4	+21	+23	+25	dBm
	LTE 850 Band 5	+21	+23	+25	dBm
	LTE 2600 Band 7	+21	+23	+25	dBm
	LTE 900 Band 8	+21	+23	+25	dBm
	LTE 700 Band 12	+21	+23	+25	dBm
	LTE 850 Band 18	+21	+23	+25	dBm
	LTE 850 Band 19	+21	+23	+25	dBm
	LTE 800 Band 20	+21	+23	+25	dBm
	LTE 850 Band 26	+21	+23	+25	dBm
	LTE 700 Band 28	+21	+23	+25	dBm
	LTE 2600 Band 38	+21	+23	+25	dBm

Table 13: RF Antenna interface GSM/UMTS/LTE (at operating temperature range[1])

Parameter	Conditions	Min.	Typical	Max.	Unit
RF Power @ ARP with 50Ω Load	LTE 1900 Band 39	+21	+23	+25	dBm
	LTE 2300 Band 40	+21	+23	+25	dBm
	LTE 2300 Band 41	+21	+23	+25	dBm
	LTE 2600 Band 66	+21	+23	+25	dBm
UMTS/HSPA connectivity	Band I, II, III, IV, V, VI, VIII, XIX				
Receiver Input Sensitivity @ ARP Main path (TRX1)	UMTS 2100 Band I	-106	-110		dBm
	UMTS 1900 Band II	-104	-109		dBm
	UMTS 1800 Band III	-103	-111		dBm
	UMTS 1700 Band IV	-106	-111		dBm
	UMTS 900 Band VIII	-103	-112		dBm
	UMTS 850 Band V	-104	-111		dBm
	UMTS 850 Band VI	-104	-111		dBm
	UMTS 850 Band XIX	-104	-111		dBm
Receiver Input Sensitivity @ ARP Diversity path (TRX2)	UMTS 2100 Band I	-106	-112		dBm
	UMTS 1900 Band II	-104	-111		dBm
	UMTS 1800 Band III	-103	-111		dBm
	UMTS 1700 Band IV	-106	-112		dBm
	UMTS 900 Band VIII	-103	-112		dBm
	UMTS 850 Band V	-104	-113		dBm
	UMTS 850 Band VI	-104	-113		dBm
	UMTS 850 Band XIX	-104	-113		dBm
RF Power @ ARP with 50Ω Load	UMTS 2100 Band I	+21	+24	+25	dBm
	UMTS 1900 Band II	+21	+24	+25	dBm
	UMTS 1800 Band III	+21	+24	+25	dBm
	UMTS 1700 Band IV	+21	+24	+25	dBm
	UMTS 900 Band VIII	+21	+24	+25	dBm
	UMTS 850 Band V	+21	+24	+25	dBm
	UMTS 850 Band VI	+21	+24	+25	dBm
	UMTS 850 Band XIX	+21	+24	+25	dBm
GPRS coding schemes	Class 12, CS1 to CS4				
EGPRS	Class 12, MCS1 to MCS9				
GSM Class	Small MS				
Static Receiver input Sensitivity @ ARP	GSM 850 /E-GSM 900	-102	-110		dBm
	GSM 1800 / GSM 1900	-102	-109		dBm
RF Power @ ARP with 50Ω Load GSM	GSM 850 /E-GSM 900	31	33	35	dBm
	GSM 1800 / GSM 1900	28	30	32	dBm

Table 13: RF Antenna interface GSM/UMTS/LTE (at operating temperature range[1])

Parameter		Conditions	Min.	Typical	Max.	Unit
RF Power @ ARP with 50Ω Load (**ROPR=4**, i.e., no reduction)	GPRS, 1 TX	GSM 850 /E-GSM 900		33		dBm
		GSM 1800 / GSM 1900		30		dBm
	EDGE, 1 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 2 TX	GSM 850 /E-GSM 900		33		dBm
		GSM 1800 / GSM 1900		30		dBm
	EDGE, 2 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 3 TX	GSM 850 /E-GSM 900		33		dBm
		GSM 1800 / GSM 1900		30		dBm
	EDGE, 3 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 4 TX	GSM 850 /E-GSM 900		33		dBm
		GSM 1800 / GSM 1900		30		dBm
	EDGE, 4 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
RF Power @ ARP with 50Ω Load (**ROPR=5**)	GPRS, 1 TX	GSM 850 /E-GSM 900		33		dBm
		GSM 1800 / GSM 1900		30		dBm
	EDGE, 1 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 2 TX	GSM 850 /E-GSM 900		33		dBm
		GSM 1800 / GSM 1900		30		dBm
	EDGE, 2 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 3 TX	GSM 850 /E-GSM 900		32.2		dBm
		GSM 1800 / GSM 1900		29.2		dBm
	EDGE, 3 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 4 TX	GSM 850 /E-GSM 900		31		dBm
		GSM 1800 / GSM 1900		28		dBm
	EDGE, 4 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm

Table 13: RF Antenna interface GSM/UMTS/LTE (at operating temperature range[1])

Parameter		Conditions	Min.	Typical	Max.	Unit
RF Power @ ARP with 50Ω Load (**ROPR=6**)	GPRS, 1 TX	GSM 850 /E-GSM 900		33		dBm
		GSM 1800 / GSM 1900		30		dBm
	EDGE, 1 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 2 TX	GSM 850 /E-GSM 900		31		dBm
		GSM 1800 / GSM 1900		28		dBm
	EDGE, 2 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 3 TX	GSM 850 /E-GSM 900		30.2		dBm
		GSM 1800 / GSM 1900		27.2		dBm
	EDGE, 3 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 4 TX	GSM 850 /E-GSM 900		29		dBm
		GSM 1800 / GSM 1900		26		dBm
	EDGE, 4 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
RF Power @ ARP with 50Ω Load (**ROPR=7**)	GPRS, 1 TX	GSM 850 /E-GSM 900		33		dBm
		GSM 1800 / GSM 1900		30		dBm
	EDGE, 1 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 2 TX	GSM 850 /E-GSM 900		30		dBm
		GSM 1800 / GSM 1900		27		dBm
	EDGE, 2 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 3 TX	GSM 850 /E-GSM 900		28.2		dBm
		GSM 1800 / GSM 1900		25.2		dBm
	EDGE, 3 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 4 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		24		dBm
	EDGE, 4 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm

Table 13: RF Antenna interface GSM/UMTS/LTE (at operating temperature range[1])

Parameter		Conditions	Min.	Typical	Max.	Unit
RF Power @ ARP with 50Ω Load (**ROPR=8**, i.e., max. reduction)	GPRS, 1 TX	GSM 850 /E-GSM 900		33		dBm
		GSM 1800 / GSM 1900		30		dBm
	EDGE, 1 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		26		dBm
	GPRS, 2 TX	GSM 850 /E-GSM 900		30		dBm
		GSM 1800 / GSM 1900		27		dBm
	EDGE, 2 TX	GSM 850 /E-GSM 900		24		dBm
		GSM 1800 / GSM 1900		23		dBm
	GPRS, 3 TX	GSM 850 /E-GSM 900		28.2		dBm
		GSM 1800 / GSM 1900		25.2		dBm
	EDGE, 3 TX	GSM 850 /E-GSM 900		22.2		dBm
		GSM 1800 / GSM 1900		21.2		dBm
	GPRS, 4 TX	GSM 850 /E-GSM 900		27		dBm
		GSM 1800 / GSM 1900		24		dBm
	EDGE, 4 TX	GSM 850 /E-GSM 900		21		dBm
		GSM 1800 / GSM 1900		20		dBm

1. At restricted temperature range no active power reduction is implemented - any deviations are hardware related.

2.2.2 Antenna Installation

The antennas are connected by soldering the antenna pads (ANT_MAIN, ANT_DRX_MIMO, ANT_GNSS) and their neighboring ground pads directly to the application's PCB.

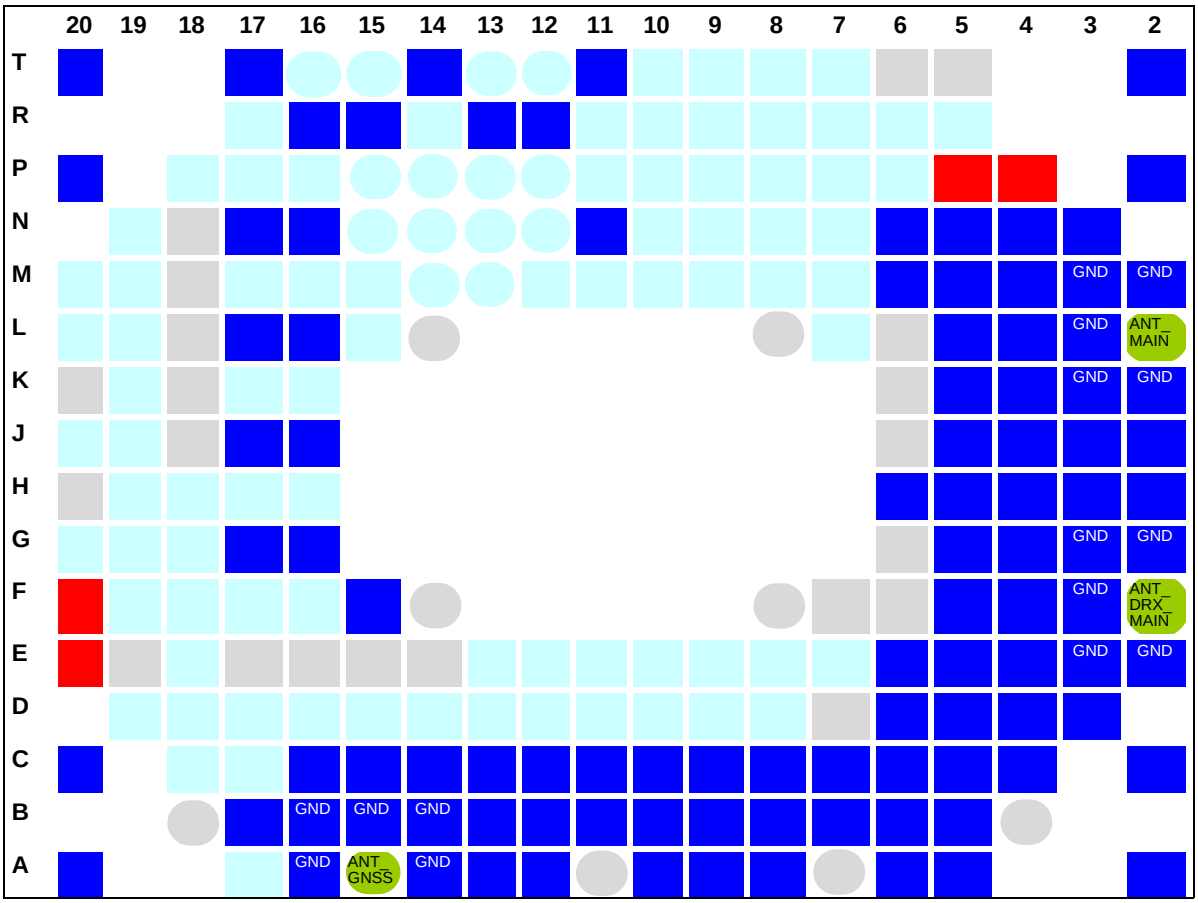


Figure 16: Antenna pads (top view)

The distance between the antenna pads and their neighboring GND pads has been optimized for best possible impedance. To prevent mismatch, special attention should be paid to these pads on the application' PCB.The wiring of the antenna connection, starting from the antenna pad to the application's antenna must result in a 50Ω line impedance. Line width and distance to the GND plane need to be optimized with regard to the PCB's layer stack.

To prevent receiver desensitization due to interferences generated by fast transients like high speed clocks on the external application PCB, it is recommended to realize the antenna connection line using embedded Stripline rather than Micro-Stripline technology.

For type approval purposes (i.e., FCC KDB 996369 related to modular approval requirements), an external application must connect the RF signal in one of the following ways:

- Via 50Ω coaxial antenna connector (common connectors are U-FL or SMA) placed as close as possible to the module's antenna pad.
- By soldering the antenna to the antenna connection line on the application's PCB (without the use of any connector) as close as possible to the module's antenna pad.
- By routing the application PCB's antenna to the module's antenna pad in the shortest possible way.

2.2.3 RF Line Routing Design

2.2.3.1 Line Arrangement Instructions

Several dedicated tools are available to calculate line arrangements for specific applications and PCB materials - for example from http://www.polarinstruments.com/ (commercial software) or from http://web.awrcorp.com/Usa/Products/Optional-Products/TX-Line/ (free software).

Embedded Stripline
This below figure shows line arrangement examples for embedded stripline.

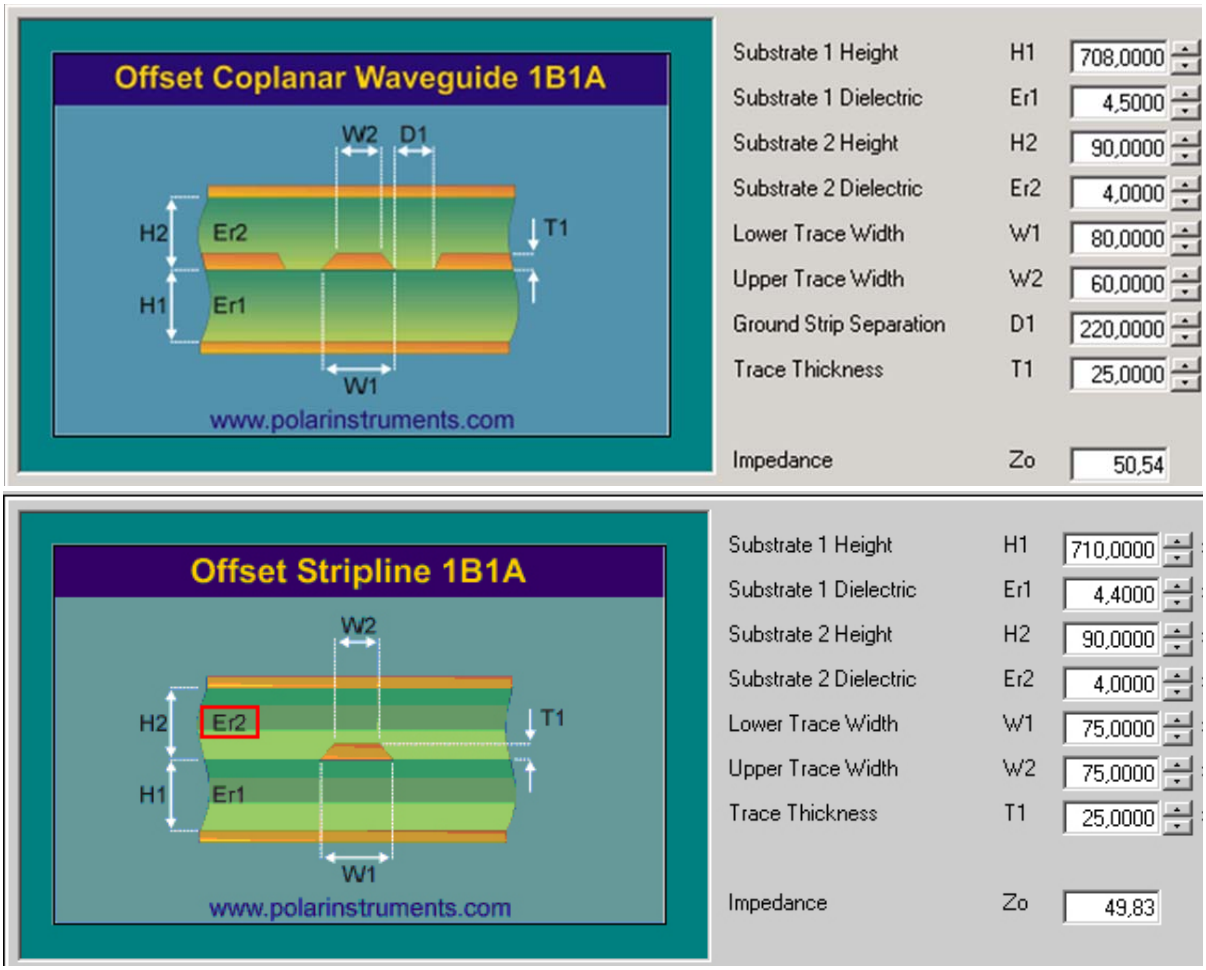


Figure 17: Embedded Stripline line arrangement

Micro-Stripline

This section gives two line arrangement examples for micro-stripline.

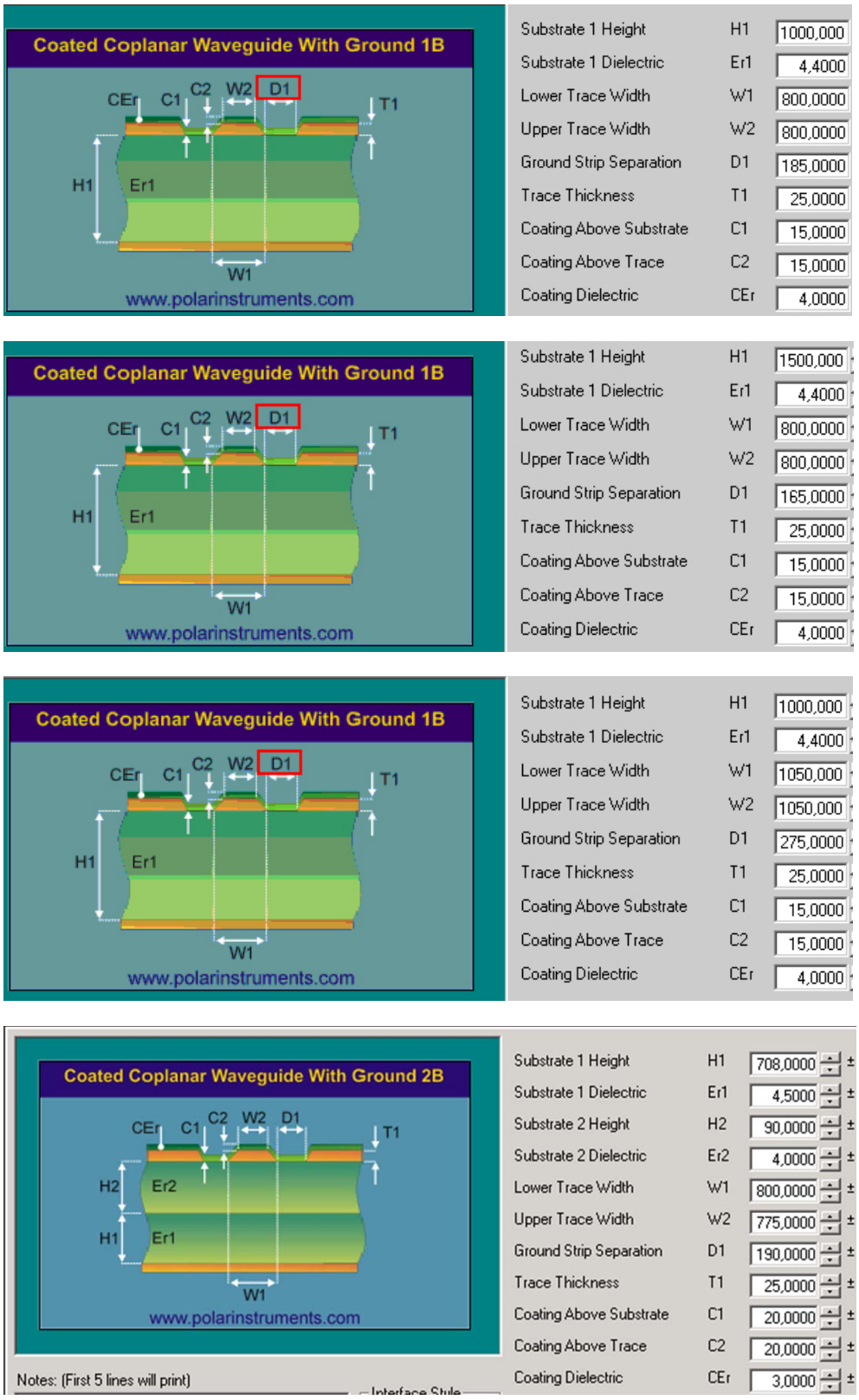


Figure 18: Micro-Stripline line arrangement samples

2.2.3.2 Routing Examples

Interface to RF Connector

Figure 19 shows a sample connection of a module‘s antenna pad at the bottom layer of the module PCB with an application PCB‘s coaxial antenna connector. Line impedance depends on line width, but also on other PCB characteristics like dielectric, height and layer gap. The sample stripline width of 0.40mm is recommended for an application with a PCB layer stack resembling the one of the ALAS5V evaluation board. For different layer stacks the stripline width will have to follow stripline routing rules, avoiding 90 degree corners and using the shortest distance to the PCB’s coaxial antenna connector.

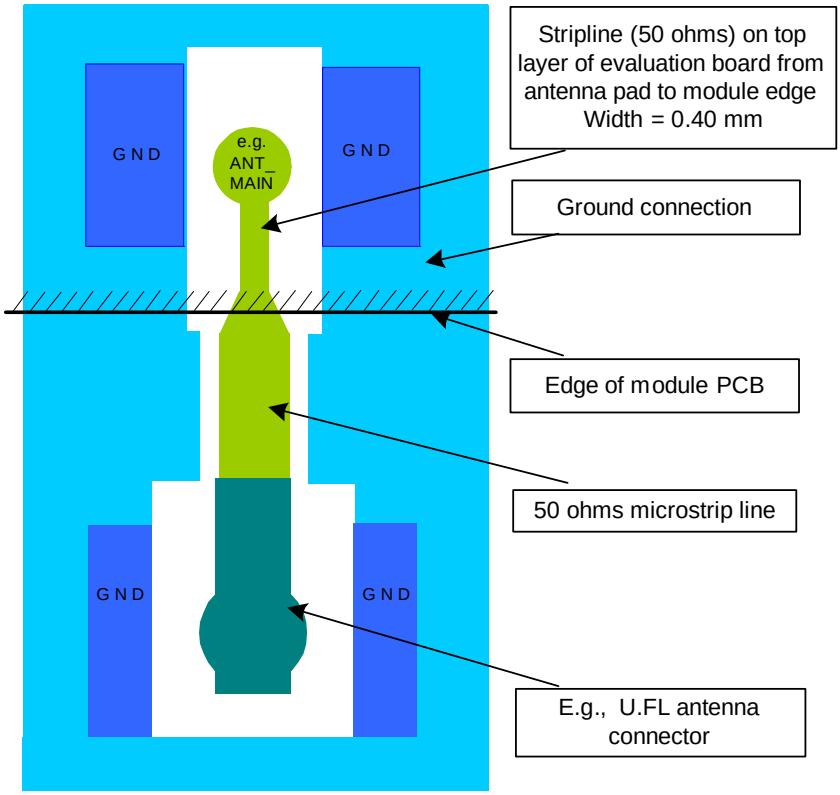


Figure 19: Routing to application‘s RF connector

2.2.4 RF Antenna Diagnostic

RF antenna (GSM/UMTS/LTE) diagnosis requires the implementation of an external antenna detection circuit. An example for such a circuit is illustrated in Figure 21. It allows to check the presence and the connection status of RF antennas.

To properly detect the antenna and verify its connection status the antenna feed point must have a DC resistance R_{ANT} of 9kΩ (±3kΩ).

A positive or negative voltage drop (referred to as $V_{disturb}$) on the ground line may occur without having any impact on the measuring procedure and the measuring result. A peak deviation ($V_{disturb}$) of ≤ 0.8V from ground is acceptable.
$V_{disturb}$ (peak) = ± 0.8V (maximum); $f_{disturb}$ = 0Hz … 5kHz

Waveform: DC, sinus, square-pulse, peak-pulse (width = 100µs)
$R_{disturb}$ = 5Ω

To make sure that the antenna detection operates reliably, the capacitance at the module's antenna pad (i.e., the cable capacitance plus the antenna capacitance (C_{ANT})) should not be greater than 1000pF. Some types of antennas (for example "inverted F antenna" or "half loop antenna") need an RF short circuit between the antenna structure and ground to work properly. In this case the RF short circuit has to be realized via a capacitance (C_{ANT}) . For C_{ANT} we recommend a capacitance lower than 100pF (see Figure 20).

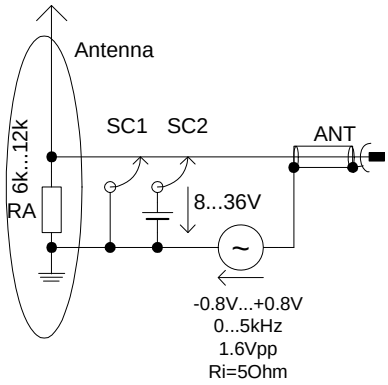


Figure 20: Resistor measurement used for antenna detection

Figure 21 shows the basic principles of an antenna detection circuit that is able to detect antennas and verify their connection status. The GPIO pads can be employed to enable the antenna detection, the ADCx_IN pads can be used to measure the voltage of external devices connected to these ADC input pads - thus determining R_{ANT} values. The AT^SRADC write command configures the parameters required for ADC measurement and returns the measurement result(s) - for command details see [1].

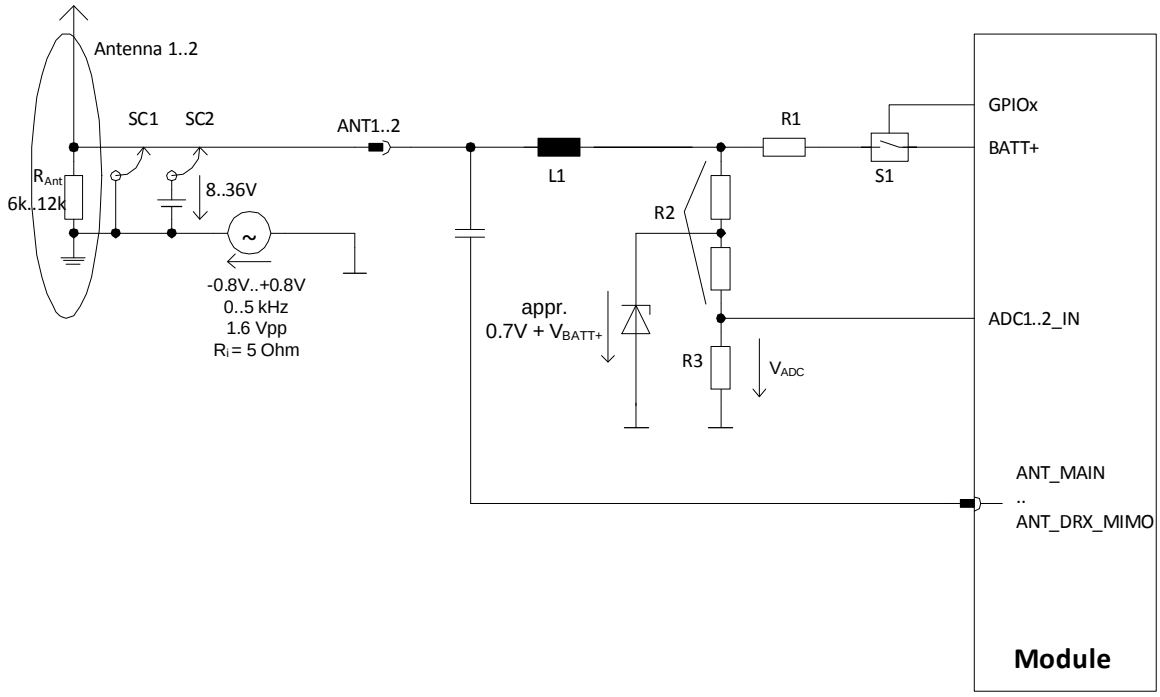


Figure 21: Basic circuit for antenna detection

The following Table 14 lists possible signal states for the GPIOx signal lines in case these lines are configured and used for antenna detection. For GPIO configuration and control commands see [1].

Table 14: Possible GPIOx signal states if used for antenna diagnosis

Signal state	Meaning
GPIOx: Input Pull down or Output low Output high	Antenna detection control (S1 in above figure): Off (diagnostic measurement is off) On (diagnostic measurement is on)

Table 15 lists assured antenna diagnostic states depending on the measured R_{ANT} values. Note that the R_{ANT} ranges not mentioned in the below table, i.e., 1kΩ...6kΩ and 12kΩ...40kΩ are tolerance ranges. Within these tolerance ranges a decision threshold for a diagnostic application may be located. For more details on the sample antenna detection circuit please refer to Section 2.3.1.

Table 15: Assured antenna diagnostic states

Antenna state	R_{ANT} range
Normal operation, antenna connected (resistance at feed point as required)	R_{ANT} = 6kΩ…12kΩ
Antenna pad short-circuited to GND	R_{ANT} = 0…1kΩ
Antenna not properly connected, or resistance at antenna feed point wrong or not present	R_{ANT} = 40kΩ…∞Ω
Antenna pad is short-circuited to the supply voltage of the host application, for example the vehicle's on-board power supply voltage	max. 36V

Measuring procedure for the basic circuit given in Figure 21:
The battery current flows through R1 and RA. The voltage drop on RA is divided by R3/(R3+R2) and measured by the ADCx_IN input. For the ADCx_IN voltage V_{ADCx} (monitored using AT^SRADC) and the BATT+ supply voltage V_{BATT+} (monitored using AT^SBV) several measuring samples should be taken for averaging. The measured and averaged value V_{ADCx} will then be compared to three decision thresholds. The decision thresholds depend on BATT+:

Table 16: GSM/UMTS/LTE antenna diagnostic decision threshold

Decision threshold[1]		V_{ADCx}	Result
Short to GND	Appr. 0,176*V_{BATT+} (580mV…738mV)	<	Short-circuited to ground
		>	Antenna connected
No antenna	Appr. 0,337*V_{BATT+} (1111mV…1414mV)	<	
		>	Antenna nor properly connected
Short to power	0.146+0.405*V_{BATT+} (1482mV…1888mV)	<	
		>	Short-circuited to power

1. The decision thresholds depends on BATT+ and has to be calculated separately for each decision (the BATT+ voltage level V_{BATT+} is known to the system: 3.3V ≤ V_{BATT+} ≤ 4.2V).

2.3 GNSS Antenna Interface

In addition to the RF antenna interface ALAS5V also has a GNSS antenna interface. See Section 2.1.1 to find out where the GNSS antenna pad is located. The GNSS pad's shape is the same as for the RF antenna interface (see Section 2.2.2).

It is possible to connect active or passive GNSS antennas. In either case they must have 50Ω impedance. The simultaneous operation of GSM/UMTS/LTE and GNSS is implemented. For electrical characteristics see Section 2.2.

ALAS5V provides the signal GNSS_EN to enable an active GNSS antenna power supply. Figure 22 shows the flexibility in realizing the power supply for an active GNSS antenna by giving a sample circuit realizing the supply voltage for an active GNSS antenna.

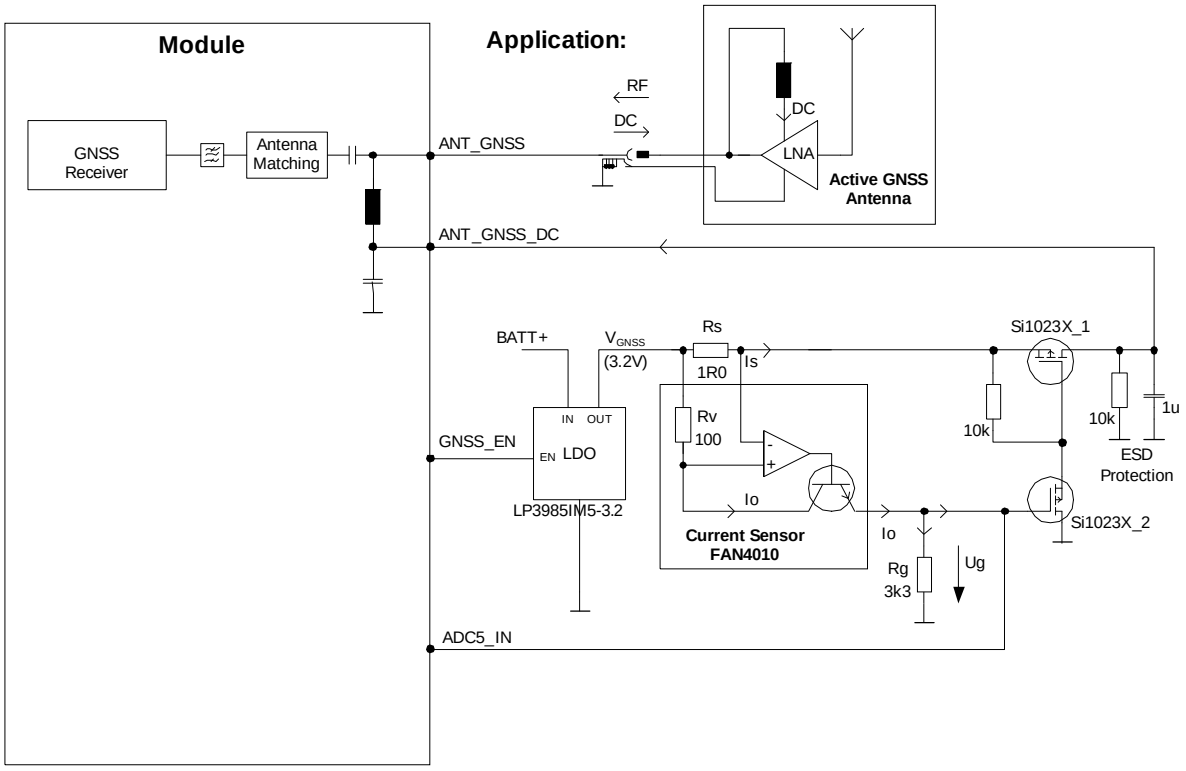


Figure 22: Supply voltage for active GNSS antenna

Figure 23 shows a sample circuit realizing ESD protection for a passive GNSS antenna. Connecting the input ANT_GNSS_DC to GND prevents ESD from coupling into the module.

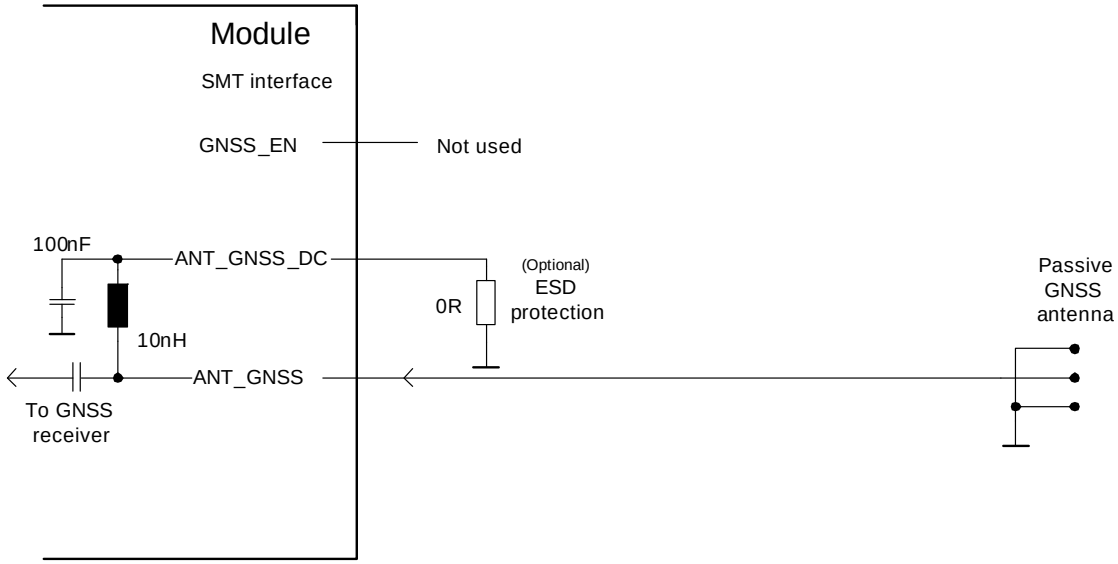


Figure 23: ESD protection for passive GNSS antenna

2.3.1 GNSS Antenna Diagnostic

GNSS antenna diagnosis does require an external detection circuit. The antenna DC supply current can be measured via ADC5_IN. The ADC5_IN input voltage (Ug) may be generated by a sample circuit shown in Figure 22. The circuit allows to check the presence and the connection status of an active GNSS antenna. Passive GNSS antennas cannot be detected. Therefore, GNSS antenna detection is only available in active GNSS antenna mode.

Having enabled the active GNSS antenna mode the presence and connection status of an active GNSS antenna can be checked. The following table lists sample current ranges for possible antenna states as well as sample voltage ranges as possible decision thresholds to distinguish between the antenna connection states.

Table 17: Sample ranges of the GNSS antenna diagnostic measurements and their possible meaning

Antenna connection status	Current ranges (I_S)[1]	Voltage ranges (U_G)
Antenna not connected	<1.4mA	
Decision threshold		59mV ±20%
Antenna connected	2.2mA...20mA	
Decision threshold		825mV ±20%
Antenna short circuited to ground	>30mA	
GNSS antenna detection is not possible because GNSS antenna power supply is switched off.	--	

1. Please note that the mA ranges 1.4mA...2.2mA and 20mA...30mA are tolerance ranges. The decision threshold should be defined within these ranges.

2.4 Sample Application

Figure 24 shows a typical example of how to integrate an ALAS5V module with an application.

The PWR_IND line is an open collector that needs an external pull-up resistor which connects to the voltage supply VCC µC of the microcontroller. Low state of the open collector pulls the PWR_IND signal low and indicates that the ALAS5V module is active, high level notifies the Power Down mode.

If the module is in Power Down mode avoid current flowing from any other source into the module circuit, for example reverse current from high state external control lines. Therefore, the controlling application must be designed to prevent reverse flow.

While developing SMT applications it is strongly recommended to provide test points for certain signals, i.e., lines to and from the module - for debug and/or test purposes. The SMT application should allow for an easy access to these signals. For details on how to implement test points see [3].

The EMC measures are best practice recommendations. In fact, an adequate EMC strategy for an individual application is very much determined by the overall layout and, especially, the position of components.

Some LGA pads are connected to clocks or high speed data streams that might interfere with the module's antenna. The RF receiver would then be blocked at certain frequencies (self interference). The external application's PCB tracks connected to these pads should therefore be well shielded or kept away from the antenna. This applies especially to the USB and UICC/SIM interfaces.

Depending on the micro controller used by an external application ALAS5V's digital input and output lines may require level conversion. Section 2.4.2 shows a possible sample level conversion circuit.

The analog-to-digital converter (ADCx_IN lines) can be used for antenna diagnosis. A sample antenna detection circuit can be found in Figure 26 and Figure 27.

Disclaimer:
No warranty, either stated or implied, is provided on the sample schematic diagram shown in Figure 24 and the information detailed in this section. As functionality and compliance with national regulations depend to a great amount on the used electronic components and the individual application layout manufacturers are required to ensure adequate design and operating safeguards for their products using ALAS5V modules.

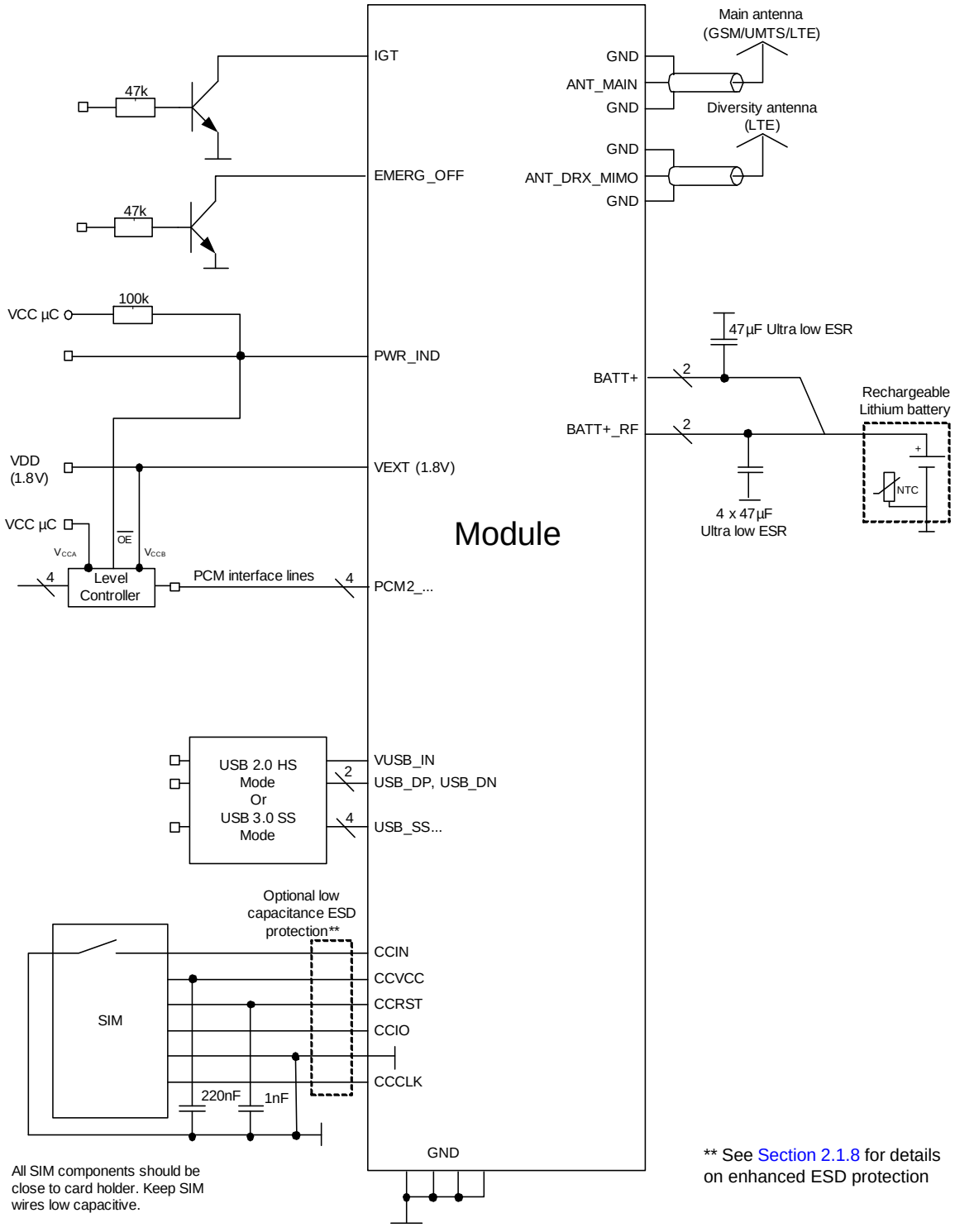


Figure 24: ALAS5V sample application

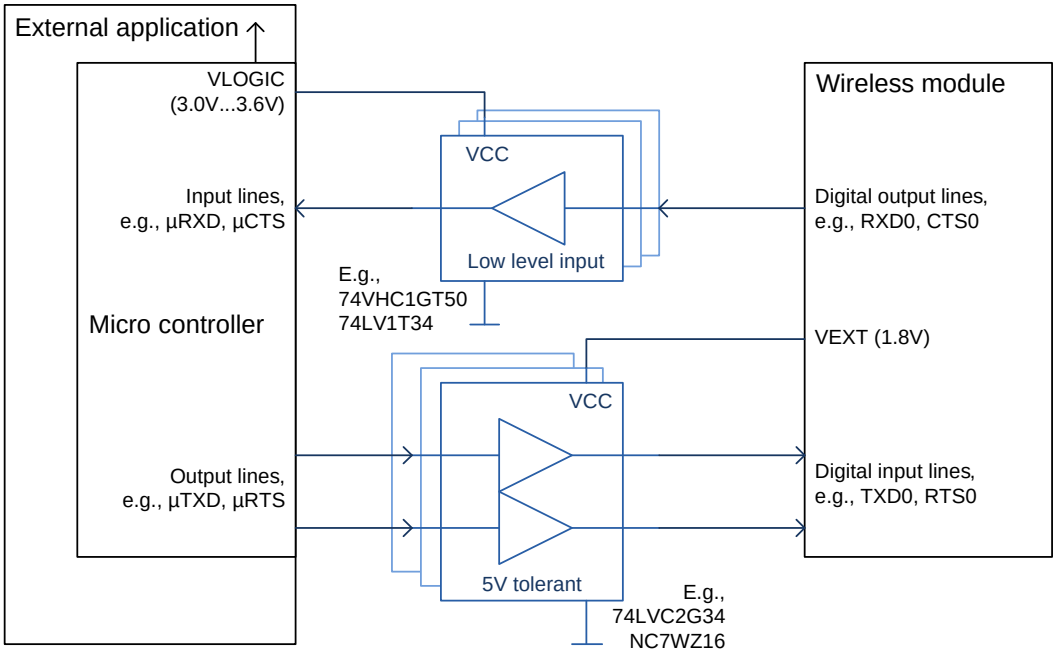
2.4.1 Prevent Back Powering

Because of the very low power consumption design, current flowing from any other source into the module circuit must be avoided in any case, for example reverse current from high state external control lines while the module is powered down. Therefore, the external application must be designed to prevent reverse current flow. Otherwise there is the risk of undefined states of the module during startup and shutdown or even of damaging the module. A simple solution preventing back powering is the usage of VEXT for level shifters, as Figure 25 shows. If level shifters are not really required, it is also possible to employ buffers.

While the module is in power down mode, VEXT must have a level lower than 0.3V after a certain time. If this is not the case the module is fed back by the application interface - recognizing such a fault state is possible by VEXT.

2.4.2 Sample Level Conversion Circuit

Depending on the micro controller used by an external application ALAS5V's digital input and output lines (i.e., ASC0 lines) may require level conversion. The following Figure 25 shows sample circuits with recommended level shifters for an external application's micro controller (with VLOGIC between 3.0V...3.6V). The level shifters can be used for digital input and output lines with V_{OH}max=1.85V or V_{IH}max =1.85V. The circuits recommend below would also be suitable for back powering protection.



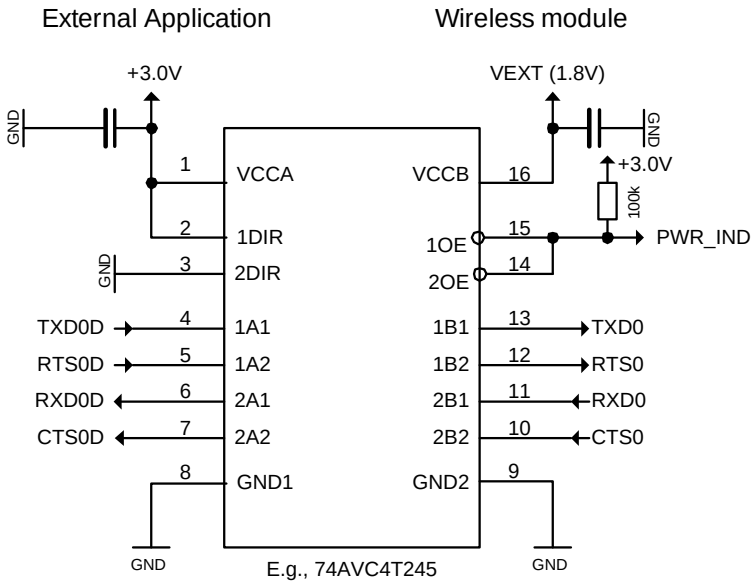


Figure 25: Sample level conversion circuits

2.4.3 Sample Circuit for Antenna Detection

The following figures explain how an RF antenna detection circuit may be implemented for ALAS5V to be able to detect connected antennas (for basic circuit and diagnostic principles - including usage of GPIO and ADCx_IN pads - please refer to Section 2.2.4). Figure 26 gives a general overview, Figure 27 depicts the actual antenna detection layout and shows how ESD protection, i.e., the RF/DC bridge, will have to be handled.

Properties for the components mentioned in Figure 26 and Figure 27 are given in Table 18 - parts list.

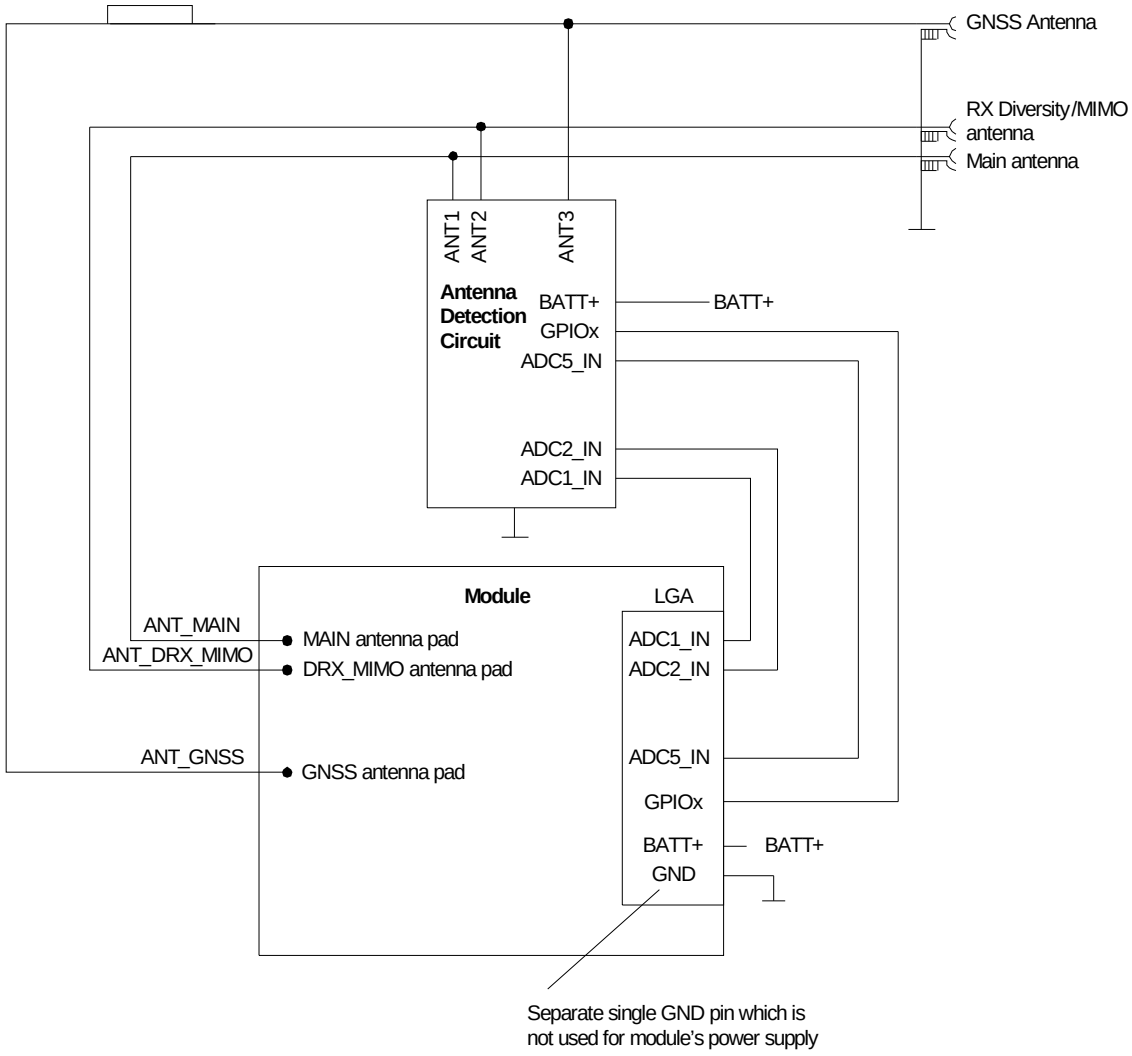


Figure 26: Antenna detection circuit sample - Overview

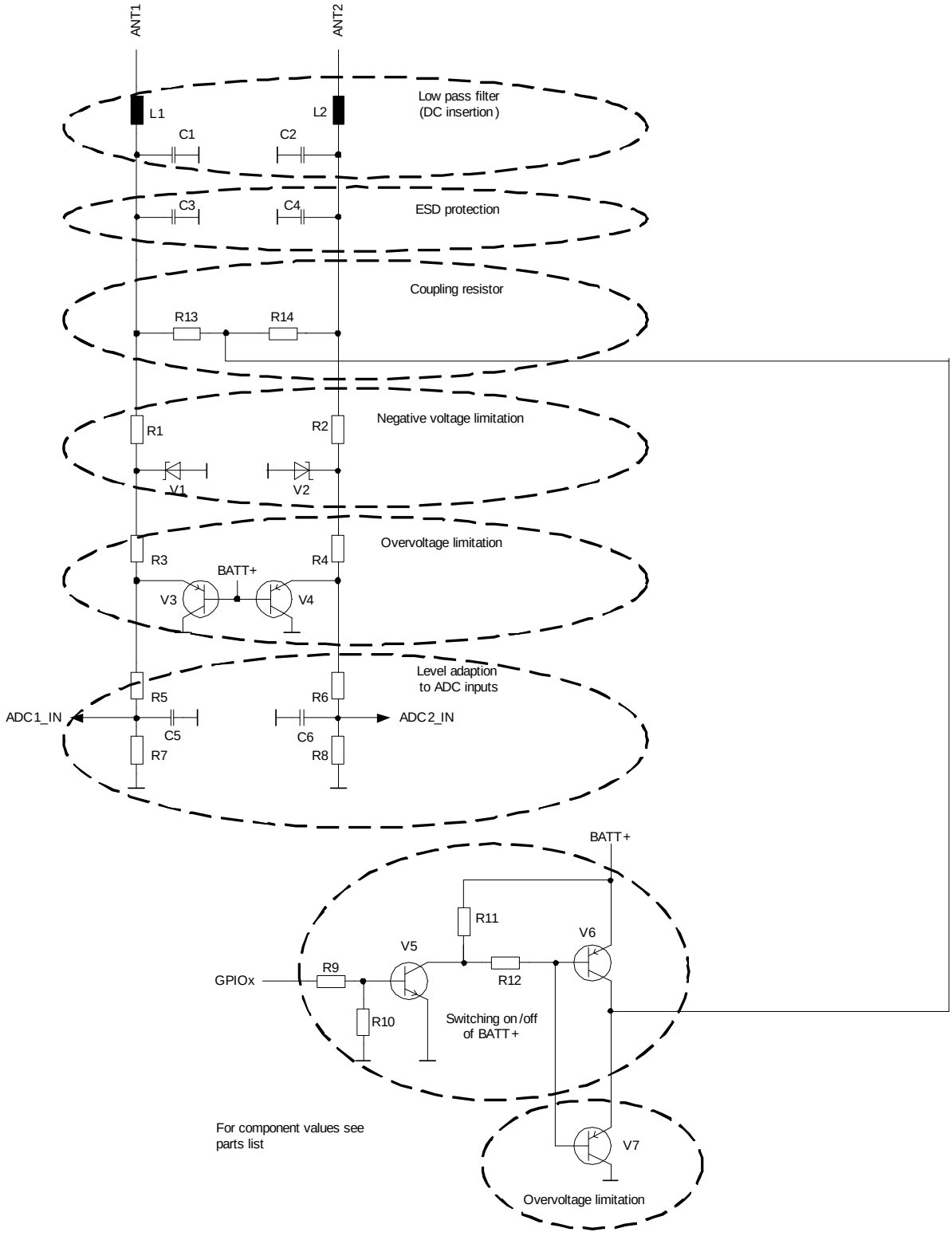


Figure 27: Antenna detection circuit sample - Schematic

Table 18: Antenna detection reference circuit - parts list

Reference	Part	Value	Tolerance	Conditions	Size
R1,2	Resistor	22R			
R3,4	Resistor	10k		≥ 125mW	
R5,6	Resistor	140k	1%		
R7,8	Resistor	100k	1%		
R9,10	Resistor	100k			
R11,12	Resistor	10k		≥ 125mW	
R13,14	Resistor	4k4 (e.g., 2x2k2 or 4x1k1)	1%	≥ 300mW	
C1,2	Capacitor	22p		50V	≤ 0402
C3,4	Capacitor	100n		50V	
C5,6	Capacitor	100n		10V	
V1,2	Schottky diode	RB520-40		40V	
V3,4,6,7	Transistor	BC857			
V5	Transistor	BC847			
L1,2	Inductor	39nH		Wire wound High Q	0402

3 GNSS Interface

ALAS5V integrates a GNSS receiver that offers the full performance of GPS/GLONASS technology. The GNSS receiver is able to continuously track all satellites in view, thus providing accurate satellite position data.

The integrated GNSS receiver supports the NMEA protocol via USB or ASC0 interface. NMEA is a combined electrical and data specification for communication between various (marine) electronic devices including GNSS receivers. It has been defined and controlled by the US based National Marine Electronics Association. For more information on the NMEA Standard please refer to http://www.nmea.org.

Depending on the receiver's knowledge of last position, current time and ephemeris data, the receiver's startup time (i.e., TTFF = Time-To-First-Fix) may vary: If the receiver has no knowledge of its last position or time, a startup takes considerably longer than if the receiver has still knowledge of its last position, time and almanac or has still access to valid ephemeris data and the precise time. For more information see Section 3.1.

By default, the GNSS receiver is switched off. It has to be switched on and configured.

Dead Reckoning Sync Line:
Dead reckoning solutions are used in (automotive) platforms to determine the (vehicles) location even when there is no GPS signal available (e.g. in tunnels, basement garages or even between high buildings in cities).

In addition to dead reckoning related NMEA sentences (for details see [1]: GNSS sentences), ALAS5V provides a dead reckoning synchronization line (DR_SYNC line) to be employed in external dead reckoning applications. DR_SYNC is derived from the GNSS signal clock as 1 pulse per second (1PPS) signal, with a frequency of 1Hz, an accuracy of +/-5 ms, and a high state pulse of 1ms. The DR_SYNC signal is provided as long as synchronized with the GNSS satellite clock, and continues after GNSS signal loss. DR_SYNC can be configured for the GPIO1 pad. For electrical characteristics see Table 22.

3.1 GNSS Interface Characteristics

The following tables list general characteristics of the GNSS interface.

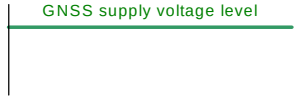
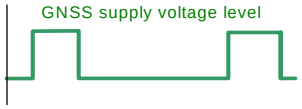
Table 19: GNSS properties

Parameter	Conditions	Min.	Typical	Max.	Unit
Frequency	GPS	1575	1575.42	1585	MHz
	GLONASS	1597	1602	1607	
	Beidou[1]	--	--	--	
	Galileo	1597	1575.42	1585	
Tracking Sensitivity	Open sky Active antenna or LNA[2] Passive antenna: GPS GLONASS Beidou[1] Galileo		 -159 -156 -154 -- -150		dBm
Acquisition Sensitivity	Open sky Active antenna or LNA[2] Passive antenna: GPS GLONASS Beidou[1] Galileo		 -149 -145 -140 -- -140		dBm
Cold Start sensitivity	GPS		-145		dBm
	GLONASS		-140		
	Beidou[1]		--		
	Galileo		-140		
Time-to-First-Fix (TTFF)	Cold		25	32	s
	Warm		10	29	s

1. Conditions and measurements not yet finalized.
2. Only measured for GPS.

Through the external GNSS antenna DC feeding the module is able to supply an active GNSS antenna. The supply voltage level at the GNSS antenna interface depends on the GNSS configuration.

Table 20: Power supply for active GNSS antenna

Function	Setting samples	IO	Signal form and level
GNSS active antenna supply	Supply voltage with: GNSS receiver off Active antenna off	O	
	Supply voltage with: GNSS receiver on Active antenna on SLEEP mode	O	
	Supply voltage with: GNSS receiver on Active antenna auto	O	

4 Operating Characteristics

4.1 Operating Modes

The table below briefly summarizes the various operating modes referred to throughout the document.

Table 21: Overview of operating modes

Mode	Function	
Normal operation	GSM / GPRS / UMTS / HSPA / LTE SLEEP	Power saving set automatically when no call is in progress and the USB connection is detached and no active communication via ASC0. Also, the GNSS active antenna mode has to be turned off or set to "auto"
	GSM / GPRS / UMTS / HSPA / LTE IDLE	Power saving disabled or an USB connection active, but no data transfer in progress.
	GSM TALK/ GSM DATA	Connection between two subscribers is in progress. Power consumption depends on the GSM network coverage and several connection settings (e.g. DTX off/on, FR/EFR/HR, hopping sequences and antenna connection). The following applies when power is to be measured in TALK_GSM mode: DTX off, FR and no frequency hopping.
	GPRS DATA	GPRS data transfer in progress. Power consumption depends on network settings (e.g. power control level), uplink / downlink data rates and GPRS configuration (e.g. used multislot settings).
	EGPRS DATA	EGPRS data transfer in progress. Power consumption depends on network settings (e.g. power control level), uplink / downlink data rates and EGPRS configuration (e.g. used multislot settings).
	UMTS TALK/ UMTS DATA	UMTS data transfer in progress. Power consumption depends on network settings (e.g. TPC Pattern) and data transfer rate.
	HSPA DATA	HSPA data transfer in progress. Power consumption depends on network settings (e.g. TPC Pattern) and data transfer rate.
	LTE DATA	LTE data transfer in progress. Power consumption depends on network settings, data transfer rates, and carrier aggregation/MIMO configuration.
Power Down	Normal shutdown after sending the AT^SMSO command. Software is not active. Interfaces are not accessible. Operating voltage (connected to BATT+) remains applied. Only a voltage regulator is active for powering the RTC, as long as operating voltage applied at BATT+ does not drop below approx. 1.4V.	
Airplane mode	Airplane mode shuts down the radio part of the module, causes the module to log off from the GSM/GPRS network and disables all AT commands whose execution requires a radio connection. Airplane mode can be controlled by AT command (see [1]).	

4.2 Power Up/Power Down Scenarios

In general, be sure not to turn on ALAS5V while it is beyond the safety limits of voltage and temperature stated in Section 6.1. ALAS5V immediately switches off after having started and detected these inappropriate conditions. In extreme cases this can cause permanent damage to the module.

4.2.1 Turn on ALAS5V

When the ALAS5V module is in Power Down mode, it can be started to Normal mode by driving the IGT (ignition) line to ground. It is required to use an open drain/collector driver to avoid current flowing into this signal line. Pulling this signal low triggers a power-on sequence. To turn on ALAS5V, it is strongly recommended to keep IGT active low at least 100 milliseconds, even though under certain conditions a period of less than 100 milliseconds might be sufficient. After turning on ALAS5V, IGT should be set inactive to prevent the module from turning on again after a shut downby AT command or EMERG_OFF. For details on signal states during startup see also Section 4.2.2.

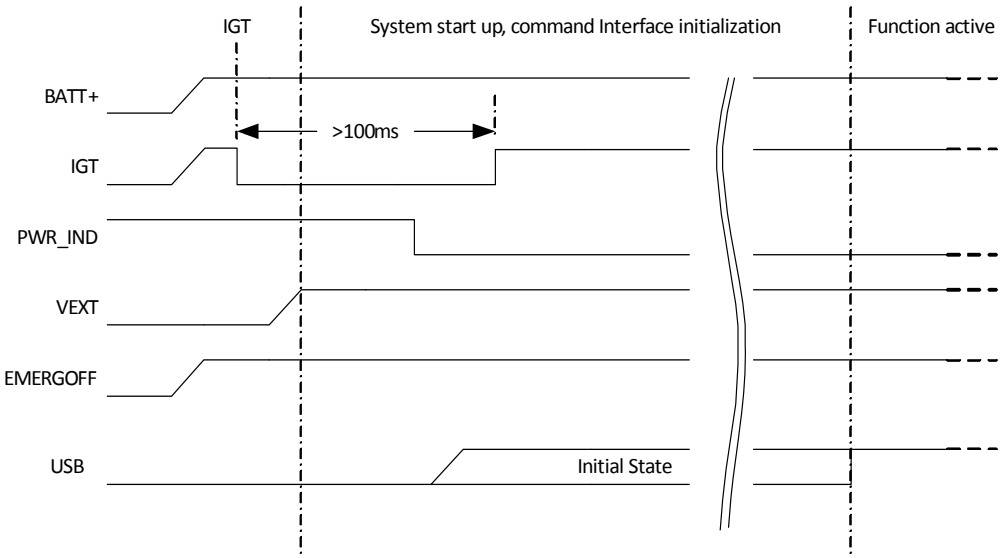


Figure 28: Power-on with IGT

Note: After power up IGT should remain high. Also note that with a USB connection the USB host may take some seconds to set up the virtual COM port connection.

After startup or mode change the following URCs are sent to every port able to receive AT commands indicating the module's ready state (this may take up to approx. 32s):
- "^SYSSTART" indicates that the module has entered Normal mode.
- "^SYSSTART AIRPLANE MODE" indicates that the module has entered Airplane mode.

These URCs notify the external application that the first ATcommand can be sent to the module. If these URCs are not used to detect then the only way of checking the module's ready state can be checked by polling, e.g., send characters (e.g. "at")until the module is responding.

Please note that on USB ports these URCs are only sent if the USB interface is in state 'configured', and with AT^SCFG= "MEopMode/ExpectDTR being enabled (see also Section 4.3) the connected USB host has signaled being ready to receive data.

4.2.2 Signal States after First Startup

Table 22 describes the various states each interface signal passes through after startup and during operation.

Signals are in an initial state while the module is initializing. Once the startup initialization has completed, i.e. when the software is running, all signals are in defined state. The state of several signals will change again once the respective interface is activated or configured by AT command.

Table 22: Signal states

Signal name	Pad no.	Reset phase (ignition) 0 - 100ms	Hardware init 100ms - 5s	Firmware init 5s - 32s	System active >32s
CCIN1	N19	PD	PU	PU	PU
CCRST1	L19	L	L	1.8V/3V Data	L
CCIO1	J19	L	L	1.8V/3V Data	L
CCCLK1	M19	PD	PD	PD --> 1.8V/3V CLK --> L	L
CCIN2	N18	Tri	PD --> PU	PU --> Tri	Tri
CCRST2	K18	Tri	PD	PD --> L	L
CCIO2	J18	Tri	PD	PD --> L	L
CCCLK2	M18	Tri	PD	PD --> L	L
RXD0	F18	Tri	PD --> PU	PU --> Tri	Tri
TXD0	H19	Tri	PD --> PU	PU --> Tri	Tri
CTS0	G19	Tri	PD --> PU	PU --> Tri	Tri
RTS0	G20	Tri	PD --> PU	PU --> Tri	Tri
DSR0	F17	PD	PD	PD	PD
DTR0	F19	Tri	PD	PD	PD
DCD0	G18	PD	PD --> PU --> PD	PD	PD
RING0	J20	Tri	PD --> PU	PU	PU
RXD1	R9	Tri	PD --> PU	PU --> Tri	Tri
TXD1	R8	Tri	PD --> PU	PU --> Tri	Tri
CTS1	R7	Tri	PD --> PU	PU --> Tri	Tri
RTS1	R6	Tri	PD --> PU	PU --> Tri	Tri
DIN2	N9	Tri	PU --> PD	PD	PD
BCLK2	N10	Tri	PD	PD	PD
FSC2	N7	Tri	PD	PD	PD
MCLK	P11	Tri	PD	PD	PD
DOUT2	N8	Tri	PD	PD	PD
I2CDAT1	M9	Tri	PD --> PU	PU	PU
I2CCLK1	M10	Tri	PD --> PU	PU	PU
EMERG_OFF	F16	PD/PU	PU	PU	PU
PCIE_HOST_RST	R11	Tri	PD --> L	L	L
PCIE_HOST_WAKE	R10	Tri	PD	PD --> Tri	Tri
PCIE_CLK_ REQ	R14	Tri	PD	PD --> L	L
PCIE_CLK_P	P16	Tri/PCIe	Tri/PCIe	2 packets activity (11s and 13s)	Tri/PCIe

Table 22: Signal states

Signal name	Pad no.	Reset phase (ignition) 0 - 100ms	Hardware init 100ms - 5s	Firmware init 5s - 32s	System active >32s
PCIE_CLK_M	P17	Tri/PCIe	Tri/PCIe	2 packets activity (11s and 13s)	Tri/PCIe
PCIE_RX_P	T12	Tri/PCIe	Tri/PCIe	2 packets activity (11s and 13s)	Tri/PCIe
PCIE_RX_M	T13	Tri/PCIe	Tri/PCIe	2 packets activity (11s and 13s)	Tri/PCIe
PCIE_TX_P	T15	Tri/PCIe	Tri/PCIe	2 packets activity (11s and 13s)	Tri/PCIe
PCIE_TX_M	T16	Tri/PCIe	Tri/PCIe	2 packets activity (11s and 13s)	Tri/PCIe
GPIO12	E12	Tri	PD	PD	PD
GPIO13	E11	Tri	PD	PD	PD
GPIO14	E10	Tri	PD	PD	PD
ANT_GNSS_ DC	A17	L	L	L	L
GNSS_EN	D13	PD	PD	PD	PD
ADC1_IN	D10	Tri	Tri	Tri	Tri
ADC2_IN	D11	Tri	Tri	Tri	Tri
ADC4_IN	D8	Tri	Tri	Tri	Tri
ADC5_IN	D9	Tri	Tri	Tri	Tri
JTAG_WD_ DISABLE	M8	Tri	PD	PD --> H	H
JTAG_TCK	C18	L	H	H	H
JTAG_TMS	D14	L	H	H	H
JTAG_TRST	D15	Tri	PD	PD	PD
JTAG_TDI	D16	L	H	H	H
JTAG_SRST	D17	L	H	H	H
JTAG_TDO	D18	L	H	H	H
JTAG_PS_ HOLD	E13	Tri	PD --> H	H	H
EMMC_D0	N15	Tri	PD	50ms PU and 950ms PD	50ms PU and 950ms PD
EMMC_D1	M14	Tri	PD	50ms PU and 950ms PD	50ms PU and 950ms PD
EMMC_D2	N14	Tri	PD	50ms PU and 950ms PD	50ms PU and 950ms PD
EMMC_D3	P14	Tri	PD	50ms PU and 950ms PD	50ms PU and 950ms PD
EMMC_D4	N12	Tri	L	L	L
EMMC_D5	N13	Tri	L	L	L
EMMC_D6	M13	Tri	L	L	L
EMMC_D7	P12	Tri	L	L	L
EMMC_CLK	P15	Tri	PD --> L	50ms CLK and 950ms PD	50ms CLK and 950ms PD
EMMC_CMD	P13	Tri	PD	50ms PU and 950ms PD	50ms PU and 950ms PD
EMMC_DETECT	L7	Tri	PD	PD	PD
EMMC_PWR	L15	L	L	50ms 2.9V and 950ms L	50ms 2.9V and 950ms L

Table 22: Signal states

Signal name	Pad no.	Reset phase (ignition) 0 - 100ms	Hardware init 100ms - 5s	Firmware init 5s - 32s	System active >32s
GPIO1	E8	Tri	PD	PD --> L	L
GPIO3	C17	Tri	PD	PD	PD
GPIO4	L20	Tri	PD	PD	PD
GPIO5	P6	Tri	PD	PD	PD
GPIO6	H18	Tri	PU --> PD	PD	PD
GPIO7	E9	Tri	PD	PD	PD
GPIO8	M20	Tri	PD	PD	PD
GPIO11	D12	Tri	PD	PD	PD
GPIO12	E12	Tri	PD	PD	PD
GPIO13	E11	Tri	PD	PD	PD
GPIO14	E10	Tri	PD	PD	PD
GPIO15	T9	Tri	PD	PD --> H (after 3s)	H
GPIO16	R17	Tri	PD	PD --> PU (after 28s)	PU
GPIO17	M7	Tri	PD	PD --> H (after 24s)	H
GPIO22	M15	Tri	PD	PD	PD
FwSwap	T7	Tri	PD	PD	PD
USB_SSTX_P	H16	Tri/USB	Tri/USB	Tri/USB	Tri/USB
USB_SSTX_N	H17	Tri/USB	Tri/USB	Tri/USB	Tri/USB
USB_SSRX_P	K16	Tri/USB	Tri/USB	Tri/USB	Tri/USB
USB_SSRX_N	K17	Tri/USB	Tri/USB	Tri/USB	Tri/USB
USB_DP	M16	Tri/USB	Tri/USB	Tri/USB	Tri/USB
USB_DN	M17	Tri/USB	Tri/USB	Tri/USB	Tri/USB
VUSB_IN	P18	L	L	L	L
IGT	D19	PU	PU	PU	PU
PWR_IND	R5	Tri	L	L	L
VEXT	E18	L	1.8V	1.8V	1.8V

L = Low level H = High level I = Input O = Output	PD = Pull down resistor between 18k...65k PD(…k) = Pull down resistor with ...k PU = Pull up resistor between 18k...65k PU(…k) = Pull up resistor with ...k, Z = High impedance

4.2.3 Turn off or Restart ALAS5V

To switch off or restart the module the following procedures may be used:

- *Software controlled shutdown procedure*: Software controlledby sending an AT command over the serial application interface. See Section 4.2.3.1.
- *Software controlled restart procedure*: Software controlled by sending an AT commandover the serial application interface. See Section 4.2.3.2.
- *Hardware controlled shutdown procedure*: Hardware controlled shutdown by IGT line. See Section 4.2.3.3.
- *Hardware controlled shutdown or restart procedure*: Hardware controlled shutdown or restart by EMERG_OFF line. See Section 4.2.3.4.
- *Automatic shutdown (software controlled)*: See Section 4.2.4
  - Takes effect if ALAS5V board temperature exceeds a critical limit.

4.2.3.1 Switch off ALAS5V Using AT Shutdown Command

The best and safest approach to powering down ALAS5V is to issue the AT^SMSO command. This procedure lets ALAS5V log off from the network and allows the software to enter into a secure state and save data before disconnecting the power supply. The mode is referred to as Power Down mode. After sending AT^SMSO do not enter any other AT commands. While powering down the module may still send some URCs. The AT command's "OK" response indicates that the data has been stored non-volatile and the module will turn down in a few seconds. The complete power down procedure may take approx. 20s.To verify that the module definitely turned off, it is possible to monitor the PWR_IND signal. A high state of the PWR_IND signal line indicates that the module is being switched off as shown in Figure 29.

Be sure not to disconnect the supply voltage V_{BATT+} before the module's switch off procedure has been completed. Otherwise you run the risk of losing data. Signal states during switch off are shown in Figure 29.

While ALAS5V is in Power Down mode the application interface is switched off and must not be fed from any other source. Therefore, your application must be designed to avoid any current flow into any digital signal lines of the application interface. No special care is required for the USB interface which is protected from reverse current.

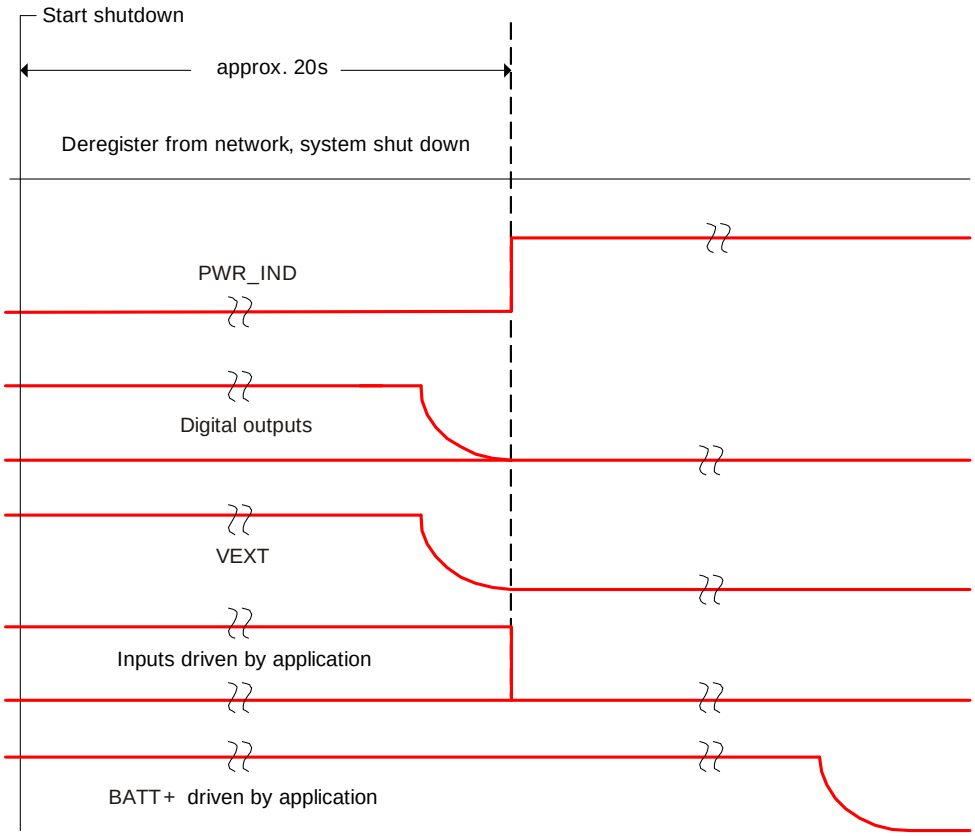


Figure 29: Signal states during turn-off procedure

Note 1: VEXT can be used in solutions to prevent back powering (see also Section 2.4.1). It should have a level lower than 0.3V after module shutdown.

Note 2: After module shutdown by means of AT command, i.e., after the VEXT level went below 0.3V, please allow for a time period of at least 1 second before restarting the module.

4.2.3.2 Restart ALAS5V Using AT Command

The best and safest approach to restart ALAS5V is by AT command. For more information on the AT^CFUN command please refer to is described in detail in [1].

4.2.3.3 Turn off ALAS5V Using IGT Line

The IGT line can be configured for use in two different switching modes: You can set the IGT line to switch on the module only, or to switch it on and off. The switching mode is determined by the parameter "MEShutdown/OnIgnition" of the AT^SCFG command.

By factory default, the ON/OFF switch mode of IGT is disabled:

```
AT^SCFG=”MEShutdown/OnIgnition”          # Query the current status of IGT.
^SCFG: "MEShutdown/OnIgnition","off"     # IGT can be used only to switch on ALAS5V.
OK                                       IGT works as described in Section 4.2.1.
```

To configure IGT for use as ON/OFF switch:

```
AT^SCFG=”MEShutdown/OnIgnition”,”on”     # Enable the ON/OFF switch mode of IGT.
^SCFG: "MEShutdown/OnIgnition","on"      # IGT can be used to switch on and off ALAS5V.
OK
```

Take great care before changing the switching mode of the IGT line. To ensure that the IGT line works properly as ON/OFF switch it is of vital importance that the following conditions are met:

Switch-on condition: If the ALAS5V is off, the IGT line must be asserted for at least 100 milliseconds before being released.

Switch-off condition: If the ALAS5V is on, the IGT line must be asserted for at least 2.1 seconds before being released. The module switches off after the line is released. The switch-off routine is identical with the procedure initiated by AT^SMSO, i.e. the software performs an orderly shutdown as described in Section 4.2.3.1.
Before switching off the module wait at least 32 seconds after startup.

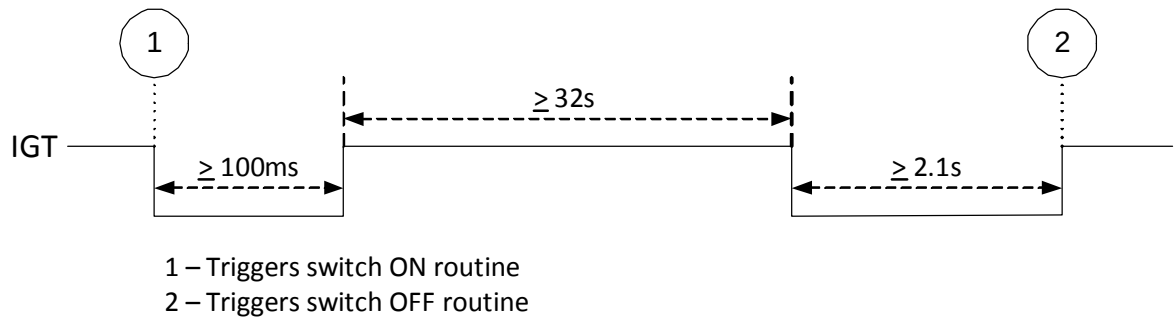


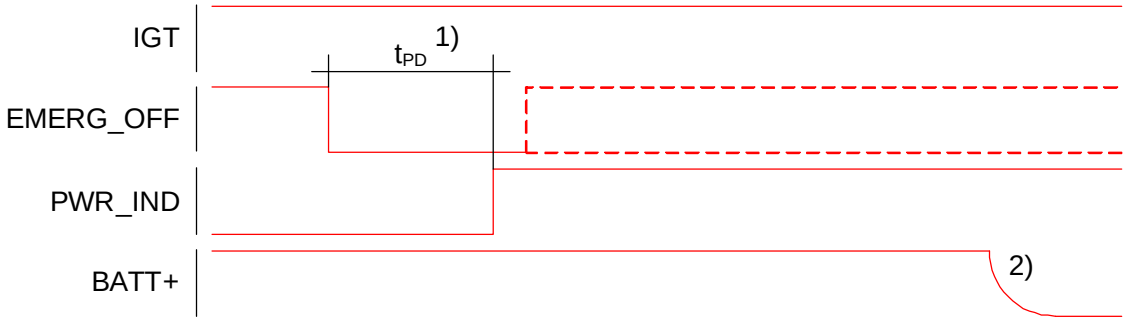
Figure 30: Timing of IGT if used as ON/OFF switch

4.2.3.4 Turn off or Restart ALAS5V in Case of Emergency

Caution: Use the EMERG_OFF line only when, due to serious problems, the software is not responding for more than 5 seconds. Pulling the EMERG_OFF line causes the loss of all information stored in the volatile memory. Therefore, this procedure is intended only for use in case of emergency, e.g. if ALAS5V does not respond, if reset or shutdown via AT command fails.

The EMERG_OFF line is available on the application interface and can be used to turn off or to restart the module. In any case the EMERG_OFF line must be pulled to ground until the Power Down mode is reached, as indicated by PWR_IND=high. To control the EMERG_OFF line it is required to use an open drain / collector driver. EMERG_OFF is pulled high internally.

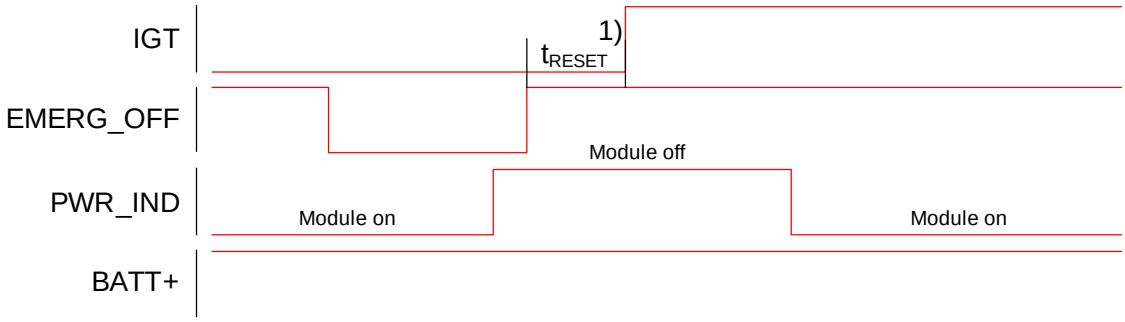
Now, to permanently turn off the module, the IGT line has to be set to high (inactive) before the EMERG_OFF line is released. The module will then switch off and needs to be restarted at a later time. This switch off behavior is shown in Figure 31.



1) The time to Power Down mode (t_{PD}) depends on the operating state, and can be up to 2000ms. PWR_IND should be monitored by the external application. Note that a low impulse at EMERG_OFF for more than 2000ms will reset the module's RTC.
2) The the power supply voltage (BATT+) may be disconnected only after having reached Power Down mode as indicated by the PWR_IND signal going high. The power supply has to be available (again) before the module is restarted.

Figure 31: Shutdown by EMERG_OFF signal

To simply restart the module, the IGT line has to continue to be driven low (active) for at least 100ms after having released the EMERG_OFF line. The module will then switch off and restart automatically. This restart behavior is shown in Figure 32.



1) The time to module reset (t_{RESET}) must be ≥ 100ms

Figure 32: Restart by EMERG_OFF signal

4.2.3.5 Overall Shutdown Sequence

In case the above described dedicated software or hardware controlled shutdown procedures fail or hang for some reason, it may become necessary to disconnect BATT+ in order to ultimately shut down the module. Figure 33 shows a flow chart that illustrates how an overall shutdown sequence might be implemented.

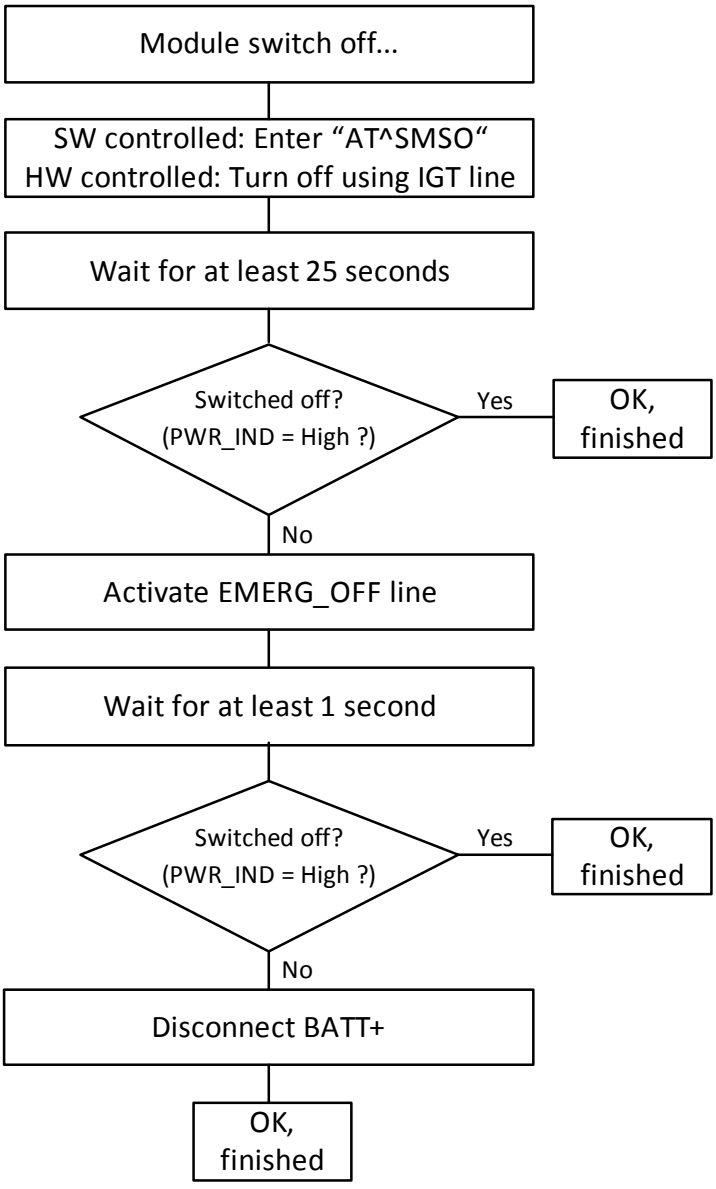


Figure 33: Overall shutdown sequence

4.2.4 Automatic Shutdown

Automatic shutdown takes effect if:
- The ALAS5V board is exceeding the critical limits of overtemperature or undertemperature
- Undervoltage or overvoltage is detected

The automatic shutdown procedure is equivalent to the power down initiated with the AT^SMSO command, i.e. ALAS5V logs off from the network and the software enters a secure state avoiding loss of data.

Alert messages transmitted before the device switches off are implemented as Unsolicited Result Codes (URCs). The presentation of the temperature URCs can be enabled or disabled with the command AT^SCTM. The URC presentation mode varies with the condition, please see Section 4.2.4.1 to Section 4.2.4.4 for details. For further instructions on AT commands refer to [1].

4.2.4.1 Thermal Shutdown

The board temperature is constantly monitored by an internal NTC resistor located on the PCB. The values detected by the NTC resistor are measured directly on the board and therefore, are not fully identical with the ambient temperature.

Each time the board temperature goes out of range or back to normal, ALAS5V instantly displays an alert (if enabled).

- URCs indicating the level "1" or "-1" allow the user to take appropriate precautions, such as protecting the module from exposure to extreme conditions. The presentation of the URCs depends on settings selected with the AT^SCTM write command.
  AT^SCTM=1: Presentation of URCs is always enabled.
  AT^SCTM=0 (default): Presentation of URCs is enabled during the 2 minutes guard period after start-up of ALAS5V. After expiry of the 2 minutes guard period, the presentation will be disabled, i.e. no URCs with alert levels "1" or "-1" will be generated.
- URCs indicating the level "2" and ”-2” are instantly followed by an orderly shutdown, except for cases described in Section 4.2.4.2. The presentation of these URCs is always enabled, i.e. they will be output even though the factory setting AT^SCTM=0 was never changed.

The (maximum) temperature ratings are stated in Section 4.5. Temperature limits and associated URCs are listed in the below Table 23.

Table 23: Board temperature warning and switch off level

Parameter	Temperature	URC	Notes
High temperature switch off active	≥ +97°C	^SCTM_B: 2	The possible deviation is typically ± 2°C.
High temperature switch off release	≤ +96°C	^SCTM_B: 1	
High temperature warning active	≥ +86°C	^SCTM_B: 1	
High temperature warning release	≤ +85°C	^SCTM_B: 0	
Operating temperature range	-30°C...+85°C	---	
Low temperature warning release	≥ -30°C	^SCTM_B: 0	The possible deviation is typically ± 2°C.
Low temperature warning active	≤ -31°C	^SCTM_B: -1	
Low temperature switch off release	≥ -40°C	^SCTM_B: -1	
Low temperature switch off active	≤ -42°C	^SCTM_B: -2	

The AT^SCTM command can also be used to check the present status of the board. Depending on the selected mode, the read command returns the current board temperature in degrees Celsius or only a value that indicates whether the board is within the safe or critical temperature range. See [1] for further instructions.

4.2.4.2 Deferred Shutdown at Extreme Temperature Conditions

In the following cases, automatic shutdown will be deferred if a critical temperature limit is exceeded:

- While an emergency call is in progress.
- During a two minute guard period after power-up. This guard period has been introduced in order to allow for the user to make an emergency call. The start of any one of these calls extends the guard period until the end of the call. Any other network activity may be terminated by shutdown upon expiry of the guard time.

While in a "deferred shutdown" situation, ALAS5V continues to measure the temperature and to deliver alert messages, but deactivates the shutdown functionality. Once the 2 minute guard period is expired or the call is terminated, full temperature control will be resumed. If the temperature is still out of range, ALAS5V switches off immediately (without another alert message).

Caution: Automatic shutdown is a safety feature intended to prevent damage to the module. Extended usage of the deferred shutdown facilities provided may result in damage to the module, and possibly other severe consequences.

4.2.4.3 Undervoltage Shutdown

If the measured battery voltage is no more sufficient to set up a call the following URC will be presented:

^SBC: Undervoltage.

The URC indicates that the module is close to the undervoltage threshold. If undervoltage persists the module keeps sending the URC several times before switching off automatically.

This type of URC does not need to be activated by the user. It will be output automatically when fault conditions occur.

4.2.4.4 Overvoltage Shutdown

The overvoltage shutdown threshold is 100mV above the maximum supply voltage V_{BATT+} specified in Table 4.

When the supply voltage approaches the overvoltage shutdown threshold the module will send the following URC:

^SBC: Overvoltage warning

This alert is sent once.

When the overvoltage shutdown threshold is exceeded the module will send the following URC

^SBC: Overvoltage shutdown

before it shuts down cleanly.

This type of URC does not need to be activated by the user. It will be output automatically when fault conditions occur.

Keep in mind that several ALAS5V components are directly linked to BATT+ and, therefore, the supply voltage remains applied at major parts of ALAS5V, even if the module is switched off. Especially the power amplifier is very sensitive to high voltage and might even be destroyed.

4.3 Power Saving

ALAS5V is able to reduce its functionality to a minimum (during the so-called SLEEP mode) in order to minimize its current consumption. The following sections explain the module's network dependent power saving behavior. The power saving behavior is further configurable by AT command:

- AT^SCFG= "MEopMode/PwrSave": The power save mode is by default enabled. While inactive, the module stays in power save (SLEEP) state, waking up only upon any of the following events:
  - Cyclically to meet basic technical demands, e.g. network requirements (such as regularly listening to paging messages from the base station as described in Section 4.3.1, Section 4.3.2 and Section 4.3.3.
  - Cyclically after expiry of a configured power saving period.
  - Data at any interface port, e.g., URCs for incoming calls.
  - A level state transition at GPIO3, GPIO5, GPIO7, GPIO8, or GPIO16 (if configured).
- AT^SCFG= "MEopMode/ExpectDTR": Power saving will take effect only if there is no transmission data pending on any of the module's USB ports. The expect DTR AT command ensures that data becoming pending on any USB port before an external application has signaled its readiness to receive the data is discarded. By default this behavior is enabled for all available USB CDC ACM and CDC ECM ports.
- AT^SCFG="Radio/OutputPowerReduction": Output power reduction is possible for the module in GPRS multislot scenarios to reduce its output power according to 3GPP 45.005 section.

Please refer to [1] for more information on the above AT commands used to configure the module's power saving behavior.

The implementation of the USB host interface also influences the module's power saving behavior and therefore its current consumption. For more information see Section 2.1.3.

Another feature influencing the current consumption is the configuration of the GNSS antenna interface. For details see Section 3.1.

Also note that the module does not wake up from SLEEP mode just to measure the supply voltage, and that the command AT^SBV reports an average over the values it was able to measure last (see also Section 4.4.3). Therefore, the shorter the power saving periods are, the faster and more precisely will the reported average adjust to possible voltage changes.

4.3.1 Power Saving while Attached to GSM Networks

The power saving possibilities while attached to a GSM network depend on the paging timing cycle of the base station. The duration of a paging timing cycle can be calculated using the following formula:

t = 4.615 ms (TDMA frame duration) * 51 (number of frames) * DRX value.

DRX (Discontinuous Reception) is a value from 2 to 9, resulting in paging timing cycles between 0.47 and 2.12 seconds. The DRX value of the base station is assigned by the GSM network operator.

Now, a paging timing cycle consists of the actual fixed length paging plus a variable length pause before the next paging. In the pauses between listening to paging messages, the module resumes power saving, as shown in Figure 34.

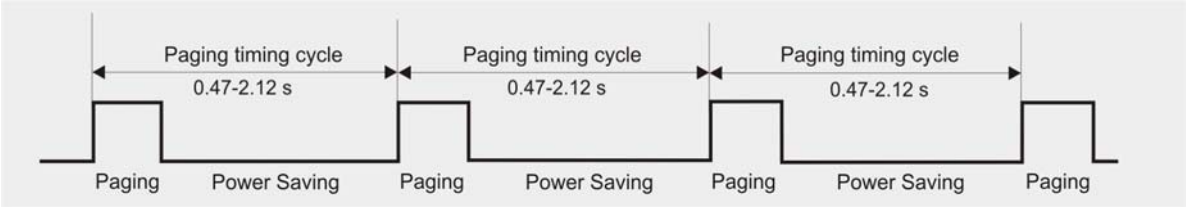


Figure 34: Power saving and paging in GSM networks

The varying pauses explain the different potential for power saving. The longer the pause the less power is consumed.

Generally, power saving depends on the module's application scenario and may differ from the above mentioned normal operation. The power saving interval may be shorter than 0.47 seconds or longer than 2.12 seconds.

4.3.2 Power Saving while Attached to WCDMA Networks

The power saving possibilities while attached to a WCDMA network depend on the paging timing cycle of the base station.

During normal WCDMA operation, i.e., the module is connected to a WCDMA network, the duration of a paging timing cycle varies. It may be calculated using the following formula:

$t = 2^{DRX\ value} * 10$ ms (WCDMA frame duration).

DRX (Discontinuous Reception) in WCDMA networks is a value between 6 and 9, thus resulting in paging timing cycles between 0.64 and 5.12 seconds. The DRX value of the base station is assigned by the WCDMA network operator.

Now, a paging timing cycle consists of the actual fixed length paging plus a variable length pause before the next paging. In the pauses between listening to paging messages, the module resumes power saving, as shown in Figure 35.

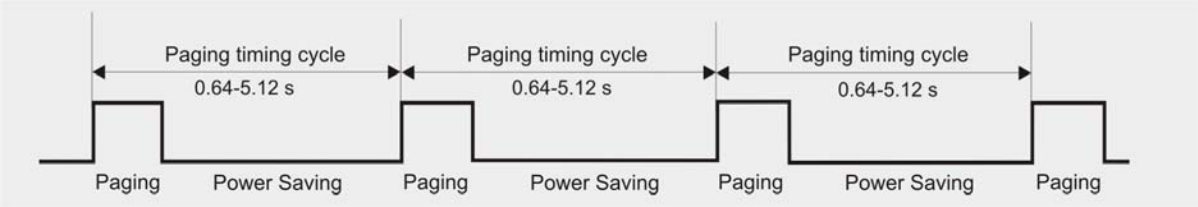


Figure 35: Power saving and paging in WCDMA networks

The varying pauses explain the different potential for power saving. The longer the pause the less power is consumed.

Generally, power saving depends on the module's application scenario and may differ from the above mentioned normal operation. The power saving interval may be shorter than 0.64 seconds or longer than 5.12 seconds.

4.3.3 Power Saving while Attached to LTE Networks

The power saving possibilities while attached to an LTE network depend on the paging timing cycle of the base station.

During normal LTE operation, i.e., the module is connected to an LTE network, the duration of a paging timing cycle varies. It may be calculated using the following formula:

t = DRX Cycle Value * 10 ms

DRX cycle value in LTE networks is any of the four values: 32, 64, 128 and 256, thus resulting in paging timing cycles between 0.32 and 2.56 seconds. The DRX cycle value of the base station is assigned by the LTE network operator.

Now, a paging timing cycle consists of the actual fixed length paging plus a variable length pause before the next paging. In the pauses between listening to paging messages, the module resumes power saving, as shown in Figure 36.

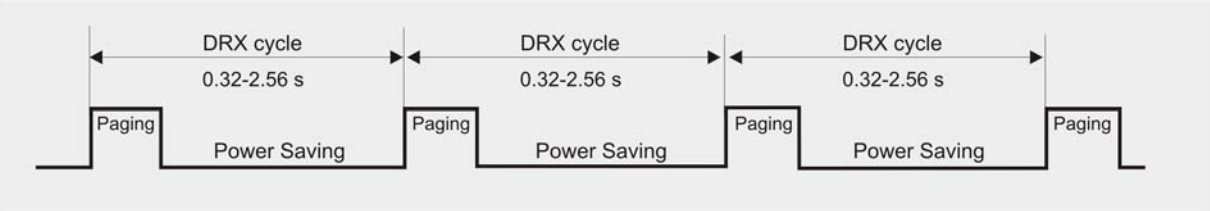


Figure 36: Power saving and paging in LTE networks

The varying pauses explain the different potential for power saving. The longer the pause the less power is consumed.

Generally, power saving depends on the module's application scenario and may differ from the above mentioned normal operation. The power saving interval may be shorter than 0.32 seconds or longer than 2.56 seconds.

4.4 Power Supply

ALAS5V needs to be connected to a power supply at the SMT application interface - 4 lines BATT+, and GND. There are two separate voltage domains for BATT+:
- BATT+_RF with 2 lines for the RF power amplifier supply
- BATT+ with 2 lines for the general power management.

The main power supply from an external application has to be a single voltage source and has to be expanded to two sub paths (star structure). Each voltage domain must be decoupled by application with low ESR capacitors (≥ 47µF MLCC @ BATT+; ≥ 4x47µF MLCC @ BATT+_RF) as close as possible to LGA pads. Figure 37 shows a sample circuit for decoupling capacitors for BATT+.

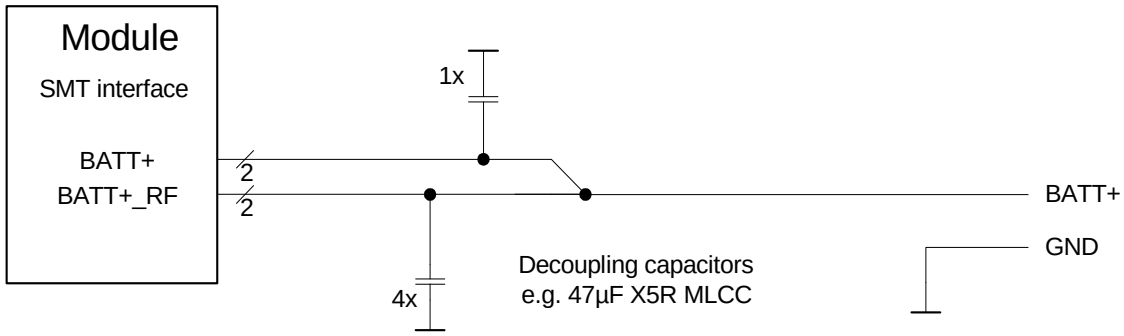


Figure 37: Decoupling capacitor(s) for BATT+

The power supply of ALAS5V must be able to provide the peak current during the uplink transmission.

All key functions for supplying power to the device are handled by the power management IC. It provides the following features:
- Stabilizes the supply voltages for the baseband using switching regulators and low drop linear voltage regulators.
- Switches the module's power voltages for the power-up and -down procedures.
- Delivers, across the VEXT line, a regulated voltage for an external application.
- LDO to provide SIM power supply.

4.4.1 Power Supply Ratings

Table 24 and Table 25 assemble various voltage supply and current consumption ratings for the supported modules. Possible ratings are preliminary and will have to be confirmed.

Table 24: Voltage supply ratings

	Description	Conditions	Min	Typ	Max	Unit
BATT+	Supply voltage	Directly measured at Module. Voltage must stay within the min/max values, including voltage drop, ripple, spikes	3.3	3.8	4.2	V
	Maximum allowed voltage drop during transmit burst	Normal condition, power control level for Pout max			400	mV
	Voltage ripple	Normal condition, power control level for Pout max @ f <= 250 kHz @ f > 250 kHz			 120 90	 mV_{pp} mV_{pp}

Table 25: Current consumption ratings

	Description	Conditions			Typical rating	Unit
I_{BATT+} [1]	OFF State supply current	Power Down	RTC off	USB disconnected	30	µA
				USB connected	60	
			RTC on	USB disconnected	90	
				USB connected	120	
	Average GSM supply current	SLEEP[2] @ DRX=9 (no communication with the module)		USB disconnected	1.7	mA
				USB suspend	13.2	
		SLEEP[2] @ DRX=5 (no communication with the module)		USB disconnected	1.9	mA
				USB suspend	13.4	
		SLEEP[2] @ DRX=2 (no communication with the module)		USB disconnected	2.5	mA
				USB suspend	14	
		IDLE[3] @ DRX=2 (UART/USB active, but no communication with the module)		USB disconnected	60	mA
				USB active	70	
		Voice call GSM850/900; PCL=5		@ 50Ω	330	mA
		GPRS Data transfer GSM850/900; PCL=5; 1Tx/4Rx		ROPR=8 (max. reduction)	320	mA
				ROPR=4 (no reduction)		
		GPRS Data transfer GSM850/900; PCL=5; 2Tx/3Rx		ROPR=8 (max. reduction)	430	mA
				ROPR=4 (no reduction)	540	
		GPRS Data transfer GSM850/900; PCL=5; 4Tx/1Rx		ROPR=8 (max. reduction)	650	mA
				ROPR=4 (no reduction)	980	
				@ total mismatch	1200	

Table 25: Current consumption ratings

	Description	Conditions		Typical rating	Unit
I_{BATT+} [1]	Average GSM supply current	EDGE Data transfer GSM850/900; PCL=5; 1Tx/4Rx	ROPR=8 (max. reduction)	220	mA
			ROPR=4 (no reduction)		
		EDGE Data transfer GSM850/900; PCL=5; 2Tx/3Rx	ROPR=8 (max. reduction)	340	mA
			ROPR=4 (no reduction)	360	
		EDGE Data transfer GSM850/900; PCL=5; 4Tx/1Rx	ROPR=8 (max. reduction)	600	mA
			ROPR=4 (no reduction)	630	
		Voice call GSM1800/ 1900; PCL=0	@ 50Ω	240	mA
		GPRS Data transfer GSM1800/1900; PCL=0; 1Tx/4Rx	ROPR=8 (max. reduction)	230	mA
			ROPR=4 (no reduction)		
		GPRS Data transfer GSM1800/1900; PCL=0; 2Tx/3Rx	ROPR=8 (max. reduction)	340	mA
			ROPR=4 (no reduction)	390	
		GPRS Data transfer GSM1800/1900; PCL=0; 4Tx/1Rx	ROPR=8 (max. reduction)	500	mA
			ROPR=4 (no reduction)	690	
		EDGE Data transfer GSM1800/1900; PCL=0; 1Tx/4Rx	ROPR=8 (max. reduction)	190	mA
			ROPR=4 (no reduction)		
		EDGE Data transfer GSM1800/1900; PCL=0; 2Tx/3Rx	ROPR=8 (max. reduction)	300	mA
			ROPR=4 (no reduction)	330	
		EDGE Data transfer GSM1800/1900; PCL=0; 4Tx/1Rx	ROPR=8 (max. reduction)	470	mA
			ROPR=4 (no reduction)	630	
	Peak current during GSM transmit burst	Voice call GSM850/900; PCL=5	@ 50Ω	2.2	A
			@ total mismatch	2.9	
		Voice call GSM1800/ 1900; PCL=0	@ 50Ω	1.5	A
			@ total mismatch	1.7	
I_{BATT+} [1]	Average GSM supply current (GNSS on)	GSM active (UART/USB active); @ DRX=2 & GNSS NMEA output off		80	mA
		GSM active (UART/USB active); @ DRX=2 & GNSS NMEA output on[4]		80	mA

Table 25: Current consumption ratings

	Description	Conditions		Typical rating	Unit
I_{BATT+} [1]	Average UMTS supply current Voice calls and Data transfers measured @ maximum Pout	SLEEP[2] @ DRX=9 (no communication with the module)	USB disconnected	1.6	mA
			USB suspend	13.1	
		SLEEP[2] @ DRX=8 (no communication with the module)	USB disconnected	1.8	mA
			USB suspend	13.3	
		SLEEP[2] @ DRX=6 (no communication with the module)	USB disconnected	2.3	mA
			USB suspend	13.8	
		IDLE[3] @ DRX=6 (UART/USB active, but no communication with the module)	USB disconnected	60	mA
			USB active	70	
		UMTS Data transfer Band I	@ 50Ω	600	mA
			@ total mismatch	810	
		UMTS Data transfer Band II	@ 50Ω	600	mA
			@ total mismatch	890	
		UMTS Data transfer Band III	@ 50Ω	640	mA
			@ total mismatch	820	
		UMTS Data transfer Band IV	@ 50Ω	640	mA
			@ total mismatch	790	
		UMTS Data transfer Band V/VI/XIX	@ 50Ω	590	mA
			@ total mismatch	690	
		UMTS Data transfer Band VIII	@ 50Ω	530	mA
			@ total mismatch	620	
I_{BATT+} [1]	Average UMTS supply current (GNSS on)	WCDMA active (UART / USB active); @ DRX=6 & GNSS NMEA output off		80	mA
		WCDMA active (UART / USB active); @ DRX=6 & GNSS NMEA output on[4]		80	mA

Table 25: Current consumption ratings

	Description	Conditions		Typical rating	Unit
I_{BATT+} [1]	Average LTE supply current (FDD)[5] Data transfers measured @ maximum Pout	SLEEP[2] @ "Paging Occasions" = 256	USB disconnected	1.9	mA
			USB suspend	13.5	
		SLEEP[2] @ "Paging Occasions" = 128	USB disconnected	2.3	mA
			USB suspend	13.9	
		SLEEP[2] @ "Paging Occasions" = 64	USB disconnected	2.9	mA
			USB suspend	14.5	
		SLEEP[2] @ "Paging Occasions" = 32	USB disconnected	4.0	mA
			USB suspend	15.2	
		IDLE[3] (UART/USB active, but no communication with the module)	USB disconnected	55	mA
			USB active	65	
		LTE Data transfer Band 1	@ 50Ω	630	mA
			@ total mismatch	790	
		LTE Data transfer Band 2	@ 50Ω	630	mA
			@ total mismatch	880	
		LTE Data transfer Band 3	@ 50Ω	620	mA
			@ total mismatch	690	
		LTE Data transfer Band 4	@ 50Ω	660	mA
			@ total mismatch	750	
		LTE Data transfer Band 5, 18, 19	@ 50Ω	560	mA
			@ total mismatch	590	
		LTE Data transfer Band 7	@ 50Ω	770	mA
			@ total mismatch	800	
		LTE Data transfer Band 8	@ 50Ω	550	mA
			@ total mismatch	600	
		LTE Data transfer Band 12	@ 50Ω	520	mA
			@ total mismatch	590	
		LTE Data transfer Band 20	@ 50Ω	540	mA
			@ total mismatch	620	
		LTE Data transfer Band 26	@ 50Ω	510	mA
			@ total mismatch	570	
		LTE Data transfer Band 28	@ 50Ω	620	mA
			@ total mismatch	690	
		LTE Data transfer Band 66	@ 50Ω	600	mA
			@ total mismatch	680	
I_{BATT+} [1]	Average LTE supply current (FDD) (GNSS on)	LTE active (UART/USB active); IDLE; NMEA output off		110	mA
		LTE active (UART/USB active); IDLE; NMEA output on[4]		110	mA

Table 25: Current consumption ratings

	Description	Conditions		Typical rating	Unit
I_{BATT+} [1]	Average LTE supply current (TDD)[5]	SLEEP[2] @ "Paging Occasions" = 256	USB disconnected	1.9	mA
			USB suspend	13.5	
	Data transfers measured @ maximum Pout	SLEEP[2] @ "Paging Occasions" = 128	USB disconnected	2.3	mA
			USB suspend	13.9	
		SLEEP[2] @ "Paging Occasions" = 64	USB disconnected	2.9	mA
			USB suspend	14.5	
		SLEEP[2] @ "Paging Occasions" = 32	USB disconnected	4.0	mA
			USB suspend	15.2	
		IDLE[3] (UART/USB active, but no communication with the module)	USB disconnected	55	mA
			USB active	65	
		LTE Data transfer Band 38	1 UL / 8 DL	230	mA
			6 UL / 2 DL	490	
		LTE Data transfer Band 39	1 UL / 8 DL	200	mA
			6 UL / 2 DL	410	
		LTE Data transfer Band 40	1 UL / 8 DL	210	mA
			6 UL / 2 DL	430	
		LTE Data transfer Band 41	1 UL / 8 DL	240	mA
			6 UL / 2 DL	530	
	Peak LTE current (TDD)	LTE Band 39	@ 50Ω	480	mA
			@ total mismatch	580	
		LTE Band 38 / 40 / 41	@ 50Ω	640	mA
			@ total mismatch	850	

Table 25: Current consumption ratings

	Description	Conditions		Typical rating	Unit
I_{BATT+} [1]	Average TD-SCDMA supply current (GNSS off) Data transfers measured @ maximum Pout	SLEEP[2] @ DRX=9 (no communication with the module)	USB disconnected	1.6	mA
			USB suspend	13.1	
		SLEEP[2] @ DRX=8 (no communication with the module)	USB disconnected	1.8	mA
			USB suspend	13.3	
		SLEEP[2] @ DRX=6 (no communication with the module)	USB disconnected	2.3	mA
			USB suspend	13.8	
		IDLE[3] (UART/USB active, but no communication with the module)	USB disconnected	60	mA
			USB active	70	
		TD-SCDMA Data transfer Band 34 (Band A)		210	mA
		TD-SCDMA Data transfer Band 39 (Band F)		210	mA
I_{BATT+} [1]	Average TD-SCDMA supply current (GNSS on)	TD-SCDMA active (UART / USB active) IDLE @ DRX=6, NMEA output off		80	mA
		TD-SCDMA active (UART / USB active) IDLE @ DRX=6, NMEA output on[4]		80	
I_{VUSB_IN}	USB typical and maximum ratings are mentioned in Table 4: VUSB_IN.				

1. With an impedance of Z_{LOAD}=50Ω at the antenna pads. Measured at 25°C and 4.2V - except for Power Down ratings that were measured at 3.4V.
2. Measurements start 6 minutes after switching ON the module,
   Averaging times: SLEEP mode - 3 minutes, transfer modes - 1.5 minutes
   Communication tester settings:no neighbor cells, no cell reselection etc,
   RMC (Reference Measurement Channel)
3. The power save mode is disabled via configuration command
4. One fix per second.
5. Communication tester settings:
   - Channel Bandwidth: 5MHz
   - Number of Resource Blocks: 25 (DL), 1 (UL)
   - Modulation: QPSK

4.4.2 Minimizing Power Losses

When designing the power supply for your application please pay specific attention to power losses. Ensure that the input voltage V_{BATT+} never drops below 3.3V on the ALAS5V board, not even in a transmit burst where current consumption can rise to typical peaks of 2A. It should be noted that ALAS5V switches off when exceeding these limits. Any voltage drops that may occur in a transmit burst should not exceed 400mV to ensure the expected RF performance in 2G networks.

The module switches off if the minimum battery voltage (V_{BATT}min) is reached.

Example:
$V_I$min = 3.3V
Dmax = 0.4V

V_{BATT}min = $V_I$min + Dmax
V_{BATT}min = 3.3V + 0.4V = 3.7V

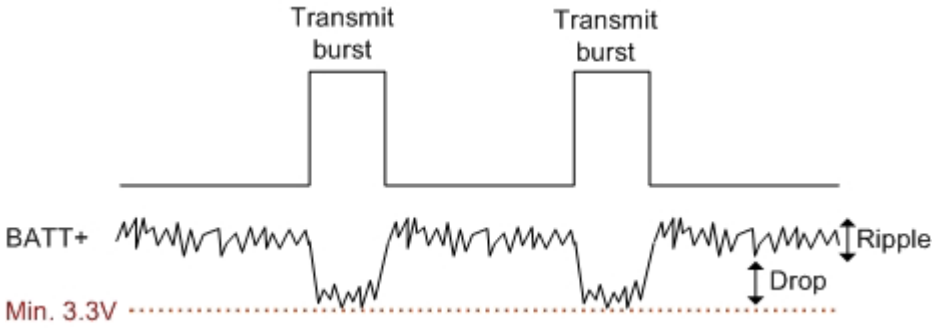


Figure 38: Power supply limits during transmit burst

4.4.3 Monitoring Power Supply by AT Command

To monitor the supply voltage you can use the AT^SBV command which returns the averaged value related to BATT+ and GND at the SMT application interface.

As long as not in SLEEP mode, the module measures the voltage periodically every 110 milliseconds. The maximum time the module remains in SLEEP mode can be limited with a the AT command AT^SCFG="MeOpMode/PwrSave" (see [1]). The displayed voltage (in mV) is an average of the last eight measurement results before the power supply query.

4.5 Operating Temperatures

Table 26: Board temperature

Parameter	Min	Typ	Max	Unit
Operating temperature range	-30	+25	+85	°C
Restricted temperature range[1]	-40		+95	°C
Automatic shutdown[2] Temperature measured on ALAS5V board	<-40	---	>+95	°C

1. Restricted operation allows normal mode data transmissions for limited time until automatic thermal shutdown takes effect. Within the restricted temperature range (outside the operating temperature range) the specified electrical characteristics may be in- or decreased.
2. Due to temperature measurement uncertainty, a tolerance on the stated shutdown thresholds may occur. The possible deviation is in the range of ± 2°C at the overtemperature limit.

See also Section 4.2.4.1 for information about the NTC for on-board temperature measurement, automatic thermal shutdown and alert messages.

Note that within the specified operating temperature ranges the board temperature may vary to a great extent depending on operating mode, used frequency band, radio output power and current supply voltage. Note also the differences and dependencies that usually exist between board (PCB) temperature and ambient temperature as shown in the following Figure 39. The possible ambient temperature range depends on the mechanical application design including the module and the PCB with its size and layout. A thermal solution will have to take these differences into account and should therefore be an integral part of application design.

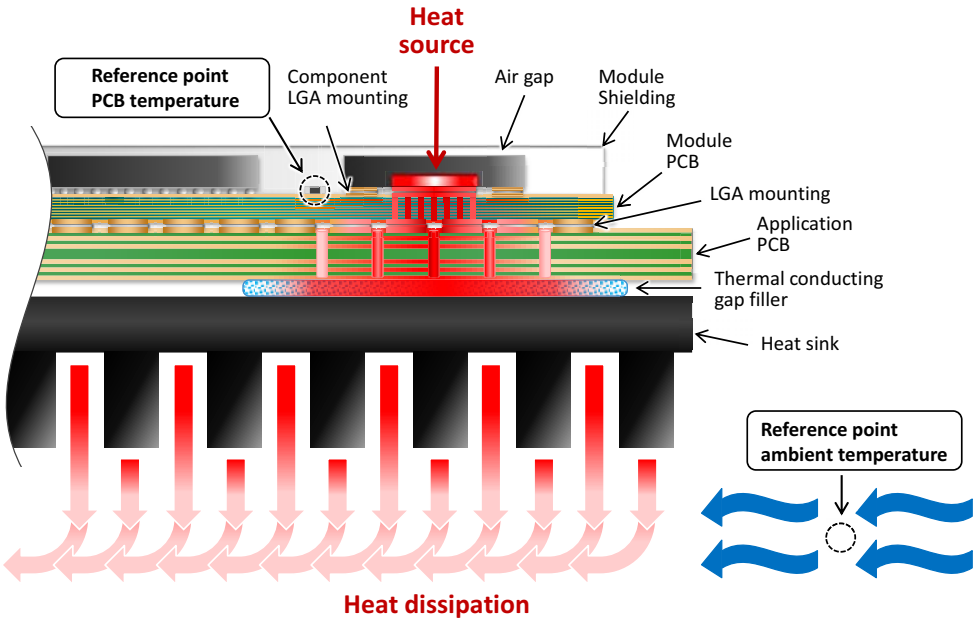


Figure 39: Board and ambient temperature differences

4.6 Electrostatic Discharge

The module is not protected against Electrostatic Discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates a ALAS5V module.

Special ESD protection provided on ALAS5V*:*
BATT+: Inductor/capacitor
An example for an enhanced ESD protection for the SIM interface is shown in Section 2.1.8.

The remaining interfaces of ALAS5V with the exception of the antenna interface are not accessible to the user of the final product (since they are installed within the device) and are therefore only protected according to the ANSI/ESDA/JEDEC JS-001-2011 requirements.

ALAS5V has been tested according to the following standards. Electrostatic values can be gathered from the following table.

Table 27: Electrostatic values

Specification / Requirements	Contact discharge	Air discharge
ANSI/ESDA/JEDEC JS-001-2014		
All SMT interfaces	± 1kV Human Body Model	n.a.
ANSI/ESDA/JEDEC JS-002-2014		
All SMT interfaces	± 250V Charged Device Model (CDM)	n.a.
ETSI EN 301 489-1/7		
Antenna pads	n.a.	± 8kV

Note: The values may vary with the individual application design. For example, it matters whether or not the application platform is grounded over external devices like a computer or other equipment.

4.7 Reliability Characteristics

TBD.

5 Mechanical Dimensions and Mounting

5.1 Mechanical Dimensions of ALAS5V

Figure 40 shows a 3D view[1] of ALAS5V and provides an overview of the board's mechanical dimensions[2]. For further details see Figure 41.

Length: 40mm
Width: 36mm
Height: 3mm

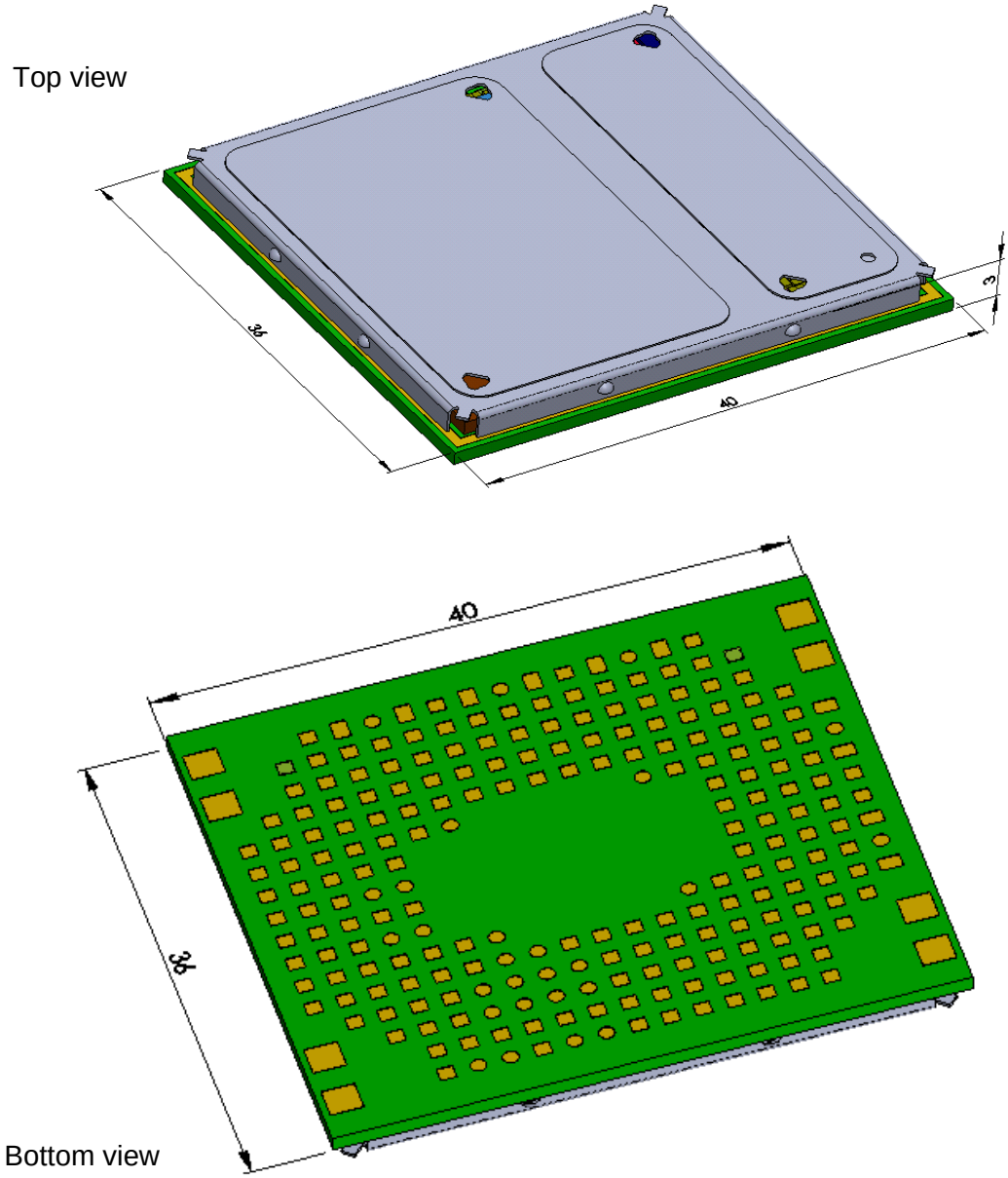


Figure 40: ALAS5V – top and bottom view

1. The coloring of the 3D view does not reflect the module's real color.
2. **Note:** The holes in the shielding (top view) are significantly smaller than the radiated wavelength from the module. Gemalto guarantees that there will be no emissions outside the limits from these. The RF circuitry of the module is fully shielded.

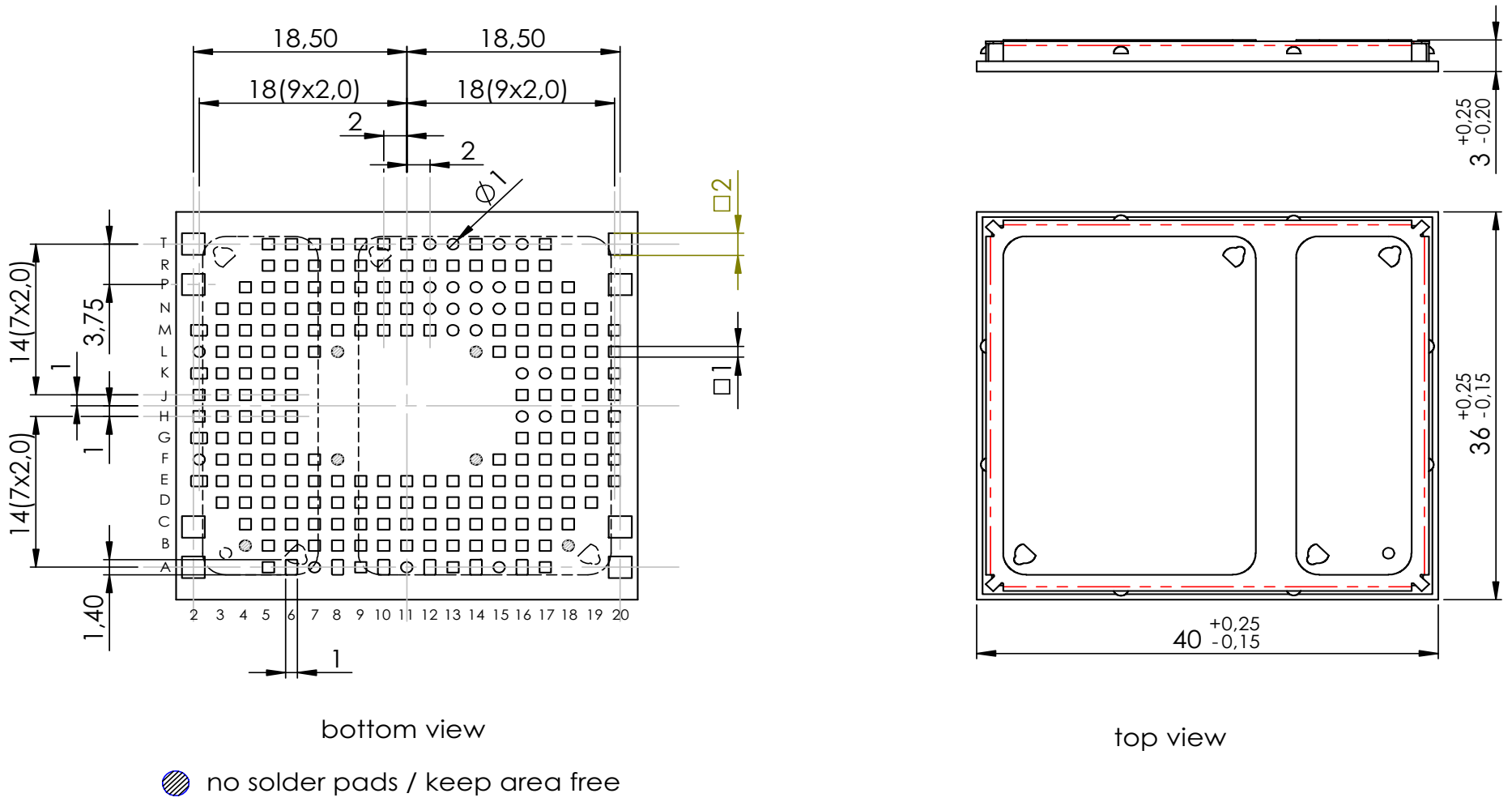


Figure 41: Dimensions of ALAS5V (all dimensions in mm)

5.2 Mounting ALAS5V onto the Application Platform

This section describes how to mount ALAS5V onto the PCBs, including land pattern and stencil design, board-level characterization, soldering conditions, durability and mechanical handling. For more information on issues related to SMT module integration see also [3].

Note: Gemalto strongly recommends to solder all connecting pads for mechanical stability and heat dissipation. Not only must all supply pads and signals be connected appropriately, but all pads denoted as “Do not use“ should also be soldered (but not electrically connected). Note also that in order to avoid short circuits between signal tracks on an external application's PCB and various markings at the bottom side of the module, it is recommended not to route the signal tracks on the top layer of an external PCB directly under the module, or at least to ensure that signal track routes are sufficiently covered with solder resist.

5.2.1 SMT PCB Assembly

5.2.1.1 Land Pattern and Stencil

The land pattern and stencil design as shown below is based on Gemalto M2M characterizations for lead-free solder paste on a four-layer test PCB and a 110 micron-thick stencil.

The land pattern given in Figure 42 reflects the module‘s pad layout, including signal pads and ground pads (for pad assignment see Section 2.1.1). Besides these pads there are ground areas on the module's bottom side that must not be soldered, e.g., the position marker. To prevent short circuits, it has to be ensured that there are no wires on the external application side that may connect to these module ground areas.

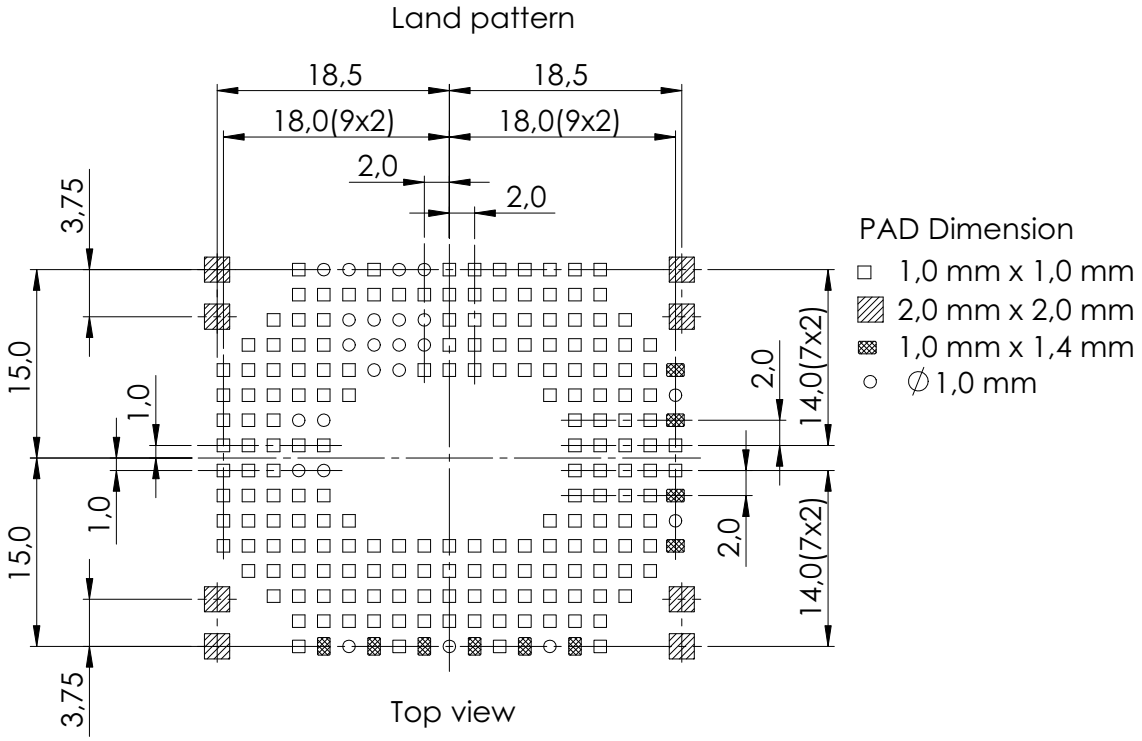


Figure 42: Land pattern (top layer)

The stencil design illustrated in Figure 43 is recommended by Gemalto M2M as a result of extensive tests with Gemalto M2M Daisy Chain modules.

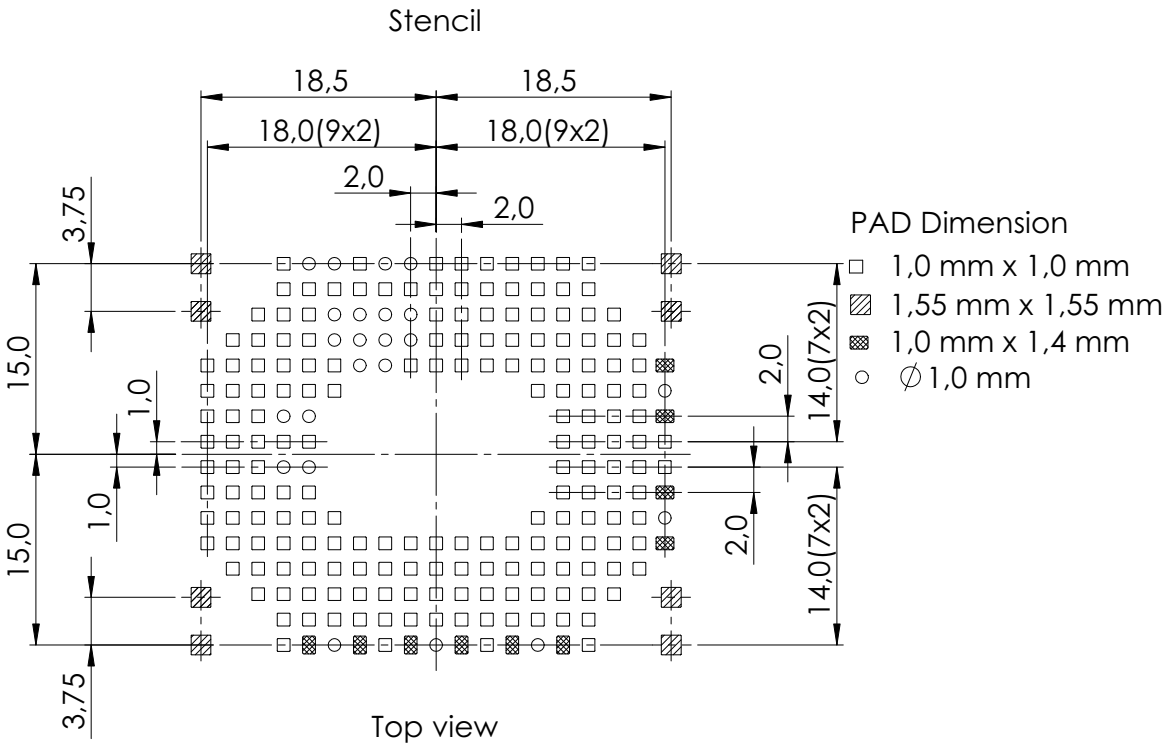


Figure 43: Recommended design for 110 micron thick stencil (top layer)

5.2.1.2 Board Level Characterization

Board level characterization issues should also be taken into account if devising an SMT process.

It is recommended to characterize land patterns before an actual PCB production, taking individual processes, materials, equipment, stencil design, and reflow profile into account. For land and stencil pattern design recommendations see also Section 5.2.1.1. Optimizing the solder stencil pattern design and print process is necessary to ensure print uniformity, to decrease solder voids, and to increase board level reliability.

Daisy chain modules for SMT characterization are available on request. For details refer to [3].

Generally, solder paste manufacturer recommendations for screen printing process parameters and reflow profile conditions should be followed. Maximum ratings are described in Section 5.2.3.

5.2.2 Moisture Sensitivity Level

ALAS5V comprises components that are susceptible to damage induced by absorbed moisture.

Gemalto M2M's ALAS5V module complies with the latest revision of the IPC/JEDEC J-STD-020 Standard for moisture sensitive surface mount devices and is classified as MSL 4.

For additional moisture sensitivity level (MSL) related information see Section 5.2.4.

5.2.3 Soldering Conditions and Temperature

5.2.3.1 Reflow Profile

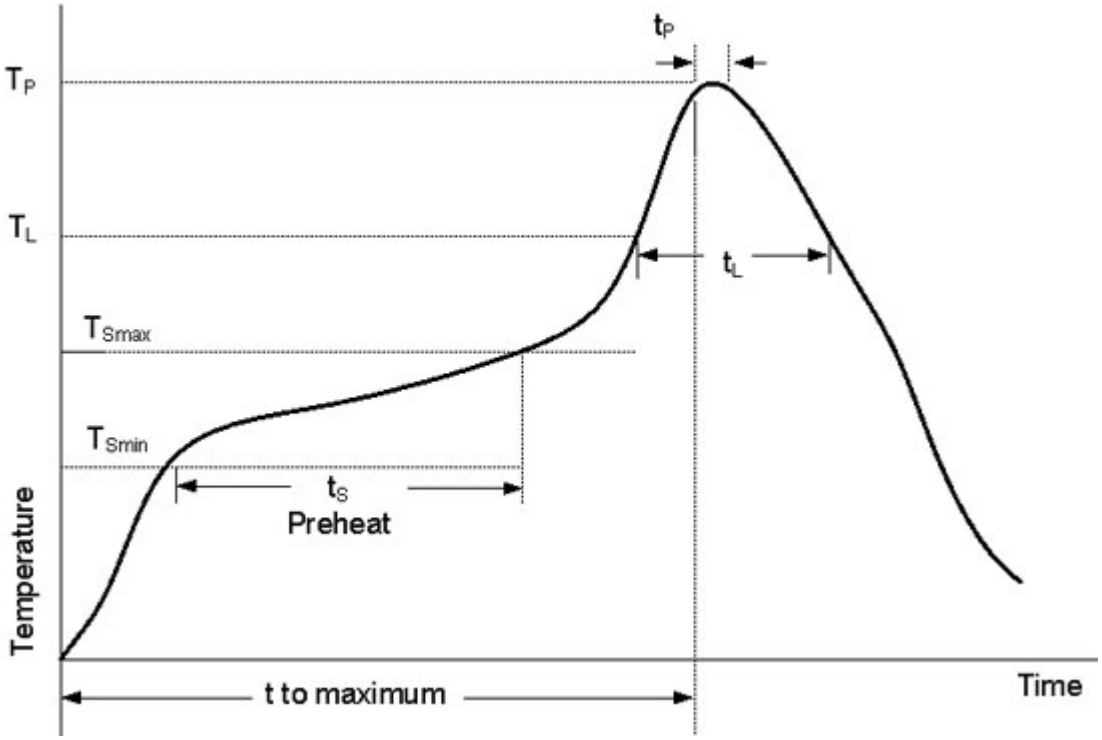
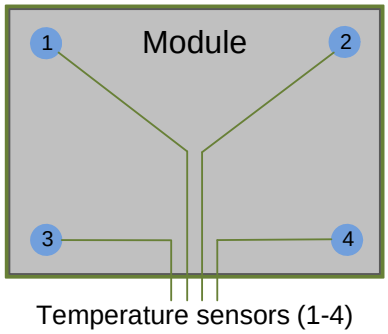


Figure 44: Reflow Profile

Table 28: Reflow temperature recommendations[1]

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature Minimum (T_{Smin}) Temperature Maximum (T_{Smax}) Time (t_{Smin} to t_{Smax}) (t_S)	 150°C 200°C 60-120 seconds
Average ramp up rate (T_L to T_P)	3K/second max. [2]
Liquidous temperature (T_L) Time at liquidous (t_L)	217°C 60-90 seconds
Peak package body temperature (T_P)	245°C +0/-5°C
Time (t_P) within 5 °C of the peak package body temperature (T_P)	30 seconds max.
Average ramp-down rate - Limited ramp-down rate between 225°C and 200°C	6K/second max.[2] 3K/second max.[2]
Time 25°C to maximum temperature	8 minutes max.

1. Please note that the listed reflow profile features and ratings are based on the joint industry standard IPC/JEDEC J-STD-020D.1, and are as such meant as a general guideline. For more information on reflow profiles and their optimization please refer to [3].
2. Temperatures measured on shielding at each corner. See also [3].



Temperature sensors (1-4)

5.2.3.2 Maximum Temperature and Duration

The following limits are recommended for the SMT board-level soldering process to attach the module:

- A maximum module temperature of 245°C. This specifies the temperature as measured at the module's top side.
- A maximum duration of 30 seconds at this temperature.
- Ramp-down rate from T_P to 200°C should be controlled in order to reduce thermally induced stress during the solder solidification phase (see Table 28 - limited ramp-down rate). Therefore, a cool-down step in the oven's temperature program between 200°C and 180°C should be considered. For more information on reflow profiles and their optimization see [3].

Please note that while the solder paste manufacturers' recommendations for best temperature and duration for solder reflow should generally be followed, the limits listed above must not be exceeded.

ALAS5V is specified for one soldering cycle only. Once ALAS5V is removed from the application, the module will very likely be destroyed and cannot be soldered onto another application.

5.2.4 Durability and Mechanical Handling

5.2.4.1 Storage Conditions

ALAS5V modules, as delivered in tape and reel carriers, must be stored in sealed, moisture barrier anti-static bags. The conditions stated below are only valid for modules in their original packed state in weather protected, non-temperature-controlled storage locations. Normal storage time under these conditions is 12 months maximum.

Table 29: Storage conditions

Type		Condition	Unit	Reference
Air temperature:	Low High	-25 +40	°C	IPC/JEDEC J-STD-033A
Humidity relative:	Low High	10 90 at 40°C	%	IPC/JEDEC J-STD-033A
Air pressure:	Low High	70 106	kPa	IEC TR 60271-3-1: 1K4 IEC TR 60271-3-1: 1K4
Movement of surrounding air		1.0	m/s	IEC TR 60271-3-1: 1K4
Water: rain, dripping, icing and frosting		Not allowed	---	---
Radiation:	Solar Heat	1120 600	W/m^2	ETS 300 019-2-1: T1.2, IEC 60068-2-2 Bb ETS 300 019-2-1: T1.2, IEC 60068-2-2 Bb
Chemically active substances		Not recommended		IEC TR 60271-3-1: 1C1L
Mechanically active substances		Not recommended		IEC TR 60271-3-1: 1S1
Vibration sinusoidal: Displacement Acceleration Frequency range		 1.5 5 2-9 9-200	 mm m/s^2 Hz	IEC TR 60271-3-1: 1M2
Shocks: Shock spectrum Duration Acceleration		 Semi-sinusoidal 1 50	 ms m/s^2	IEC 60068-2-27 Ea

5.2.4.2 Processing Life

ALAS5V must be soldered to an application within 72 hours after opening the moisture barrier bag (MBB) it was stored in.

As specified in the IPC/JEDEC J-STD-033 Standard, the manufacturing site processing the modules should have ambient temperatures below 30°C and a relative humidity below 60%.

5.2.4.3 Baking

Baking conditions are specified on the moisture sensitivity label attached to each MBB:

- It is *not necessary* to bake ALAS5V, if the conditions specified in Section 5.2.4.1 and Section 5.2.4.2 were not exceeded.
- It is *necessary* to bake ALAS5V, if any condition specified in Section 5.2.4.1 and Section 5.2.4.2 was exceeded.

If baking is necessary, the modules must be put into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

5.2.4.4 Electrostatic Discharge

Electrostatic discharge (ESD) may lead to irreversible damage for the module. It is therefore advisable to develop measures and methods to counter ESD and to use these to control the electrostatic environment at manufacturing sites.

Please refer to Section 4.6 for further information on electrostatic discharge.

5.3 Packaging

5.3.1 Trays

ALAS5V is shipped in 6x3 trays as illustrated in Figure 45.

The figure also shows the proper module orientation in the trays: The small round hole marking pad A1 is furthest away from the beveled corner of the tray.

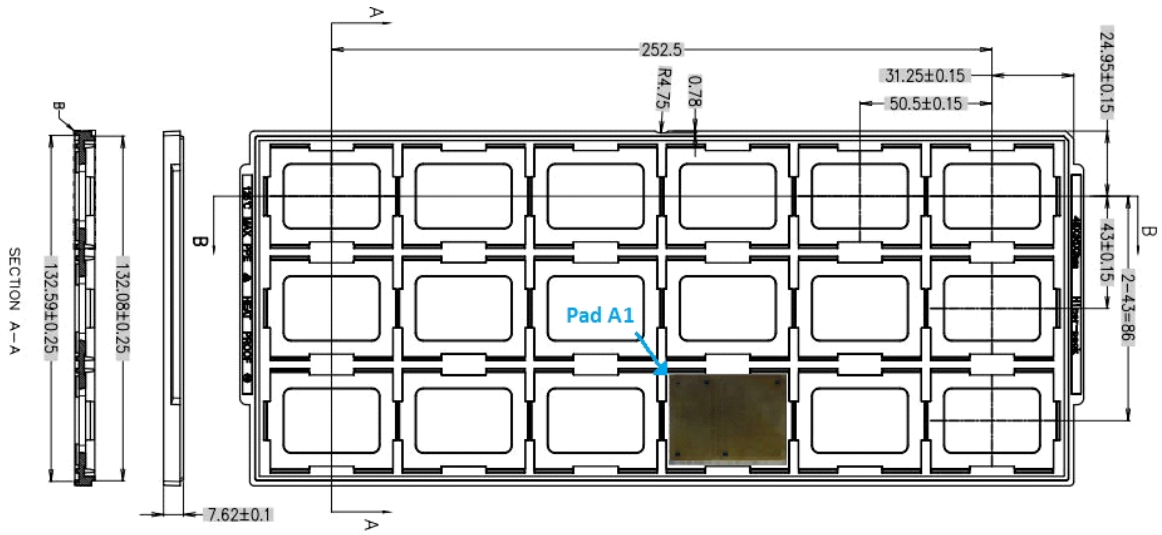


Figure 45: Shipping tray dimensions

5.3.2 Shipping Materials

The shipping trays are normally stacked as units of 10 trays plus one extra as a cover, and secured with packaging tape. All trays have the beveled corner aligned in the same orientation. A stacking unit (10 x 18 modules = 180 modules) together with a foam protection makes up the content of a moisture barrier bag (MBB).

5.3.2.1 Moisture Barrier Bag

The foam protected stacking units are stored inside of a MBB, together with a humidity indicator card and desiccant pouches. The bag is ESD protected and delimits moisture transmission. It is vacuum-sealed and should be handled carefully to avoid puncturing or tearing. The bag protects the ALAS5V modules from moisture exposure. It should not be opened until the devices are ready to be soldered onto the application.

The label shown in Figure 46 summarizes requirements regarding moisture sensitivity, including shelf life and baking requirements. It is attached to the outside of the moisture barrier bag.

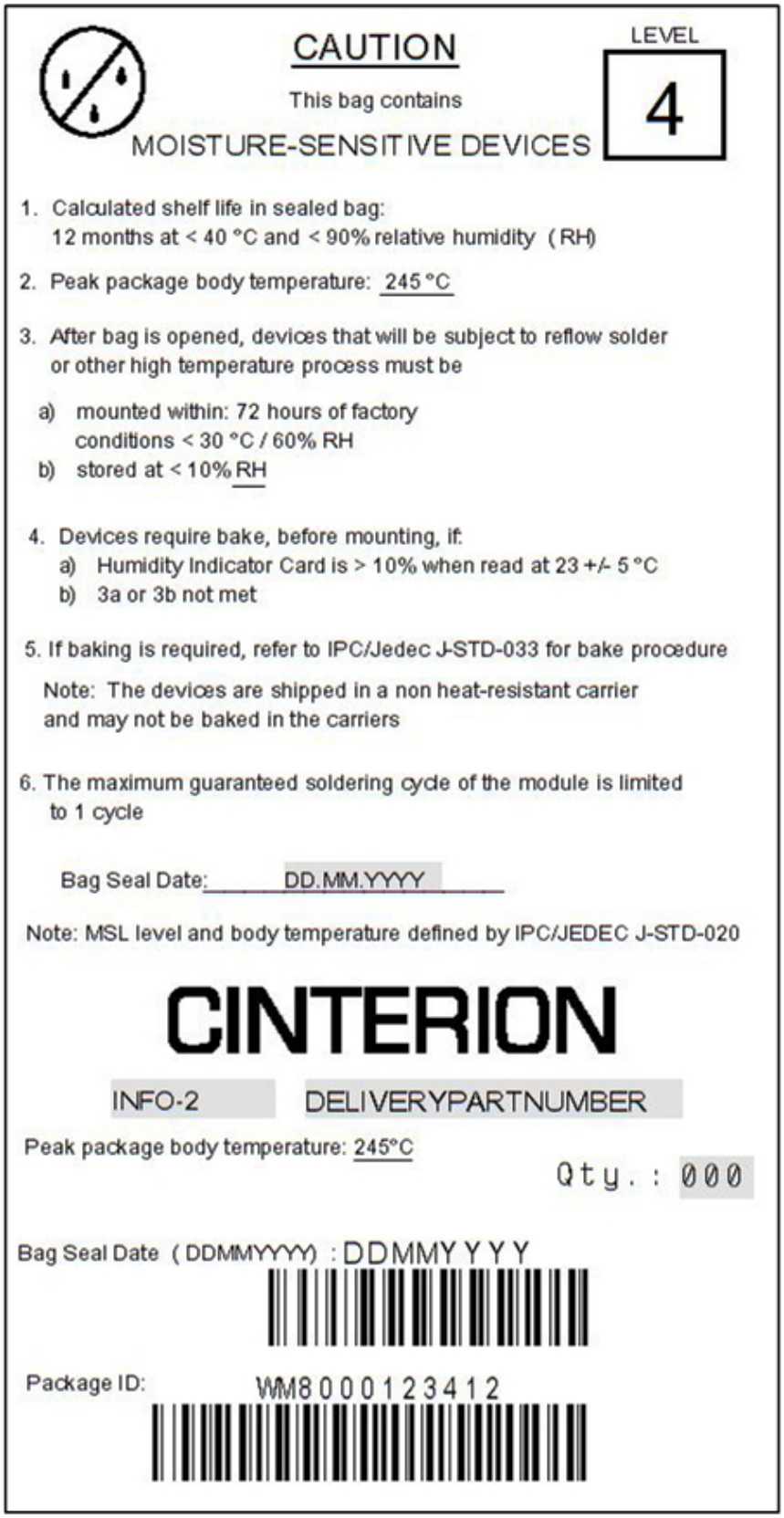


Figure 46: Moisture Sensitivity Label

MBBs contains two desiccant pouches to absorb moisture that may be in the bag. The humidity indicator card described below should be used to determine whether the enclosed components have absorbed an excessive amount of moisture.

The desiccant pouches should not be baked or reused once removed from the MBB.

The humidity indicator card is a moisture indicator and is included in the MBB to show the approximate relative humidity level within the bag. A sample humidity card is shown in Figure 47. If the components have been exposed to moisture above the recommended limits, the units will have to be rebaked.

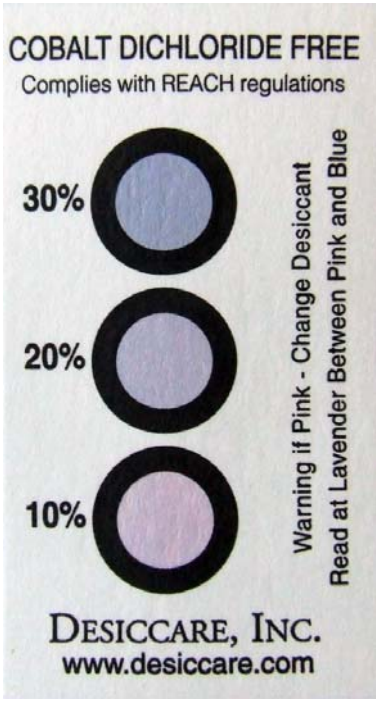


Figure 47: Humidity Indicator Card - HIC

A baking is required if the humidity indicator inside the bag indicates 10% RH or more.

5.3.2.2 Transportation Boxes

Stacked tray units are distributed in over boxes, so-called VP boxes, containing up to two MBBs. Thus, a VP box may contain up to 360 (180x2) modules.

The VP boxes in turn may be placed in master boxes for up to two layers with six VP boxes. Thus, a master box packaging unit may contain up to 4320 (180x2x12) modules.

6 Regulatory and Type Approval Information

6.1 Directives and Standards

ALAS5V has been designed to comply with the directives and standards listed below.

It is the responsibility of the application manufacturer to ensure compliance of the final product with all provisions of the applicable directives and standards as well as with the technical specifications provided in the "ALAS5V Hardware Interface Description".[1]

Table 30: Directives

2014/53/EU	Directive of the European Parliament and of the council of 16 April 2014 on the harmonization of the laws of the Member States relating to the making available on the market of radio equipment and repealing Directive 1999/05/EC. The product is labeled with the CE conformity mark.
2002/95/EC (RoHS 1) 2011/65/EC (RoHS 2) 2015/863/EU (RoHS 3)	Directive of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS) Revised on 8 June 2011. Further revision on 31 March 2015 - amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances.

Table 31: Standards of North American type approval[1]

CFR Title 47	Code of Federal Regulations, Part 22, Part 24, Part 27, and Part 90; US Equipment Authorization FCC
OET Bulletin 65 (Edition 97-01)	Evaluating Compliance with FCC Guidelines for Human Exposure to Radiofrequency Electromagnetic Fields
UL 60 950-1	Product Safety Certification (Safety requirements)
NAPRD.03 V5.35	Overview of PCS Type certification review board Mobile Equipment Type Certification and IMEI control PCS Type Certification Review board (PTCRB)
RSS132, RSS133, RSS139	Canadian Standard

1. Standards apply to ALAS5V-W and ALAS5V-US only.

1. Manufacturers of applications which can be used in the US shall ensure that their applications have a PTCRB approval. For this purpose they can refer to the PTCRB approval of the respective module.

Table 32: Standards of European type approval

3GPP TS 51.010-1	Digital cellular telecommunications system (Release 7); Mobile Station (MS) conformance specification;
ETSI EN 301 511 V12.5.1	Global System for Mobile communications (GSM); Mobile Stations (MS) equipment; Harmonized Standard covering the essential requirements of article 3.2 of Directive 2014/53/EU
GCF-CC V3.70	Global Certification Forum - Certification Criteria
ETSI EN 301 489-01 V2.1.1	Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements; Harmonized Standard covering the essential requirements of article 3.1(b) of Directive 2014/53/EU and the essential requirements of article 6 of Directive 2014/30/EU
Draft ETSI EN 301 489-52 V1.1.0	Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 52: Specific conditions for Cellular Communication Mobile and portable (UE) radio and ancillary equipment; Harmonized Standard covering the essential requirements of article 3.1(b) of Directive 2014/53/EU
ETSI EN 301 908-01 V11.1.1	IMT cellular networks; Harmonized Standard covering the essential requirements of article 3.2 of the Directive 2014/53/EU; Part 1: Introduction and common requirements
ETSI EN 301 908-02 V11.1.1	IMT cellular networks; Harmonized Standard covering the essential requirements of article 3.2 of the Directive 2014/53/EU; Part 2: CDMA Direct Spread (UTRA FDD) User Equipment (UE)
ETSI EN 301 908-13 V11.1.1	IMT cellular networks; Harmonized Standard covering the essential requirements of article 3.2 of the Directive 2014/53/EU; Part 13: Evolved Universal Terrestrial Radio Access (E-UTRA) User Equipment (UE)
EN 60950-1:2006/ A11:2009+A1:2010+A12:2011+A2:2013	Safety of information technology equipment

Table 33: Requirements of quality

IEC 60068	Environmental testing
DIN EN 60529	IP codes

Table 34: Standards of the Ministry of Information Industry of the People's Republic of China

SJ/T 11363-2006	"Requirements for Concentration Limits for Certain Hazardous Substances in Electronic Information Products" (2006-06).
SJ/T 11364-2006	"Marking for Control of Pollution Caused by Electronic Information Products" (2006-06).  According to the "Chinese Administration on the Control of Pollution caused by Electronic Information Products" (ACPEIP) the EPUP, i.e., Environmental Protection Use Period, of this product is 20 years as per the symbol shown here, unless otherwise marked. The EPUP is valid only as long as the product is operated within the operating limits described in the Hardware Interface Description. Please see Table 35 for an overview of toxic or hazardous substances or elements that might be contained in product parts in concentrations above the limits defined by SJ/T 11363-2006.

Table 35: Toxic or hazardous substances or elements with defined concentration limits

部件名称 Name of the part	有毒有害物质或元素 Hazardous substances					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
金属部件 (Metal Parts)	O	O	O	O	O	O
电路模块 (Circuit Modules)	X	O	O	O	O	O
电缆及电缆组件 (Cables and Cable Assemblies)	O	O	O	O	O	O
塑料和聚合物部件 (Plastic and Polymeric parts)	O	O	O	O	O	O

O:
表示该有毒有害物质在该部件所有均质材料中的含量均在SJ/T11363-2006 标准规定的限量要求以下。
Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.

X:
表示该有毒有害物质至少在该部件的某一均质材料中的含量超出SJ/T11363-2006标准规定的限量要求。
Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part *might exceed* the limit requirement in SJ/T11363-2006.

6.2 SAR requirements specific to portable mobiles

Mobile phones, PDAs or other portable transmitters and receivers incorporating a GSM module must be in accordance with the guidelines for human exposure to radio frequency energy. This requires the Specific Absorption Rate (SAR) of portable ALAS5V based applications to be evaluated and approved for compliance with national and/or international regulations.

Since the SAR value varies significantly with the individual product design manufacturers are advised to submit their product for approval if designed for portable use. For US and European markets the relevant directives are mentioned below. It is the responsibility of the manufacturer of the final product to verify whether or not further standards, recommendations or directives are in force outside these areas.

Products intended for sale on US markets

ES 59005/ANSI C95.1	Considerations for evaluation of human exposure to electromagnetic fields (EMFs) from mobile telecommunication equipment (MTE) in the frequency range 30MHz - 6GHz

Products intended for sale on European markets

EN 50360	Product standard to demonstrate the compliance of mobile phones with the basic restrictions related to human exposure to electromagnetic fields (300MHz - 3GHz)
EN 62311:2008	Assessment of electronic and electrical equipment related to human exposure restrictions for electromagnetic fields (0 Hz - 300 GHz)

IMPORTANT:
Manufacturers of portable applications based on ALAS5V modules are required to have their final product certified and apply for their own FCC Grant and Industry Canada Certificate related to the specific portable mobile.

6.3 Reference Equipment for Type Approval

The Gemalto M2M general reference setup submitted to type approve ALAS5V is shown in the figure below: Figure 48 illustrates the setup for general tests and evaluation purposes. The evaluation module can be plugged directly onto the so-called “Audio(-Ethernet) Adapter”. The GSM/UMTS/LTE as well as the GNSS test equipment is connected via antennas at the SMA connectors on the evaluation module[1]. The PC is connected via USB interface on the evaluation module, and the audio test equipment via audio jack on the Audio(-Ethernet) Adapter.

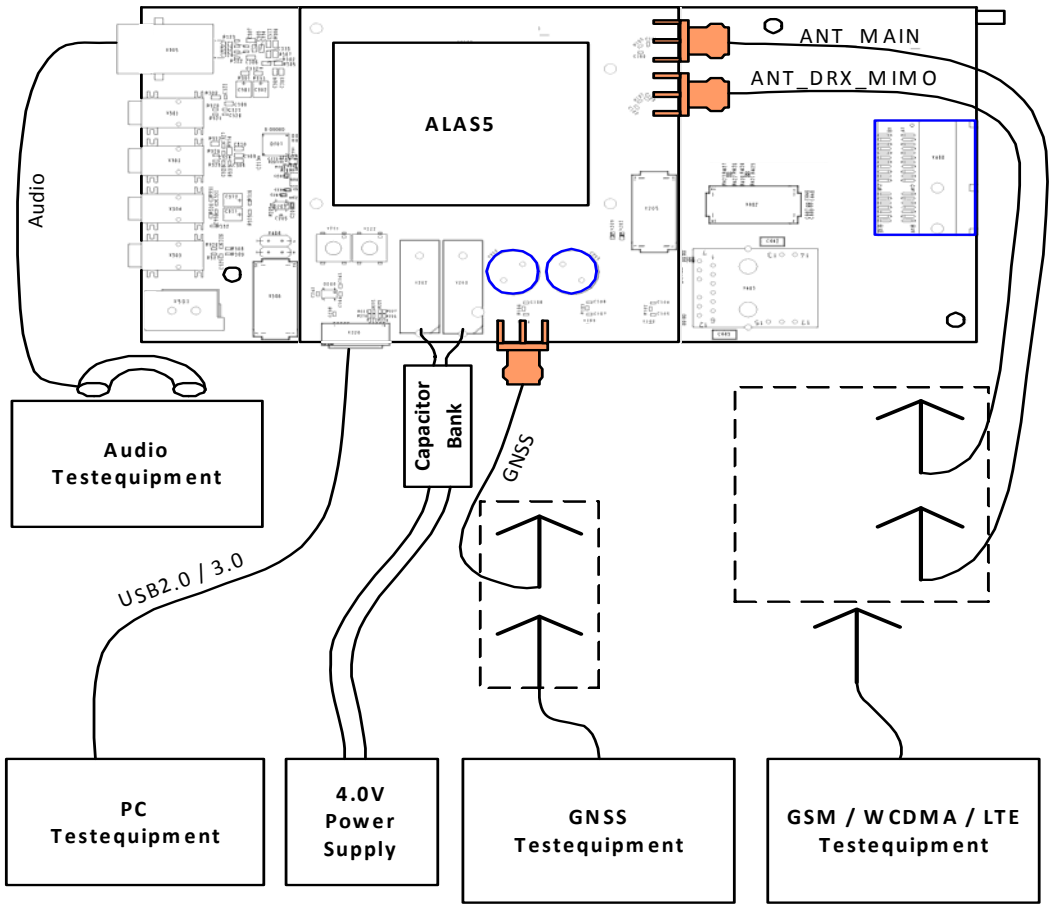


Figure 48: Reference equipment for type approval

Please note that for EMC and RF performance tests, slightly different reference equipment configurations are used. If necessary, please contact Gemalto for further details.

1. The following antennas were used with the approval reference equipment:
   - RF antennas: LPBEM-7-27 (for details see www.panorama-antennas.com)
   - GNSS antenna: AA.162.301111 (for details see www.taoglas.com)

6.4 Compliance with FCC and ISED Rules and Regulations

The Equipment Authorization Certification for the Gemalto M2M modules reference application described in Section 6.3 will be registered under the following identifiers:

- ALAS5V-W:
  FCC Identifier QIPALAS5V-W
  Granted to Gemalto M2M GmbH

- ALAS5V-US:
  FCC Identifier QIPALAS5V-US
  ISED Certification Number: 7830A-ALAS5VUS
  Granted to Gemalto M2M GmbH

Note[1]: Manufacturers of mobile or fixed devices incorporating ALAS5V-W/*-US* modules are authorized to use the FCC Grants and ISED Certificates of the ALAS5V-W modules for their own final products according to the conditions referenced in these documents. In this case, the FCC label of the module shall be visible from the outside, or the host device shall bear a second label stating "Contains FCC ID: QIPALAS5V-W"or "Contains FCC ID: QIPALAS5V-US", and accordingly “Contains IC: 7830A-ALAS5VUS“. The integration is limited to fixed or mobile categorized host devices, where a separation distance between the antenna and any person of min. 20cm can be assured during normal operating conditions.

For mobile and fixed operation configurations the antenna gain, including cable loss, must not exceed the limits listed in the following Table 36 and Table 37 for FCC and/or ISED.

Table 36: Antenna gain limits for FCC for ALAS5V-W (TBD.)

Maximum gain in operating band	FCC limit	Unit
850MHz (GSM)		dBi
1900MHZ (GSM)		dBi
Band V (UMTS)		dBi
Band 5 (LTE-FDD)		dBi
Band 7 (LTE-FDD)		dBi
Band 26 (LTE-FDD)		dBi

1. Label note in French for ISED: Les fabricants d'équipement mobile ou fixe intégrant le module ALAS66A-W/-US sont autorisés à utiliser les accords FCC et certificats d'Innovation, Sciences et Développement économique Canada (ISED) du module ALAS5V-W/-US pour leur propre produit final suivant les conditions référencées dans ces documents. Dans ce cas, le label FCC du module doit être visible de l'extérieur, sinon l'équipement hôte doit disposer d'un second label avec la déclaration suivante " Contains FCC ID : QIPALALAS5V-W ", ou " Contains FCC ID : QIPALALAS5V-US " et en conséquence " Contains IC : 7830A-ALAS5VUS ". L'intégration est limitée aux catégories d'équipement hôte mobile ou fixe, respectant une distance minimum de 20 centimètres entre l'antenne et toute personne avoisinante pour des conditions d'utilisation normale.

Table 37: Antenna gain limits for FCC and ISED for ALAS5V-US (TBD.)

Maximum gain in operating band	FCC limit	ISED limit	Unit
850MHz (GSM)			dBi
1900MHZ (GSM)			dBi
Band II (UMTS)			dBi
Band IV (UMTS)			dBi
Band V (UMTS)			dBi
Band 2 (LTE-FDD)			dBi
Band 4 (LTE-FDD)			dBi
Band 5 (LTE-FDD)			dBi
Band 7 (LTE-FDD)			dBi
Band 12 (LTE-FDD)			dBi
Band 66(LTE-FDD)			dBi

IMPORTANT:
Manufacturers of portable applications incorporating ALAS5V-W/-US modules are required to have their final product certified and apply for their own FCC Grant and ISED Certificate related to the specific portable mobile. This is mandatory to meet the SAR requirements for portable mobiles (see Section 6.2 for detail).

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules and with ISED license-exempt RSS standard(s). These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This Class B digital apparatus complies with Canadian ICES-003.

If Canadian approval is requested for devices incorporating ALAS5V modules the above note will have to be provided in the English and French language in the final user documentation. Manufacturers/OEM Integrators must ensure that the final user documentation does not contain any information on how to install or remove the module from the final product.

Notes (ISED):
(EN) This Class B digital apparatus complies with Canadian ICES-003 and RSS-210. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

(FR) Cet appareil numérique de classe B est conforme aux normes canadiennes ICES-003 et RSS-210. Son fonctionnement est soumis aux deux conditions suivantes: (1) cet appareil ne doit pas causer d'interférence et (2) cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement.

(EN) Radio frequency (RF) Exposure Information
The radiated output power of the Wireless Device is below the Industry Canada (IC) radio frequency exposure limits. The Wireless Device should be used in such a manner such that the potential for human contact during normal operation is minimized.
This device has also been evaluated and shown compliant with the IC RF Exposure limits under mobile exposure conditions. (antennas are greater than 20cm from a person‘s body).

(FR) Informations concernant l'exposltion aux fréquences radio (RF)
La puissance de sortie émise par l'appareil de sans fiI est inférieure à la limite d'exposition aux fréquences radio d‘Innovation, Sciences et Développement économique Canada (ISDE). Utilisez l'appareil de sans fil de façon à minimiser les contacts humains lors du fonctionnement normal.
Ce périphérique a également été évalué et démontré conforme aux limites d'exposition aux RF d'ISDE dans des conditions d'exposition à des appareils mobiles (les antennes se situent à moins de 20cm du corps d'une personne).

7 Document Information

7.1 Revision History

Preceding document: "Cinterion® ALAS5V Hardware Interface Description" v00.030
New document: "Cinterion® ALAS5V Hardware Interface Description" v**00.030a**

Chapter	What is new
Throughout document	Defined GPIO6 as interrupt enabled.
1.2	Added TD-SCDMA to Table 1, removed “Uplink CA” from Table 2.
1.3	Revised Figure 1.
2.1.2	Revised/Added some signal characteristics.
2.1.9	Added note to Table 8 and Table 9 for BCLK2 signal and power saving mode.
2.2.1	Updated Table 13 listing antenna interface specifications.
3.1	Completed Table 19 listing GNSS properties.
4.4.1	Updated Table 25 listing current consumption ratings.
4.6	Added ESD values.
5.2.3	Added recommendations for soldering conditions.
5.1	Added note to Figure 40.
5.3	New section Packaging.
6.1	Added Table 31 listing standards of North American type approval.
6.2	Revised section to include US markets.
6.3	Added RF and GNSS antennas used with the approval reference equipment.
6.4	New section Compliance with FCC and ISED Rules and Regulations.
8.1	Added ordering information for ALAS5V-US CIMEI product variant.

Preceding document: "Cinterion® ALAS5V Hardware Interface Description" v00.022
New document: "Cinterion® ALAS5V Hardware Interface Description" v00.030

Chapter	What is new
--	Updated version number only.

Preceding document: "Cinterion® ALAS5V Hardware Interface Description" v00.018
New document: "Cinterion® ALAS5V Hardware Interface Description" v00.022

Chapter	What is new
6.3	Reinstated section.

Preceding document: "Cinterion® ALAS5V Hardware Interface Description" v00.014
New document: "Cinterion® ALAS5V Hardware Interface Description" v00.018

Chapter	What is new
Throughout document	Added ASC2 (RXD2/TXD2 lines) serial interface as debug interface including test point recommendation. Removed support for LTE-TDD Band 41 (for ALAS5V-W). Removed support for second I^2C interface (I2CDAT2, I2CCLK2).
2.1.2	Revised test point requirements/recommendations for various interface lines.
2.1.7	Revised connecting circuit for voltage suppressor shown in Figure 11.
4.2.3.1	Added notes to Figure 29.

Preceding document: "Cinterion® ALAS5V Hardware Interface Description" v00.012
New document: "Cinterion® ALAS5V Hardware Interface Description" v00.014

Chapter	What is new
1.2.1	Revised Table 1 listing supported frequency bands, and added note regarding Bd41.
1.2.2	New section Supported CA Configurations.
4.2.1	Clarified remark on startup timing.
4.2.2	Added signal states after startup, and revised timings.
5.2.4.1	Added air temperature as storage condition.
6.3	Set section to TBD.
8.1	Updated ordering information.

Preceding document: "Cinterion® ALAS5V Hardware Interface Description" v00.006
New document: "Cinterion® ALAS5V Hardware Interface Description" v00.012

Chapter	What is new
Throughout document	Removed mention of RING0 as line with possible remote wakeup functionality.
2.1.2	Added accuracy for ADCx_IN lines.
3	Revised information about the Dead Reckoning Sync Line.
4.2.3.5	New section Overall Shutdown Sequence.
4.2.4.1	Revised description of undertemperature shutdown URC.

New document: "Cinterion® ALAS5V Hardware Interface Description" v00.006

Chapter	What is new
--	Initial document setup.

7.2 Related Documents

[1] ALAS5V AT Command Set
[2] ALAS5V Release Note
[3] Application Note 48: SMT Module Integration
[4] Universal Serial Bus Specification Revision 3.0
[5] Universal Serial Bus Specification Revision 2.0

7.3 Terms and Abbreviations

Abbreviation	Description
ANSI	American National Standards Institute
ARP	Antenna Reference Point
CA	Carrier Aggregation
CE	Conformité Européene (European Conformity)
CS	Coding Scheme
CS	Circuit Switched
CSD	Circuit Switched Data
DL	Download
dnu	Do not use
DRX	Discontinuous Reception
DSB	Development Support Board
DTX	Discontinuous Transmission
EDGE	Enhanced Data rates for GSM Evolution
EGSM	Extended GSM
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission (U.S.)
FDD	Frequency Division Duplex
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HiZ	High Impedance
HSDPA	High Speed Downlink Packet Access
I/O	Input/Output
IMEI	International Mobile Equipment Identity
ISO	International Standards Organization

Abbreviation	Description
ITU	International Telecommunications Union
kbps	kbits per second
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long term evolution
MBB	Moisture barrier bag
Mbps	Mbits per second
MCS	Modulation and Coding Scheme
MIMO	Multiple Input Multiple Output
MLCC	Multi Layer Ceramic Capacitor
eMMC	Embedded MultiMediaCard
MO	Mobile Originated
MS	Mobile Station, also referred to as TE
MSL	Moisture Sensitivity Level
MT	Mobile Terminated
nc	Not connected
NTC	Negative Temperature Coefficient
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCL	Power Control Level
PD	Pull Down resistor
PDU	Protocol Data Unit
PS	Packet Switched
PSK	Phase Shift Keying
PU	Pull Up resistor
QAM	Quadrature Amplitude Modulation
R&TTE	Radio and Telecommunication Terminal Equipment
RF	Radio Frequency
rfu	Reserved for future use
ROPR	Radio Output Power Reduction
RTC	Real Time Clock
Rx	Receive Direction
SAR	Specific Absorption Rate
SELV	Safety Extra Low Voltage
SIM	Subscriber Identification Module
SMD	Surface Mount Device

Abbreviation	Description
SMS	Short Message Service
SMT	Surface Mount Technology
SRAM	Static Random Access Memory
SRB	Signalling Radio Bearer
TE	Terminal Equipment
TPC	Transmit Power Control
TS	Technical Specification
Tx	Transmit Direction
UL	Upload
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
UICC	USIM Integrated Circuit Card
USIM	UMTS Subscriber Identification Module
WCDMA	Wideband Code Division Multiple Access

7.4 Safety Precaution Notes

The following safety precautions must be observed during all phases of the operation, usage, service or repair of any cellular terminal or mobile incorporating ALAS5V. Manufacturers of the cellular terminal are advised to convey the following safety information to users and operating personnel and to incorporate these guidelines into all manuals supplied with the product. Failure to comply with these precautions violates safety standards of design, manufacture and intended use of the product. Gemalto M2M assumes no liability for customer's failure to comply with these precautions.

	When in a hospital or other health care facility, observe the restrictions on the use of mobiles. Switch the cellular terminal or mobile off, if instructed to do so by the guidelines posted in sensitive areas. Medical equipment may be sensitive to RF energy. The operation of cardiac pacemakers, other implanted medical equipment and hearing aids can be affected by interference from cellular terminals or mobiles placed close to the device. If in doubt about potential danger, contact the physician or the manufacturer of the device to verify that the equipment is properly shielded. Pacemaker patients are advised to keep their hand-held mobile away from the pacemaker, while it is on.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it cannot be switched on inadvertently. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communications systems. Failure to observe these instructions may lead to the suspension or denial of cellular services to the offender, legal action, or both.
	Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard.
	Your cellular terminal or mobile receives and transmits radio frequency energy while switched on. Remember that interference can occur if it is used close to TV sets, radios, computers or inadequately shielded equipment. Follow any special regulations and always switch off the cellular terminal or mobile wherever forbidden, or when you suspect that it may cause interference or danger.
	IMPORTANT! Cellular terminals or mobiles operate using radio signals and cellular networks. Because of this, connection cannot be guaranteed at all times under all conditions. Therefore, you should never rely solely upon any wireless device for essential communications, for example emergency calls. Remember, in order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength. Some networks do not allow for emergency calls if certain network services or phone features are in use (e.g. lock functions, fixed dialing etc.). You may need to deactivate those features before you can make an emergency call. Some networks require that a valid SIM card be properly inserted in the cellular terminal or mobile.

8 Appendix

8.1 List of Parts and Accessories

Table 38: List of parts and accessories

Description	Supplier	Ordering information
ALAS5V	Gemalto M2M	Standard module Gemalto M2M IMEI: Packaging unit (ordering) number: L30960-N5900-A100 (ALAS5V-W) L30960-N5910-A100 (ALAS5V-E) L30960-N5920-A100 (ALAS5V-CN) L30960-N5930-A100 (ALAS5V-US) Module label number: L30960-N5900-A100-1[1] (ALAS5V-W) L30960-N5910-A100-1[1] (ALAS5V-E) L30960-N5920-A100-1[1] (ALAS5V-CN) L30960-N5930-A100-1[1] (ALAS5V-US) Customer IMEI module: Packaging unit (ordering) number: L30960-N5935-A100 (ALAS5V-US) Module label number: L30960-N5935-A100-1[1] (ALAS5V-US)
ALAS5V Evaluation module	Gemalto M2M	Ordering number: L30960-N5901-A100 (ALAS5V-W) L30960-N5911-A100 (ALAS5V-E) L30960-N5921-A100 (ALAS5V-CN) L30960-N5931-A100 (ALAS5V-US)
Votronic Handset	VOTRONIC / Gemalto M2M	Votronic ordering number: HH-SI-30.3/V1.1/0 Votronic Entwicklungs- und Produktionsgesellschaft für elektronische Geräte mbH Saarbrücker Str. 8 66386 St. Ingbert Germany Phone: +49-(0)6 89 4 / 92 55-0 Fax: +49-(0)6 89 4 / 92 55-88 Email: contact@votronic.com
SIM card holder incl. push button ejector and slide-in tray	Molex	Ordering numbers: 91228 91236 Sales contacts are listed in Table 39.
U.FL antenna connector	Molex or Hirose	Sales contacts are listed in Table 39 and Table 40.

1. Note: At the discretion of Gemalto M2M, module label information can either be laser engraved on the module's shielding or be printed on a label adhered to the module's shielding.

Table 39: Molex sales contacts (subject to change)

Molex For further information please click: http://www.molex.com	Molex Deutschland GmbH Otto-Hahn-Str. 1b 69190 Walldorf Germany Phone: +49-6227-3091-0 Fax: +49-6227-3091-8100 Email: mxgermany@molex.com	American Headquarters Lisle, Illinois 60532 U.S.A. Phone: +1-800-78MOLEX Fax: +1-630-969-1352
Molex China Distributors Beijing, Room 1311, Tower B, COFCO Plaza No. 8, Jian Guo Men Nei Street, 100005 Beijing P.R. China Phone: +86-10-6526-9628 Fax: +86-10-6526-9730	Molex Singapore Pte. Ltd. 110, International Road Jurong Town, Singapore 629174 Phone: +65-6-268-6868 Fax: +65-6-265-6044	Molex Japan Co. Ltd. 1-5-4 Fukami-Higashi, Yamato-City, Kanagawa, 242-8585 Japan Phone: +81-46-265-2325 Fax: +81-46-265-2365

Table 40: Hirose sales contacts (subject to change)

Hirose Ltd. For further information please click: http://www.hirose.com	Hirose Electric (U.S.A.) Inc 2688 Westhills Court Simi Valley, CA 93065 U.S.A. Phone: +1-805-522-7958 Fax: +1-805-522-3217	Hirose Electric Europe B.V. German Branch: Herzog-Carl-Strasse 4 73760 Ostfildern Germany Phone: +49-711-456002-1 Fax: +49-711-456002-299 Email: info@hirose.de
Hirose Electric Europe B.V. UK Branch: First Floor, St. Andrews House, Caldecotte Lake Business Park, Milton Keynes MK7 8LE Great Britain Phone: +44-1908-369060 Fax: +44-1908-369078	Hirose Electric Co., Ltd. 5-23, Osaki 5 Chome, Shinagawa-Ku Tokyo 141 Japan Phone: +81-03-3491-9741 Fax: +81-03-3493-2933	Hirose Electric Europe B.V. Hogehillweg 8 1101 CC Amsterdam Z-O Netherlands Phone: +31-20-6557-460 Fax: +31-20-6557-469

About Gemalto

Since 1996, Gemalto has been pioneering groundbreaking M2M and IoT products that keep our customers on the leading edge of innovation.

We work closely with global mobile network operators to ensure that Cinterion® modules evolve in sync with wireless networks, providing a seamless migration path to protect your IoT technology investment.

Cinterion products integrate seamlessly with Gemalto identity modules, security solutions and licensing and monetization solutions, to streamline development timelines and provide cost efficiencies that improve the bottom line.

As an experienced software provider, we help customers manage connectivity, security and quality of service for the long lifecycle of IoT solutions.

For more information please visit
www.gemalto.com/m2m, www.facebook.com/gemalto, or Follow@gemaltoIoT on Twitter.

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security to be free