DISTANCE RELAYS, FAULT LOCATORS AND THEIR DESIGN USING ANALOG/DIGITAL CIRCUITS

A DISSERTATION

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C E R T I F I C A T E

Certified that the dissertation entitled 'Distance Relays, Fault Locators and their Design Using Analog/ Digital Circuits' which is being submitted by Sri L.A.Narendra in partial fulfilment for the award of the Degree of Master of Engineering in Water Resources Development (Electrical) of the University of Roorkee is a record of the candidate's own work carried out by him under our supervision and guidance. The matter embodied in this dissertation has not been submitted for the award of any other degree or diploma.

This is further to certify that he has worked for a period of 6 months from 1.10.1977 to 3.4.78 for preparing the dissertation for Master of Engineering degree of the University.

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C O N T E N T S

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LIST OF ABBREVIATIONS

KV	Kilovolts
ft	feet
P.F'd/p.f.'d	Potential transformers
V.F'd/v.f'd	Voltage transformers
C.F./c.f	Current transformers
OCB'd	Over current relays
-vo/-vo	positive/negative
R/r	Resistance
X/x	Reactance
Z	Impedance
EHV/e.h.v.	Extra high voltage
H.V./h.v.	High voltage
a.c.	alternating current
d.c.	Direct current
CRO	Cathode Ray Oscillograph
S.C./s.c.	Short Circuit
O.C./o.c.	Open circuit
r.f.	radio frequency
KHz	Kilo Hertz
max./min.	Maximum/Minimum
mc	Millicoulomb
e.g.	example
I.C.	Integrated circuits
i.e.	that is
m.m.f'd	Magnetomotive force
e.m.f'd	electromotive force
VA	Voltampere

CHAPTER - 1

INTRODUCTION

1.1 The huge capital investment involved in a power system for the generation, transmission and distribution of electrical power is so great that proper precautions must be taken to ensure that the equipment not only operates as nearly as possible at its peak efficiency but also that it is protected from faults and accidents ensuring thereby reliability, dependability, uninterrupted service of quality and loss of revenue. This fact has all the more been accentuated by the complexity of system designs involved by large scale interconnections coupled with it's associated problems of stability, autoreclosing, faster fault clearing times, higher degree of accuracy, speed and sensitivity.

1.2 Transmission lines have air as it's principal insulation in addition to an insulation of a high resistivity material such as porcelain which is used as a mechanical support to the structure carrying the line conductors. Air insulation can be accidentally short circuited by birds, rodents, snakes, kitestrings, tree limbs, creepers etc. or reduced in insulation strength by ionisation due to lightning, corona etc., Porcelain insulators may be bridged by moisture with dirt or salt and can become cracked. They may even flashover due to atmospheric pollution such as is caused by dust and soot deposits. Other disturbancesto the system may be caused by power swings, loss of synchronism etc.

1.3 The protection of transmission lines against all eventualities has been and is still engaging the attention of power and relay engineers to attain the art of perfection in the protection of transmission lines and so also has been the continuing development in the field of transmission line fault locators. This is very much true as line patrolling to locate a fault on an overhead line is time consuming, expensive and moreso in bad weather, rough country on long extra high voltage lines.

1.4 This dissertation therefore reviews the development in the field of transmission line protection with particular referenceto distance relaying and fault location methods. The possibilities in the development of a distance relay along with a fault locator using analog and digital circuits has been indicated.

1.5 The historical development of relays, both conventional electromagnetic and static have been briefly discussed and dealt with in Chapter II, as also the recent trends in the application of microprocessors, minicomputers and on-line digital computers for distance relaying purposes.

1.6 The characteristics of electromagnetic distance relays and of the static distance relays are dealt with in Chapter III, along with a discussion on the desirable characteristics of the distance relays.

1.7 The historical development of the fault locators, their different types that have been used and are being used, is treated in Chapter IV. The requirements and capabilities of a fault locator as also the necessity of having a fault locator in service have also been spelt out in the said chapter.

1.8 The design possibilities in developing a distance relay along with a fault locator having a digital display which indicates directly the distance to the fault is detailed out at the end in Chapter V along with the required circuitry. A resume of digital principles and applications of the same for developing the relay and the fault locator is treated in the earlier part of the said chapter.

1.9 The conclusions drawn from this dissertation and the scope for further work is made known in Chapter VI.

CHAPTER-II

RELAY ELEMENTS THEIR TYPES AND RECENT DEVELOPMENTS IN DISTANCE RELAYING

2.1. INTRODUCTION

The earliest form of protection was the fuse which still today is in use on distribution circuits and lines because of its simplicity and cheapness. It however suffered from the disadvantage of not only requiring replacement before power supply could be restored but also lacked in speed of operation, selectivity, discrimination etc., and was therefore replaced ultimately by electromagnetic relays.

2.2. ELECTROMAGNETIC RELAYS

2.2.1. Early development

The earliest form of electromagnetic relays were of the attracted armature, solenoid and plunger, hinged armature and balanced beam types. These relays have a tendency to operate inadvertently on sudden changes in circuit conditions and as measuring units are handicapped by inherently low reset/pick up ratios[1] The attracted armature type relays are still used for all auxiliary relays such as annunciators, semaphore indicators, alarm relays etc., The balanced beam type relay has been used extensively for high speed differential relays and impedance relays. This relay provides a very fast clearing time of the order of one cycle but tends to overreach on faults, has a low resetting value compared to it's operating value and is susceptible to the transients due to the asymmetrical d.c. in the current wave[1]. It may, however, be stated that the balanced beam type is a simple and economical

relay and as such has been extensively used in the relays manufactured by M/S Brown Boveri Ltd.[2] and M/S ASEA[3] with improved designs.

2.2.2. Subsequent Development

As power systems increased in size and complexity it was necessary to employ more precise relay mechanisms with selectivity on an inverse current basis. This was achieved in the induction disc watthour meter which was converted into a relay by substituting contacts for the indicating register. This resulted in the inverse time overcurrent relays which are still in use today, although in an improved form.

2.2.3. The induction relay in it's improved form has a cup shaped armature and is made for fast operation with reasonable immunity from system transients and it's drop out is within a few percent of it's pick up so that it is used where normal and abnormal conditions are very close to oneanother. These relays can be of the 2 or 4 pole single phase or 8 pole 3 phase or a split cup 4 pole unit with shaded pole arrangements[1]. The 4 pole induction cup relay has been widely used by M/S General Electric Co., and M/S Westinghouse Co. Ltd. of U.S.A.[4,5] and as well by M/S English Electric Co., of India Ltd., Madras[6] for distance protection owing to the following advantages such as

(i) high speed of operation,

(ii) absence of second harmonic torques due to transients as is encountered in the balanced beam type,

(iii) low burden on C.T's and V.T's,

(iv) uniformity in the torque produced during the period of operation.

2.2.4. The 8 pole induction cup relay was first developed and used as a polyphase distance relay[7] in 1937 and was subsequently improved upon by Beeman and Board in 1941. It was in 1934 that A.R.Van C.Warrington[8] attempted to reduce the number of relays by switching the proper voltages on the occurrence of a fault by means of a phase selector relay which discriminates between different types of fault. The involvement of a phase selector relay, did not find much practical use, for it's applicability. It was however in 1954 that the first polyphase distance relay developed by Gavenko, Popov and Sapiro[9] to operate correctly on all interphase faults was applied to actual systems. In 1948[5], M/S Westinghouse Co., Ltd. developed a polyphase relay for phase faults only and was subsequently modified to the K-Dar Compensator distance relaying scheme to cover all types of faults. The switched reactance relays to cover both phase and ground faults is used currently in the JSRR3V English Electric Relays[6].

2.2.5. Salient Features of Electromagnetic Relays

The salient features of electromagnetic relays used currently for distance protection may be summarised as follows -

(i) positive operation because of rigid specifications and quality control in the design and manufacture of contacts, coils, bearings and other mechanical components backed by over 50 years of experience in manufacture.

(ii) consistent operation as proved by field experience

(iii) fast operating time of the order of 1/ $\frac{1}{2}$ cycle.

(iv) their use as back up relays in connection with carrier protection schemes.

(v) apathy on the part of power engineers in our country to go in for static relays but to rely heavily on electromagnetic relays more so out of conservatism to depend upon time proved performance, experience gained in their application, testing, maintenance and also perhaps due to lack of knowledge of electronic and transistor circuitry to which our older engineers never had an opportunity of being exposed to, either, in their curriculum or in the field.

2.3.1. ELECTRONIC RELAYS

2.3.1. Early Development

It was realised as long back as in 1948 in a paper[10] presented by R.H. Mc Pherson et al that the development in system design, high speed reclosing problems connected with stability and the increasing demand for higher degrees of accuracy, speed and dependability have accentuated these problems to a point where the inherent limitations of electromagnetic relays are raising barriers to the achievements of the desired goals. The increasing use of electronic circuits coupled with the great strides made by electronics in nearly every field of engineering and the widespread interest in electronic devices of all kinds, pointed out the way to protection engineers to use electronic means for lifting these barriers. The said paper reports that it was in 1927 that Mr. A.S. Fitzgerald developed an electronic pilot relaying system to overcome the limitations of pilot wires when

operating over long lines. The scheme was abandoned because of the short life and the high cost of the tubes available then. But a somewhat similar scheme is still in use today in the phase comparison carrier current relaying. In 1931, Rolf Hidorse[11] of Norway developed electronic circuits for most of the common protective relays using thyratron tubes wherein the undervoltage, over current, power directional and distance relays used input circuits consisting of transformers, metal rectifiers, linear resistance, inductance, capacitance elements to sum up and compare functions of system voltage to form a resultant single voltage for operation of the thyratron tube relay. In 1932, in the U.S. a laboratory sample reactance relay was built and tested but was not developed further[10], because the electromagnetic relay was fully adequate for the needs of the industry and no steps were taken to put the electronic relay into production. This type of electronic relay was built because it embodied all the common relay principles in a single relay and hence presented all the problems of the different types such as over current, under voltage directional, differential and distance relays. The experience gained from this development was destined to become valuable for all future developments.

2.3.2. Carrier relaying was the principal source of experience with tubes. In the early days, tubes had an irregular life, required frequent replacement and led to the general impression that the tripping of the circuit breaker should not be dependent upon the operation of the tube. The gradual improvement in tubes and replacement averaging once a year reduced skepticism that

tripping via tubes was not acceptable. The interest in electronic tubes was all the more aroused with the advent of long life tubes, consistent operating time as well as consistent low operating times even at low currents for more effective use of instantaneous reclosing. It was also realised that the lack of inertia, in tubes unlike in the case of electromagnetic relays which tends to operate the relay at the remote end of a fault more slowly, would enable an electronic relay with an operating time totally independent of the magnitude of the current or location of the fault and consequently would also enable simultaneous tripping of the breakers at both ends of the line.

2.3.3. The first relay using thermonic valves was described by Mc Pherson et al[10] and was applied for distance protection, wherein the line voltage was compared with the line current and consisted of a pulsing circuit, measuring circuit and the tube circuits. The pulsing circuit was used to generate a pulse at the moment of maximum line voltage and the pulse was used to overcome a large grid bias of the tube allowing it to conduct. The measuring circuit compared the line voltage with the line current. The tube circuit was the sensitive element which made responsive to signals emanating both from the pulsing circuit and measuring circuit. The response of the tube circuit initiated the tripping signal when the impedance being measured fell below the set value of the relay. The operating time of this relay was found to be instantaneous and the burden negligible.

2.3.4. Subsequent Developments

In 1954, Borgseth[12] published a paper on direct phase comparison distance scheme using a diode co-incidence circuit.

In the same year Kennedy[13] described an electronic carrier relaying scheme using no electromagnetic relay and even the tripping was performed by the use of a heavy duty thyratron. A resume was also given in the same year by A.R. Van C. Harrington[14] on electronic protective relays.

2.3.5. Reasons for non use of electronic relays

Electronic relays however did not find much favour with power engineers though used extensively for carrier communication and relaying principally on account of:

i) large volume of space occupied in assembling the circuitry and its cost

ii) fragility of electronic tubes and components

iii) uncertainty in the operation of the tubes

iv) requirements of anode supplies and cathode heater requirements.

v) problems encountered to ensure correct operation during transient conditions, and

vi) the inability of electronic circuits and relays to surpass the quality and reliable performance of the well established and cheap electromagnetic relays which were backed by several years of proven field experience.

2.3.6. Operational advantages of Electronic relays

These relays operationally claimed to have the following advantages:

i) low burden on C.T's and V.T's since operating power is from an auxiliary d.c. supply.

ii) absence of mechanical inertia and contact bounce.

iii) very high speed of operation - almost instantaneous

iv) low maintenance, owing to the absence of moving parts.

2.4. STATIC RELAYS

2.4.1. Definition of a static relay

The ASA definition of a static relay as published in IEEE Committee Report[35] is " A relay or (relay unit) in which there is no armature or other moving element, the designed response being developed by electronic, solid state, magnetic or other components withoutmechanical motion ".

2.4.2. As such a static protective relay refers to a relay in which the measurement or comparison of electrical quantities is done in a static network which is designed to give an output signal in the tripping condition when a threshold condition is passed. The output signal operates a tripping device which may be electronic semi-conductor or electromagnetic.

2.4.3. Classification

Static relays are classified according to the type of the measuring unit or the comparator and are as follows :-

i) Electronic relays

ii) Transductor relays

iii) Rectifier bridge relays

iv) Transistor relays

v) Hall effect relays

vi) Gauss effect relays.

Amongst the above relays, the transistorised relays and rectifier bridge relays are the most widely accepted type of static relays so much so that the word static relays is synonymous with transistorised and semi-conductor relays[15]. Accordingly

though electronic relays do fall in the domain of static relays they have been described earlier to review their historic development. Semi-conductor devices have overcome the limitations of thermionic tubes and have eventually taken the pride of place of being described as static devices.

2.4.4. Advantages of static relays

In 1962, M.Kaufman[16] reported the opinion of a committee of experts constituting the countries represented by Belgium, France, Germany, Poland, Switzerland, Sweden, U.K. and U.S.A. conferring the following advantages upon static relays over the electromagnetic relays and are.

i) quick response, long life, high resistance to shock and vibration

ii) quick reset action - a high reset value and absence of overshoot which is easily achieved because of the absence of mechanical inertia and thermal storage.

iii) No bearing friction or contact troubles such as corrosion, bouncing, wear and hence minimising maintenance.

iv) Ease of providing amplification thus enabling higher degree of sensitivity to be obtained.

v) The low energy levels required in the measuring circuits permit miniaturisation and at the same time minimise current transformer inaccuracies.

vi) Greatly improved pick up/ drop off ratio

vii) The basic building blocks of semiconductor circuitry permit a greater degree of sophistication in the shaping of operating characteristics enabling the practical realisation of relays with threshold characteristics more closely approaching the ideal requirements.

viii) Use of printed or integrated circuits avoids wiring errors and facilitates rationalisation of batch production.

2.4.5. Static relays employing transistors have their limitations and which are :

i) variation in their characteristics with temperature and age

ii) dependence of reliability on a large number of small components and their electrical connections

iii) low short ~~circuit~~ time over load capacity as compared with electromagnetic relays.

It has fortunately now become possible to compensate for all of the above limitations. The use of thermistors eliminate temperature error, whilst ageing may be minimised by presoaking for several hours at a relatively high temperature. The factors (ii) and (iii) listed above are the design features of the circuit and careful design can compensate if not eliminate those limitations[15].

2.4.6. Development in Transistorised relays

In 1956, C. Adamson and Wedepohl[17,18] described the development of a Mho distance relay with junction transistors and was styled " Dual Comparator Mho type relay". The derived voltage inputs from the system fault voltages and currents were applied to a coincidence circuit. This relay was however not exploited commercially[19]. The first wholly static distance relay[20] to be produced commercially was a transistorised version of the electronic Mho relay developed by Mc Pherson et al[10] in 1960. In 1966 K. Parthasarathy developed a new 3 step solid state static relay[25]

for distance protection and as well as a polyphase static distance relay[26]. Subsequently Sri Gupta S.C.[27] developed and designed a polyphase static distance relay in 1969 based on the principle of phase sequence measurement of the relay terminal voltages and it's performance was claimed to be much better than the earlier polyphase static distance relays. In 1970, N.M.Anil Kumar[28] suggested in his paper a polyphase relaying scheme based on phase sequence detection of the compensated voltages at the relay point and also indicated how different characteristics may be obtained by modifying the relay inputs.

2.4.7 Meanwhile documented work on Rectifier bridge comparators took place in Norway[19] and Germany. These basically consist of two rectifier bridges and a moving coil or polarised relay and by variation of the taps or of the comparator used, different characteristics could be obtained. These relays are widely used today in U.K., U.S.A., Continental Europe for distance protection.

2.4.8 Static relays with conic section characteristics and quadrilateral characteristics have also been developed by A. Vitanov[37], H.P. Khincha et al[39,40] Sri Anil Kumar[28] and others. A comprehensive treatment of these type of characteristics along with their development is given in para 3.5 of Chapter III.

2.4.9 A comprehensive literature on relays based on "Hall Effect" and "Gauss Effect" relays is given by A.R.Van C.Warrington[19]. The high cost of the Hall crystals, large temperature error and low output have prevented it's commercial

exploitation except in the USSR[15]. Similarly crystals based on Gauss Effect have not been used because of it's prohibitive cost.

2.4.10 Reservations in the use of Static Relays

Though static relays have several inherent advantages, the reservations of certain utilities in their use have been exposed by the AIEE Committee Report in 1965[22]. They in order are

(i) susceptibility of static relays to maloperate on transients caused by electromagnetic and electrostatic coupling.

(ii) that they have an upper and lower ambient temperature whereas electromagnetic relays operate at any temperature.

(iii) requires a reorientation in the thinking and the servicing practices of relay engineers. Often expensive test equipment is required along with the services of engineers with good electronic training.

(iv) failure of diodes due to high voltage on pilot wires, deterioration of semiconductors due to excessive heat, failure resulting from switching surges, inductive kicks, and contact bounce of the electromagnetic relays when energising the trip coil of a circuit breaker.

The above objections to a large extent have been overcome and static relays are finding wide application in the relaying of EHV systems so as to provide a means for obtaining the desired overall characteristics as also to have the highest reliability and the highest possible security factor[21]. As such they are increasingly being used by several utilities

abroad as the main primary protection.

2.5 RECENT DEVELOPMENTS IN DISTANCE PROTECTION

2.5.1 The recent trend in the development of distance type of protection has been by the application of on-line digital computer. They employ the predictive calculation of peak fault current and voltage from a number of sampling values. The possibilities to explore the avenues open for on-line digital computer were explored by Barry J.Mann and I.F. Morrison[23] in 1971. They have in their paper described the determination of the transmission line impedance from the peak fault current and voltage sample values to determine the presence of a fault and have indicated their experiences on a model transmission line followed by subsequent field tests. The scheme initially suffered from setbacks due to the presence of d.c.transients but were successfully overcome by employing mimic impedances. Their analysis was done only for a faulted single phase line.

2.5.2. Advantages of on-line digital Computers

The use of digital computers affords the following advantages in power system protection.

(i) decreases fault clearing time

(ii) affords breaker failure protection

(iii) transient blocking

(iv) out of step blocking

(v) out of step tripping

(vi) blocking tripping on generator dropping or load dropping.

In this context it must be however mentioned that G.D.Rockfellor[29] in 1969 advocated the use of digital computers for protective relaying claiming that the hardware

cost for a given level of capability has been dropping whilst the software sophistication and knowledge has been advancing thus making it ideally suited for the use of computers for protection wherever they are installed for data acquisition, data storage and monitoring. His paper was in the nature of a feasibility report which presented the requirements and logic of the computer to sense and locate faults, the input quantities required, the speed of the computer, the storage capability and also it's reliability and economics. He also claimed that the computer speed in initiating tripping would be a max. of 4 ms for severe faults and a max.of 10 ms for moderate or distant faults.

The IEEE Committee Report[35] amongst other things such as advocating solidstate relaying has also emphasised the use of digital computer to protective relaying and quoted the program developed by one utility to calculate and print out the impedances seen by relays during fault inception.

2.5.3. On Line Digital Computer Programming

A subsequent paper of Barry J. Mann[24] et al describes a digital computer programme for the protection of a 3 phase transmission line. The programme detects the presence of a disturbance or fault, classifies the fault into one of the well known six types and using the impedance detection method described in their earlier paper clears the fault. The mode of operation is similar to an ordinary conventional distance relay in which the complex impedance of a faulted line is calculated and the value is used as the final criterion for establishing the presence or absence of a fault. The computer programme

developed samples sequentially the three line currents and voltages at the rate of 40 samples/cycle and the interval of sampling is set by a 2 KHZoscillator. Each voltage sample is compared with the value of the previous sample and if the value difference is in excess of a specified tolerance the counter of that particular point is incremented and the computer jumps into the fault determination subroutines. The aim of the subroutines is to determine which two of the R, Y, or B phases or ground to be used to derive the equivalent single phase quantity. In the manner of existing distance relays delta quantities are used for phase faults and voltages and zero sequence compensated phase currents for ground faults. The authors claim that after final debugging the program was tested successfully for 1000 faults and no program indicated falsely R, Y or B or ground involvement in a fault.

G.D.Rockfeller in his subsequent paper[54] described the test results of an experimental general purpose process control digital computer, which provides high speed phase and ground distance fault protection of a 230 KV transmission line. The stored programme performs all the functions of relaying using the output of an analog to digital convertor which reads the instantaneous values of power system currents & voltages.

2.5.4. Use of Micro Processors and Mini Computers

A Report by CIGRE Committee Working Group 01 of Study Committee No.34 (Protection) published in Jan. 1977[32] among other things states that recently, the heavy fall in prices on the semiconductor market and rapid progress in large scale

integration (LSI) technology has promoted further development in computer relaying. The relatively cheap microprocessors now available claim to offer economic solutions, provided as the committee report states that users are ready to pay additional capital for the improved performance which the computer relaying can give compared with conventional relays.

2.5.5. Advantages and Disadvantages of Microprocessors/Mini Computers

2.5.5.1. Signficant advantages over conventional equipment is as follows :

(i) greater sophistication of protective characteristics

(ii) greater flexibility

(iii) self monitoring of computer hardware by diagnostic programs

(iv) ability to validate input data and cater for missing or erroneous information.

(v) suitable input/output interfaces to enable communication with other monitoring or control devices or the control engineer

(vi) high speed analogue input peripherals allow instantaneous values of a.c. currents and voltages to be processed. The actual instantaneous values of several cycles of power frequency can be stored and printed out after a fault. This recording function provides a very valuable means for fault analysis or post mortem review.

2.5.5.2 Disadvantages

(i) At present all inputs must be converted from analogue to digital form

(ii) computers are more difficult for users to operate and maintain

(iii) the hardware is subject to rapid obsolescence.

2.5.6. Requirements of Computer based Relaying Schemes

Any computer based relaying scheme will have to meet very stringent requirements both as regards power system protection and power system operation. The computer system if used as main protection will have to compete with the present analogue devices having operating times ranging from 1/2 to 1½ cycles. Nevertheless in the back up mode of protection, the speed will naturally be not because of the inherent speed of operation of computers. Selectivity improvements will require better modelling of the characteristics of the protected power system plant and a larger tolerance to errors that may be present in the input information, if conventional instrument transformers are to be used as input sources to computer based relaying systems. The technique of measurement, the algorithms used and the hierachy of the system must be such that a greater certainty of operation is available as compared with what can be achieved with modern analogue techniques and equipment. The total reliability of the computer system must be proved to be equal to or exceed the reliability of existing devices that perform similar duties. A margin in favour of the latter devices will automatically lead to a delicate balance between improvements as regards power system protection aspects and drawbacks

from the system operation point of view. The downtime of the computer must be kept down to a minimum. The quality of the hardware and it's compatability with power system environment must be assessed with the utmost care and the software must be thoroughly checked to avoid programming errors or program degradation. The true cost of a computer based relay system is rather difficult to assess and especially so if the relaying tasks form only a part of the activities of a larger computer installation.

2.5.7. Types of Computerised Versions

The present competing computer versions in the market are the mini computers and microprocessors.

2.5.8. Mini Computers

Mini computers have been available since the early part of 1960's and the recent ones are fast, with a cyclic time of the order of 1microsec, are powerful in calculation and are easy to handle because of their highly developed software. It's initial hardware cost is rather high and it can perform only one arithmetic or logic operation at a time. This makes it difficult even with sub microsecond memory cycles to match the speed of modern solid state relays that work in parallel. In order to prevent hardware failures it is absolutely necessary to provide for duplicate computer systems and as such it's cost is one order of magnitude higher than that of conventional relays.

2.5.9. Micro Processors

Micro processors have been on the markets for about four years. They have lower processing power than mini computers, but their lower cost permits them to be used as dedicated devices which work in parallel, each performing only a limited number

of functions. This system has the advantage of less complexity and therefore higher reliability.

2.5.10. Solution to Relaying Problems

The mathematical treatment and the solution of relaying problems related to the protection of transmission lines/feeders depends to a large extent on whether the measurement is being carried out with the knowledge of only local quantities or whether information is available from other parts of the power system and or whether provision can be made to minimise the influence of unwanted frequency components in a signal without penalising the operating time and the characteristics of the computer to be used for the task.

The majority of the work done on computers in the field of protection is on ∅ feeders. This is partly because of the relative simplicity of the equation describing the protected object.

The feeder protection based on inductance-resistance or impedance measurements can be achieved by a number of different techniques. R. Poncelot presented in his paper[33] a method employed in the formulation of a protection programme which is as follows :

(i) Fault detection

(ii) Selection of faulty phases

(iii) Line i, distance

(iv) Disconnection

In 1975 A.M.Ranjbar and B.J.Cory of the Imperial College, London[30] proposed digital methods for the protection of long e.h.v. lines on transient faults and the method suggested is the accurate determination of the resistance and inductance of the line so that any number of harmonics on the current and voltage waveforms are eliminated. The authors claim that this method is suitable for the distance protection of transmission lines so as to clear the fault in the first cycle of it's occurrence and the method is claimed by M.Chamia & S. Ziegler[32] in the elimination of harmonics of any order by successive integration over particular time intervals.

In 1973, Hope and Umamaheshwaran[34] have also shown that the effects of harmonics can be totally eliminated by using Fourier Integral method using orthogonal pair of functions. Such as sine, cosine functions, odd and even square waves.

2.5.11 Other Application of Computer

The other important computer applications are that the result of state estimation programs can be used for automatic adjustment of relay settings to the actual load flow and infeed conditions and to mark splitting points for load loss minimisation. Automatic adjustment of operating settings to a new system configuration, for instance, after a major breakdown it will help maintain sensitivity and improve selectivity during network restoration.

2.6 CONCLUSIONS

The trend in the development is to return to protective equipments similar to well known conventional equipments but with operation in a digital mode. Software packages have been

developed for nearly all protective functions, the majority being, however, only a transposition of analogue relay functions into digital form[32]. It must nevertheless be emphasised that the application of computers to relaying tasks requires careful study of the power system environment with particular reference to the effects of electric and magnetic interference and to maintain programs of both software and hardware. Servicing has however been rendered easier by relatively simple incorporation of self checking features for fast and accurate fault diagonosis. To have a on-line digital computer exclusively for protective relaying will work out to be a very costly affair If a computer is installed for other purposes, then the functions of protective relaying may be achieved without any extra cost. The use of microprocessors and mini computers exclusively for protective relaying is equally a costly affair particularly in our country where these have to be imported.

The following lines from A.R.Van C.Warrington's book[1] will sum up the development and trends in relaying. It is clear that the future of protective relays still holds an interesting challenge to engineers, since the technique of automatic protection has by no means settled down to a predictable pattern, in fact the number of unsolved problems seems to increase each year.

CHAPTER-III

CHARACTERISTICS OF DISTANCE RELAYS

3.1. DISTANCE RELAYS AS COMPARATORS

All distance relays whether of the electromagnetic or of the static type are basically comparators and they operate when an electrical quantity of the protected circuit either changes from it's normal value or changes its ratio and or phase relation with respect to another electrical quantity of the circuit. The comparison is usually made in the relays by turning the electrical quantities into forces, torques, e.m.f's. or e.m.f's. proportional to the two quantities compared.

3.2. CLASSIFICATION OF COMPARATORS

Relay movements are distinctly associated with the characteristics of the relay and accordingly the movements are classified into two groups[1] -

i) Amplitude Comparators

Eg. a) Balanced beam relay

b) Induction disc element with shaded pole driving magnets

c) Opposed rectifier bridges

d) Transductor relays

ii) Phase Comparators

Eg. a) Induction cup relay

b) Induction disc element with wattmetric type of driving magent

(c) Induction dynamometer

(d) Polarised rectifier bridges

(e) Hall effect crystals

Basically an inherent amplitude comparator becomes a phase comparator and vice versa if the input quantities are changed to the sum and difference of the original two input quantities. A comprehensive treatment of this aspect is given in reference cited No.(1).

3.3. CONVENTIONAL OR ELECTROMAGNETIC DISTANCE RELAYS-CHARACTERISTICS

3.3.1. The two input quantities in these relays produces a torque in co-operation and the equation for the characteristic of the relay at the threshold of operation under steady state conditions when plotted on a diagram whose axes are $\left|\frac{B}{A}\right| \cos\phi$ and $j\left|\frac{B}{A}\right| \sin\phi$ is of the form

$$K\,|A|^2 - K'\,|B|^2 + |A|\,|B| \cos(\phi - \theta) - K'' = 0$$

Where A and B are the two electrical quantities being compared,

K and K' are scalar constants

K'' is a constant representing a bias which is a mechanical restraint.

ϕ is the phase angle between A and B

θ is a predetermined fixed angle which in these relays is the value of ϕ which provides maximum relay torque.

The above equation represents all the circular and straight line characteristics of electromagnetic distance relays, as obtained from two electrical input quantities.

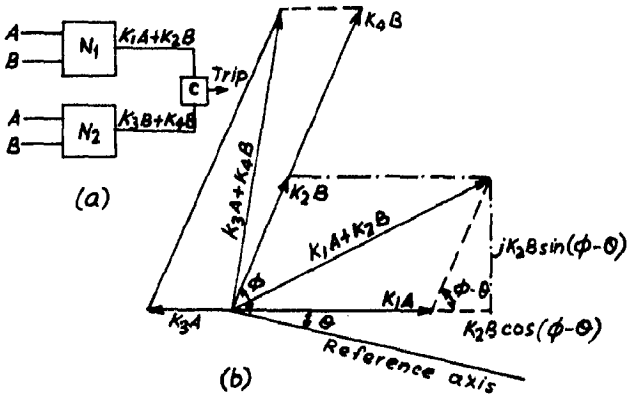


FIG. 3.0_GENERAL CASE OF VECTOR QUANTITIES FOR SUPPLYING COMPARATORS

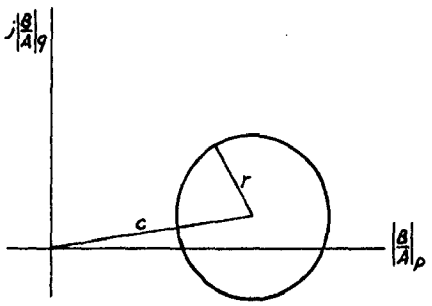


FIG. 3.0_THRESHOLD CHARACTERISTIC OF ANY PHASE

It must however be mentioned that K'' is a finite quantity in single quantity relays (level detectors) but is made substantially zero for comparators. Thus we have for distance relays the above equation to be of the form(1)

$$K\,|A|^2 - K'\,|B|^2 + |A|\,|B|\,\mathrm{Cos}\,(\phi - \theta) = 0$$

Dividing throughout by $K'A^2$ we have

$$\frac{K}{K'} - \left|\frac{B}{A}\right|^2 + \left|\frac{B}{A}\right| \frac{\mathrm{Cos}\,(\phi - \theta)}{K'} = 0$$

Adding $\left(\frac{\lambda}{2K'}\right)^2$ to both sides of the above equation and re-arranging terms we have

$$\left|\frac{B}{A}\right|^2 - \left|\frac{B}{A}\right| \frac{\mathrm{Cos}\,(\phi - \theta)}{K'} + \left|\frac{\lambda}{2K'}\right|^2$$

$$= \frac{K}{K'} + \left|\frac{\lambda}{2K'}\right|^2$$

$$= \sqrt{\frac{\lambda^2 + 4\,KK'^2}{2K'}}$$

The above is the equation of a circle on a complex plane having $\left|\frac{B}{A}\right|$ Cos ϕ and $j\left|\frac{B}{A}\right|$ sin ϕ as co-ordinates, the radius being $\sqrt{\frac{\lambda^2 + 4\,KK'}{2K'}}$ and the centre at $\frac{\lambda}{2K'}$ from the origin and at an angle θ from the reference axis (Refer Fig.3.0).

The axes have been designated as $\left|\frac{B}{A}\right|_p$ and $j\left|\frac{B}{A}\right|_q$ for $\left|\frac{B}{A}\right|$ Cos ϕ and $j\left|\frac{B}{A}\right|$ Sin ϕ respectively. In the case of distance relays A will be current and B the voltage and the coordinates of the diagram will be $\left|\frac{V}{I}\right|$ Cos ϕ and $j\left|\frac{V}{I}\right|$ Sin ϕ or R and jX. The diagram in which the characteristic is plotted

on R and jX as co-ordinates is called the impedance diagram or the complex impedance plane or Z-plane. Similarly if $\left|\frac{A}{B}\right|$ is plotted the diagram has coordinates G and jB and the diagram is called the Admittance diagram or Y-plane.

3.3.2. Admittance is the reciprocal of Impedance so that YZ=1 Hence if the locus of Z is a circle, then the inverse of it is a straight line parallel to the real axis[31]. Again by inversion we have that if the locus is a circle on one plane, then the locus will also describe a circle on the inverse plane except in the special case when the circle passes through the origin in which case it will be a straight line. Thus from the general equation of the electromagnetic distance relays we have their characteristics described by circles or straight lines, when drawn on the impedance or admittance plane. The relay operates if the tip of the impedance vector on the impedance plane which is determined by the ratio of voltage and current applied to the relay terminals is placed within the limit of the region of complex plane limited by the relay characteristic. When the tip of the impedance vector is moved to another part of the complex plane, the relay does not operate if this part is outside the limits of the characteristic equation in question.

3.3.3. <u>Classification of electromagnetic relays based on their Characteristics</u>

It is by considering the operating characteristics drawn in the complex plane we can distinguish or rather classify the following main types of electromagnetic distance relays.

3.3.3.(i) Non directional distance relay with a circular characteristic with its centre at origin called the ' Impedance Relay '. Thus in the balanced beam type, if we substitute the current I for A and the voltage V for B we have the relay to operate when

$$K |I|^2 > K' |V|^2$$

$$\text{or } \left|\frac{V}{I}\right|^2 < \left|\frac{K}{K'}\right|$$

$$|Z| < \sqrt{\frac{K}{K'}}$$

The above is the equation of a circle with origin at centre and radius equal to $\sqrt{K/K'}$.

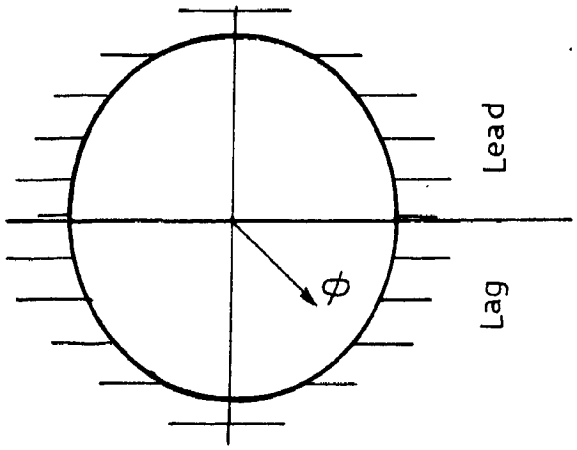
Such a relay is set to operate when the impedance measuredby the relay is less than the impedance of the protected line AB ref. Fig.3.1.

3.3.3.(ii) Non directional distance relay with a straight line characteristic parallel to the real axis or (R-axis) in the impedance plane called the ' Reactance Relay.

In 1928, Mr. A.R. Van C. Warrington developed the first induction disc type distance relay which had a reactive VA magnet instead of the usual potential restraining magnet, and subsequently in 1934 it was improved to the 4 pole induction cup instead of an induction disc to design the first high speed reactance relay. Two opposite poles had current windings, while the other two had opposed current and potential windings such that by substituting in the general characteristic equation (1), $A = I$, $B = V$, $K' = K'' = 0$, $\theta = 90$. We have

POLAR DIAGRAM

ADMITTANCE OR CURRENT



IMPEDANCE OR POTENTIAL

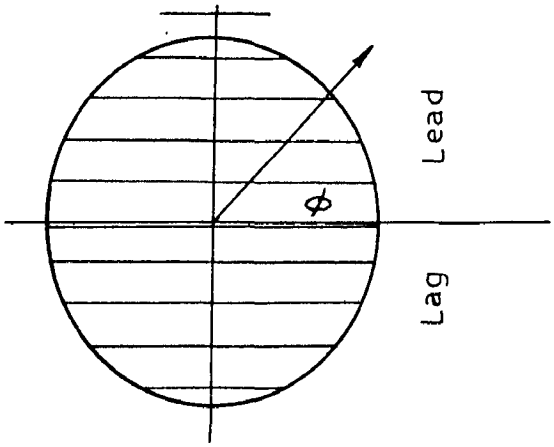


FIG. 3.1_ IMPEDANCE RELAY CHARACTERISTIC

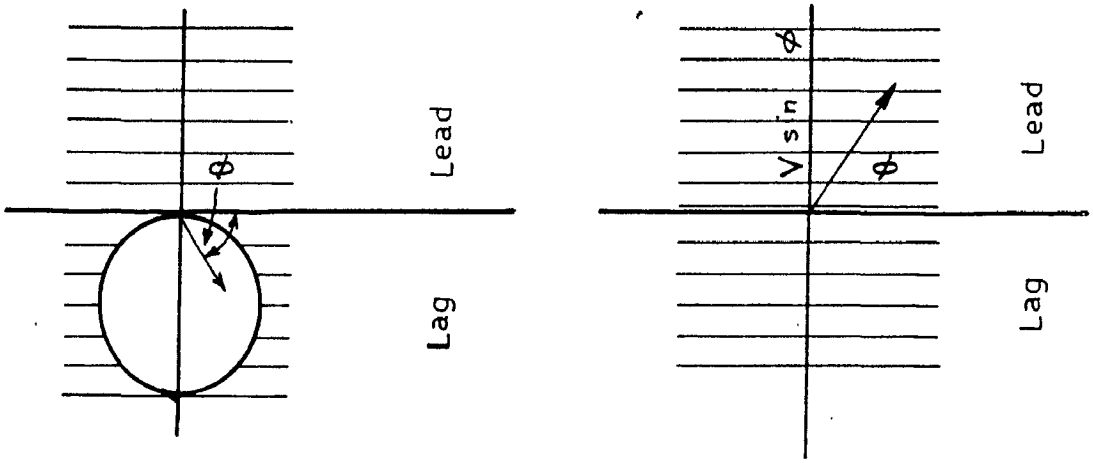


FIG. 3.2_ REACTANCE RELAY CHARACTERISTIC

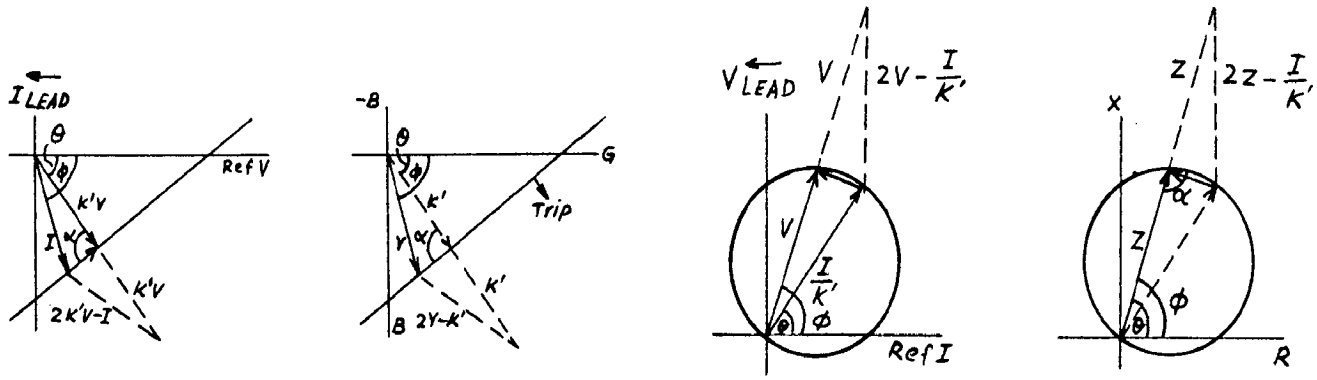


FIG. 3.3_Mho RELAY CHARACTERISTIC

$$M^2 + VI \cos(\phi - 90) = 0$$

$$M^2 - VI \sin\phi = 0$$

$$M = V \sin\phi$$

$$\frac{V \sin\phi}{I} = K$$

The relay operates when $\frac{V \sin\phi}{I} < K$

i.e. when $I < K$. the ohmic setting of the relay

This equation gives a straight line characteristic Fig.3.2

3.3.3.(iii) The directional distance relay with a circular characteristic, passing through the origin called the ' Mho relay' or the Admittance Relay.

This relay was developed in 1932 by Mr. A.R. Van. C. Warrington. The relay measures a component of admittance Y/θ and the relay is also known as the Angle Impedance relay in U.S.A.

In this relay a 4 pole induction cup had potential windings or two opposite poles and or opposed current and potential windings on the other two poles.

Thus in the general characteristic equation $A = I$, $B = V$, $K, K' = 0$

$$-K'V^2 + VI \cos(\phi - \theta) = 0$$

$$\text{or } I \cos(\phi - \theta) - K'V = 0$$

$$\frac{I}{V} \cos(\phi - \theta) = K'$$

$$\frac{1}{Z} \cos(\phi - \theta) = K' \text{ or } Y \cos(\phi - \theta) = K'$$

$$Z = \frac{1}{K'} \cos (\phi - \theta)$$

$$\text{or } Z = K \cos (\phi - \theta)$$

The above is the equation of a circle passing through the origin vide fig.3.3 The relay operates when Y cos $(\phi - \theta) > K'$ or when $Z < K \cos (\phi - \theta)$.

3.3.3(iv) Ohm Relay

This relay measures a particular component of the Impedance Z/θ . The threshold characteristic is a straight line on an impedance diagram fig.3.4 i.e. in the general characteristic equation

$$K' = K'' = 0, \quad A = I, \quad B = V,$$

$$KI^2 - VI \cos (\phi - \theta) = 0$$

$$K = \frac{V}{I} \cos (\phi - \theta)$$

$$\text{or } Z \cos (\phi - \theta) = K$$

The relay operates when $Z \cos (\phi - \theta) > K$. It is seen from the above that the reactance relay is a particular case of the ohm relay when the relay measures $Z/ 90^{\circ}$.

3.3.3.(v) Offset Mho Relay

This is the term given to a relay whose circular characteristic in an impedance diagram does not pass through the origin, vide fig.3.5. This characteristic is obtained by adding current bias to a mho relay. The bias provides an extra I^2 term and the general equation would be of the form

$K |I|^2 - K'|V|^2 + |V| |I| \cos (\phi - \theta) = 0$ and this represents a circl of radius $r = \sqrt{(1 + 4KK')}/2K'$ and centre at a distance from the

POLAR DIAGRAM

ADMITTANCE OR CURRENT

IMPEDANCE OR POTENTIAL

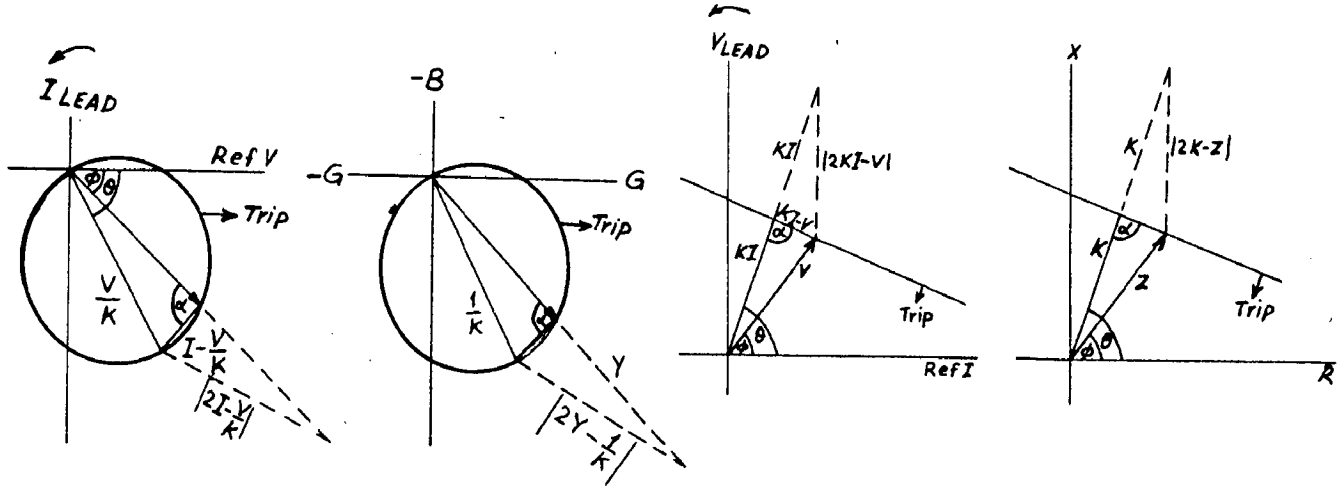


FIG. 3.4_Ohm RELAY CHARACTERISTIC

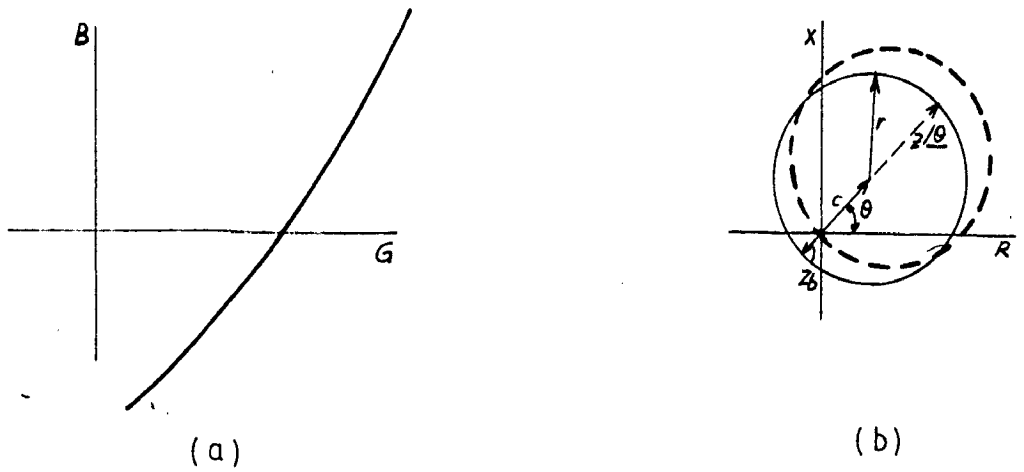


FIG. 3.5_ OFFSET mho RELAY CHARACTERISTIC

origin given by $C = \frac{1}{2K'} \angle\theta$. The offset mho relay characteristic when plotted on an Admittance diagram is again a circle but its radius and distance of the centre from the origin are inversely related to those of the circle drawn on an impedance diagram.

The off set of the impedance circle is secured as described above by adding to the line potential a biasing potential IZ_b, proportional to the current, which has the effect of moving the characteristic impedance circle bodily by an amount IZ_b. Thus in the mho relay characteristic substituting $(V + IZ_b)$ for V we have

$$-K'(V+IZ_b)^2 + (V+IZ_b)\, I \cos(\phi - \theta) = 0$$

Dividing throughout by I^2 we have

$$-K'\left(\frac{V^2}{I^2} + \frac{2VIZ_b}{I^2} + \frac{Z_b^2 I^2}{I^2}\right) + \left(\frac{VI}{I^2} + \frac{I^2 Z_b}{I^2}\right)\cos(\phi-\theta) = 0$$

$$-K'(Z^2 + 2ZZ_b + Z_b^2) + (Z + Z_b)\cos(\phi-\theta) = 0$$

$$-K'(Z+Z_b)^2 + (Z+Z_b)\cos(\phi-\theta) = 0$$

$$(Z+Z_b)\left[-K'(Z+Z_b) + \cos(\phi-\theta)\right] = 0$$

$$\text{or } -K'(Z+Z_b) + \cos(\phi-\theta) = 0$$

$$K'(Z+Z_b) = \cos\phi\ (\phi-\theta)$$

$$Z + Z_b = \frac{\cos(\phi-\theta)}{K'}$$

$$\therefore \quad Z = \frac{\cos(\phi-\theta)}{K'} - Z_b$$

This shows the characteristic equation is similar to that of the Mho relay except moved by the impedance Z_b ref.Fig.3.5. The biasing potential is obtained by introducing a reactor in the current circuit.

3.3.4. Special Distance Relay Characteristics

The following are various ways in which the standard impedance, admittance and reactance can be modified. These modifications were done so that the distance relays develop better tolerance to fault resistance, and less susceptibility to power swings.

3.3.4.(1) Modified Impedance Relay

The standard impedance relay characteristic can be moved outwards along the R-axis by current biassing the potential circuit with the Ir drop across a resistor so that it has more tolerance for fault resistance as shown in figure 3.6. The maximum possible offset is when the circle passes through the origin. Biassing may also be done in the -R direction as well as in the R-direction so that a bigger impedance circle results which tends towards a reactance characteristic. Thus in the general characteristics equation of an Impedance relay, introducing the Ir bias changes the equation to

$$|KI|^2 - |V + Ir|^2 = 0$$

$$K^2I^2 - V^2 - I^2r^2 - 2VIr \cos\phi = 0$$

Dividing throughout by $-I^2$ we have

$$Z^2 + 2Zr\cos\phi - R^2 + r^2 = 0$$

The above is the equation of a circle passing through the origin with its centre on the R-axis and distance r from the origin if r = R ohms.

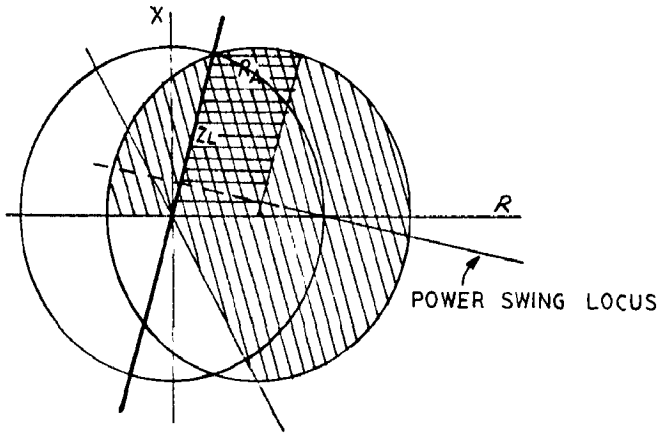


FIG. 3.6_MODIFIED IMPEDANCE CHARACTERISTIC ON IMPEDANCE DIAGRAM

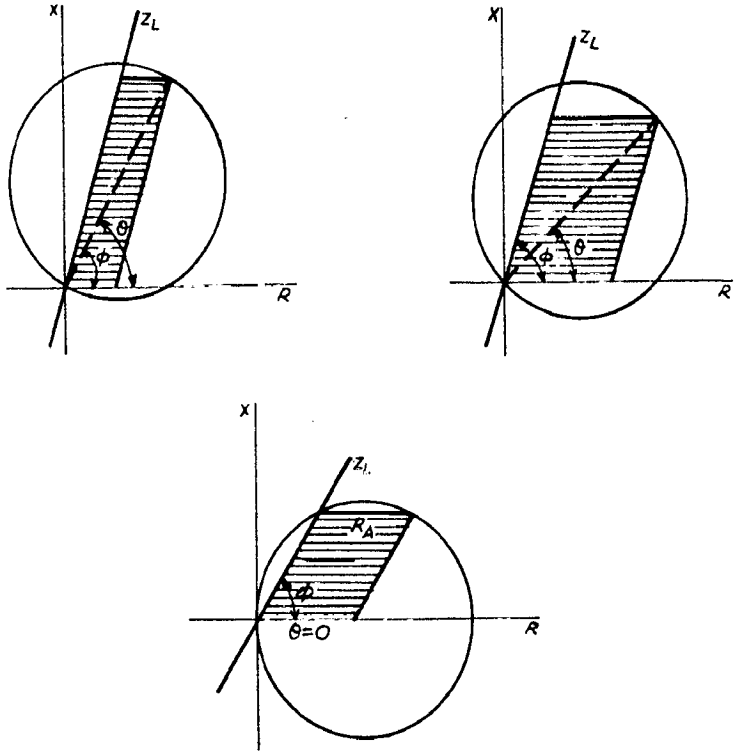


FIG. 3.7_PHASE ANGLE BIASSING OF mho RELAY (Ø−θ) TO INCREASE TOLERANCE TO FAULT RESISTANCE

3.3.4.(ii) Conductance Relay

By swivelling the mho relay characteristic in the leading direction, clockwise in the impedance diagram its tolerance to fault resistance can be increased with less vulnerability to power swings in the modified impedance relay. In the limiting position along the R-axis it becomes a " conductance Relay". In the conductance relay there is no change in the balance equation from the mho relay, i.e. $Z = K \cos(\phi - \theta)$ except that θ is now zero instead of the normal value of 60°, but the ohmic setting of the relay has to be multiplied by $Z/(\cos\phi)$ so that the impedance cycle will still pass through the ohmic value $Z\angle\phi$. Refer. Fig.3.7 for its characteristic.

3.3.5. Switched Distance Relays

Theoretically, four fault detectors and 18 measuring units are required for providing three time distance steps for the ten varieties of phase to phase and phase to ground faults. The cost and the space required for installing such large units has been reduced in practice by using measuring units for more than one purpose.

The number of measuring units is sometimes reduced to three by using the same set for phase and ground faults. The distance measuring units in modern schemes of this type are normally connected for phase faults, that is with delta potential and delta current and are switched to wye connections only when a single phase to ground fault occurs. A scheme of this type

provides immediate clearing of inter phase faults and a small delay in clearing single phase to ground faults. However, the economy of using a single measuring unit has to be balanced against the following effects.

(a) time delay required for the fault detectors to access the type of fault

(b) complete loss of protection if the switching contacts fail

(c) possible wrong tripping if the type of fault changes during operation of the relay (effect of wind upon arc)

(d) inaccuracy due to differing phase impedance (effect of unsymmetrical transposition of conductors)

(e) possible reduction in reliability due to dependance upon a number of contacts in series.

The Delta-Wye switching is used for distance relays of the impedance or admittance type with the timing unit started by a poly phase over current or mho type fault detector for phase faults and by a residual current or power relay on ground faults.

The inter phase switching consists of one unit for phase faults and one for ground faults, these units being switched to the appropriate phase or phase pair by the fault detectors. Thus the phase and ground protection are two separate schemes.

Poly phase distance relays are no doubt ideal for protecting a polyphase system than single phase relays, but so far it has not been possible to devise the circuitry for obtaining uniform performance on all types of faults[1], though considerable efforts have been made in this direction by Gupta[27].

3.4. CHARACTERISTICS OF STATIC R RLAYS

3.4.1. The measurement of impedance, reactance or angle admittance in static relays is done by the comparison of two different input combinations of current and voltage which result in circular or straight line characteristics as explained in the earlier part of this chapter under electromagetic relays. However, in a static relay the two input quantities must be similar that is two currents or two voltages because they are not electrically separate as in the case of electromagnetic relays. As such in a voltage comparator the current is turned into a voltage by passing it through an impedance $Z_r \angle \theta$ which is a replica of the impedance of the protected line section. Here the line voltage is compared with the voltage drop across the replica impedance. In the current comparator the current is derived from the voltage by connecting the replica impedance in series with it giving a current V/Z_r which is compared with the line current I. The use of the replica impedance is not only convenient but permits fast tripping since it eliminates error due to transients in the fault current, and is due to the fact that the fault current passing through the line impedance produces the same voltage wave form as the secondary current passing through the replica impedance Thus any transients that appear in the primary current appear equally in the voltage V and IZ_r and thus cancell out their effect on the impedance measurement.

3.4.2. Both amplitude and phase comparators have been used. An amplitude comprator compares only the magnitudes of the input

signals and ignores their phase angle. The phase comparator on the other hand responds only to the phase relation between the two input quantities irrespective of their magnitudes. For linear and circular characteristics it operates when $90^{\circ} > \varphi > -90^{\circ}$ where φ is the angle between the two inputs.

3.4.3. The characteristics of the static distance relays are as in the case of electromagnetic relays plotted on the Impedance diagram (R and jX axes) and Admittance diagram (G and jB axes).

The characteristic is either a straight line passing through the origin or a circle with the origin at the centre depending upon whether a phase comparison or an amplitude comparison is made and further as to whether the characteristic is plotted on an Impedance diagram or on an Admittance diagram. A circular characteristic not passing through the origin of one diagram is a reciprocal circle on the other diagram that is the distance of each point on one circle is the reciprocal of the distance from the origin of the corresponding on the other circle. Furthermore each point will be lagging as much the resistance axis as the corresponding point on the other circle was leading the conductance axis and vice versa.

3.4.5. In 1954, Borgseth[12] described the means of obtaining distance relay characteristic such as reactance, mho, elliptical etc. on the impedance plane using electronic relays and using the principle of phase comparators.

3.4.6. It was however in 1960, that C.G. Dewey[44] et al explained as to how the mechanical complexity of electromagnetic

relays could be replaced by transistorised circuitry to perform the desired mechanical functions. The logic symbols of AND, NOT, OR have also been explained and block diagrams for these functions as applicable to phase comparison principle of comparing the instantaneous directions of current flow at opposite ends of a transmission line using a pilot channel is set out therein. The successful results of laboratory and field tests has been given in the companion paper to the above vide S.H. Horowitz et al[45].

3.4.7. In 1963, C.G. Dewey et al[20] described the necessary principles and circuitry for directional comparison relaying and static relaying equipment for transmission lines with mho distance unit circuits for the time delay unit on pick up and drop out along with the pulse stretcher circuit to convert the pulse output. The successful application of this scheme was reported in their companion paper[46] as testified by field and laboratory tests.

3.4.8. In 1968, L. Jackson et al[47] reported the ease with which transistor comparators for distance relays can be designed for high speed operation taking into consideration the overall position and integrity of operation. It is reported therein that the operating speed must be defined over the whole working range of the relay and that neither, the speed nor the measuring accuracy should be unduly affected by the severe transients generated by modern e.h.v. net works. The advantages of transistor comparator which affords greater freedom of design for specific laws of operation and/or characteristics embracing freedom of

design in both static and dynamic characteristics has been exemplified. The basically different methods of obtaining useful characteristics from a comparator circuit is confined to the following :

(i) block instantaneous comparison in which the duration of polarity coincidence determines the output. The tripping criterion is that the duration of the first coincidence should exceed a specified time usually one quarter of a cycle of the power frequency period.

(ii) Block average comparison, a development of the above in which the duration of polarity coincidence is measured on both the half cycles of the input signals and the averaging value is determined in an integrating circuit, a trip signal being produced if a specified average value is maintained for more than the prescribed duration.

(iii) pulse comparison in which the polarity of one signal is measured during a short interval in the cycle of the second signal, usually but not necessarily at the latter's peak.

The relative merits of practical comparators of each category have been compared by considering phase angle comparators since practical comparators under (iii) above have been realised only as phase angle comparators[47]. A comparison reveals that the overall characteristics of circle and straight lines in the complex plane can be easily obtained by all three of the above cited methods with basically no difference in the steady state. However their comparison in their dynamic static reveals that (i) and

(iii) are inherently susceptible to system transients and other spurious signals by virtue of their near instantaneous operation and unless all unwanted surges and transients are removed effectively, the measuring accuracy cannot be maintained under dynamic conditions without sacrificing operating speed. The block average comparator as described in (ii) however has inherent transient free characteristics and its operating time is significantly unaffected by the degree of d.c. offset transient in the input signals. This has been confirmed by the author after extensive laboratory tests on a proto type relay that was developed. The basic block diagram of the same is as shown in Fig.3.8. The relay performance with a d.c. offset in one input only to the comparator and subsequently with d.c. offsets in both inputs were considered on the practical prototype relay for different source-system impedance ration. Their performance curves plotted as (i.) relay accuracy against syste m impedance ratio is almost a straight line except near the boundary conditions where there is a marked fall in accuracy.

(ii) relay operating time against relay accuracy which is almost a straight line. Accordingly the authors have spelt out the specification of the design requirements for the block average comparators as -

i) measuring accuracy - to be maintained over the full working range

ii) timing characteristic- should be of the definite minimum type for all faults within the protected zone with an operating time of the order of 1 cycle of power frequency being considerably desirable.

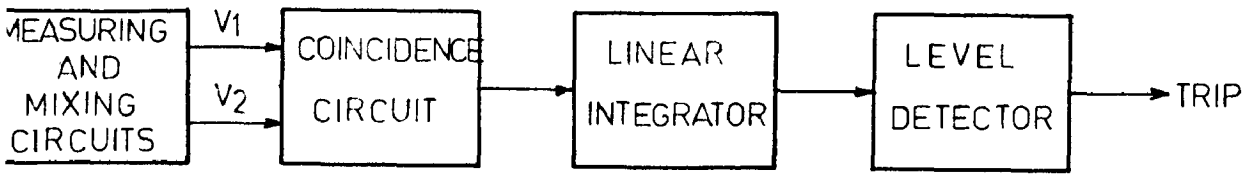

MEASURING AND MIXING CIRCUITS
V1
V2
COINCIDENCE CIRCUIT
LINEAR INTEGRATOR
LEVEL DETECTOR
TRIP

FIG. 3.8

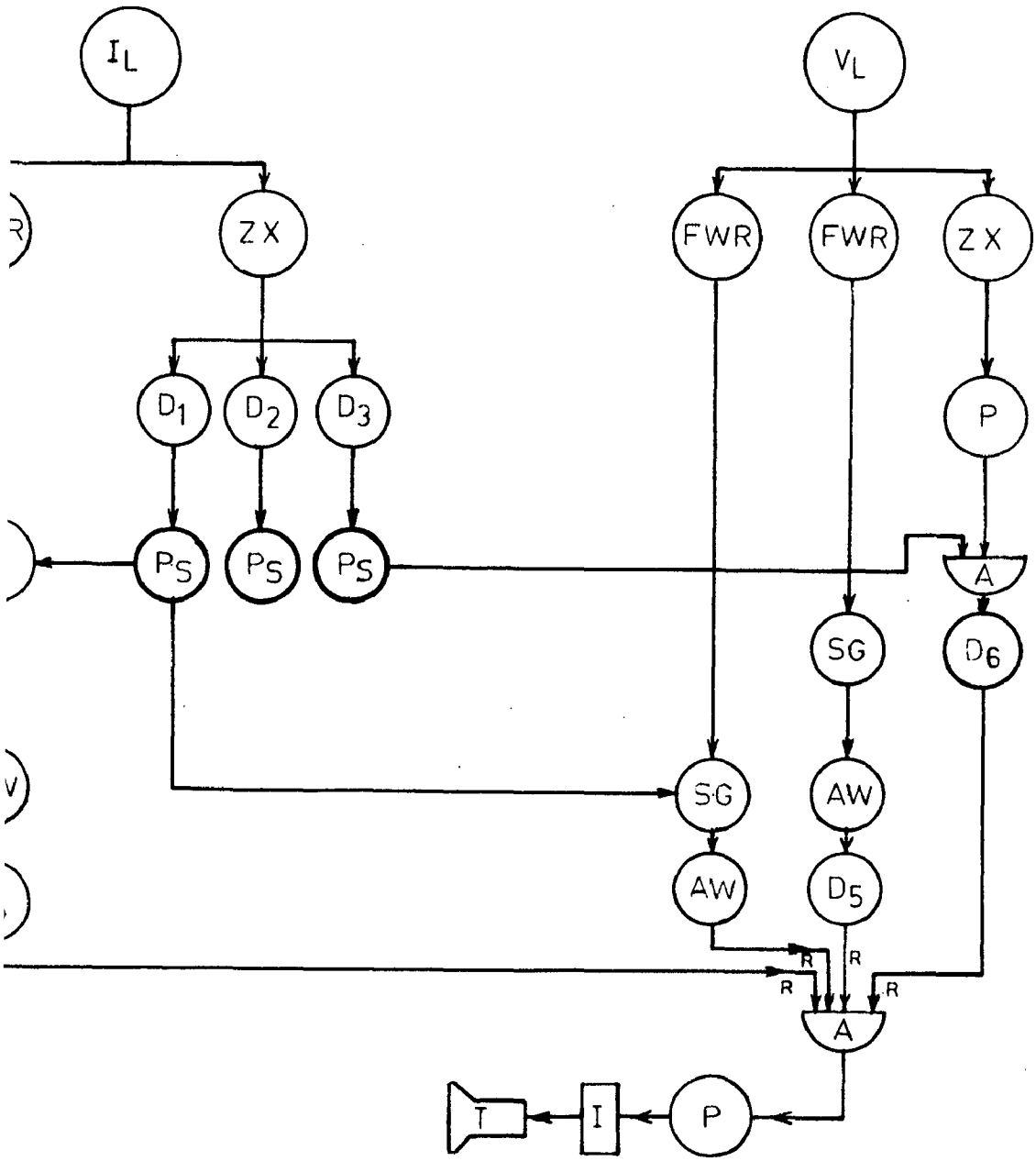

IL
VL
ZX
FWR
FWR
ZX
D1
D2
D3
P
PS
PS
PS
A
SG
D6
SG
AW
AW
D5
R
R
R
R
A
T
I
P

FIG. 3.9

iii) Stability - should have inherent resistance to high amplitude, short duration, system generated surges both with regard to maloperation and to surge damage.

3.4.9. In the same year, P.G. Mcdaven[48] described in his paper a sampling technique developed which allows a comparison of instantaneous values derived at different instants of time, thereby dispensing with the need to phase shift and mix signals derived from the primary line quantities. However the process of elimination of phase shifting requires a greater degree of sophistication in the relay circuitry. But it achieves on the other hand, a saving in both space and cost. The sampling period is of the order of 50 micro seconds in each half cycle and have been classified by the author under the following headings:

i) those taking the zero crossing of line current I_L as time reference and referred to as current polarised relays.

ii) those taking the zero crossing of V_L as time reference and referred to as voltage polarised relays.

The block diagram of the current polarised relay is as shown in fig.3.9. In this if the current and voltage signals are interchanged, the voltage polarised relay is obtained.

ZX - Zero crossing detector
D - Delay Unit
P - Pulse unit
P_S - Pulse sampling unit
SG - Sampling rate
AW - Amplitude/Pulse width convertor
I - Integrator and level detector
T - Thyristor

Here ZX detects both the +ve and -ve going zeros and to avoid duplication of the circuits after the measuring gates the signals are rectified. The amplitude/ pulse width convertor produces a pulse length proportional to the amplitude of the sampled quantity at the instant of sampling. Signals represented by 'R' are restraining signals and signal 'O' is the operating signal. The output produces a zero pulse and fires a thyristor circuit or it can be fed to a level detector and integrator and thence to the thyristor. The relaying scheme therefore requires -

i) zero crossing detector

ii) delay or pulse unit

iii) measuring unit

iv) AND gate

Maloperation due to voltage spikes has been reported in the performance of these relays. The relay without an integrator has a tendency to over shoot which has been stated to be about 15% but this has been considerably reduced by having the integrator in the circuit.

3.4.10. In 1969, K.S. Mehta et al[49] described a new type of phase comparator which operates on double the normal angular limits and which strikes a particularly fine balance between static single and dual phase comparator during transient conditions. The relay has an angular over reach of less than 5% and an operating time of about 3/4 cycle. The relay particularly overcomes the over-reach/underreach of static relays during transient conditions, the nature of the over-reach depending upon the polarity of the d.c. offset. Dual comparators overcome the

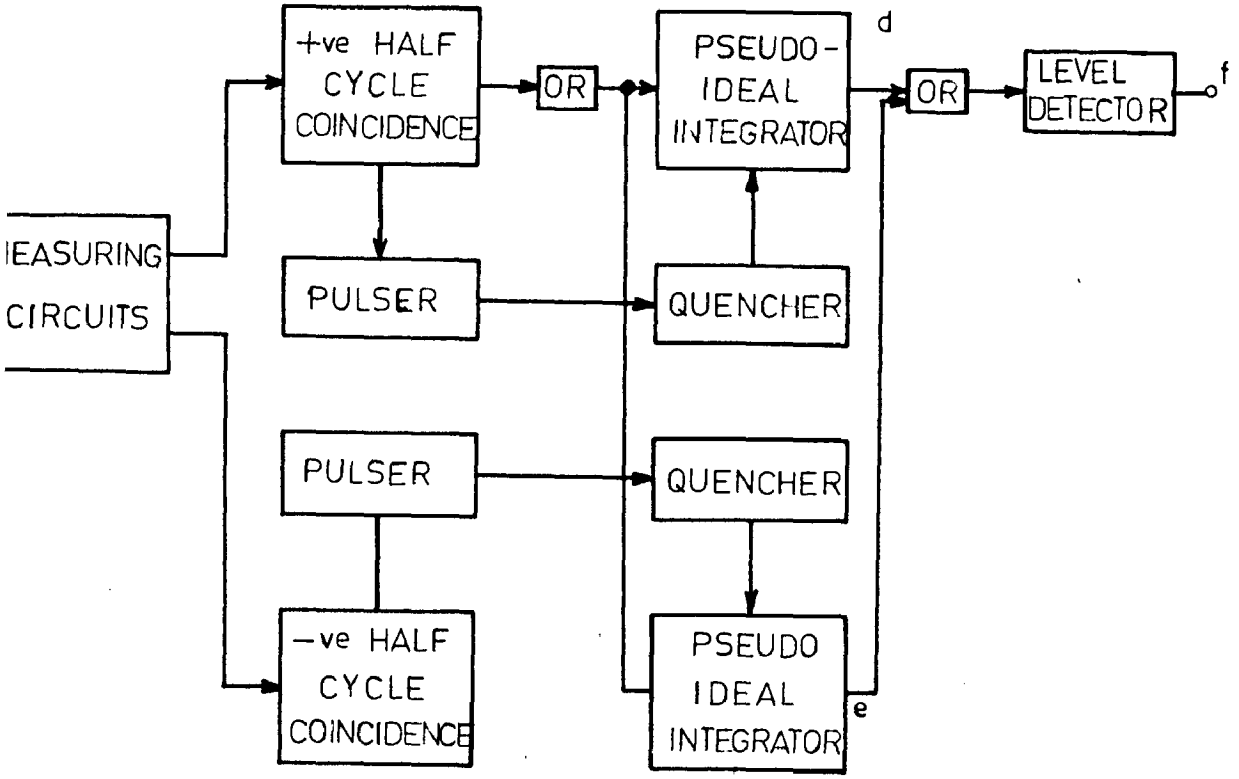


FIG. 3.10

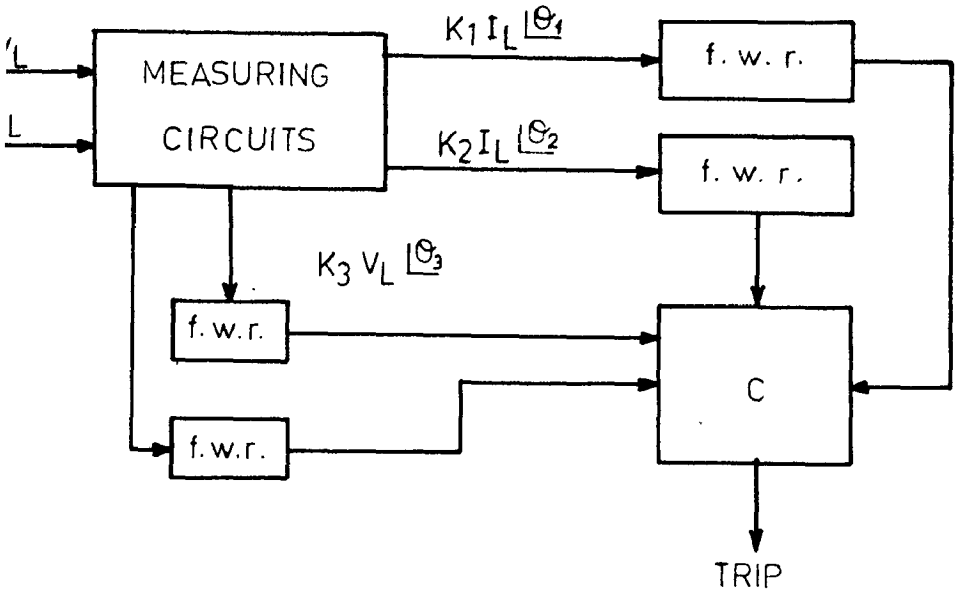


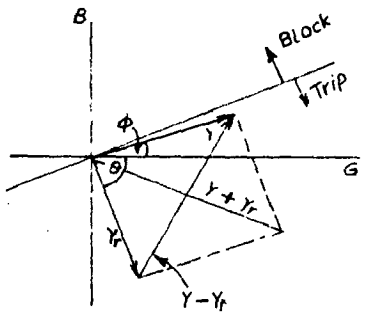
FIG. 3.11

offset but at the cost of operating time. The block diagram of the scheme is as shown in fig.3.10. The operating principle is that phase comparison is carried out both during the +ve and -ve half cycles and the resulting coincidence outputs are OR gated. The output of the OR gate is integrated and fed to a level detector and the quenching of the integrator is carried out at the end of each pair of coincidence measurements. An arrangement of this kind with a single integrator will both over-reach and under-reach depending upon the polarity of the d.c. offset and the sequence of phase measurements. The degree of over-reach/underreach is a function of the X/R ratio of the line and the amount of d.c. offset. The under reach is avoided by using two integrators and quenchers as shown. The test values of the over-reach/under reach values tabulated indicates that the angular over reach is less than 5% even in the worst case of X/R ratio equal to unity.

3.4.11. In 1970, H.P. Khincha[4C] et al described the development of amplitude comparator techniques based on the instantaneous comparison of the amplitude of the signals derived from primary line quantities. The block diagram of the scheme is as shown in fig.3.11. The scheme allows all the conventional and special characteristics of the distance relays by suitable adjustment of the constants in the relay circuitry.

N. Ramamoorthy et al[50] reported in 1970 the new developments in amplitude and phase comparison techniques for distance relaying with the amplitude comparator having its base of operation on the integrals of the rectified voltage and current waveform

ADMITTANCE DIAGRAM



IMPEDANCE DIAGRAM

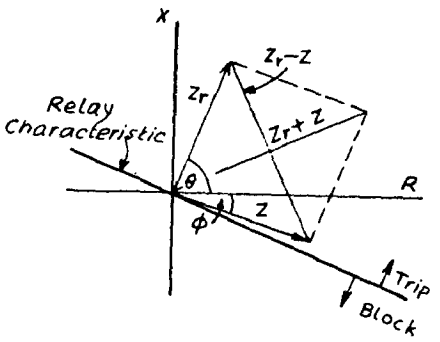
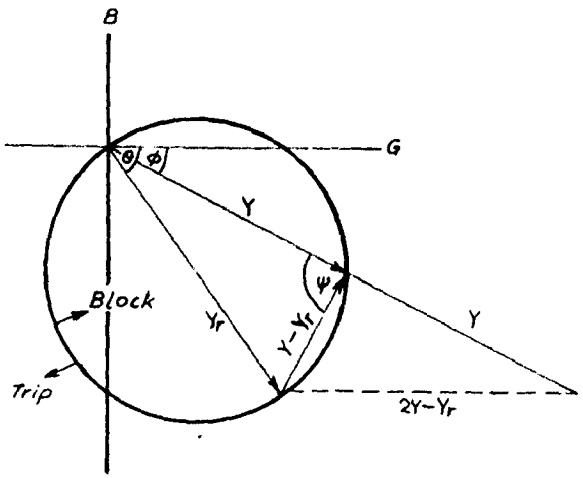


FIG. 3.12 — DIRECTIONAL RELAY CHARACTERISTIC



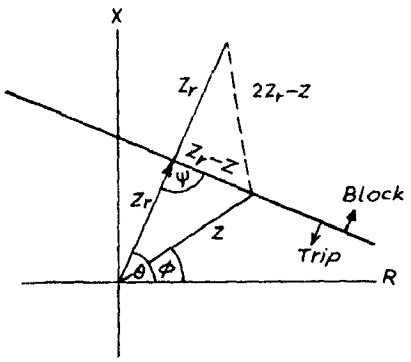


FIG. 3.13 — ANGLE IMPEDANCE RELAY CHARACTERISTIC

obtained at the end of each half cycle. The relay operation is shown to be immune to high frequency components and is less dependent on d.c. transient effects. Operational amplifiers have been used and the author has suggested that the use of I.C.'s will make the relay circuits more compact and economical.

3.4.12 Types of Static Distance Relays

These are classified by their characteristics.

3.4.12(i) Directional Relay

This is strictly not a distance measuring relay but has been included as such (a) to complete the mathematical pattern since it is the dual of the impedance relay (b) because it is required for some types of distance relays which are not inherently directional.

Its characteristic is a straight line passing through the origin on either the impedance or Admittance diagrams. The characteristic results from comparing the voltage inputs V and IZ_r in a phase comparator, and is also equally obtained by comparing their sum and difference namely ($V + IZ_r$) and ($V-IZ_r$) in an amplitude comparator (Ref. Fig.3.12.) In (a) and (b) Phase Comparator trips when $90^o > (\phi - \theta) > -90^o$ and Amplitude Comparator in (a) trips when $|Z_r+Z| > |Z_r-Z|$ and in (b) when $|Y_r+Y| > |Y_r - Y|$.

3.4.12(ii) Angle Impedance Relay

It's characteristic on an impedance diagram is offset from the origin by biasing the voltage drop across the replica impedance. Refer Fig.3.13.

In a phase comparator, the relay trips when $90^{\circ} > \psi > -90^{\circ}$ where

$= \text{Ang} \left[Z_r/(Z_r-Z)\right]$. In an amplitude comparator the relay trips when $|Z| > |2Z_r-Z|$

i.e. $Z^2 > 4 Z_r^2 - 4 Z_r Z + Z^2$

i.e. $Z_r (Z_r-Z) > 0$

$$Z_r \left[Z_r - \frac{V}{I} \text{Cos} (\phi - \theta)\right] > 0$$

or $^{\circ} IZ_r \left[IZ_r - V \text{ Cos} (\phi - \theta)\right] > 0$

On an admittance diagram the characteristic is a circle passing through the origin whose diameter is equal in length to the reciprocal of the perpendicular from the impedance characteristic to the origin and to cause tripping the head of theadmittance vector must extend outside the circle.

This characteristic is also obtained in the polarised current relay under sampled distance relays[47] by I_L and V_L at θ° after current zero.

3.24.12(iii) Reactance Relay

This is a particular case of the Angle Impedance Relay in which the reactive component of the impedance is measured. It's characteristic is parallel to the resistance axis on the impedance diagram and a circle passing through the origin on the Admittance diagram. Refer Fig.3.14.

ADMITTANCE DIAGRAM

IMPEDANCE DIAGRAM

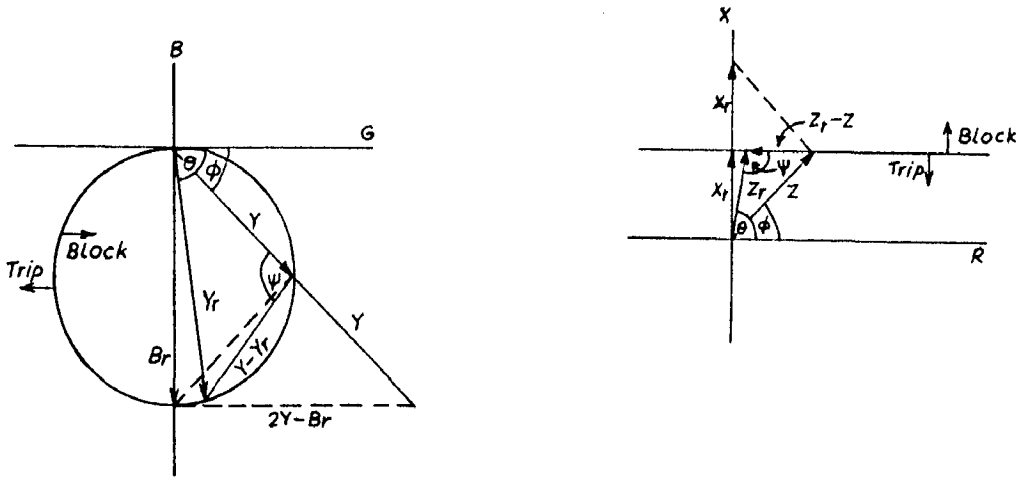


FIG. 3.14_REACTANCE RELAY

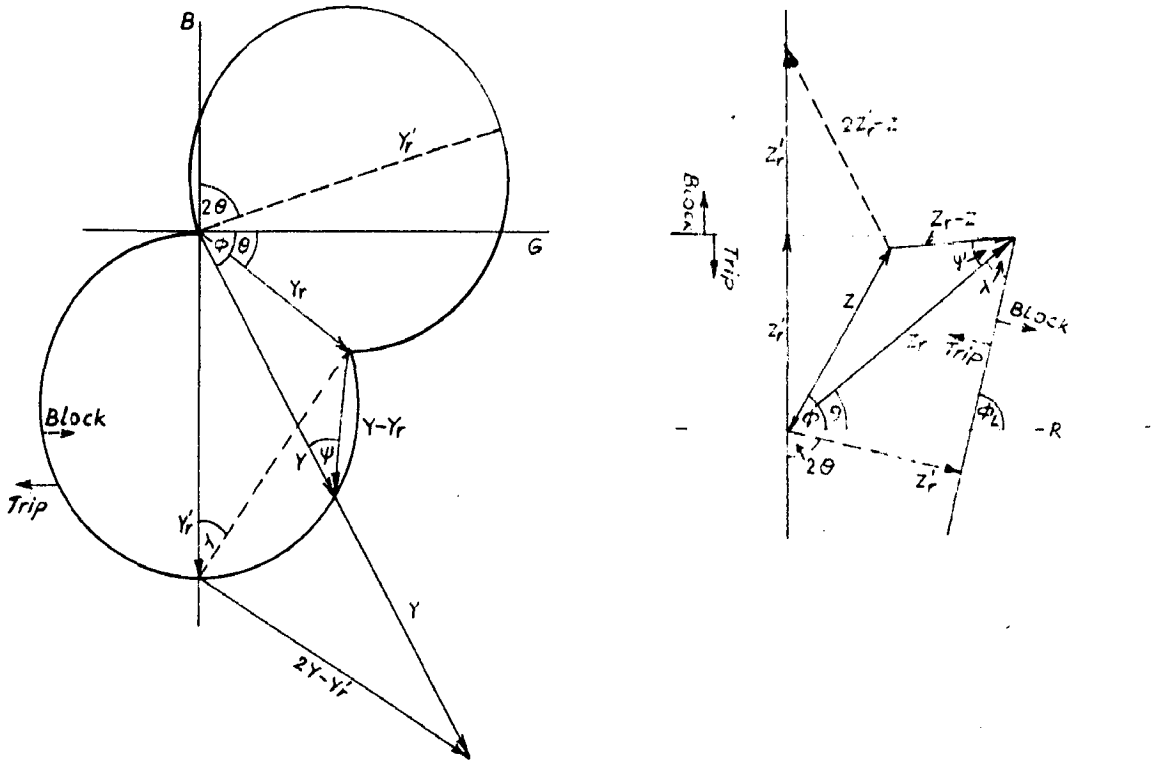


FIG. 3.15__RESTRICTED REACTANCE RELAY

In the phase comparator the quantity IZ_F is compared with $(IZ_F - V)$ and the relay trips when $\pi > (\psi + \theta) > 0$ in both the above diagrams. Here θ is the phase angle of the replica impedance Z_F. If Z_F were a pure resistance then ψ would be 90^0.

In the amplitude comparator on the Impedance Diagram the relay trips when $|Z| < |2Z_F - Z|$ and the voltage inputs to the comparator are V and $2IZ_F - 2IR_F - V$ where R_F is made equal to the resistance of the replica impedance, thus leaving it's reactive component X_F only, and in the case of the Admittance diagram it trips when $|2Y - B_F| > |B_F|$. This characteristic is also obtained in the current polarised relay under compled distance relays[47] by coupling I_L and V_L at different intervals of time i.e. V_L at $\theta = 0$ and I_L at $\theta = \psi$

3.4.12 (iv) Restricted Resistance Relay

The characteristic on the impedance diagram is a straight line bent at a predetermined point. On the admittance diagram the characteristic is a couple of circular arcs. Ref. Fig.3.15.

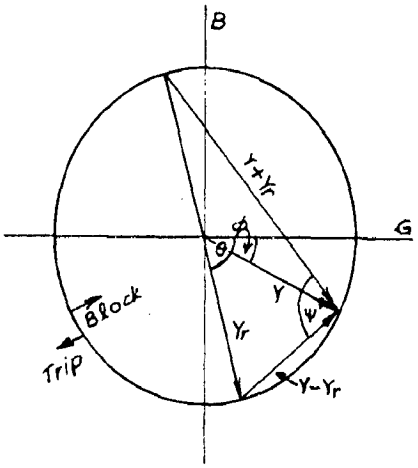
The inputs to this relay are similar to those of the normal resistance relay and the tripping criterion is similar except that the limiting values of ψ are $\pm \lambda$ instead of $\pm 90^0$.

In a phase comparator IZ_F is compared with $(IZ_F - V)$ and in the amplitude comparator the inputs are $|V|$ and $|2IZ_F - V|$.

3.4.12(v) Impedance Relay

It's characteristic is a circle at the origin on both the Impedance and Admittance diagrams. Ref. Fig.3.16.

ADMITTANCE DIAGRAM



IMPEDANCE DIAGRAM

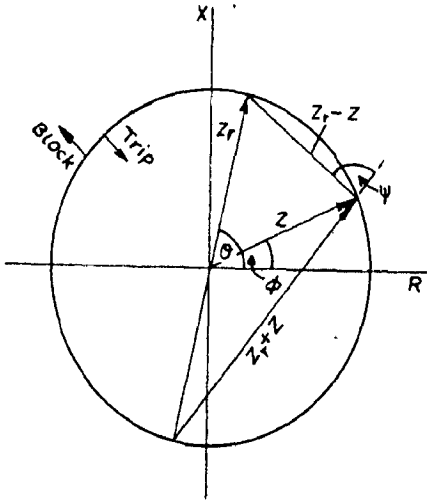
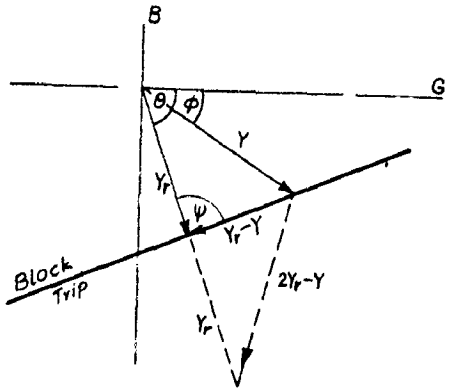


FIG. 3.16_IMPEDANCE RELAY



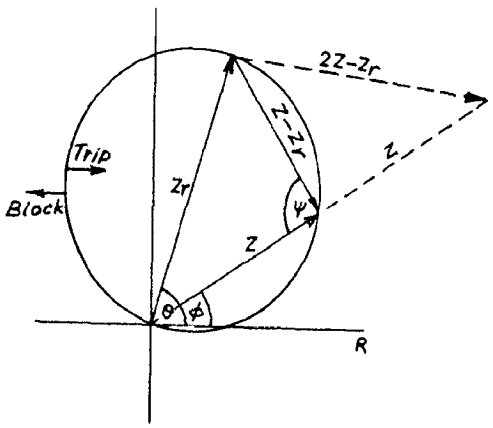


FIG. 3.17_ANGLE-ADMITTANCE (mho) RELAY

Impedance is inherently an amplitude comparison of current and voltage and the relay trips when $|Z| < |Z_r|$ so that the inputs required for an amplitude comparator are V and IZ_r. The phase comparator presents certain difficulties and as such is not used in distance relays.(19)

3.4.12(vi) Angle Admittance or Mho Relay

On an admittance diagram the characteristic is a straight line offset from the origin in the lagging quadrant as shown Refer Fig.3.17. On the Impedance diagram it is a circle passing through the origin as shown and is the inverse of the angle impedance relay. Refer Fig 3.17. The mho characteristics can be conveniently obtained with both the phase and the amplitude comparators. The inputs in the phase comparator are $(IZ_r - V)$ and V and the relay trips when $90^\circ > \varphi > -90^\circ$. A product device operates when

$V\left[IZ_r \cos(\phi - \theta) - V\right] > 0$ where ϕ is the angle between V and I, θ is the phase angle of Z_r.

Rearranging the above terms we have the relay to operate when $Z < Z_r \cos(\phi - \theta)$. The inputs in the amplitude comparator are $|IZ_r|$ operating and $|2V - IZ_r|$ restraining and the relay trips when $|2Z - Z_r| < |Z_r|$. This characteristic is also obtained in the voltage polarised relays under sampled distance relays(47) by sampling V_L and I_L at θ° after voltage zero.

3.4.12(vii) Offset Mho Relay

This characteristic is obtained by biasing either the impedance relay or the mho relay with an additional replica impedance Z_0 and the amount of biasing required decides the choice of the relay to be used. Both negative offsets i.e. characteristic overlapping the origin and positive offset i.e. characteristic with origin outside the mho circle can be obtained.

The characteristics of the offset mho circle on the impedance diagram and admittance diagram are as shown for negative offsets. Ref. Fig.3.10. The Mho relay with negative offset phase comparator trips when $(3/2\ \pi) > \phi > (\pi/2)$ in both the Impedance and Admittance diagrams. However in the case of Amplitude Comparator it trips when $|2Z-Z_F-Z_0| < |Z_F-Z_0|$ in the Impedance diagram or when $|Y_0-Y_F| < |2Y-Y_0-Y_F|$ in the Admittance diagrams. In the above Z_F is the secondary impedance of the protected line, Z_0 the impedance by which the mho circle is offset. It is seen that the radius of the circle is the mean of those impedances i.e. $(Z_F-Z_0)/2$ and the centre displaced from the origin by $C = \frac{Z_F + Z_0}{2}$.

If Z is any impedance which is on the threshold of operating the relay, the extremity of vector Z will be on the circle.

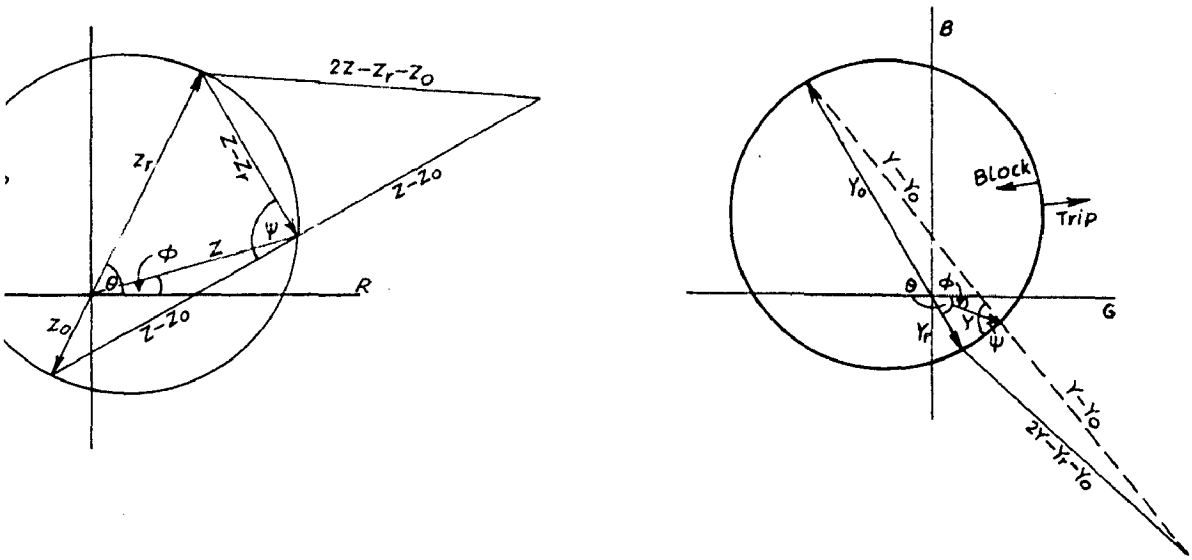
i.e. $|Z - C| = r$

$$\left| Z - \frac{Z_F + Z_0}{2} \right| = \left| \frac{Z_F - Z_0}{2} \right|$$

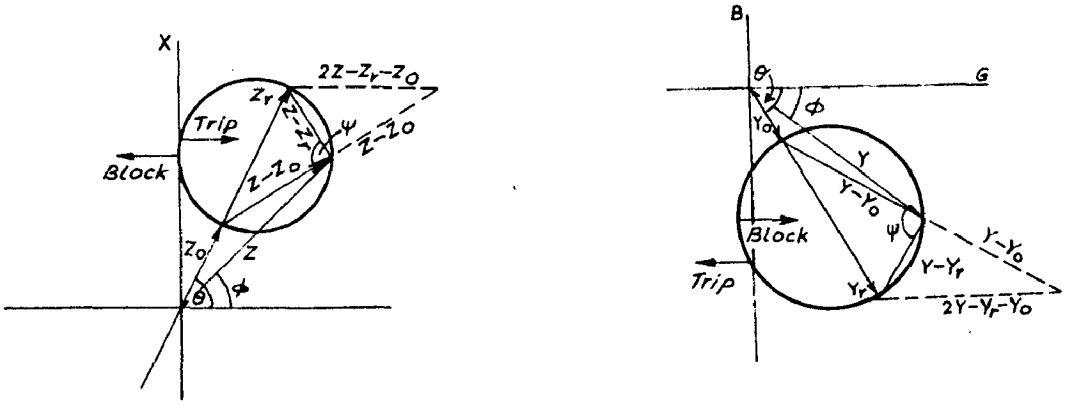
The above is the characteristic equation of the offset Mho circle on the Impedance diagram. Multiplying the above equation

EDANCE DIAGRAM

ADMITTANCE DIAGRAM



IG. 3.18 __ Mho RELAY WITH NEGATIVE OFFSET



IG. 3.19__Mho RELAY WITH POSITIVE OFFSET

throughout by 2I, we obtain the two inputs to the amplitude comparator

$$\text{i.e. } \left| 2ZI - \frac{(Z_r+Z_o)2I}{2} \right| = \left| \frac{2I(Z_r-Z_o)}{2} \right|$$

$$\left| 2V - I(Z_r+Z_o) \right| = \left| I(Z_r - Z_o) \right|$$

For a phase comparator, it can be seen from the characteristic on the Impedance diagram that the vector $(Z-Z_r)$ must be at right angles to the vector $|Z-Z_o|$ for Z to be on the circle. Hence the equation for the threshold operation of the phase comparator is when $(Z-Z_o)(Z-Z_r)\cos\phi = 0$

If ϕ is the angle between the two vectors operation occurs when $270^\circ > \phi > 90^\circ$. in a rectifier bridge comparator or $180^\circ > \phi > 0^\circ$ in a spike and block phase comparator (sinewave). The alternative method of bias which gives the positive offset is obtained by polarising the voltage inputs of the phase comparator to give inputs $(V-IZ_r)$ and $(V-IZ_o)$ corresponding to equation.

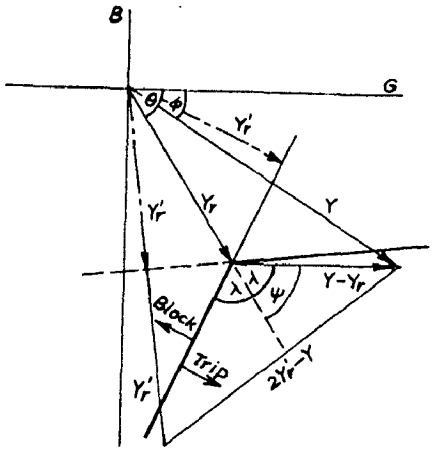
$V-IZ_o - IZ_r = V-IZ_o$ at threshold

or $(Z-Z_o-Z_r)(Z-Z_o)\cos\phi > 0$ for tripping

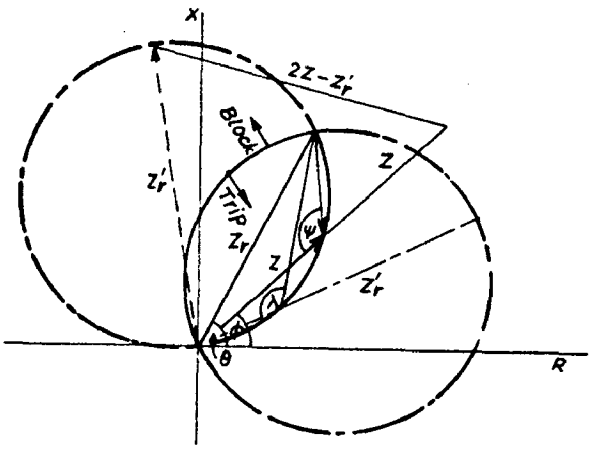
However the characteristic for the amplitude comparator is that the bias is applied to only one of the inputs which are IZ_r and $V-IZ_r-IZ_o$ and tripping occurs when

$$|Z_r| > |Z - Z_r - Z_o|$$

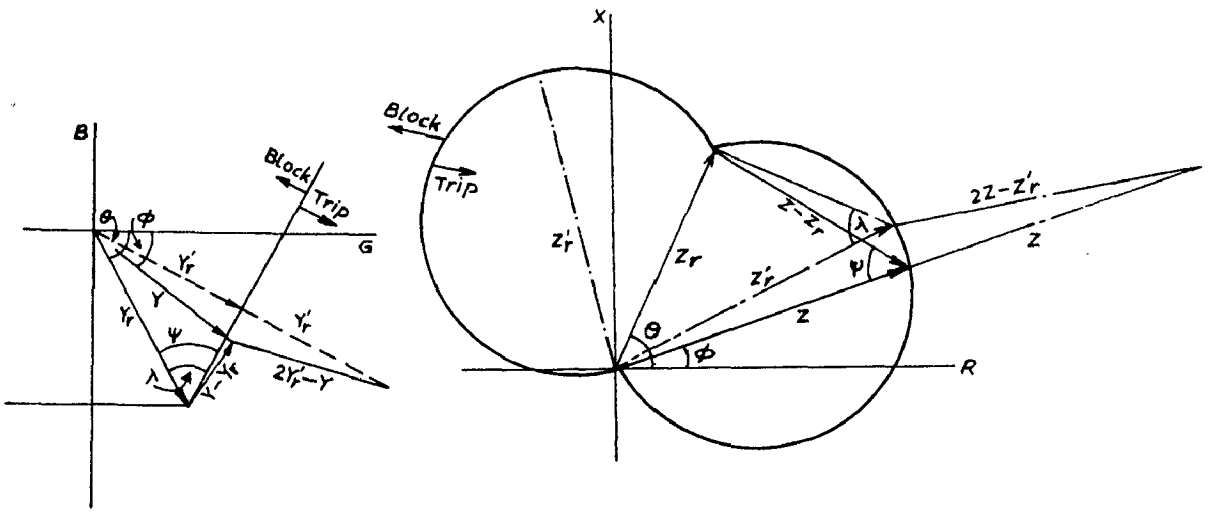
ADMITTANCE DIAGRAM



IMPEDANCE DIAGRAM



.20(a)_Mho RELAY WITH COMPARATOR THRESHOLD ANGLE > 90°



0(b)_Mho RELAY WITH COMPARATOR THRESHOLD ANGLE < 90°

The characteristics are plotted on both the Impedance and Admittance diagrams as shown. Ref. Fig.3.19.

3.4.12 (viii) Restricted Mho Relay

The mho relay characteristic can be modified by making the operating angle of the phase comparator not equal to 90^0, just as in the case of the Restricted Reactance Relay. The Mho circle consists of two sectors of a circle which are semi-circles when $\lambda = 90^0$ making an impedance characteristics Ref. Fig.3.20. When $\lambda > 90^0$ as shown in fig the sectors are less than a semi-circle and the impedance characteristic becomes narrow and makes the relay less vulnerable to power swings. When $\lambda < 90^0$ the sectors are larger than semi-circles and the impedance characteristic becomes apple shape providing more tolerance for fault resistance which is advantageous for short lines and ground faults.

3.5. SPECIAL CHARACTERISTICS

3.5.1. It was in 1962 that John E. Skudorna in his paper(17) proposed a relay which will provide new types of pick up characteristics such as conic, hyperbola, parabola, ellipse by simple adjustments of the circuitry of the ohm and mho relays.

The mho pick up characteristic has proved very valuable in protecting long transmission lines which are heavily loaded as they are less likely to trip on power swings, than the ohm and impedance units. The extension of this distribution indicates that an elliptic pick up characteristic wouldbe ideal because

it is less likely to trip on power swings than a conventional mho unit. With this end in view, he in his paper outlined the possibility of manufacturing a relay in which the special characteristics as cited above could be obtained. It was however a novel idea then and the mathematical basis as presented in his paper for the various characteristics is as follows.

The pick up characteristic of the ohm unit is given by (Electromagnetic relays)

$$I\left[KI - E\cos(\phi - \theta)\right] = 0$$

where θ is the angle of the relay characteristic

ϕ angle between E and I

K winding constant

Dividing the equation throughout by I^2 we have

$$K - \frac{E}{I}\cos(\phi - \theta) = 0$$

$$Z\cos(\phi - \theta) = K$$

$$Z = \frac{K}{\cos(\phi - \theta)}$$

Plotting the above equation on the Impedance diagram we obtain a straight line characteristic. Fig.3.21(a). However if a capacitor is added in the potential circuit to make $\theta = 90^{\circ}$, then

$$Z = \frac{K}{\sin\phi}$$

This gives a horizontal characteristic on the Impedance diagram Ref. Fig.3.21 (b).

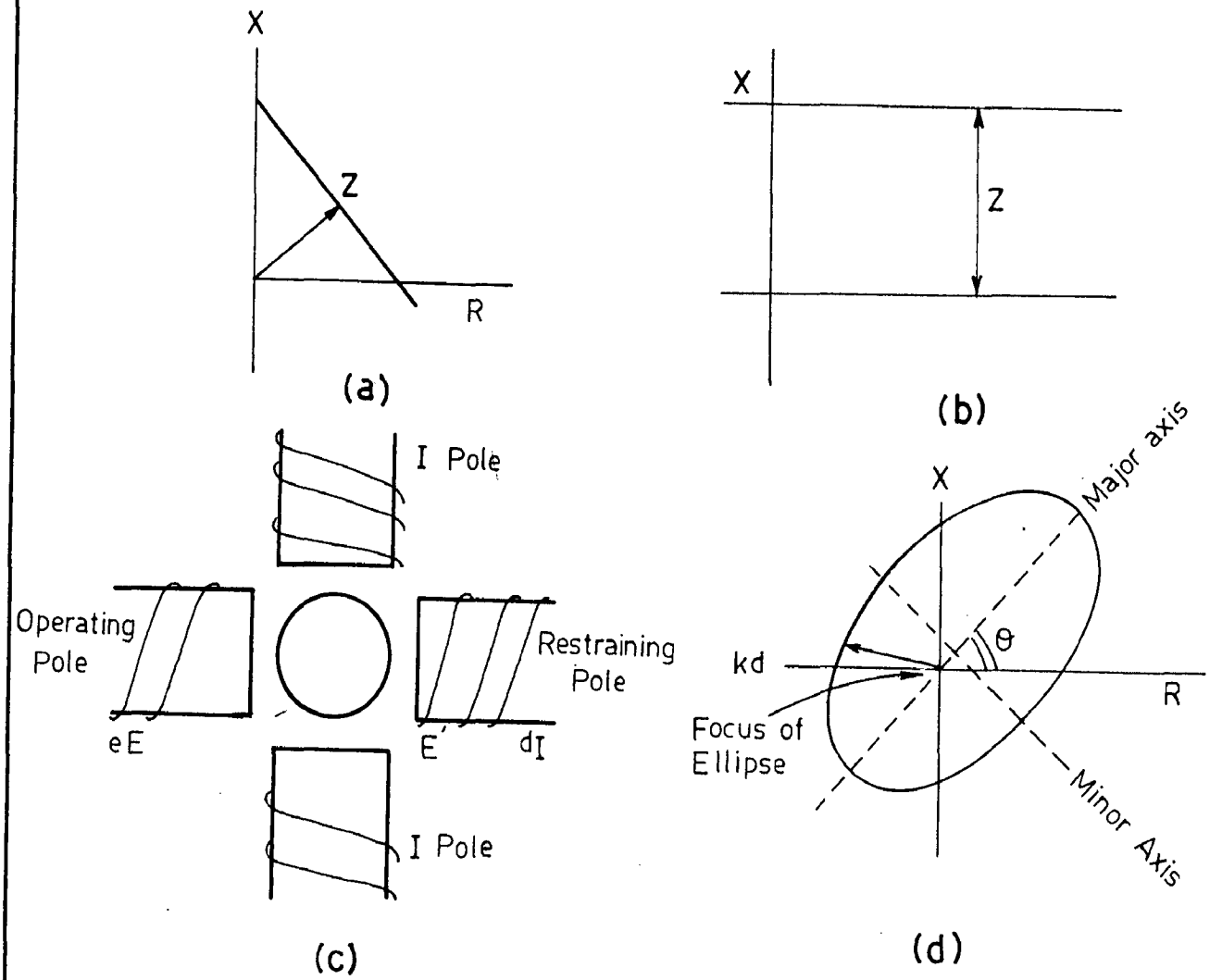


FIG. 3.21

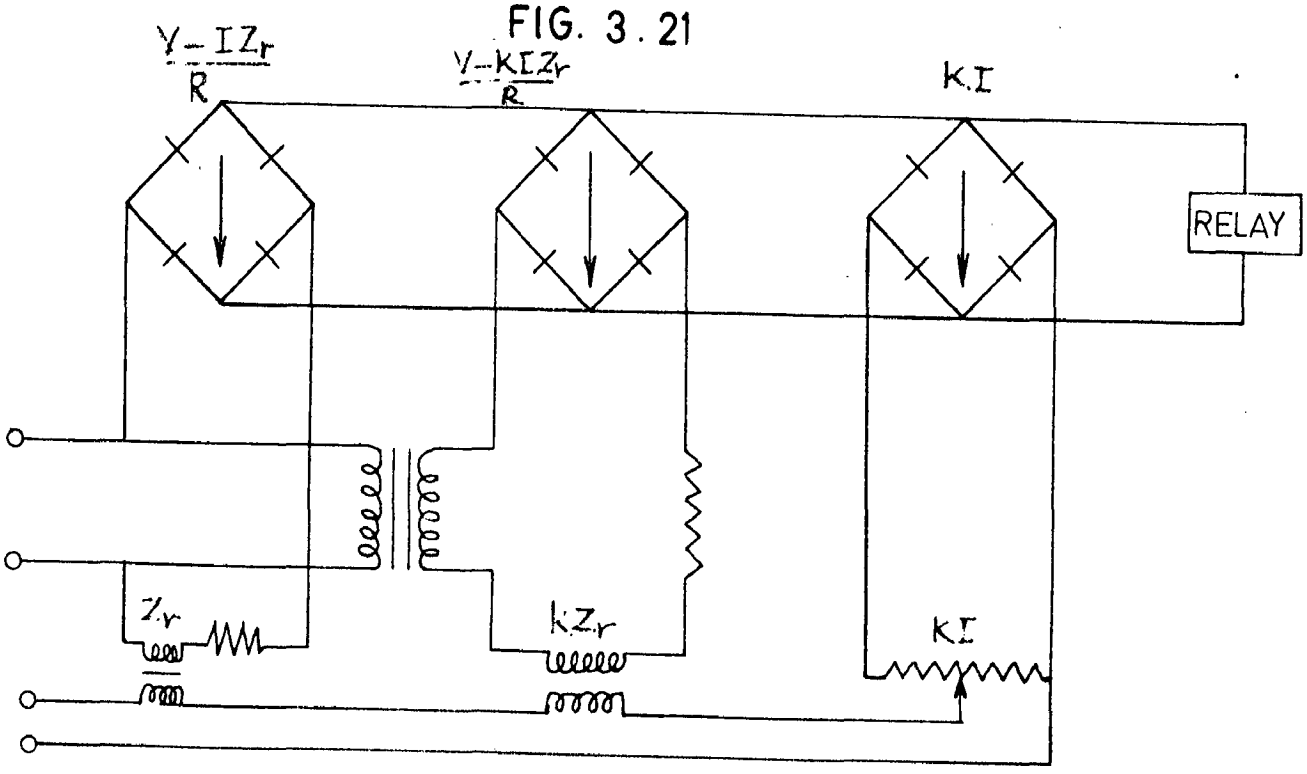


FIG. 3.22 (a)

Now referring to Fig.3.21(c) let

d = Scalar factor of proportionality, ratio of current in one winding on the restraining pole / I (Polarising current)

E = p.t. sec. voltage

K = Winding constant

E' = Voltage equal in magnitude to E but in phase with I

c = scalar factor of proportionality = voltage impressed across operating pole / E

The operating characteristic of such a relay would be

$$I\left[cE\cos(\phi-\theta) - (E' - kdI)\right] = 0$$

Dividing by I^2 we have

$$\frac{cE}{I}\cos(\phi-\theta) - \frac{E' - kdI}{I} = 0$$

$$\text{But } \frac{E}{I} = \frac{E'}{I} = Z$$

$$Zc\cos(\phi-\theta) - Z + kd = 0$$

$$Z = \frac{-kd}{\left[c\cos(\phi-\theta) - 1\right]}$$

$$Z = \frac{kd}{\left[1 - c\cos(\phi-\theta)\right]} \qquad \text{Eqn. (A)}$$

The above is a polar equation of a cone with eccentricity c

If the value of e is adjusted to be less than, equal or greater than 1 by means of an auxiliary transformer to obtain characteristics as follows:

$e > 1$	equation (A) describes a hyperbola
$e = 1$	equation(A) describes an ellipse
$e < 1$	equation(A') describes a parabola.

These have been referred to as the conic characteristics. Ref. 3.21(d).

A characteristic for e=1 is shown here elliptical. The major axis of the elliptical characteristic is inclined at an angle θ to the R-ordinate.

Kd - distance from the edge of the ellipse to the origin or focus.

d - can be adjusted to any value by an auxiliary C.T.

e - can be determined graphically as the ratio of the distance between foci of the ellipse to the length of the major axis. It can also be determined by measuring the lengths of the major and minor axis.

Let $G = \frac{\text{major axis}}{\text{minor axis}}$

Then $e = \sqrt{1 - \frac{1}{G^2}}$

$$Z_{\text{reach}}\ (\text{tripping}) = K d \left(\frac{1+e}{1-e^2}\right)$$

$$Z_{\text{offset}}\ (\text{nontripping}) = K d \left(\frac{1-e}{1-e^2}\right)$$

In the above set up all quantities can be easily obtained except for E' for which he proposed a clipper circuit. A circuitry for the conic unit was also indicated in the aforesaid paper.

It was however that Parthasarthy R.[36] in 1965 developed static circuits for these Conic Distance Relays, based upon the above mathematical treatment and the comparators used fall in the category of multi-input comparators.

3.5.2. Conic Section Characteristics

A conic section is the locus of a point which moves so that the distance from a fixed point, the focus bears a constant ratio to its distance from a straight line, the directrix.

An amplitude comparator with suitable inputs can produce any type of conic section characteristic. These inputs may be simple input quantities such as V and I or they may be derivations of ($V - IZ_r$) where Z_r is a replica impedance. A conic characteristic is also obtained with both current and voltage polarised relays under sampled distance relays[47].

3.5.2.(a) Elliptical Impedance Characteristic

The production of this ... was first described by Bratton and Hool[4] engineers of Norway in their paper presented to CIGRE in 1950 with multi input (three input comparators). The three inputs were ($V-IZ_r$), ($V - IKZ_r$) and KI where Z_r and KZ_r were replica impedances with the same phase angle and the corresponding bridge currents were $|(V-IZ_r)/R|$,

$|(V-IKZ_R)/R|$ and KI. The circuitry of the scheme deployed by them is shown. Ref. 3.22. By making $k = \left|\frac{(Z_F + KZ_R)}{R}\right|$ the equation for operation becomes

$$|V-IZ_F| + |V- KIZ_F| < |I(Z_F+KZ_F)|$$

Dividing throughout by I, we have

$$|Z -Z_F| + |Z-KZ_F| < |Z_F + KZ_F|$$

An ellipse is defined as the locus of points the sum of whose distances from two other points, the foci is constant. Thus the above equation describes an ellipse going through the origin in which the first two terms of the above equation are the distances of the two foci from the curve and the third the major diameter. By suitably modifying the inputs an offset ellipse characteristic with one focus at the origin can be obtained whose equation is described by

$|Z -Z_F| + |Z| < |Z_F + 2KZ_F|$ and is shown in Fig. 3.22(c)

Similarly by varying the constants other conic sections can be obtained such as hyperbola, parabola, limacons etc.

Conic section characteristics can also be obtained by using hybrid comparators. Hybrid comparators are combinations of amplitude and phase comparators wherein one type of comparator is supplied with one of its inputs from a comparator of another type. The inputs if related by the following polar equation will enable to obtain the desired characteristics.

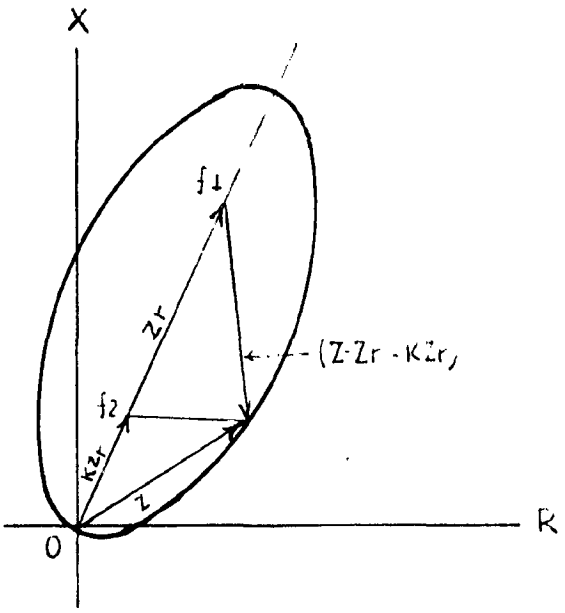


FIG:-3.22(c).

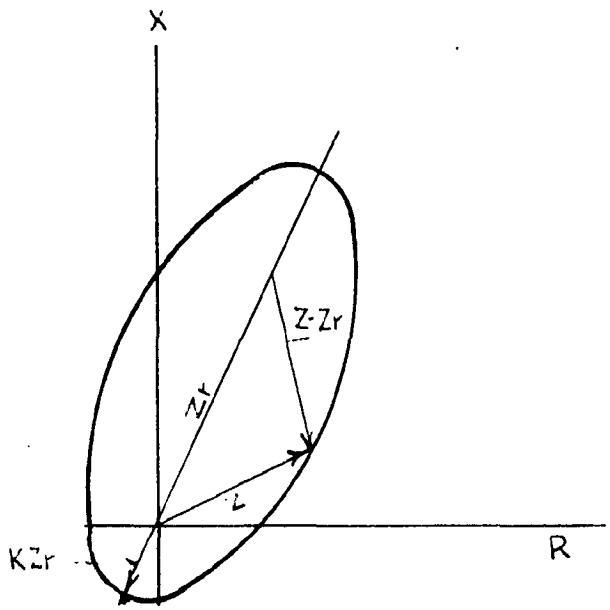
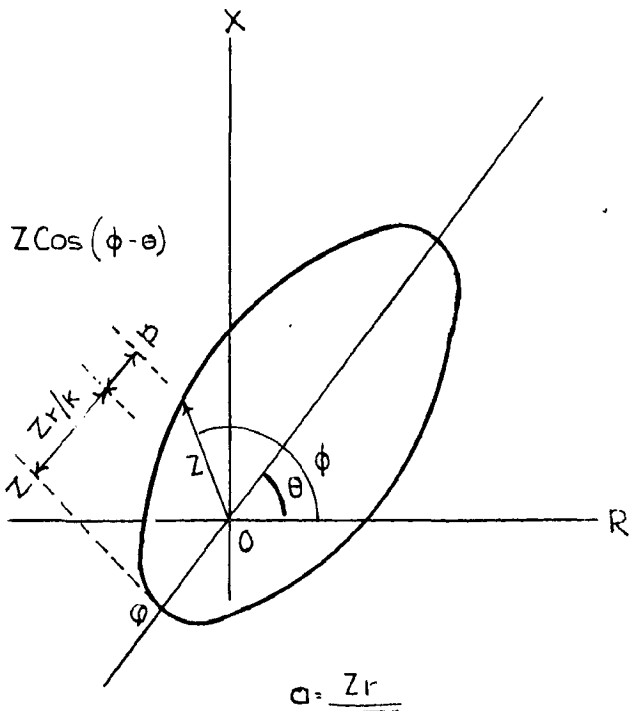


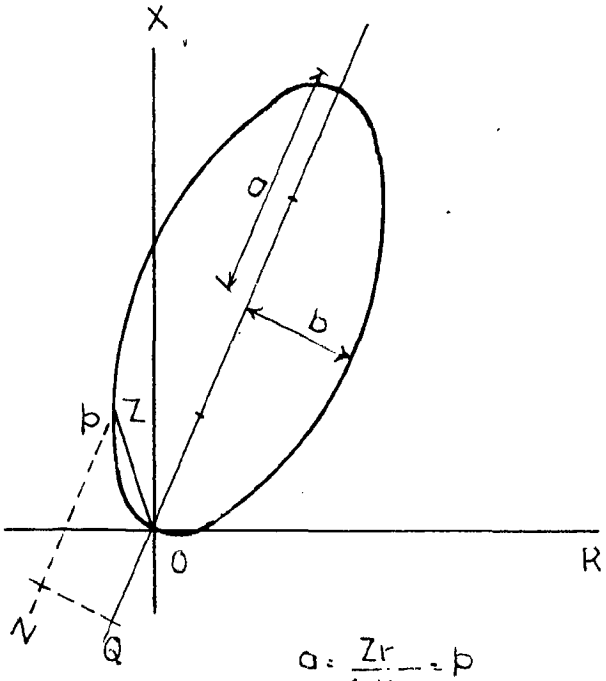
FIG:- 3.22(C)



$$a = \frac{Zr}{\sqrt{1-K^2}}$$

$$b = \frac{Zr}{1-K^2} \; ; \; p = \frac{KZr}{1-KZr}$$

FIG:3.22(d)-FOCUS AT ORIGIN.



$$a = \frac{Zr}{1-K} = p$$

$$b = Zr\sqrt{\frac{1+K}{1-K}}$$

FIG:-3.22(e) - ELLIPSE PASSING THROUGH THE ORIGIN

$$Z = \frac{Z_r}{1 - K \cos (\phi - \theta)}$$

If $K < 1$ it is an ellipse

$K = 1$ a parabola

$K > 1$ a hyperbola

$K = 0$ a circle

The hybrid comparators may consist of an amplitude comparator with an auxiliary phase comparator in which the inputs are IZ_r, V fed directly to the amplitude comparator and KV cos (ϕ - θ) input obtained from an auxiliary phase comparator. The circuitry for the same is described by Sri K. Parthsarathy in his paper[36]. The characteristics of the ellipses are shown in Figs.3.22(d) and 3.22(e).

It is also possible to obtain conic characteristics using a phase comparator with an auxiliary amplitude comparator, and these give limacon or cardiod characteristics.

3.5.2.(b) Quadrilateral characteristics

This is theoretically the ideal characteristic for distance relays so that it's characteristic is coincident with the fault area and would include all conditions for which tripping is undesirable. The basis for the development of the quadrilateral characteristic has been indicated by A. Vitanov in his paper[37] presented to CIGRE in 1968. It is stated therein that every two points for example a point P_i and P_k in the complex impedance plane are connected with an arc α from which the segment $P_i P_k$ is seen at an angle. ($i = 1 \ldots j, k = 1 \ldots n$)

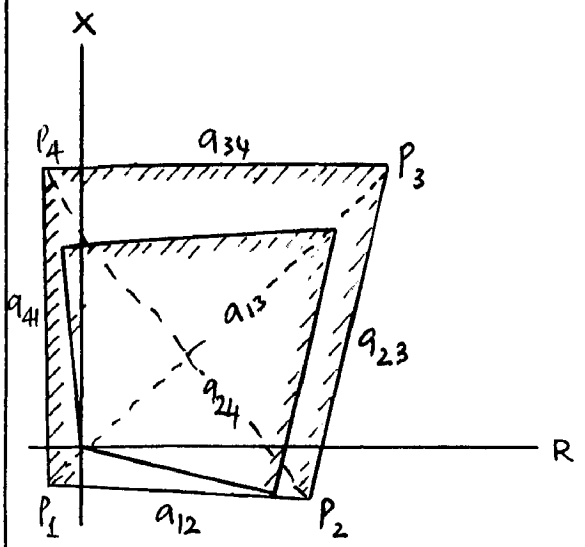


FIG:-3·23 – QUADILATERAL (a) CHARACTERISTIC.

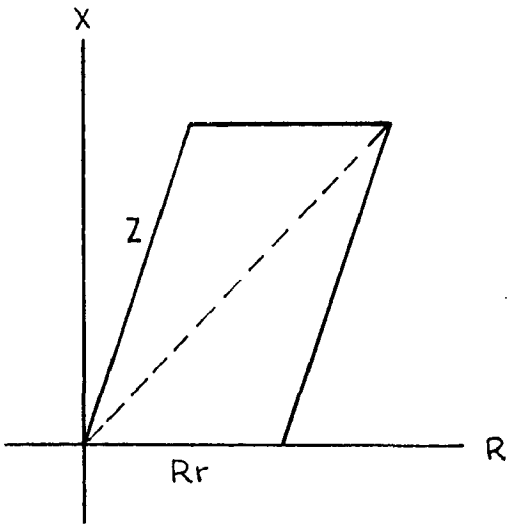


FIG:-3·23(b)- PARALLELOGRAM.

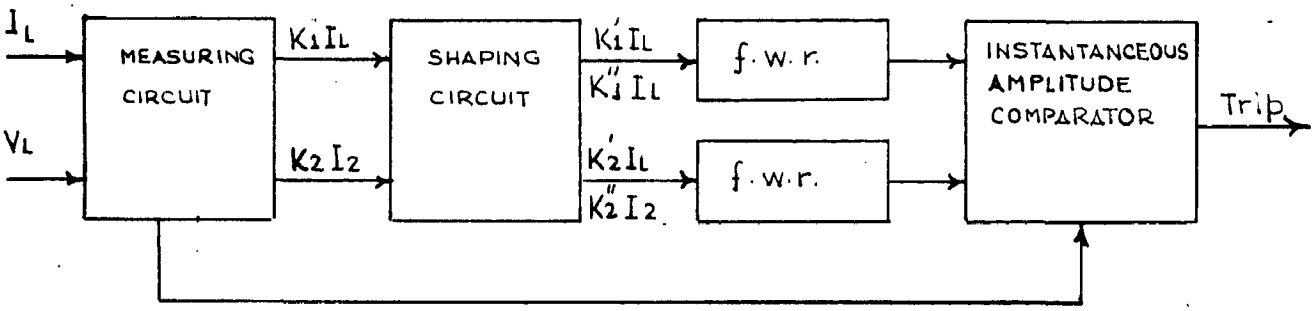


FIG:-3·24(a) PARALLELOGRAM CHARACTERISTIC.
(AMPLITUDE COMPARATOR)

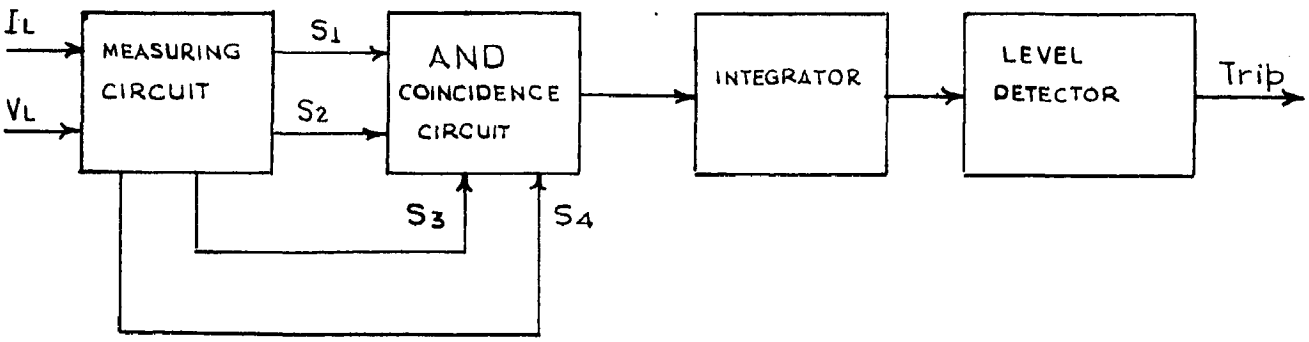


FIG:-3·24(b)- PHASE COMPARATOR.

$$\alpha_{ik} = - \arg \left(\overline{a_{ii}} / \overline{a_{ki}} \right)$$

Now if $\alpha_{ik} = \pi$ or 0, the arc is transformed respectively into a constant, or into two rays. Connecting in this way P_i to all other points depending upon the number of inputs to the comparators a quadrilateral or a polygon characteristic can be obtained.

Thus a quadrilateral characteristic is obtained by using four inputs namely

$$S_1 = Z_1 I \angle \theta_1 - \phi - K_1 \angle \alpha, V$$

$$S_2 = Z_2 I \angle \theta_2 - \phi$$

$$S_3 = Z_3 I \angle \theta_3 - \phi$$

$$S_4 = K_4 \angle \alpha_4 V$$

To enclose the fault area $Z_2 = X_F$; $Z_3 = R_F$ and $Z_1 = R_F + jX_F = Z_F$ so that the inputs are

$$S_1 = IZ_F - V$$

$$S_2 = IX_F$$

$$S_3 = IR_F$$

$$S_4 = V$$

This gives a composite characteristic ~~as shown~~ which is rectangular. However to obtain the preferred shape of a parallelogram as shown in Fig 3.23 the inputs S_1 and S_4 must be applied as pulses. Vitanov[37] has suggested to convert the input signals into rectangular pulses before being fed to the phase comparators. The circuitry developed by him and his

experimental results are stated to be in conformity with it's qualities described earlier.

3.5.3. The idea of instantaneous amplitude comparator and the subsequent development of the quadrilateral characteristic of relays in the impedance plane was reported by S.K. Basu[41] to have been developed by a Japanese firm vide quoted report of Toguchi T. in Toshiba Review in 1969 under his paper styled "Recent Trends in all Static Relaying Equipment". The same principle was also developed by Khincha H.P. et al[38,39,40] and a mode of the comparison techniques was presented in their paper[39,40] together with a mathematical theory indicating therein as to how simple and practical circuits can be developed by using a minimum number of inputs to obtain improved pick up and polar characteristics. Accordingly their block schematic diagrams to obtain a parallelogram polar characteristic and a quadrilateral characteristic are as follows. [Refer Fig 3.24(a) & (b)]

3.5.4. Sri Anil Kumar[28] presented a new technique using principles of multisignal relaying for the synthesis of an universal type quadrilateral polar characteristics. The method consisted in the determination of the phase sequence of a set of voltage phases and the provision of a trip signal for one sequence while blocking for the other. Two versions using ferrite core logic and another using transistor logic were described. The application of ferrite cores with low curie temperatures in the vicinity of room temperatures to protective relaying was described by K. Murakami et al. in his paper[42] using Mn- Cu ferrites with proper manufacturing process.

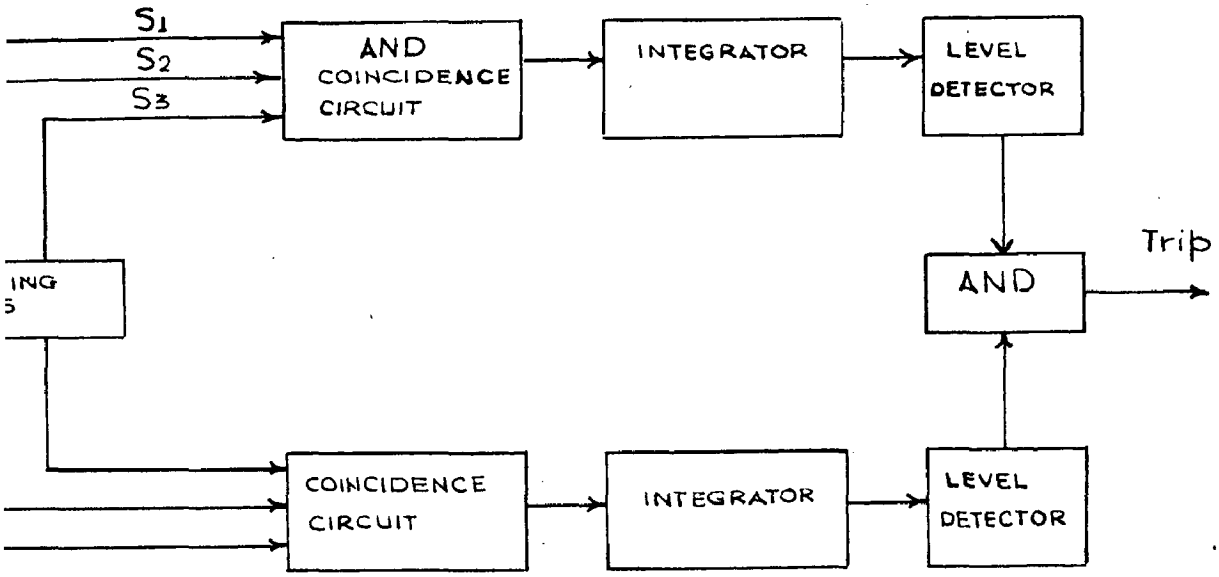
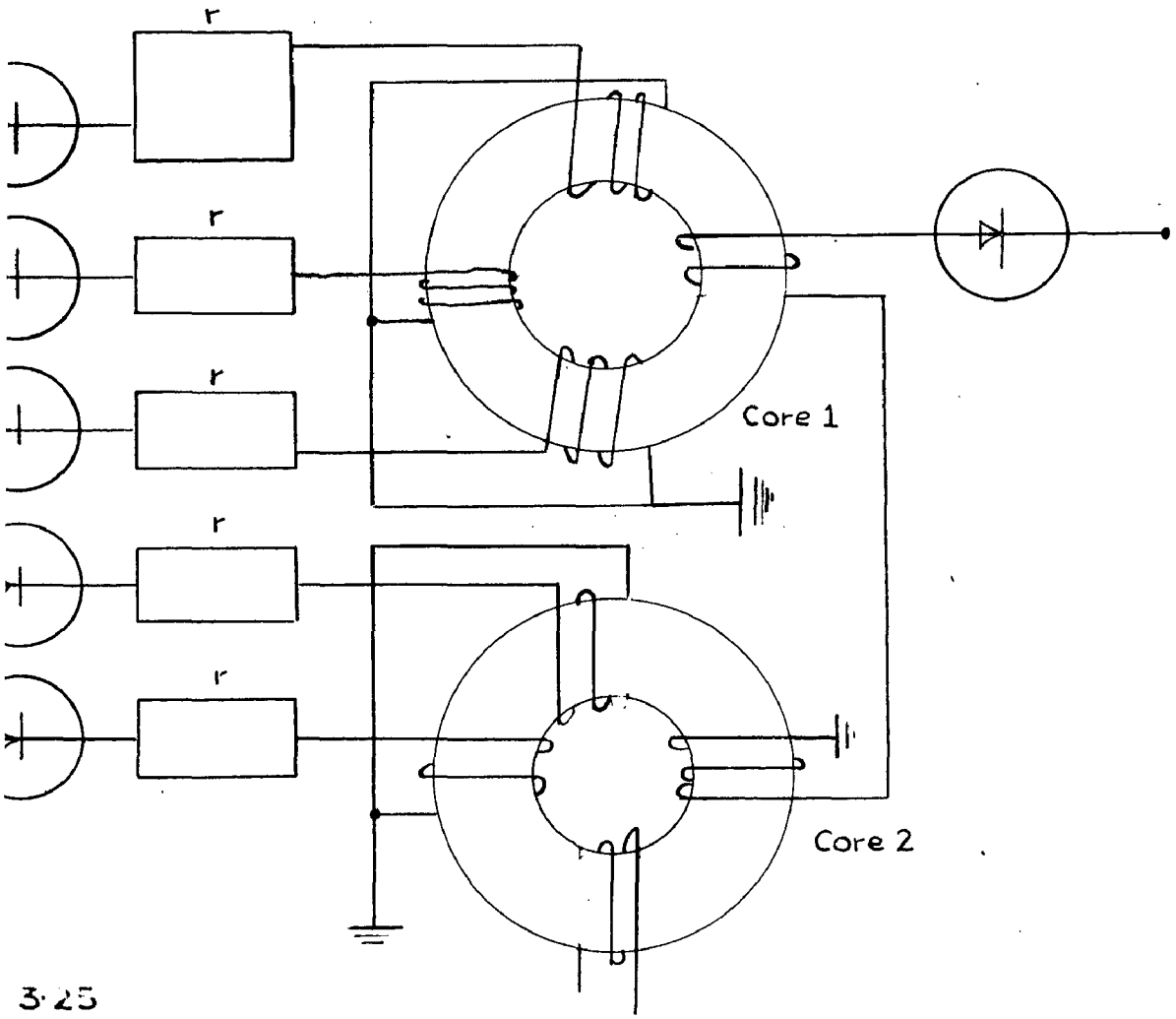


FIG:- 3·24(b) QUADRILATERAL CHARACTERISTIC.



Those ferrite cores claimed to be more compact, more reliable within the rated temperature, consumes less power, has no recoil, economically easy to manufacture and above all had the merit of simplicity without the requirements of any d.c. supply.

The ferrite core version as claimed in his paper[28] was found to be flexible permitting independent control of the characteristic on the impedance plane by suitable adjustment of replica impedance angles. The maximum operating time of this version is about 20 ms. for all switching angles and with faults within 95% of the protected line section and the maximum transient over reach recorded was about 8%. The unit with ferrite core logic is reproduced here in Fig. 3·25

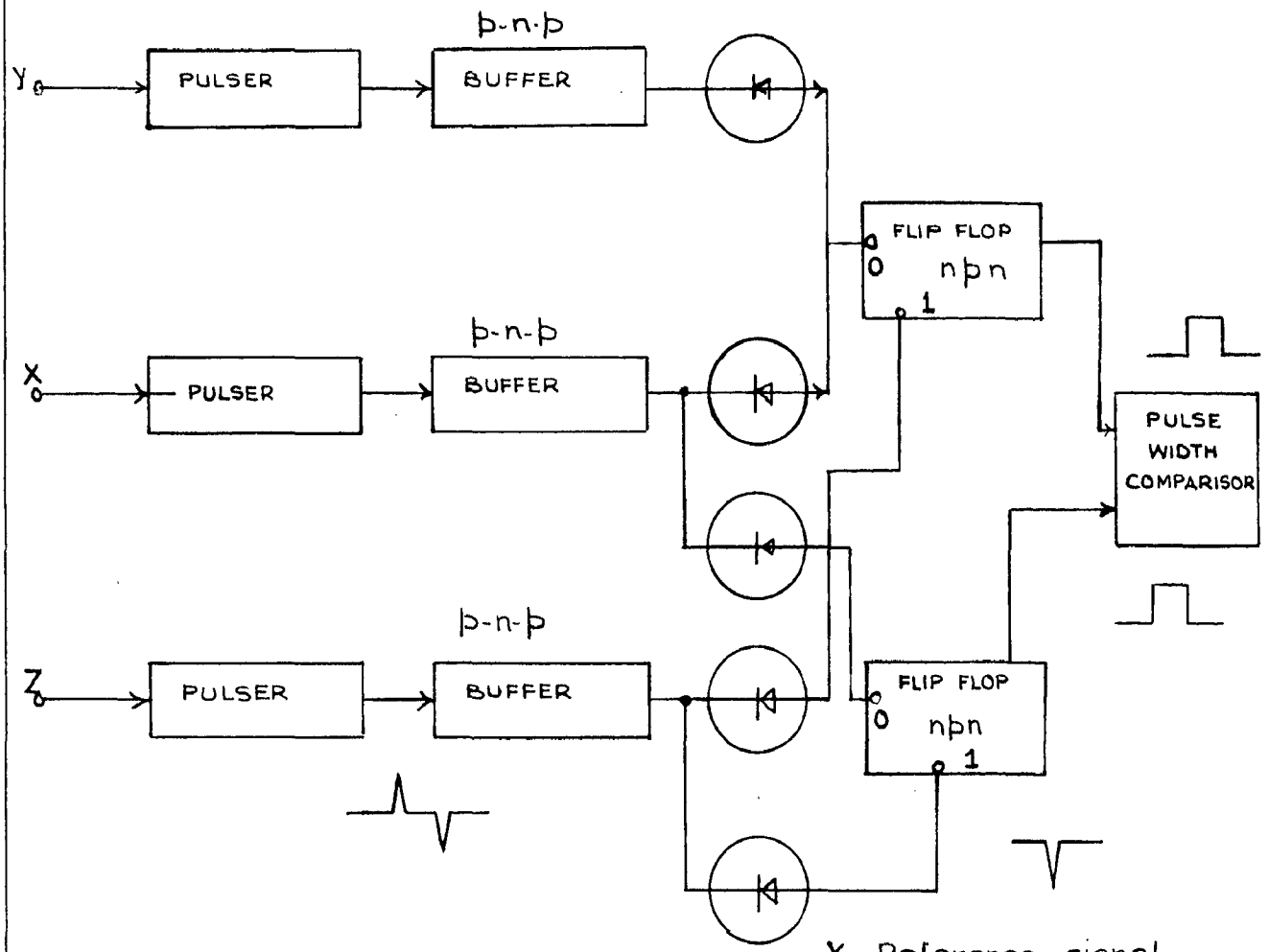
Two ferrite cores with rectangular hysterisis loops constitutes the unit and both the cores have only one output winding. Core 1 has three inputs while core 2 has two input windings. The windings are connected to arbitrary signals x,y,z through diodes so that only one half is effective in switching the cores. The input windings are connected in opposition. A positive state of magnetisation is designated as +1 while 0 indicates the negative state. In the output winding the change from negative state to the positive state of magnetisation is referred to as +1 while the reverse is designated as -1. With this convention signal 'x' is arranged to set zero on both the cores is termed as the reference signal. The signal 'y' acting on core 1 only with a zero setting is the polarising signal. Input 'z' signal with a + 1 on both cores is termed the resetting signal. The windings are so arranged to form the following logic.

	State	
Signal	Core 1	Core 2
x	0	0
y	0	-
z	1	1

Specific signals S_1, S_2, S_3 which may be the relaying signals can substitute arbitrarily signals x,y,z in any random manner so that the choice of signals providing the resetting functions decides the phase sequence under which an output is produced. A table is also given for the tripping phase sequence for various combination of resetting and polarising signals.

The block schematic of the semi conductor version is as follows: Refer Fig 3·26(a)

The output waveforms of the flip flop are that with the blocking sequence, the pulse widths are equal and occur at the same instant of time while for tripping sequence they are either different or occur at different instants. The discrimination is effected by the pulse width detecting done by a single n-p-n transistor. The disadvantage of the semi conductor flip flop units are the requirements of d.c. for transistor power and these sources act as a medium for the transmission of parasitic signals. These sets add to the bulk of the relaying equipment and impose additional C.T. burden. But the transistor circuitry is accurate, sensitive and a close tolerance on the component values is not required. The ferrite cores on the other hand can be built into a more compact design as it does not require any d.c. supply.



X- Reference signal.
Y- Polarising signal.
Z- Reseting signal

FIG:- 3.26 (a)

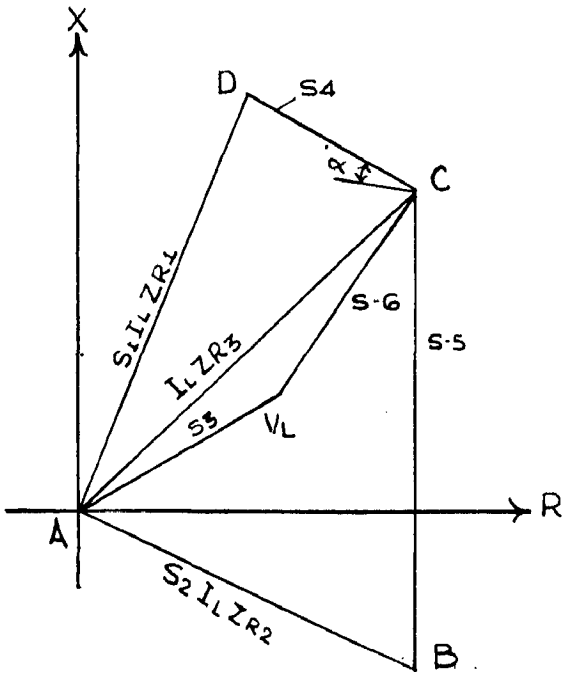


FIG:- 3.26 (b)

But it demands the use of closely controlled cores so that their output values have equal heights and any deviation from the desired values causes maloperation. The factors contributing to these are -

(a) improper design of output winding

(b) hysteresis loops being different from being rectangular

(c) unequal magnitude of input signals and

(d) unequal slopes of B-H loops prior to saturation.

Inputs to obtain characteristic DAR are [Refer Fig 3.26(b)]

$S_1 = I_L Z_{R_1}$ - reference

$S_2 = I_L Z_{R_2}$ - polarising

$S_3 = V_L$ - restraining

Inputs to obtain characteristics DCB are

$S_4 = I_L Z_{R_1} - I_L Z_{R_3}$ - reference

$S_5 = I_L Z_{R_2} - I_L Z_{R_4}$ - polarising

$S_6 = V_L - I_L - I_L Z_{R_3}$ - resetting

The relay is directional and the replica impedances Z_{R1} and Z_{R3} are designated as reactors with angles of 80° and 70° ZR_2 is realised through a combination of the output of a transactor and a resistance drop to give an angle of -20°. The accuracy of the relay has been quite good upto a source/line impedance of 25 and has a minimum voltage of 1.0 V for directional operation for all positions of impedance vector.

3.5.5. In 1973, Ayhan Tureli[51] described the mode of operation of multiple input moving coil relay with fully rectified inputs and with transistorised block average phase comparator and rectifier bridge amplitude comparator. He has also analysed the functioning and characteristics of the relay while describing the special threshold characteristics formed by the inter-section of straight lines, circle etc. Linear Amplitude Comparator is realised by adding additional coils to a moving coil relay and energising them from fully rectified signal sources. The threshold conditions for the linear multiple input-out amplitude comparator is shown to be satisfied when the sum of the distances corresponding to the inputs connected in the positive manner is equal to the sum of the distances corresponding to the inputs connected in the negative manner. By arranging the location of the points $Z_1, Z_2 \ldots\ldots Z_n$ on the R-X diagram and choosing K_1, $K_2 \ldots\ldots$ K_n suitably, characteristics such as elliptic, hyperbolic, circular and other specially shaped are shown to be obtained.

A block diagram to obtain an elliptic characteristic is shown in reference Fig.3.27 with three inputs. It is also shown that non linear types of amplitude comparators as is obtained with a three input rectifier bridge and a transistor amplifier also give correspondingly the same results as with a linear type of amplitude comparator.

3.6. RELAY RESPONSE[76]

Before we analyse the reaction of a relay to a system disturbance, or the relay response, it is worthwhile to consider the primary, secondary and system impedances.

3.6.1. Primary and Secondary Impedances

The impedance measured by a distance relay is the ratio of the voltage and current presented to it. Either primary or secondary quantities may be considered, with corresponding primary impedance Z_p or secondary impedance Z_s, the relation between the two is

$$Z_s = Z_p \text{ (C.T. ratio)/ (V.T. ratio)}$$

Relay calibration, characteristics and setting calculations are in terms of secondary impedance, which is usually based on 1 Amp. or 5 Amp. and 110 V.

3.6.2. System Impedance

The impedance of the power system may be divided into two parts. Firstly, the impedance behind the relaying point, including the generators, feeders, transformers, etc., forms the source impedance. The source impedance must be known, although not necessarily with great accuracy, to determine the fault levels and impedance ratio of the system.

The second part is the impedance to the fault in front of the relaying point, which is governed by the geometrical arrangement, size, shape, spacing and material of the conductors, mutual coupling of parallel circuits and, for earth faults, the nature of the return path to the system neutral point. The

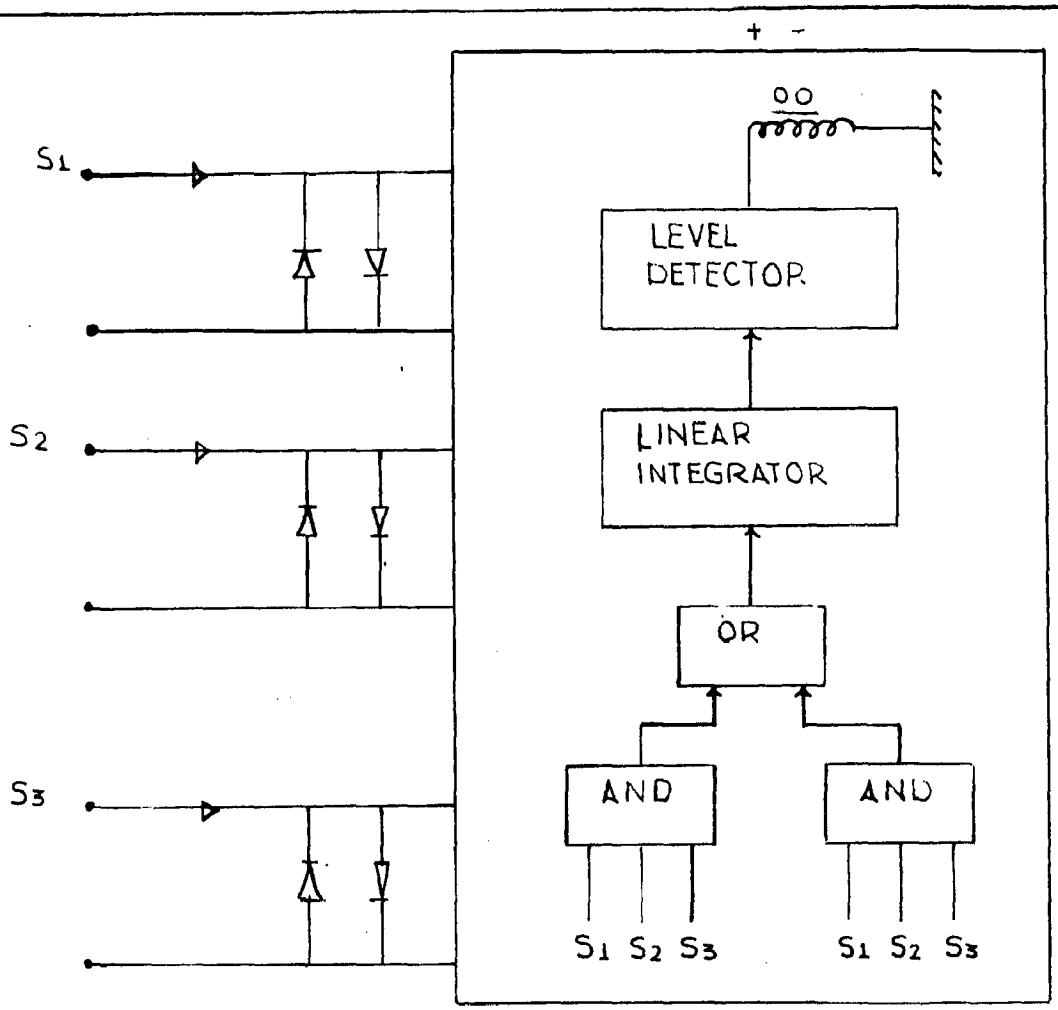


FIG:- 3.27

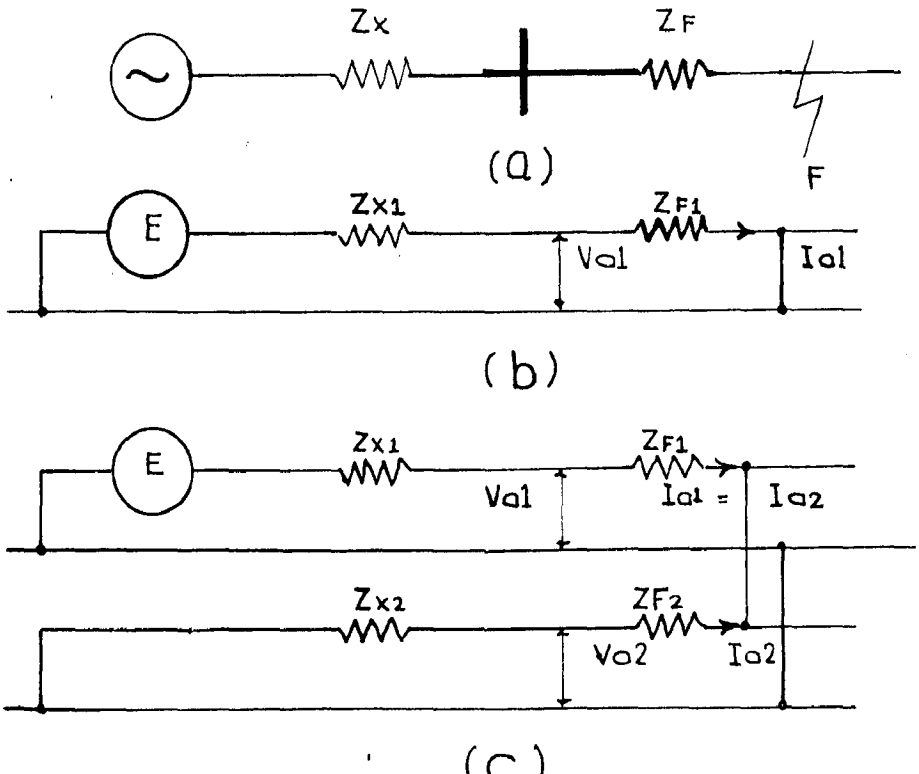


FIG:- 3.28 SEQUENCE VOLTAGES AND CURRENTS AT RELAYING POINT FOR PHASE 'A'

precision of distance measurement depends largely on the accuracy of the calculations and the impedance data for the protected feeder on which they are based.

3.6.3. The reaction of a relay to a system disturbance is determined from the voltages and currents at the relaying point. This may be done theoretically using symmetrical components. or practically using a network analyser, or from computer studies.

For simplicity only three principal types of short-circuit are considered here. In the simple circuit of Fig.3.28 the source impedance is Z_x and the impedance from the relaying point to the fault is Z_f.

3.6.3.(i) Three Phase Fault

Considering the three phase fault depicted in the sequence diagram. Fig.3.28, the positive sequence voltage and current at the relaying point for phase A are

$$V_{a1} = I_{a1}Z_{f1} \text{ and } I_{a1} = E/(Z_{x1} + Z_{f1})$$

The phase neutral voltages are $V_a = V_{a1}$, $V_b = a^2V_{a1}$ and $V_c = aV_{a1}$, the phase currentsare $I_a = I_{a1}$, $I_b = a^2I_{a1}$, $I_c = aI_{a1}$. If three single phase distance relays were energised by these quantities each would measure the positive sequence impedance, Z_{f1}.

With delta connected c.t.s. and voltage circuits the relays would measure respectively

$$(V_a - V_b)/(I_a - I_b)$$
$$(V_b - V_c)/(I_b - I_c) \text{ and}$$
$$(V_c - V_a)/(I_c - I_a)$$

and each of these expressions is equal to Z_{f1}.

If, however, the c.t.s. were star connected and the voltage circuits delta connected, the three elements would measure

$$(V_a - V_b) / I_a$$

$$(V_b - V_c) / I_b$$

and $$(V_c - V_a) / I_c$$

each of which is equal to $Z_{f1} \sqrt{3}$.

3.6.3(ii) Phase-Phase Fault

The sequence diagram of Fig.3.28 is for phase A and a B-C phase fault, $I_{a1} = - I_{a2}$ so that $I_a = 0$, $I_b = - jI_{a1}\sqrt{3}$ and $I_c = jI_{a1}\sqrt{3}$.

The positive and negative sequence impedances are considered equal. This is true for static apparatus, but not for rotating machines. The variation in positive-sequence reactance of rotating machines introduces an error, usually negligible, in the source impedance. It is least at approximately the boundary of the sub-transient and transient regions, consequently it is even less significant with high-speed distance protection than with lower-speed distance protection. In Fig.3.28, therefore,

$$V_{a1} = I_{a1} (2Z_{f1} + Z_{n1}) \text{ and } V_{a2} = I_{a1} Z_{n1}$$

Consequently,

$$V_a = 2I_{a1}(Z_{f1} + Z_{n1})$$

$$V_b = I_{a1}(a^2 2Z_{f1} - Z_{n1})$$

$$V_c = I_{a1}(a2Z_{f1} - Z_{n1})$$

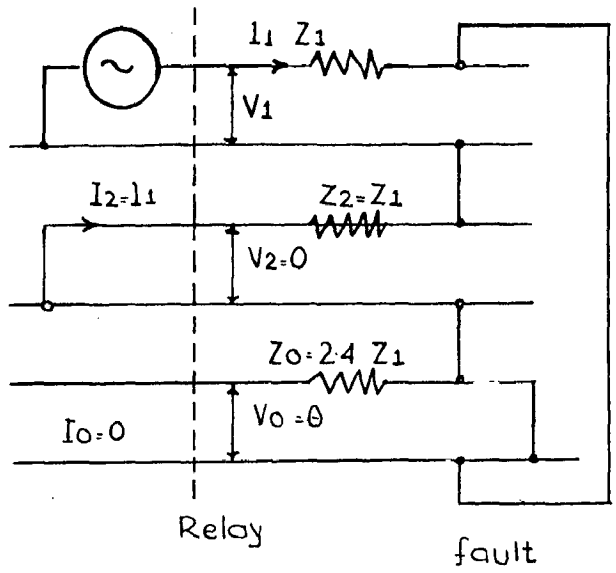
If the several methods of connecting the current and voltage circuits are considered, it is evident that with star-connected c.t.s. and delta-connected voltage circuits the relay element energized by the fault current and the voltage between the faulted phases measures 2 Z_{f1}. The same relay measures Z_{f1} if the c.t.s. are delta connected. The two other relays measure higher impedances, i.e. they under-reach.

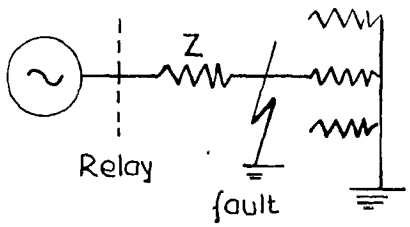
With a delta connexion for both current and voltage circuits the relays measure positive-sequence impedance, Z_{f1}, for both three-phase and phase-phase short-circuits. If the c.t.s. are star connected and the voltage circuits delta connected the relays must be set to measure $Z_{f1}\sqrt{3}$, consequently the three phase fault distance is correctly measured, but the relays under-reach by a factor of $\sqrt{3}/2$ for phase-phase faults.

3.6.3(iii) Phase-Earth Faults

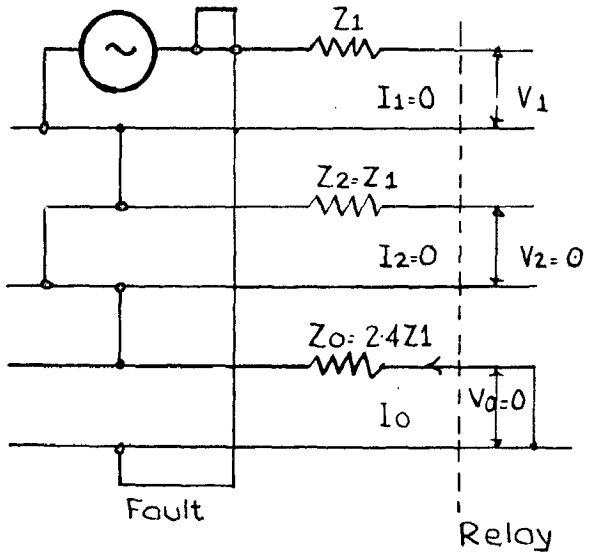
The earth-fault loop includes zero-sequence impedance, the value of which depends on the path taken by the current. Some current may return to the system neutral point through earth wires in the case of overhead lines, and through sheaths in the case of cables, the remainder returns through the earth and is considered to flow in an imaginary conductor at a depth depending on the resistivity of the earth. The zero sequence impedance varies considerably with the feeder construction and the nature of the terrain.

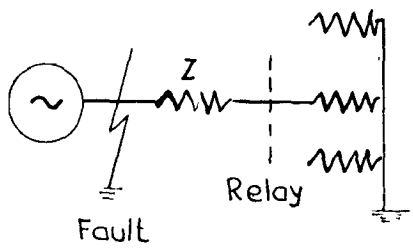
The position of the system neutral-earth point has a considerable effect on the value of impedance measured. This is shown in Fig.3.29, the source impedance is omitted for simplicity.



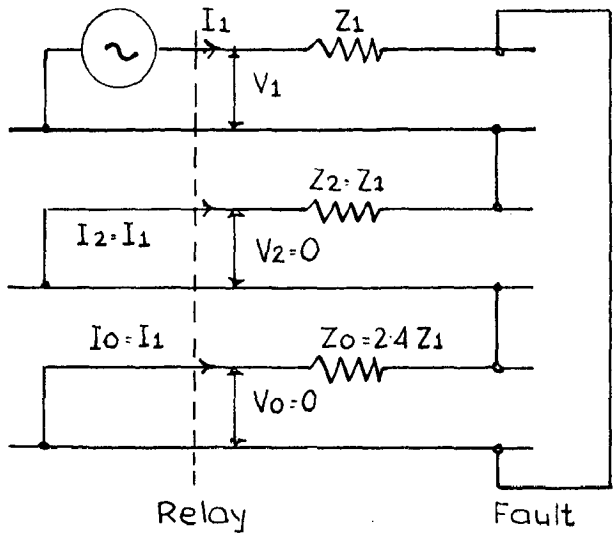


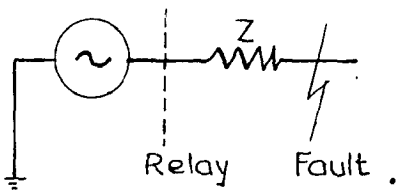
(a)





(b)





(c)

FIG:-3·29 EFFECT OF LOCATION OF NEUTRAL-EARTH POINT ON EARTH FAULT IMPEDENCE MEASUREMENT.

At (a) the system neutral is solidly earthed at a remote point, the source is at the relaying point and the earth fault is adjacent to the neutral-earth point, from the sequence diagram at the relay location

$$V_1 = 2I_1Z_1$$

$$V = V_1 + V_2 + V_0 = V_1$$

$$I = I_1 + I_2 + I_0 = 2I_1$$

Therefore $Z = V/I = Z_1$

At (b) the system neutral point is solidly earthed at the relaying point, and the system is supplied from the remote and adjacent to which is an earth fault, at the relay location

$$V_1 = I_0Z_0 = 2\times 2.4\ I_0Z_1 \quad (\text{assuming a typical value of } Z_0 = 2.4\ Z_1)$$

$$V = V_1 + V_2 + V_0 = V_1$$

$$I = I_1 + I_2 + I_0 = I_0$$

and $Z = V/I = 2.4\ Z_1$

At (c) the system neutral point is solidly earthed at the relaying point and the source is also at this point, but the earth fault is remote, at the relay location

$$V_1 = I_1 (Z_1 + Z_0 + Z_2) = 4.4I_1Z_1 \quad (\text{assumed } Z_0 = 2.4\ Z_1)$$

$$V = V_1 + V_2 + V_0 = V_1$$

$$I = I_1 + I_2 + I_0 = 3I_1$$

and $Z = V/I = 1.47\ Z_1$

In a system with more than one neutral-earth point the values of impedance measuredwould vary between Z_1 and $1.47\ Z_1$ ($Z_0 = 2.4\ Z_1$).

Earth-fault impedance measurement is made independent of the number of neutral-earth points, the relative location of these p ints, the relayand the faults by applying residual compensation.

3.6.3(iv) Residual Compensation

Residual compensation corrects earth-fault distance relays for the variable division of zero-sequence current between the several neutral earth points in a multiple earthed system. From the typical circuit of Fig.3.30 it can be seen that a fraction of the residual current is injected into each earth-fault distance relay. The phase-earth voltage measured at the relaying point is

$$V = I_1 Z_1 + I_2 Z_2 + I_0 Z_0$$

I_0 is variable but equal to one-third of the residual current, I_{res}. Z_0 can be written $K_0 I_1$, $I_1 = I_2$ and $Z_1 = Z_2$, therefore

$$V = 2I_1 Z_1 + K_0 I_{res} Z_1/3$$

and $$I = 2I_1 + I_0 = 2I_1 + I_{res}/3$$

The quantity to be measured is Z_1 and if the voltage is expressed as

$$Z_1 \left[2I_1 + I_{res}/3 + (K_0 - 1) I_{res}/3 \right]$$

it is evident that the relay current must be increased by

$$(K_0 - 1) I_{res}/3$$

With the typical value of $K_0 = 2.4$, the compensation required in each phase is $0.47 I_{res}$, and the ratio of the residual compensation auxiliary c.t.s. is I/0.47 A.

3.6.3(v) Mutual Induction

Where two feeders run in close proximity, e.g. double circuit overhead lines, and the system layout is such that for a fault on one feeder zero-sequence currents can flow in the other feeder, the zero-sequence coupling between the two affects impedance measurement. The small amount of positive and negative sequence coupling is negligible. Considering the faulted phase, the voltage at the relay location may be expressed as

$$V = I_1Z_1 + I_2Z_2 + I_o' Z_o + I_o''Z_{mo}$$

where Z_{mo} is the zero-sequence mutual impedance of the two circuits, and I_o'' is the portion of zero-sequence current in the healthy circuit.

In the preceding para 3.6.3(iv) a method of residual compensation is described which overcomes the variable nature of the $I_o'Z_o$ term. Compensation can also be applied to the current circuit of the relays to eliminate the effect of I_o'' Z_{mo}. A typical circuit is shown in Fig.3.30, from which it can be seen that the residual current in the parallel line is measured and a fraction is injected into the residual compensation circuit of the feeder under consideration via a mutual compensation auxiliary c.t.

The zero-sequence current in the parallel line is I_{res}''/ one-third of the residual current in the parallel feeder, and Z_{mo} is equal to K_m Z_1, where Z_1 is the positive sequence impedance of the faulted circuit. Therefore the induced voltage is $V_m = K_mZ_1I_{res}''/3$, and the amount of compensation required is $K_mI_{res}''/3$.

In Figure 3.30 a value of 2 is assumed for K_m. To provide the requisite compensation of $2I''_{res}/3$, the ratio of the mutual compensation auxiliary c.t. is made 1/1.43 A so that the overall ratio of this c.t. and the residual compensation c.t.s.(1/0.47A) is 1/0.67 A.

3.7. DESIRABLE CHARACTERISTICS FOR DISTANCE RELAYS

3.7.1. The desirable characteristics should have three selective functions namely -

(a) direction

(b) discrimination between fault resistance and load impedance

(c) distance measurement

Direction means confining the tripping zone to the first quadrant: although some incursions into the second and fourth may at times be desirable.

Selectivity between faults and loads is one of the major requirements of a distance relay particularly during power swings. Distance measurement by relays poses several problems particularly due to the presence of arc resistance, tower footing resistance etc.

3.7.2. The ideal characteristic would however be a quadrilateral characteristic with its reaches on the R and X axes separately adjustable. Nevertheless the characteristic should cover the impedances in question with some margin because the impedances cannot be stated exactly because the line impedance may vary along the line and as well from time to time and from phase to phase because of moderate steady state errors in

measuring transformers and relays and the practical limitation in the setting of relays.

3.7.3. The CIGRE Committee Report on Protection and Relaying[55] has recommended that the characteristic should as far as possible ensure satisfactory operation in the presence of :-

3.7.3.(i) additional resistances in arcs, tower footings etc. measured in some cases with important reactive components. This is the chief source of error in distance measurement problems. The fault resistance has two components, the resistance of the arc and the resistance of the ground and in a fault between the phases only the arc is involved whilst in a fault to the ground both are involved.

According to Warrington formula, the fault arc resistance is given by the relationship

$$R_{arc} = \frac{8750\, l}{I^{1.4}}$$

where l = length of the arc in feet in still air which initially will be the conductor spacing but will increase in the presence of a cross wind, because the arc has no inertia.

and I = is the fault current

The above formula where time is involved becomes

$$R_{arc} = \frac{8750\,(s + 3\,ut)}{I^{1.4}}$$

where s - conductor spacing

u - wind velocity in miles/hour

t - duration of time in seconds.

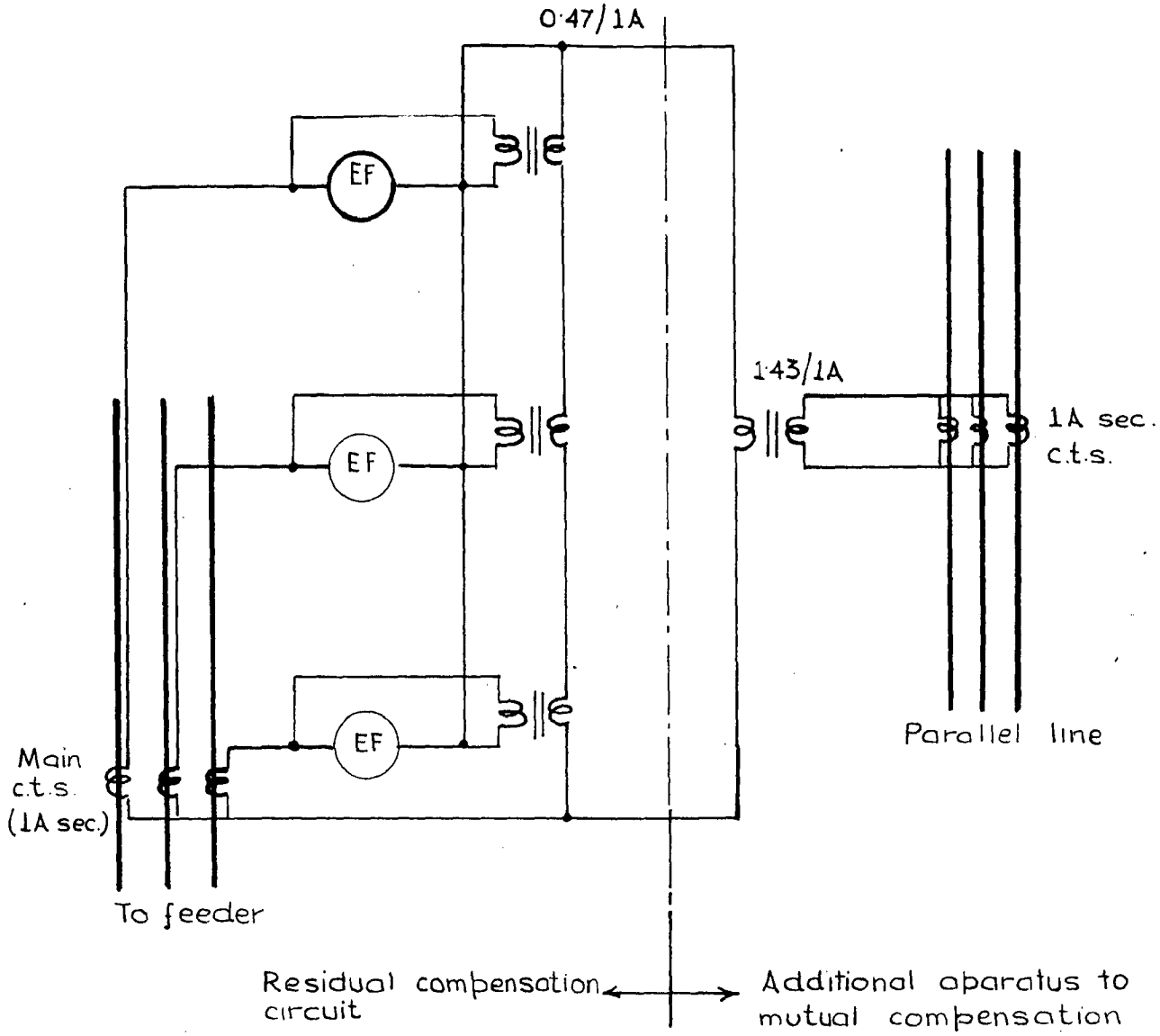


FIG:-3·30 RESIDUAL AND MUTUAL COMPENSATION.

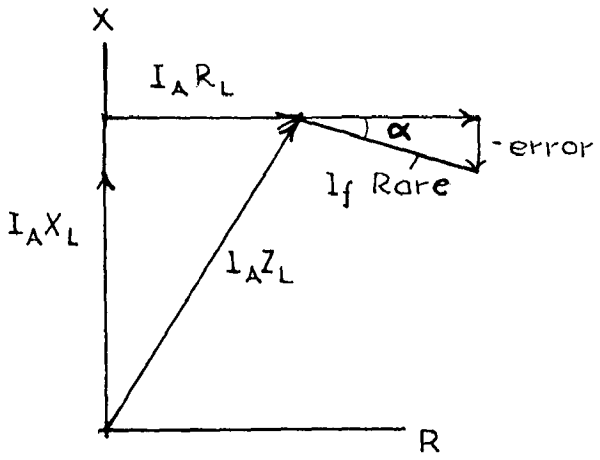


FIG:- 3·31 (a)

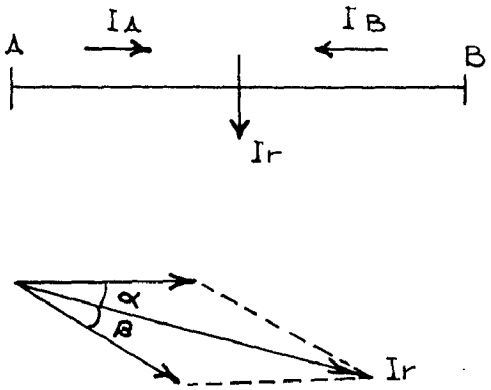


FIG:- 3·31·(b)

The above formulae have been claimed by the author[1] to have been confirmed by tests in Russia, France, U.S.A.

The reactance error is $\frac{V_{arc}}{I_A} \sin\alpha$ where I_A is the current fed in from one end and α is the angle between that current and the total fault current. The larger the current fed in from the other end the more α approaches the angle between the two currents and the greater the fictitious reactance. But on the other hand $(\alpha + \beta)$ is a small angle because (a) it is the angle between the two voltages at the ends of the protected section and (b) the larger I_B is the smaller arc voltage is, because it decreases as the 1.4 power with current magnitude. (Refer Fig 3.31)

The CIGRE[32] Committee however has recommended for simplified calculations in that the arc resistance be assumed as a certain voltage 2 or 2.5 KV/m of arc longthdivided by the current through the arc.

Tower footing resistance depends very much on the nature of the ground topography, humidity etc. and on the use of ground wires etc. and even on the amplitude of the current.

The Committee report states a distance relay is in many cases unable to measure an additional resistance correctly but will in such cases measure this resistance with an amplitude factor, called F and sometimes called with an angle called δ. The important values of F and E occur in networks with reactance grounded neutrals or isolated neutrals with faults to earth from one phase on one line and from another phase on another line and in networks with solidly grounded neutrals with phase to earth type faults.

The most effective way of preventing the fault resistance from making the distance relay under-reach is to design the measuring unit to measure the reactance rather than the impedance of the faulted circuit. Nevertheless the zone 1 should enclose as much of the line impedance and the additional resistances if possible without over reach and this concerns with the desirable shape of this part of the characteristic.

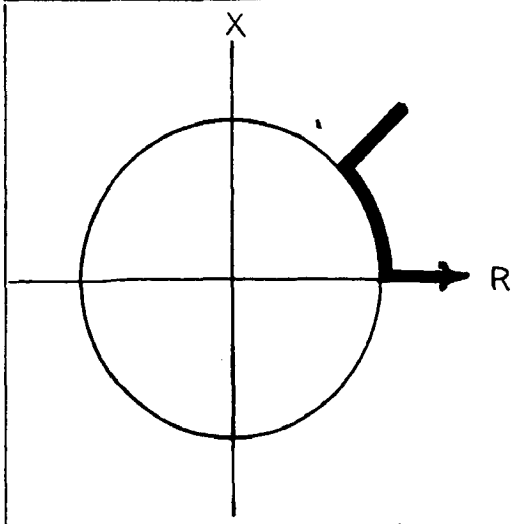
3.7.4.(ii) Small load impedance -

even if of the same order of magnitude as the fault impedance.In the simple case of a line feeding a district with no separate power supply, the load impedance may be limited by the full drawn lines as shown in the figure here 1(3.32) where the upper line is, due to the magnetising current, really a part of a large circle with the centre in the 1st quadrant near the +X-axis. In other cases the loci for the maximum load may differ somewhat from the circle in the figure.

A fault condition will also exist if the difference in phase angle between two stations with separate infeeds exceeds an angle corresponding to the maximum load condition. For lines connecting two networks, each having a certain power production the impedance loci are as shown by the circles in the figure 3.33 shown.

In this figure A and B are two stations with voltages E_A and E_B respectively, and φ is the angle between E_A and E_B.

If the voltage drop between the two stations exceeds a certain value (e.g. 20%), the impedance loci are then shown as circles on the top of the figure where the circle 0.8 corresponds to 20% voltage drop. The suppositions are as for the



Limitations by Load magnitude

FIG:- 3.32

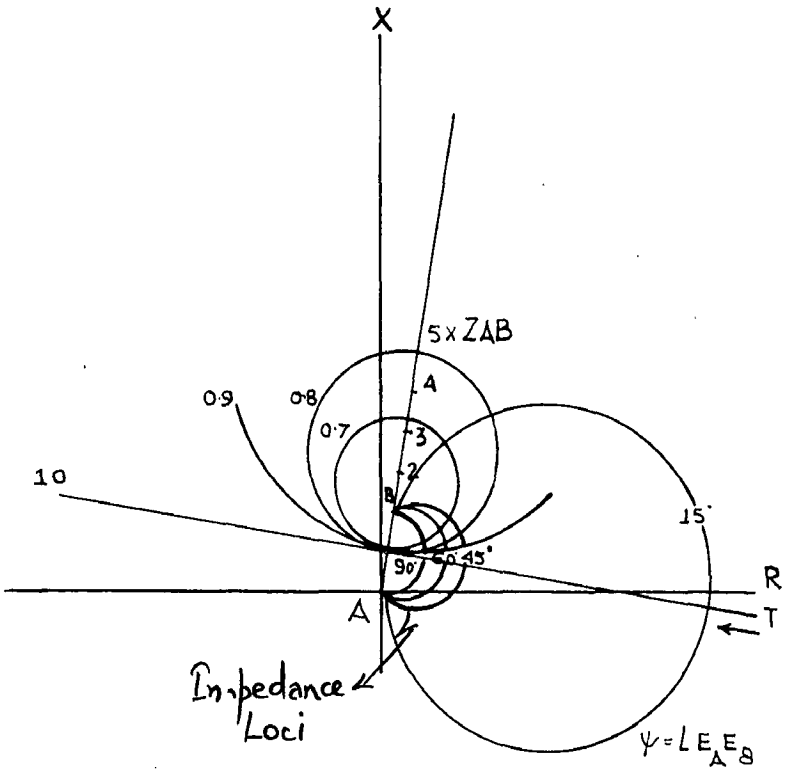


FIG:- 3.33

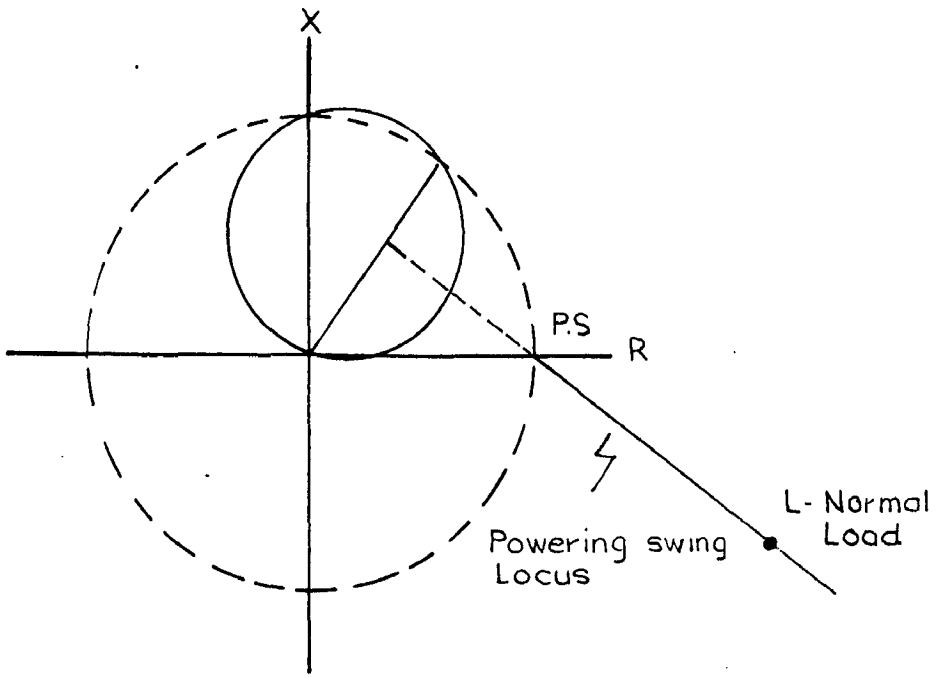


FIG:- 3.34 - POWER SWINGS.

circles to the right. The relay must then be located somewhere between A and B and the impedance measured by the relay are given by the distance from that point to the circle in question. It should, however, be remembered that this impedance, but not the shape, may differ in case of changes in the network. The network condition imposing the greatest limitation in the start zone should be considered.

It is practiced in Germany to have the impedance reach matched to the changing load conditions by making the reach roughly inversely proportional to the current e.g. from 2.5 times the rated current down to a small current. This means an increase of the maximum extension of the start zone in the case of small currents. A further increase can be obtained in the case of unsymmetrical faults by introducing current components from unfaulted phases. In Germany dependance on the angle is also practiced.

3.7.4.(iii) Power Swings

The impedance measured or'seen' by a distance relay during normal load is shown in the 3.34 figure. Normally this would be outside the tripping zone of the distance relay but, on a very long line where the length of the line in miles exceeds the system kV, the circular impedance characteristic may have to be made so large as to involve the point L. Furthermore as the load increases, L moves towards the relay characteristic in the direction of the arrow and during a power swing, it may oscillate upto a point such as P... where it may enter the tripping zone of the relay even on a medium length line. To over come this

the admittance (mho) relay was developed, which is sensitive only to a component of current at about the same phase angle as that of the protected line, so that it is insensitive to high power factor current conditions such as loads and power swings. Subsequent developments have been the elliptical and quadrilateral characteristics.

Vector diagram of one phase of a power system during a power swing, is shown in fig 3.35(b)

Power flows from the parts of the system with surplus generation to the areas with surplus load. The consequent flow of current through the system causes a voltage drop(refer above vector diagram) which, when the system is simplified to the equivalent two machine system, separates the two source e.m.f.'s E_S and E_R by an angle θ whose magnitude increases with the load transfer. Mr. A.R. Van C. Warrington has in his paper[19] given a graphical method of estimating the performance of distance relaying during faults and power swings in a detailed form.

From the above vector diagram, the swing current

$$I_S = \frac{E_S - E_R}{Z}$$

Where

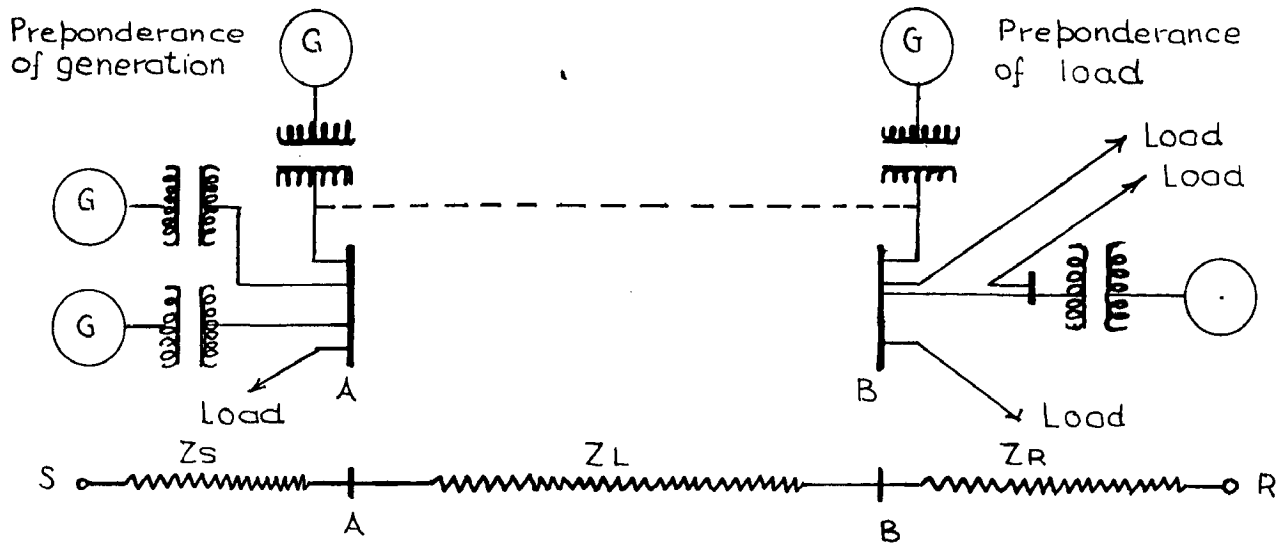
Z = total system impedance

E_S = sending end voltage

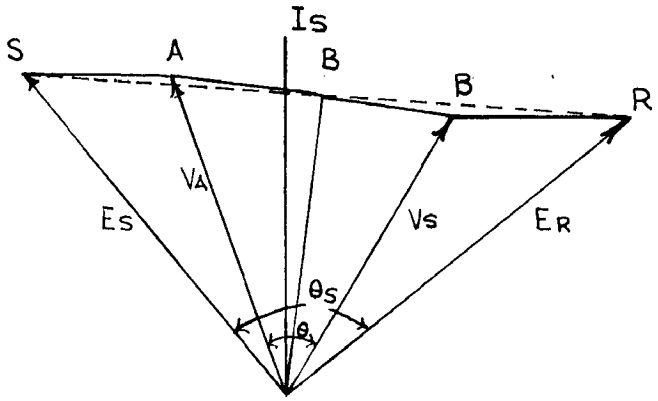
E_R = Receiving end voltage

If $|E_S| = |E_R|$ then $I_S = \frac{2E}{Z} \sin \frac{\theta}{2}$

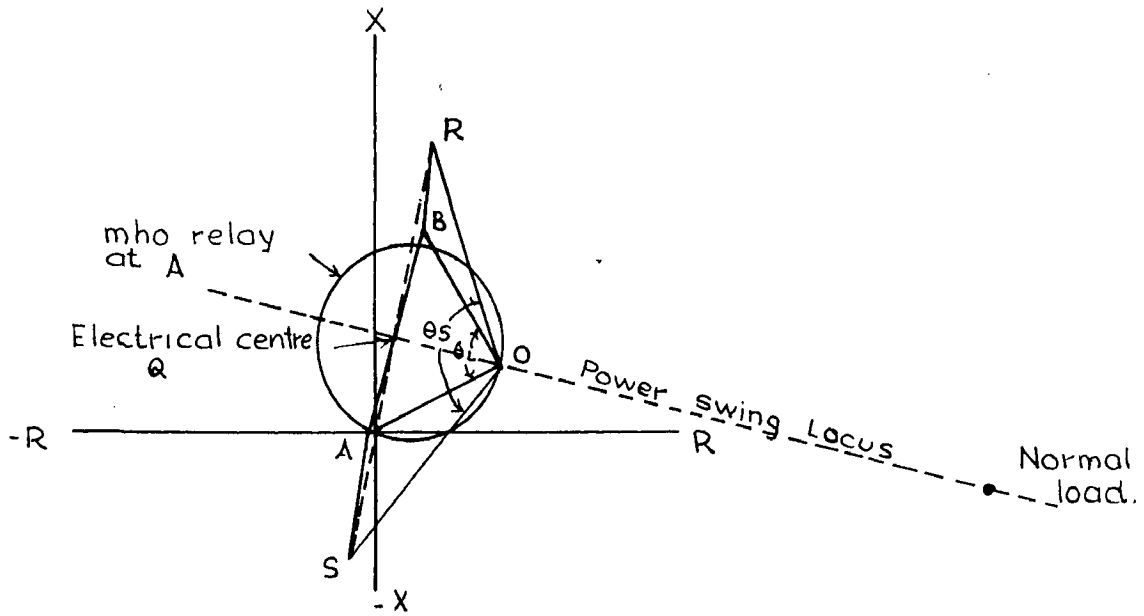
The voltage decreases towards the middle of the system and this reduction increases with θ_S until the line voltage is zero at the electrical centre of the system when $\theta_S = 180^\circ$(Refer Fig. 3.36).



(a)



(b)



(c)

FIG-3.35- POWER TRANSFER AND POWER SWINGS.

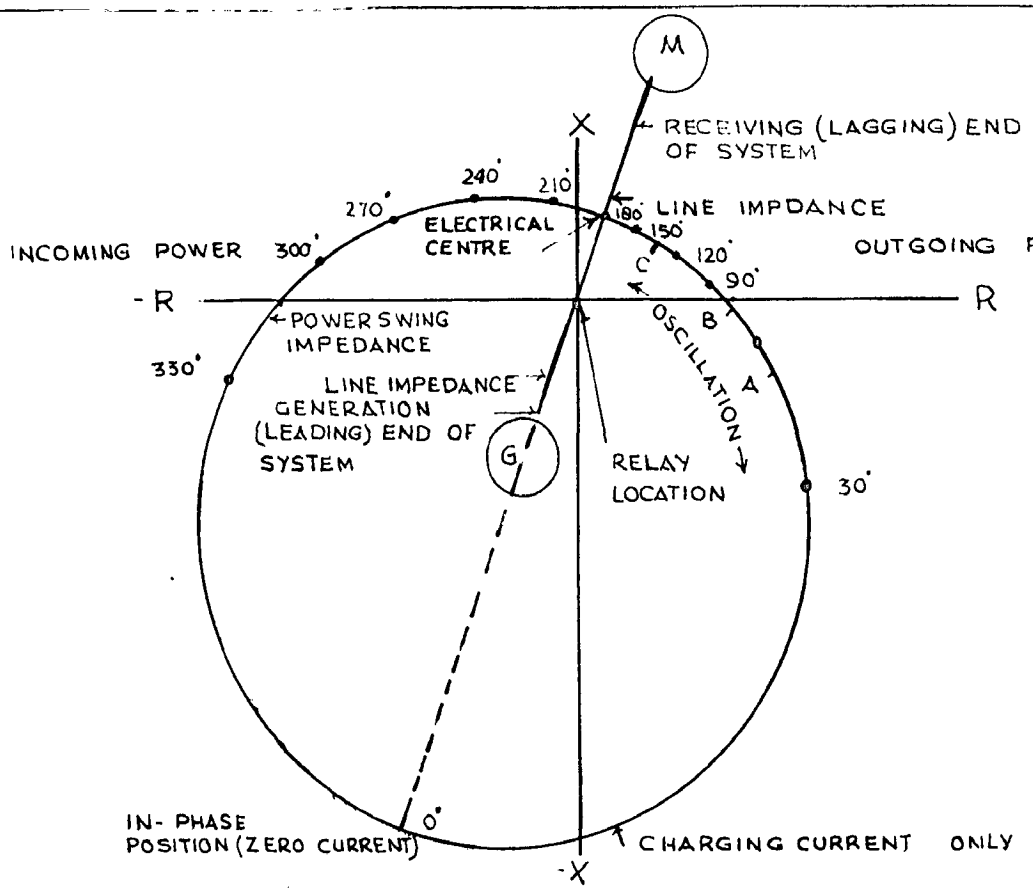


FIG:- 3·36 - LOCUS OF IMPEDENCE SEEN BY DISTANCE RELAYS DURING POWER SWING.

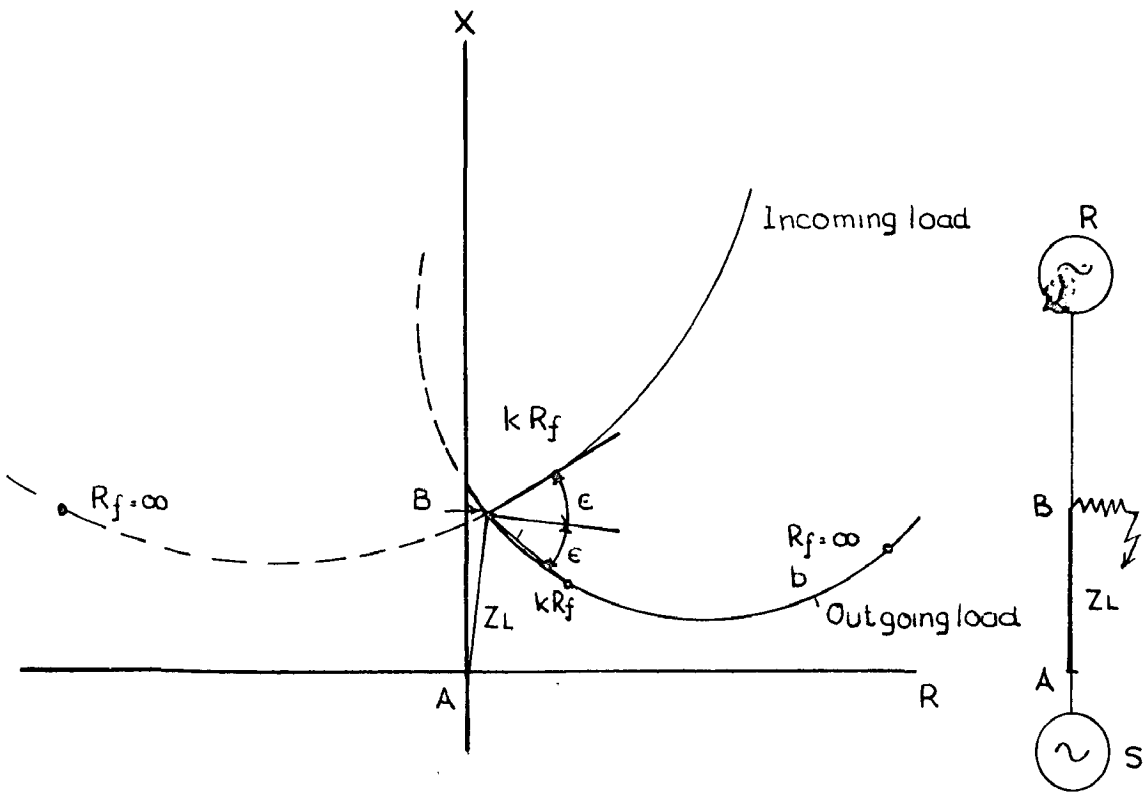


FIG:- 3·37· EFFECT OF FIXED LOAD AND VARYING FAULT RESISTANCE LOAD MEASURED AT 'B'

The effect of this upon the impedance seen by a distance relay is shown in the Fig. 3.35 a, b & c

Normally θ_s does not exceed 15° and the relays are negligibly affected, but during a power swing θ_s may oscillate upto 90°. Theoretically a swing of more than 90° should result in the generators at A and B losing synchronism because the synchronising torque is proportional to Sin θ_s and hence decreases when $\theta > 90°$. The origin of the above diagram is shown at the relay location A so that the impedances seen by the relay are measured from A. This relay would measure the impedance value AB for a fault at B, but in the case of a power swing with angle θ_s between the generated voltages it would measure the impedance AO. As the swing becomes more and more severe, and the angle of separation increases and the impedance measured by the relay will decrease to a value A' which may happen to be within the tripping characteristic of the relay. Where it is found that the power swing locus penetrates the relay characteristic the substitution of an elliptical characteristic may prevent undesirable tripping or alternatively to add ohm units as blinders.

The effect of a power swing upon distance measurement to fault is equivalent to a load impedance Z connected in parallel with the fault since the load current goes through the relay but not through the fault. The figure 3.37 shows the impedance measured by the relay as the fault resistance varies from 0 to ∞ with (a) incoming power (b) outgoing power. Referring to fig 3.38, we hav

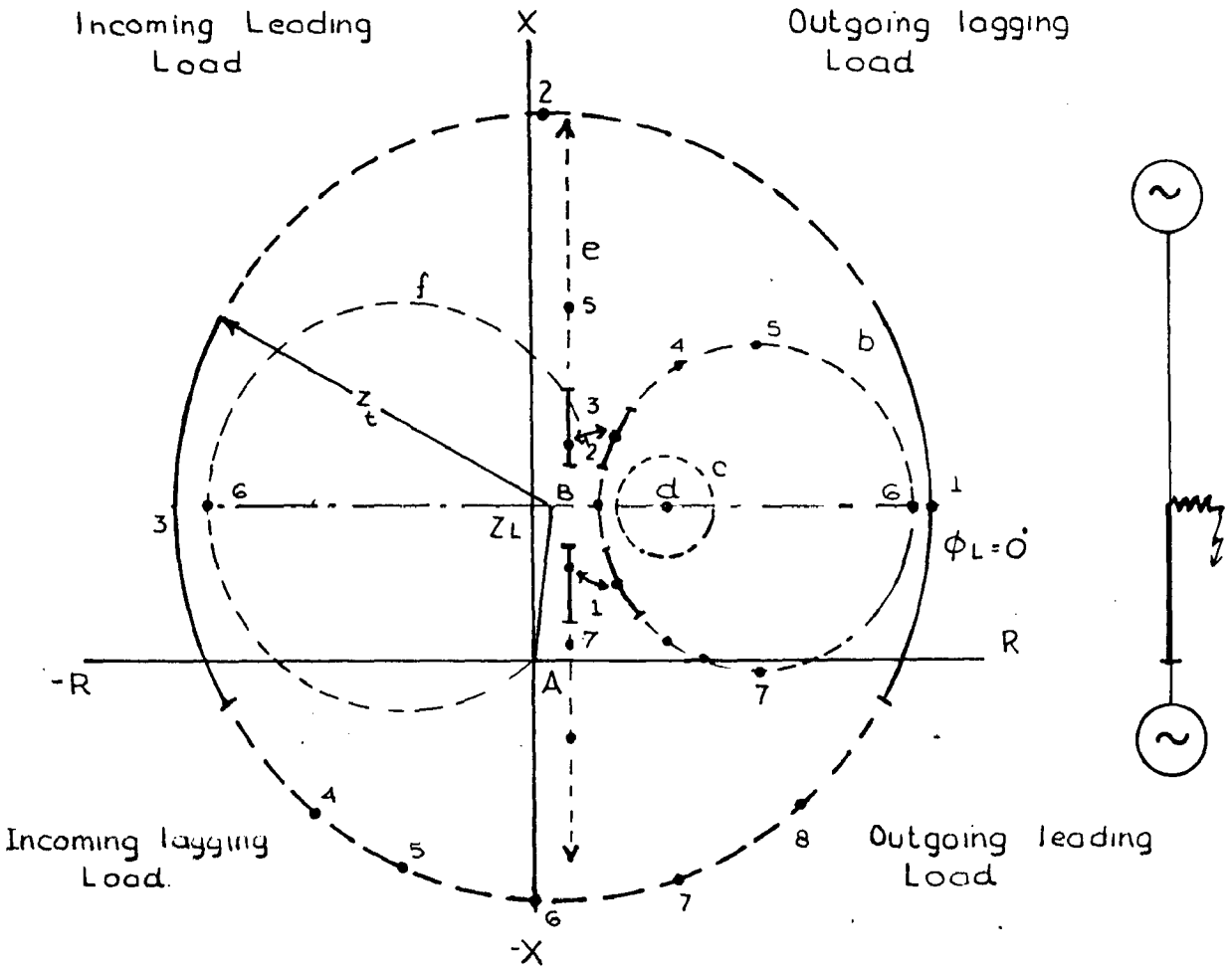


FIG:-3.38- EFFECT OF FIXED FAULT RESISTANCE AND VARYING LOAD

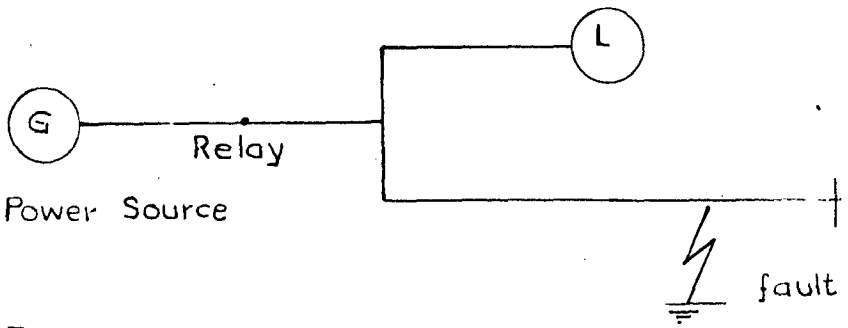


FIG:-3.39 -a-

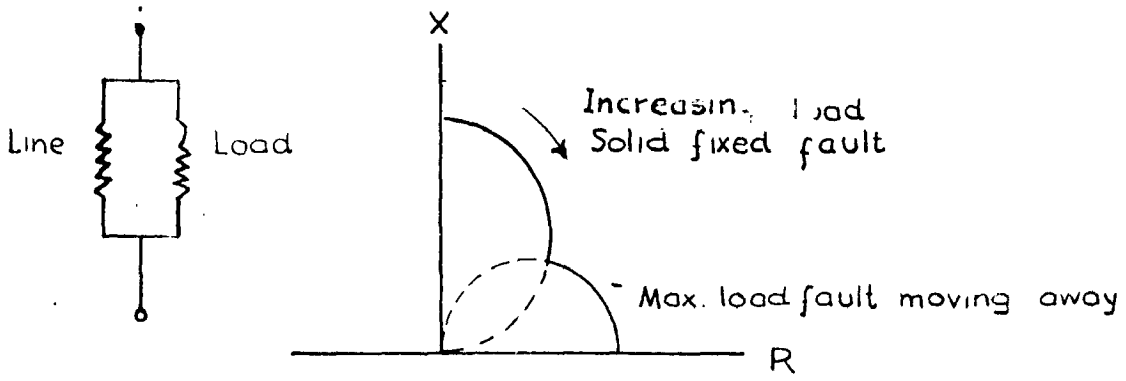


FIG:-3.39-b-

With no fault and a load of a constant magnitude but varying phase angle, the locus of the impedance seen by the relay at A is the circle 'a'. With a fault of resistance Rd and the same load condition as for 'a', the locus becomes the circle 'b'. A smaller locus gives the locus 'c', no load gives the point 'd' Larger loads give the loci 'e' and 'f'.

On these loci the points marked 1 to 8 represent the same phase angles of the load current as seen by the relay at A. For instance the point 1 represents unity power factor outgoing power, point 2 is outgoing KVAR; point 3 incoming KW, point 6 incoming KVAR.

From the above it will be seen that the relays tend to measure less reactance and hence to over-reach with outgoing power and to under-reach with incoming power. A mho relay with a circle of diameter AB would over reach for locus 'e' which however represents an enormous load.

Under-reaching occurs in most cases. Over-reaching occurs in relays with outgoing power, but it is serious only for a relay near the receiving end and with a high resistance fault. The quadrilateral characteristic would be much more vulnerable than the mho circle in this case.

Whereas the impedance measured by the relay can be increased by the fault resistance which is in series with the line impedance as shown in Fig. 3.39(a) particularly with loads in parallel with a faulted line. This would be the case with single end feed where a relay looks backward through the bus

into two lines one of which is faulted and the other has a load. An example is that of the third zone mho distance relay.

3.39(b) Figure shows the impedance seen by the relay in such a case - the fault is a solid one and the unity power factor load is varied from zero to the maximum value. The small circle shows the effect of varying the distance to the fault with a fixed (maximum) load. Those conditions can cause over-reaching which is not undesirable in the case of a reversed third zone unit. Where it is due to a heavy tap load on a very long line it can cause over-reaching of zone 1 and this must be allowed for in its setting. However in practice this error is considerably reduced by the zero sequence compensation of the relay since the zero sequence current is only associated with the fault.

3.7.4.(iv) Mutual Induction

Mutual Induction at system frequency can occur between one conductor and the other two of a three phase line, or between one 3 phase line and another. The method of compensating for the former is straightforward because the c.t.'s of the other phases are available, but compensation for induction from a parallel line is not possible if the latter does not terminate in the same bus as the line affected.

On an ideally transposed line the voltage V_a for a solid single phase fault to ground is given by

$$V_a = I_a Z + (I_b + I_c) Z_m$$

Where Z = self impedance of the conductor between the relay and the fault

Z_m = its mutual impedance to the other two conductors.

From the above equation we have

$$\frac{V_a}{Z} = I_a + (I_b + I_c)\ \frac{Z_m}{Z}$$

or $$Z = \frac{V_a}{I_a + (I_b + I_c)\frac{Z_m}{Z}}$$

But $$Z_1 = Z_2 = Z - Z_m$$

and $$Z_o = Z + 2Z_m$$

Solving for Z and Z_m we have

$$Z = 1/3\ (\ 2Z_1 + Z_o\ )$$

$$Z_m = 1/3\ (Z_o - Z_1)$$

Substituting for Z and Z_m we have

$$V_a = 1/3\ \left[I_a(2Z_1 - Z_o) + (I_b + I_c)(Z_o - Z_1) \right]$$

$$= 1/3\ \left[I_a(2Z_1 - Z_o) + (3I_o - I_a)(Z_o - Z_1) \right]$$

$$= I_a Z_1 + I_o\ (Z_o - Z_1\ )$$

$$Z = \frac{V_a}{I_a + \left(\frac{Z_o - Z_1}{Z_1}\right) I_o}$$

From the above equation we can make perfect compensation for mutual induction from the other two phases.

In the case of an untransposed symmetrical line for a solid single phase ground fault on phase 'a' we have

$$V_a = IZ_a + I_b Z_{mb} + I_c Z_{mc}$$

where Z_{ab}, Z_{ac} is the mutual impedance of the faulted conductor 'a' to conductors 'b' and 'c'. Hence the compensation from the sound phases will be

$$\frac{V_a}{I_a + \frac{Z_{ab}}{Z_a} I_b + \frac{Z_{ac}}{Z_a} \cdot I_c}$$

It may be mentioned here that the self and mutual impedances of the individual conductors are seldom known in practice and the relays in the 3 phases are set for the same impedance and supplied with the same proportion of currents from the other two phases. Under these circumstances the difference between the relay measurement of an untransposed line with zero sequence compensation and sound phase compensation is less than 2%. Hence zero sequence compensation is normally employed as it requires only one auxiliary c.t.

In 1970, U.D. Rumpago[43] made a detailed evaluation of the errors in the measurement of impedance by distance protection when applied to 400 KV double circuit lines formed in the widely used loop interconnection. An accurate separation of the errors arising from primary circuit interphase and intercircuit mutual coupling, non-transposition of phase conductors, and fault resistance is developed during the fault and prefault operating conditions, for which the errors have their greatest individual and combined effects are formulated. The errors have been evaluated by computer programming on the basis of which their consequences in relation to the fault operating performance of distance protection is assessed. The error study has been made for primary

system fault voltages and currents and hence for the relaying signals derived from them, which are sinusoidal quantities at supply frequency. The sources of error in the protected circuit is collected in the following form -

i) interphase mutual coupling , ii) intercircuit mutual coupling iii) non-transposition of conductors, iv) fault resistance

The errors have been calculated for the following specified conditions.

i) prefault transfer of active and reactive power both in magnitude and direction

ii) specified short circuit levels at the busbar terminations of the interconnection

iii) ratio of the positive sequence to the zero sequence impedance of each infeeding source

iv) type and location of the fault

v) ratio of source impedance to line impedance

The errors due to interphase and intercircuit coupling have been stated to be eliminated by compensation methods normally employed. The relaying error E_A due to lack of conductor transposition is formed as

$$E_A = \frac{V_\Omega}{I_{R(n)}} - \frac{V_\Omega}{I_{R(t)}}$$

Where $I_{R(t)}$ denotes the compensated relaying signal calculated on the basis of an assumed transposition of conductors and $I_{R(n)}$ corresponds to the same quantity calculated for a given set of impedance parameters. If $I_{RO(t)}$ is the exactly compensated signal then the error E_B arising from this source is given by

$$E_B = \frac{V_\Omega}{I_{R(t)}} - \frac{V_\Omega}{I_{RO(t)}}$$

The error F_c due to intercircuit mutual coupling is given by

$$F_C = \frac{(I_{A2} + I_{B2} + I_{C2})(1-x) Z_{n2} + (I'_{A1} + I'_{B1} + I'_{C1}) n Z_{b2}}{I_{ro}(t)}$$

The error due to fault resistance is given by

$$F_D = \frac{I_f R_f}{I_{ro}(t)}$$

Thus for sound phase compensation we have the sum total of all errors as

$$F_A + F_B + F_C + F_D = \frac{V_a}{I_{r(a)}} - (n + 1-x) Z_0$$

where Z_0 is the self impedance per unit length between conductors in the 'a' and 'b' phases with common earth return.

For residual compensation we have

$$F_A + F_B + F_C + F_D = \frac{V_a}{I_{r(a)}} - (n + 1-x) Z_1$$

where Z_1 is the sequence impedance per unit length of the faulted circuit. The errors due to lack of conductor transposition are different for each of phase and it has been shown by the author that some of the errors tend to cancel with one another and that there is an interdependence between them.

However S.A. Wheeler[52] in the same year examined the cases of significant mutual coupling impedances between the two circuits in double circuit over head lines. His study was conducted for different primary circuit arrangements and for the condition when one circuit is out of service and earthed at both ends. The conclusions of his study indicate that distance protection may over-reach when detecting earth-faults if zero

sequence currents flow in a parallel circuit in the opposite direction to zero sequence components of current in the circuit in which the measurement is made. Nevertheless the extent to which this can occur in practice is severely limited by system configuration and over-reaching has been shown not to occur if the double circuit lines are connected to the same busbar at one end only if a single phase earth fault occurs on one of the two circuits. It has also been shown that a failure in discrimination due to mutual coupling effects depends upon the distribution of sequence components of fault currents and failure in discrimination is not likely if impedance protections are set on the basis of circuit self impedances in an inter-connected multiple earthed system. The author has advocated that it would be prudent to restrict zone setting in certain particular cases where the total fault current comprises almost entirely zero sequence components.

The effect on distance relay performance of operating only one circuit with the other isolated and earthed at both ends in the case of double circuit lines was studied by W.D. Humpage and M.S. Kandil[53]. It has been stated that relaying conditions arise requiring a resetting of the forward reach settings. Earth fault conditions give rise to apparent impedance values which are generally less. Computer studies were conducted by them to evaluate the discriminative performance of distance protection under earth fault conditions both under single circuit and double circuit working. It was found that conditions necessitated in the selection of the forward reach settings of zone 1 relays so as to

gaurd against those relays responding external to the protected circuit. The errors in the reactance measurement under earth fault conditions discounting the effects of fault resistance amounted to as much as 20%. Obviously the presence of the fault resistance would accentuate those error values.

On a double circuit line with little or no generation at the far end, a fault on one line will be supplied with a substantial amount of current via the sound line. This current will induce a voltage in the faulted line which will make the relay under-reach, in that line. This tendency will decrease as the fault approaches, the remote bus, so that under-reaching will not seriously affect the zone 1. As such mutual compensation is normally omitted[19].

3.7.4.(v) Transient Errors

When a fault occurs, the current and voltage at the relay undergo a sudden change in amplitude or phase angle or both. This sudden change causes the sinusoidal current to be offset by a decaying d.c. component whose amplitude depends upon the moment in the cycle at which the fault occurs and whose duration increases with the X/R (time constant) ratio of the circuit. These transients take the form of a decaying d.c. component which offsets the current or potential wave so that one half of the wave has a greater amplitude and a longer duration than the other. This will cause decreasing alternate positive and negative errors in both amplitude and phase comparators so that they will tend to over reach during every other cycle unless means of providing average measurement are incorporated.

In voltage comparison the line voltage at the relay location is compared with the voltage drop across an impedance which is the replica of the protected line section on a secondary basis. For a fault at the end of a protected section the line voltage at the relay is produced by the line current flowing through the impedance of the protected section. Consequently, it's transient behaviour is identical to that of the voltage produced by the same current flowing through a replica impedance provided that the system impedance is homogeneous (the source impedance Z_s is invariably more lagging than the line impedance Z_L). In both amplitude or phase comparators (IZ_R-V) is compared with IZ_R or V. Since all these terms contain the primary current transient equally reproduced, it cancels out in the measurement of impedance in a homogeneous system. On a non-homogeneous system where the source impedance is more lagging than the line impedance the transient response of the line potential will not be the same as that of the current. Hence the currents or voltages compared in the relay will not be matched for a fault at the end of the protected section so that a fast relay can ever reach if the fault current is considerably offset. In practice this is prevented by delaying the relay by 10 or 20 ms for fault near the cut-off point of zone 1 so that it's operating time exceeds the time constant of the protected section. In current comparation the replica impedance is connected in series with the potential circuit. The relay current in both cases is : [Refer Figs 3.40 (a) & (b)]

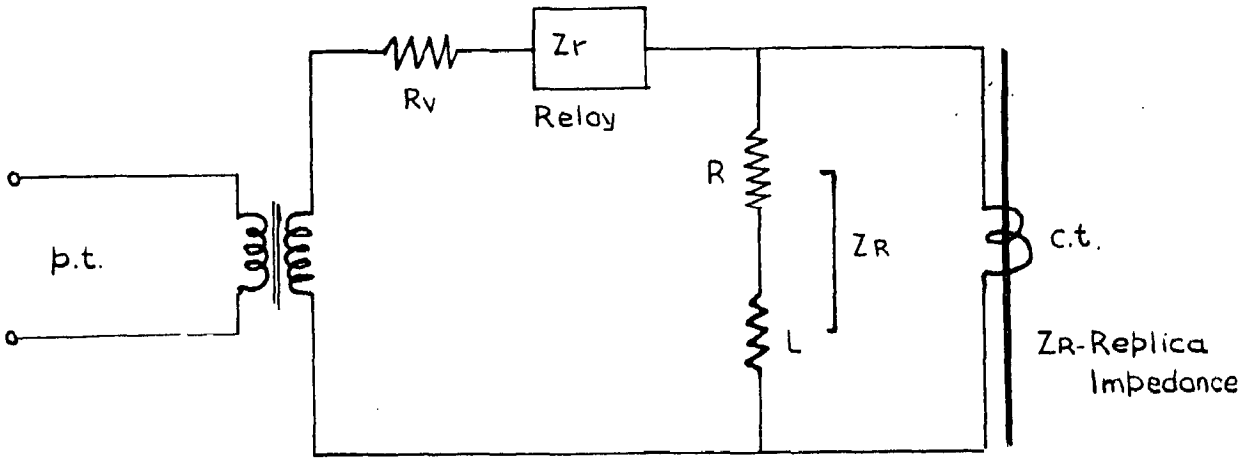


FIG:-3.40(a)- VOLTAGE COMPARISON.

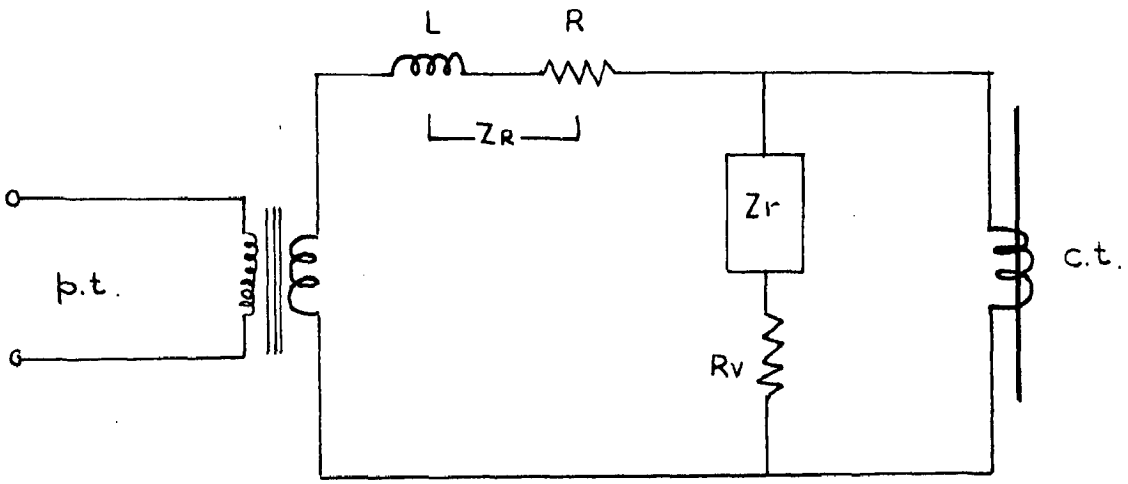


FIG:-3.40(b) CURRENT COMPARISON.

$$\frac{(IZ_R - V)}{(Z_R + Z_r + R_V)}$$

Where,

Z_r = is the relay impedance

R_V = series resistance adjusted so as to make the circuit have a low time constant

i.e. $\frac{L_R + L_r}{R_R + R_r + R_V} < 6$ ms

This low time constant prevents any transient error due to dying away of the current in the secondary of the p.t. without appreciably affecting the sensitivity of the relay except in the case of EHV lines of extremely high X/R ratio. In such cases more relay amplification may be necessary or linear couples can be used. Although the replica impedance matches the line impedance for a solid fault, it does not allow for resistance in the fault. This is not so important in a mho relay because any over reach merely makes the mho circle for transient measurement to bulge sideways and this causes an improvement in its characteristic because it provides somewhat more tolerance for fault resistance without increasing the distance reach.

3.8 In conclusion it may be stated that the commonly used distance relay characteristics are quite satisfactory in many cases. Characteristics with special and more flexible shapes are, however, desirable in the presence of additional resistances measured in some cases as large impedances with important reactive components, power swings, load

impedances of the same order as the fault impedances, transient errors and/or infeed currents not measured by the relay in question. Hence no combination of characteristics and no exact shape and setting range can be stated as the only correct ones in all cases.

CHAPTER-IV

FAULT LOCATORS - THEIR DEVELOPMENTS, TYPES AND THEIR REQUIREMENTS

4.1. INTRODUCTION:

Power system transmission line short circuits are of frequent occurance on an extensively connected high voltage system. These disturbances usually result from lightning or other mechanical causes or other causes resulting in failure of insulation. In either case it is desirable to locate and inspect the source of trouble. This is particularly true if the outage is permanent and must be attended to before service is restored. The determination of the distance to the fault also enables in organising rapid repair work.

4.2. DEVELOPMENTS IN FAULT LOCATORS

4.2.1. Use of Oscillographs

Power Engineers have been engaged since 1935 in the process of analysing the nature of faults and the location of the faults. The early documented work is reported by G.D. Gerell in his paper[56] wherein it is stated that an automatic oscillograph was installed at a 66 KV substation at Venice, Illinois and was connected to record the ground current. A fault which occurred in the system was duly isolated and the oscillographic records were analysed. From a set of general equations which the author has indicated in his paper, the probable location of the fault was determined and was subject to a physical inspection of the line as a counter check. Detailed inspection revealed that at a point 3000 ft. away from the indicated location 6 insulators had

flashed over on an insulator string. The error in the oscillograph determination of the location of the fault was less than 4% of the total length of the line. The method of determination enabled the power system engineers to have a proper perspective of the nature of the transient fault, circuit voltage and current magnitudes at fault inception and enabled to have proper coordination of the protective system.

4.2.2. Similarly in 1946, H.P. Dupins and W.B. Jacobs published a paper[57] describing a method developed for the determination of the location of ground faults after extensive studies conducted on a 140 KV grounded neutral system after obtaining oscillographic records of the system from 1941 to 1945 involving about 250 line faults out of which 96% of line faults involved one or two phases to ground. The method applied to ground faults in a grounded neutral system of two or more parallel lines and is based on the comparison of the magnitude of ground currents in the faulted circuit and in the unfaulted circuits. The oscillographs were initiated by instantaneous under voltage relays connected to the 140 KV P.T's and by instantaneous OCR's in the 140 KV neutrals of the grounded transformer banks. The initiating relays were set to ensure operation for at least two oscillographs for all faults within the network. The oscillographs in service were of the 6 element type of which three elements were used to record line to neutral voltage and the remaining three to record ground currents. The following factors were used in the ground fault analysis.

(a) magnitude and relative values of ground currents from each end of the faulted circuit with both ends closed.

(b) magnitude of ground currents in the faulted circuit after one end opens

(c) relative values and direction of ground currents in unfaulted circuits in parallel with the faulted circuit with

i) both ends of the faulted circuit closed, and

ii) after one end of the faulted circuit opens

(d) magnitude and relative values of currents in contributing circuits from ground sources

(e) recorded potential

(f) changes in magnitude of ground fault current with changes in the nature of the fault that is one line to ground fault changing over to two line to ground fault.

(g) relay operation concerning

i) operating time of time delay relays, and

ii) pick up and operating range of instantaneous relays.

The above factors were utilised in drawing up a complete set of curves consisting of impedance curves, maximum ground fault current curves and ratio curves. These data curves were made up from the +ve, -ve and zero sequence diagrams by calculating the +ve, -ve, and zero sequence impedances at a sufficient number of points between the two stations to ensure drawing of

curves so as to be accurate enough. The calculations were simplified by using linear values of impedance rather than the complex $R + jX$ quantity. The current curves were used in determining directly the fault location as these were plotted as current against distance in miles, and were particularly so if the magnitude of the fault currents happened to be near the maximum values. The ratio curves were plotted using the current in one circuit as the reference and the currents in the other circuits as a percentage of the reference current and these were applied for determining ground faults in parallel circuits. The authors claimed that with oscillographs at each station it was consistently possible for faults to be located within a mile of its occurrence. However this method also did not find favour for reasons stated in para 4.2.6 and also the method applied only for locating ground faults. The accuracy of the curves was subject to discrepancy as the effect of tower footing resistance and arc resistances were neglected.

4.2.3. In 1957, Mayashio Baba[70] has stated that the fault locators used in Japan do not use the method of measuring current and voltage at the terminal of the line because the neutrals of most of the power systems in Japan are grounded through resistance or ground fault neutralisers. Only in EHV the neutralsare solidly grounded and automatic oscillographs are made applicable for fault location. An electronic counter provided along with the equipment for distance indication has proved to be quite reliable and the electronic counter has been used as a back up to the CRO.

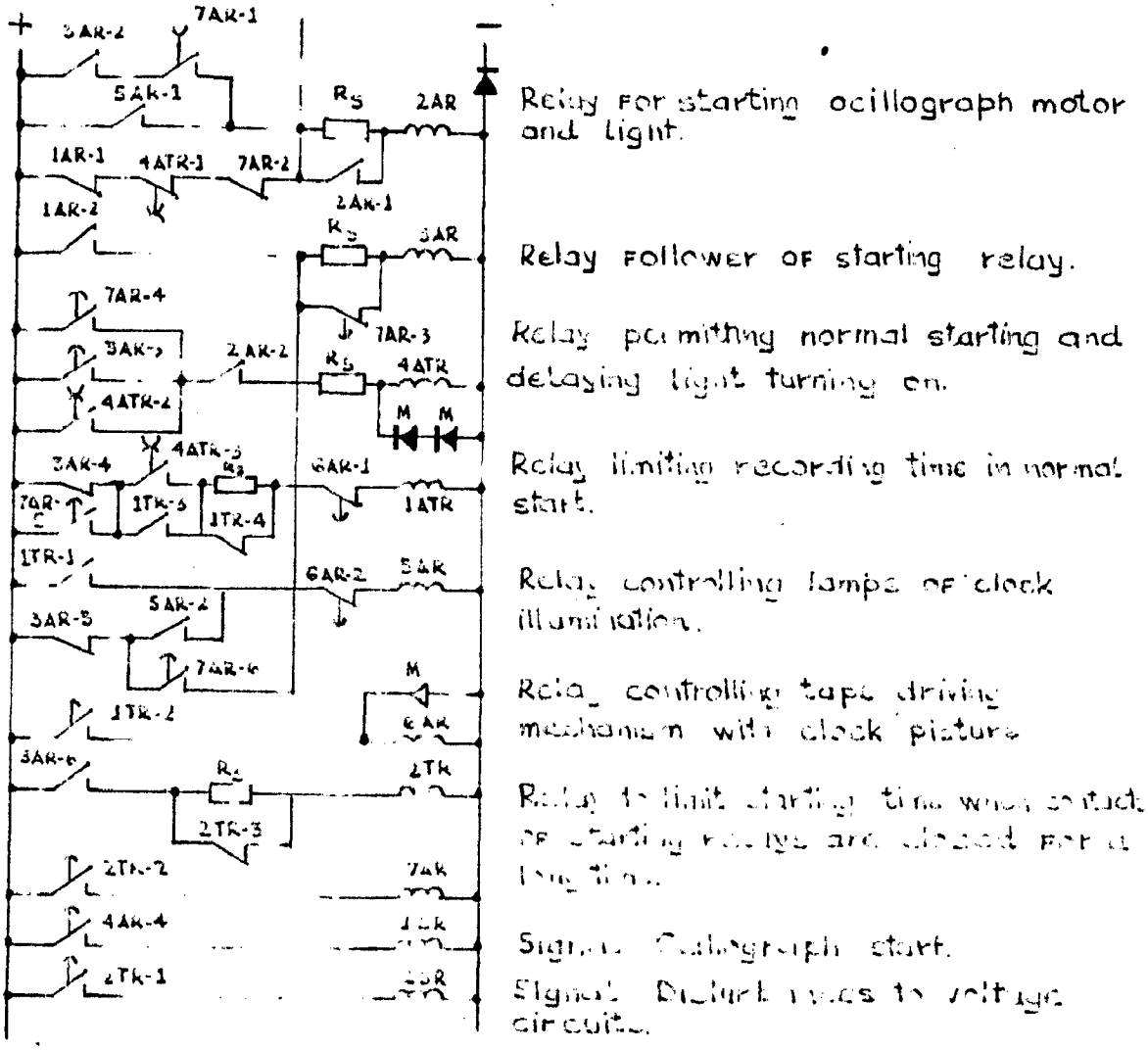
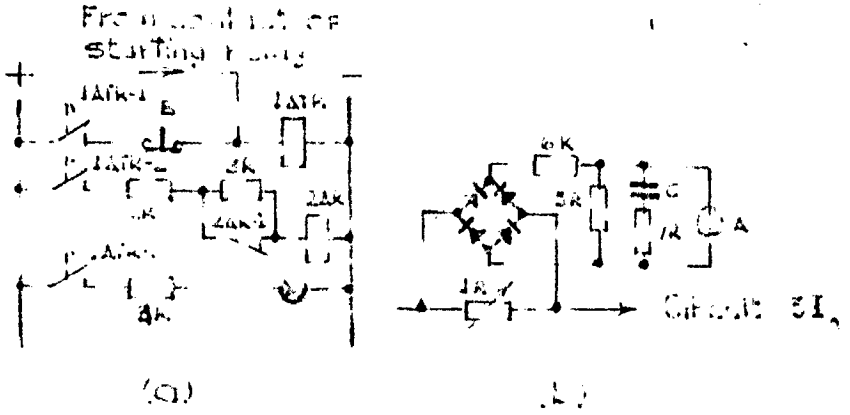


FIG. 4-1- OPERATING CIRCUITS OF STARTING DEVICE FOR OSCILLOGRAPHS.



(a) (b)

FIG. 4-2 - CONNECTION OF FIXING AMMETER Ф A-3.

1ATR- auxiliary relay, delayed on picked up for 0.25s. 2AR- relay of pressing device. R- resistor. 1-R- bypassing adjusting resistor. 2R- 3 kohm. 3R. 4 kohm. 4R- 25 kohm. 5R- 300-600 ohm. 7R- 0-30 ohm C- capacitor 600 μF. A- ammeter, range 0-100 μA, loop resistance of 650-800 ohm. B- button.

4.2.4. A.B. Barman[72] also reports of the use in U.S.S.R. of automatic oscillographs with records being made on camera film to record the nature of changes in the currents, and voltages before and after the occurrence of a fault, so as to examine the stability of parallel operation, type of short circuit, sequence of tripping or closing of individual terminations and also to determine the fault distance. The distance to the fault is estimated from a record of the zero sequence current fed from each of the faulted line, and to speed up the fault location calculations, special nomograms are used. These nomograms are used in conjunction with fixing ammeters connected to record the zero sequence current. These fixing ammeters have their readings fixed by the pointer being pressed down thus leaving a permanent record until reset manually. (Refer Figs 4.1 and 4.2)

4.2.5. The CIGRE Committee Report[68] states that perturbographs and metallised paper recorders are normally still being used by utilities the world over to record fault quantities. Calculation of the distance to the fault from these quantities is done by technical staff.

4.2.6. Disadvantages of Oscillographs on Fault locators

These fault location methods did not find much favour as it involved obtaining the oscillographic film of the fault quantities, analysis of the oscillographic film which once again depended upon human judgement and elaborate calculations which all coupled together increased both time and labour - a condition which was certainly not conducive in the event of a sustained fault.

Generally only earth faults are located by recording line zero sequence current. The method requires the services of specialised technical staff for calculation and interpretation of the recorded quantities causing delay and errors in fault location. Arc resistance, d.c. component and double circuit line effects influence the location of the fault and as such causes errors. Several countries, according to CIGRE Committee Report[68] report of 90% of accuracy with this method.

4.3. ECHO RANGING FAULT LOCATORS - THE LINASCOPE

In 1948, J.R. Leslie and R.H. Kidd developed the Linascope[58]. The "Linascope" is an electronic fault locator which uses an echo ranging method for determining the location and nature of transmission line faults. This device was in use then on open wire telephone circuits for the location of various fault conditions including open and short circuits and high resistance joints. Tests were performed on h.v. transmission lines which were isolated for the said purpose and faults were located at distances as far as at 300 miles. The equipment used the application of a high frequency pulse inserted into the line by means of a h.v. coupling capacitor, and the author proposed to have a photographic recording gear along with the instrument for the continuous inspection of live lines in order to locate transient faults such as would occur with lightning flash over of live line insulators. The principle of this method consisted of the application of a voltage pulse of a short duration of 25micro seconds to the terminals of the transmission line, the voltage would in that case travel with a certain

velocity depending upon the line parameters with negligible distortion and only slight attenuation. Now if at any point in the line there is an abrupt change in the line impedance, then a portion of the incident wave is reflected back towards the source, while the remainder of the wave continues in its original direction. The echo pulses returning from any fault on the line are displayed on a suitable time base cathode ray tube screen, and in order to obtain a steady visual pattern, the pulse is generated repetitively. The time required for the return of any particular echo was then measured and hence the distance to the source of that echo was determined. The magnitude and polarity of the echo gave information regarding the nature of the source of the echo. For example (i) O.C. on line

O.C.	$Z = \sqrt{L/C}$	Incident voltage E Reflected voltage E Transmitted voltage 0

Echo of same polarity and of same source magnitude.

(ii) S.C. on line

	S.C.	Incident voltage E Reflected voltage -E Transmitted voltage = 0

Echo of same magnitude but reversed in polarity. with source.

When locating a fault on a power line, the line is first deenergised and grounds are applied as a safety precaution. The Linascope is then applied to the line directly to one conductor and the other to the ground. The distance to fault is measured by using a calibrated mileage scale laid along the face of the CRO tube. This method is still in vogue particularly in the ITI Fault Locator type 401.[59] The range of this locator is 200 miles, operates on 230 V, 50 Hz, and sends out a pulse of 10 micro seconds duration during each cycle and receives back the echos from the fault. A oscilloscope is used to measure the time between transmitted and reflected pulses and hence the distance to the fault. The exact distance to fault is determined by counting the number of markers from the outgoing pulse upto the tip of the hip. Every marker corresponds to 5 miles length of the line.

The authors in their paper[58] also described the use of the " Linascope " as a transient fault locator as mentioned earlier by application of a high frequency pulse through a h.v. coupling capacitor and an oscilloscope with a photographic recorder. Their experimental results confirmed that all open circuited faults and line to line faults were determined to a reliable degree of accuracy. Similarly in 1949 Spaulding and C.S. Diesmond[60] confirmed the location of h.v. power line faults by the echo ranging means and indicated its use as a transient fault locator.

4.4. FAULT LOCATORS BASED ON MEASUREMENT OF WAVE TIME(RADAR FAULT LOCATORS)

In 1948, Stevens and T.W. Springfield described in their paper[61] a method of fault location based on the measurement

of the time required for a wave to travel between the fault and a known point and listed the following three methods using a general approach.

i) The " pulse radar " method

ii) The " modulated frequency method "

iii) The " fault generated surge method "

The authors inform that " The fault generated surge method" was employed then by the Bonneville Power Administration using two types both of which make use of fault generated surges and were designated as Type A and Type B, to distinguish one from the other. Both the types are automatic and are capable of being coupled to live lines and will complete their measurements before the fault arc is extinguished, and they locate faults which are not sustained. The type A fault locator is accurate, was in successful operation but it then required a photographic film. A further treatment of these fault locators is given in para 4.8 and 4.11.

4.5. GROUND FAULT LOCATORS BASED ON MEASUREMENTS OF RESIDUAL CURRENTS

4.5.1. In 1958, A.C. Lee[62] developed a ground fault locator which is made to operate on the residual current through a special instrument and an instantaneous current relay inserted in the secondary circuit of the current transformers at each end of the line. The principle used here is based on the fact that the distribution of zero sequence current in a system during ground fault depends only on the zero sequence network of the system. The percentage of the total ground current that is contributed by each end of a faulted line is constant for a

given point of fault and varies with the location of fault along the line. The measurement of the zero sequence current input to each end of line at a definite short time after the start of the fault and the ratio of input to one end of the line to the total input is computed. With this information the location of the fault is found with reference to a precalculated plot of this ratio against the distance to fault from one end of the line. The operation of the ground fault locator follows the following sequence of operations.

(i) When a ground fault occurs, the instantaneous current relay energises a telephone type slow relay which after a definite time delay closes a seal in contact so as to cause a pointer locking coil to operate, thereby locking the instrument pointer in the position it occupies.

(ii) A red bulb glows when this operation takes place

(iii) The instantaneous current relay is an ordinary commercial relay mounted externally. The reading obtained from it is then used as described above to determine the location of the fault.

4.5.2. In 1962, Martin J. Lantz published a paper[63] outlining a method for locating ground faults almost similar to the one developed by A.C. Lee[62], but by determining the current data of the phase and residual currents from a single terminal. Ground faults located by ground fault current ratios that is ratio of ground current from one terminal to the total ground current and comparing it with precalculated values has been quite successful. However, when data are available from only one

end of the line such as when one measuring device fails to record or when faults occur in a three terminal line, the ratio of ground currents cannot be used. Further the values of actual fault currents are usually not indicative of the fault location because of the unknown effect of the fault resistance. Thus the author proposed a new method to supplement the ground current ratio and in many cases to enable the fault location to be determined from current measurements of one terminal only. The method requires the values of the faulted phase current and residual line current prior to the opening of the circuit breakers in the faulted area. The method is effective for single phase to ground faults provided substantial positive and zero sequence current components of different magnitudes are flowing into the ground. The ratio of the faulted phase current to the residual line current is used. This ratio neutralises the effect of fault resistance while using current measurements from one terminal only. If data are available from both ends, the ratios of ground current from one end to the total ground current, ratio of phase current from one end to the ground current from one end, and ratio of phase current from opposite end to the ground current from opposite end can be determined. These ratios are plotted against percentage distance of the line. A set of sample curves drawn for Bonnevillo Power Administration are given in the said paper and have been used to determine the fault location. The author has also given a formula for directly calculating the fault location if the circuit does not involve mutual coupling and the formula expresses the fault location in terms of the fault current ratio of phase to ground from one end and the circuit parameters.

4.5.3. Reasons for non use of ground fault locators

The above methods did not find favour perhaps due to the fact that they were meant only for locating ground faults. Further errors due to fault resistance, arc fault resistance and those due to mutual coupling did not give the precise location. The probable uncertainty of the curves did not also help in locating the fault location precisely or to a fair degree of accuracy.

4.6 FAULT LOCATORS USING NEUTRAL AMMETERS

Fault location by neutral ammeters is similar to the method outlined in para 4.5. But these methods are no longer being carried out as this method particularly has the same troubles with arc resistance, tower footing resistance, mutual coupling of double circuit lines, d.c. components etc. and it's accuracy in recording is rather poor. As such no future is predicted for this method by the CIGRE Committee[68].

4.7. FAULT LOCATION USING STANDING WAVE METHODS

The standing wave method[64,69] is based on the resonance and impedance transformation properties of a quarter wave transmission line. The principle used is that when a sinusoidal voltage of frequency 'f', wave length ' λ ', is applied to the terminals of a line, whose length is an integral multiple of $\lambda/4$, with the line terminated in a load Z_L which is different from Z_0, the characteristic impedance, then standing wave patterns are set up on the line. The forward and reflecting waves existing on the line combine to produce nodal patterns alternating with antinodes. Such lines of length $\lambda/4$ and integral multiples of $\lambda/4$ reveal

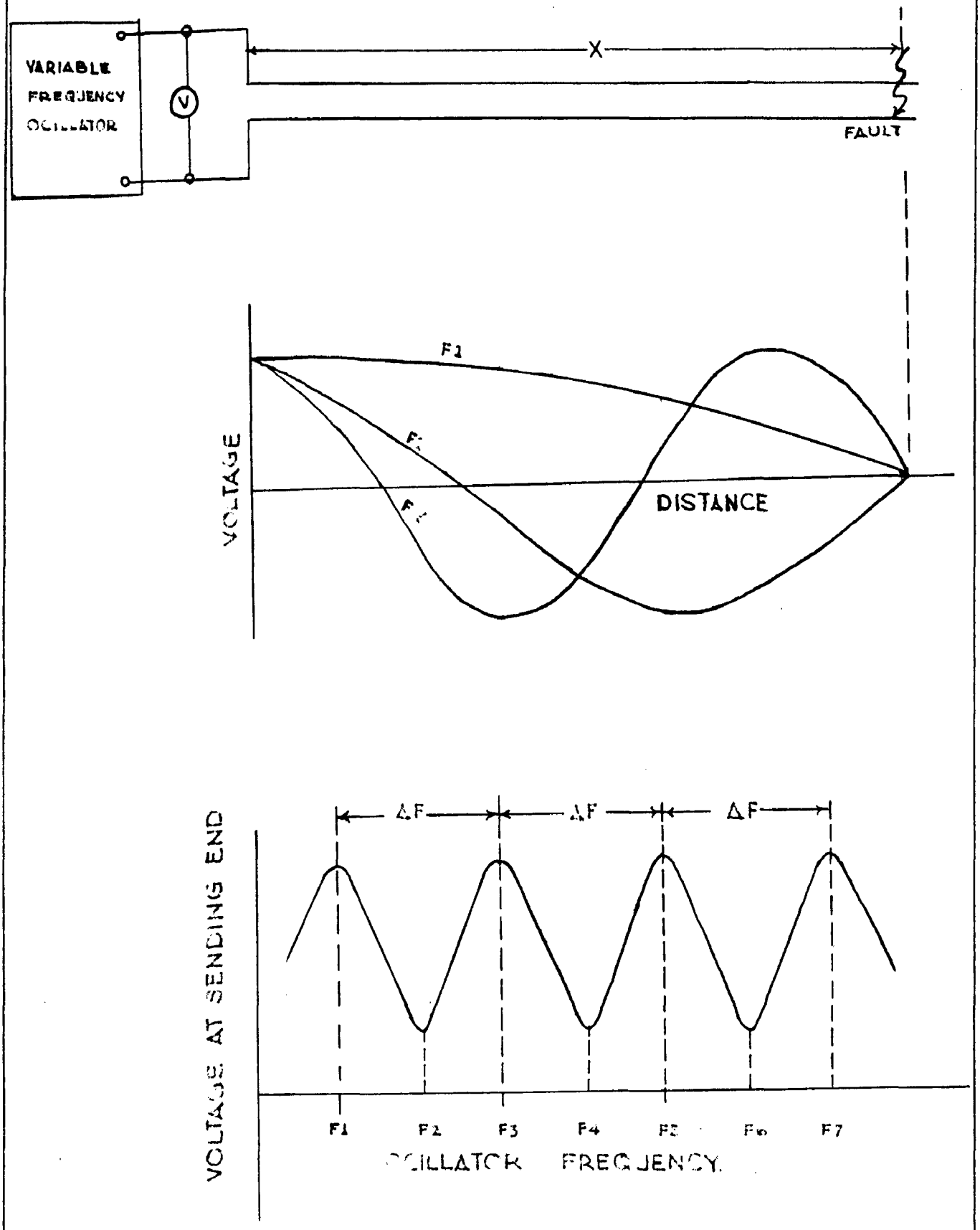


FIG.-4·3- PRINCIPLE OF STANDING WAVE METHOD.

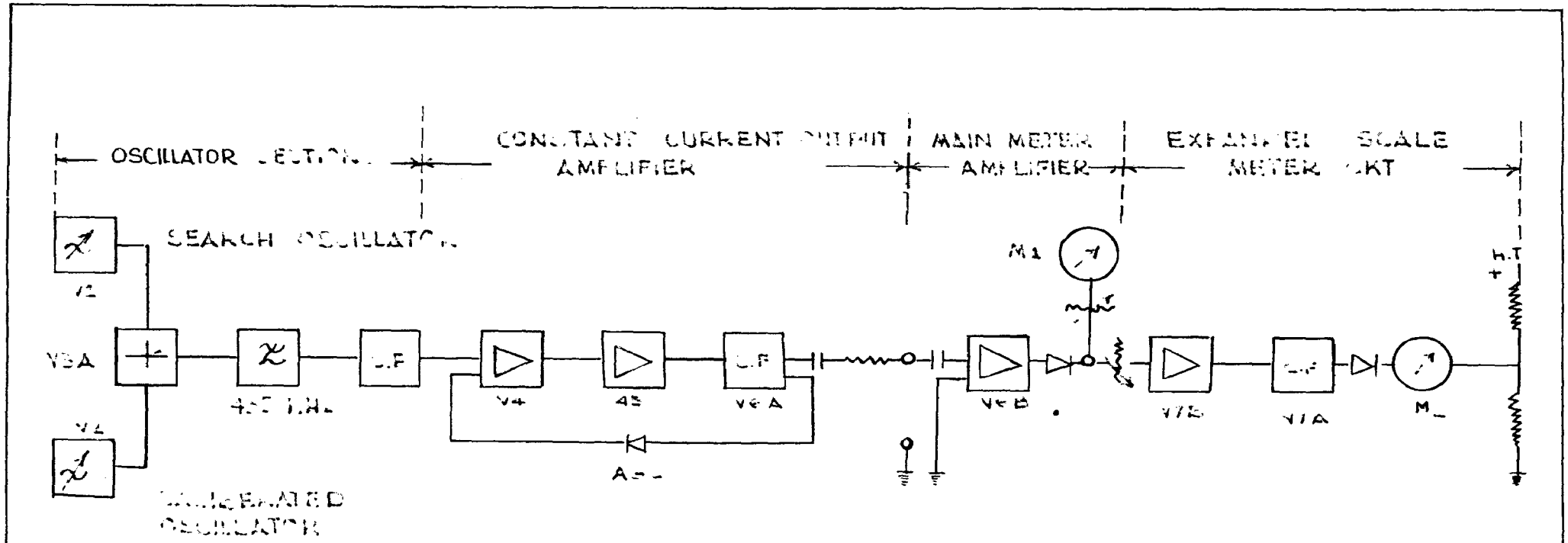


Fig. 4·7- STANDING WAVE METHOD.

the property of acting as impedance transformers in that the load impedance Z_L is presented to the input terminals as an impedance of value $\frac{Z_o}{Z_L}$, when the line length happens to be any odd multiple of $\lambda/4$ and for even multiples of $\lambda/4$, it is Z_L itself. Thus for a long line of $\lambda/4$, an O.C. at the load appears transformed as a S.C. at the source terminals and a short circuit at the load end appears as an O.C. at the sending end. The effect is likewise present when the line length is constant and the frequency of source is gradually increased. However in practice the constant length may take the form of distance 'x' between sending end and a fault somewhere along the line. As the generator frequency is increased its wave length is correspondingly decreased and passes through values $f_1, f_2, f_3 \ldots\ldots f_n$ etc. such that 'x' the fault distance becomes successively equal to $\lambda/4, \lambda_2/4, \lambda_3/4 \ldots\ldots\ldots \lambda_n/4$ etc.

Due to attenuation the S.C. and O.C. appear as maxima and minima. If Δf is the frequency difference between two successive maxima or minima and 'v' the velocity in medium then

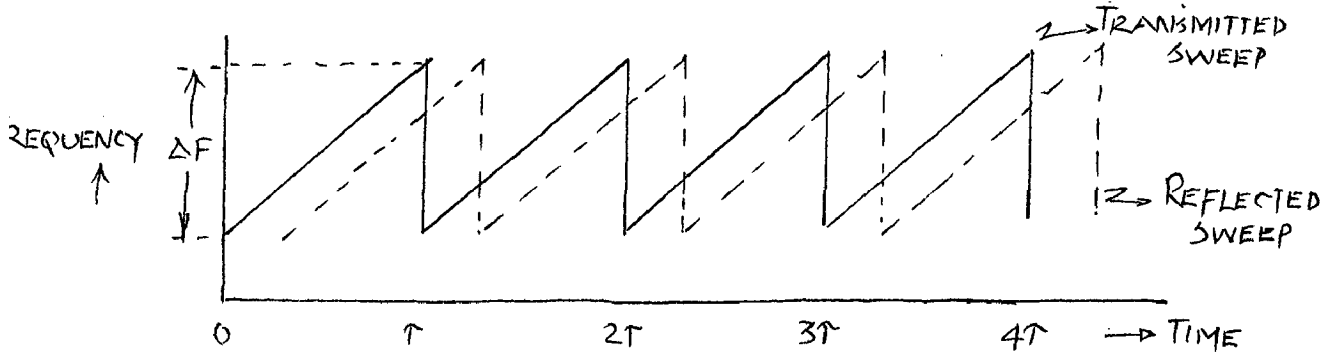
$$x = \frac{v}{2 \Delta f}$$

Hence this method consists in feeding the output of a sine wave oscillator of very wide frequency range into the terminals of the line, and to note the maxima or minima on a high impedance voltmeter such as a VTVM connected in the circuit. (Refer Figs 4.3 and 4.7)

4.8. FAULT LOCATORS USING FREQUENCY MODULATION METHODS

In the Frequency Modulation method, the frequency of a high frequency carrier is made to change linearly in a sawtooth fashion and this pattern is repeated at modulating frequency and

is impressed on the line terminals. The wave at a particular frequency travels at a time 't_1' onwards, gets reflected, and arrives at the sending end at time 't_2'. The interval (t_2-t_1) depends upon the distance of the fault and the wave velocity. During this time, however, the source frequency is constantly changing and the time 't_2' will have attained some new value. Thus we have at any instant of time, two frequencies existing at the input terminals, one lagging in value from the other by a small frequency difference. Those two frequencies are fed to a mixer circuit where they beat with each other and produce a beat or frequency difference which is proportional to the time difference and hence the distance to the fault. An interesting design, development and test results of such a fault locator is furnished by David R.Steven et al[71]. The authors have described a simple pulse radar system and haveanalysed the errors associated with it particularly those due to receiver band width and noise.The frequency modulated systems, according to the authorsnever approached beyond the analytical studies that were done in the early 1940's and the system described by them is similar to the pulse radar system in that it requires a transmitter, a receiver, an antennae and a reflecting target. This system transmits a continuous sawtooth wave form, which is used on the modulating signal. This when used as a transmitting signal varies linearly with time for a given interval and then repeats. This signal when it reaches a reflecting target, returns to the antennae, and the signals present at the antennae are as follows:



The frequency difference between the two wave forms is a constant frequency in the time interval $n\tau + T$ to $(n+1)\tau$ for $n = 1,2,3, \ldots\ldots N$ and T is the time required for the wave to travel from the ~~transmitter~~ to the target and back whilst τ is the sweep duration. This constant frequency difference is stated to be directly proportional to the distance to the target and the same is given by the equation.

$$d = \frac{cT}{2}$$

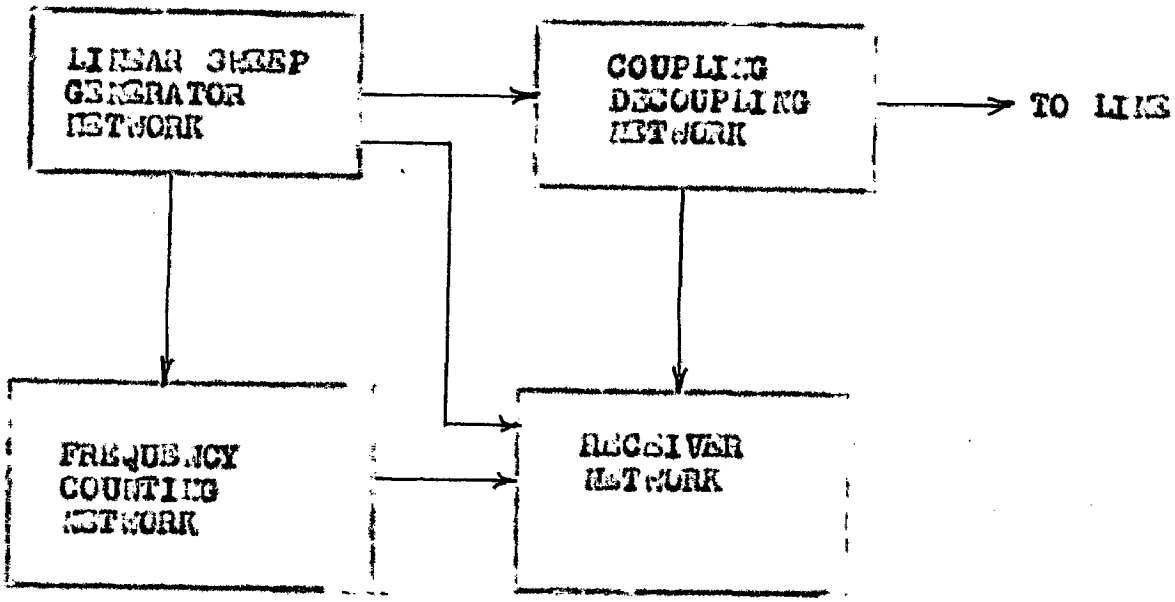
The frequency δF and time T are related by the equation

$$F = \frac{T}{\tau} \Delta F$$

$$\therefore \quad d = \frac{c\tau\delta F}{2\Delta F}$$

The author has compared the errors that would be produced in the frequency modulated system with those of the pulse radar system and has concluded, that the frequency modulated system is more accurate. In addition the frequency modulated systems possess all the advantages of a pulse radar system with a higher signal to noise ratio. The block diagram of a frequency modulated fault

location system as developed by him is as follows :

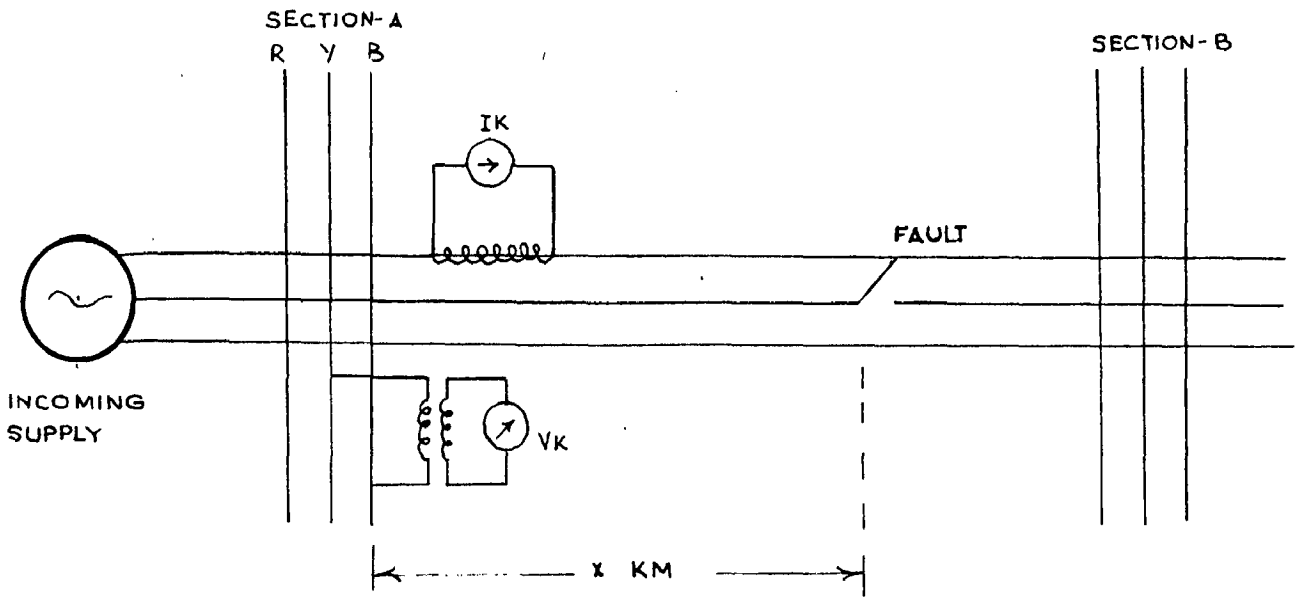


The system consists of a linear sweep generation network followed by a coupling/decoupling network to place the sweep on the line under test. The coupling/decoupling also provides a signal to the receiver network which in turn supplies the frequency difference δF to the frequency counting network. The prototype of the above fault locator was subject to tests on a simulated line to observe the waveform at various points and to photograph them. Field tests with the prototype indicated that the uncertainty in the measurement and by calculations was found to be of the order of 2.5 cycles on a 200 miles line which corresponds to about 0.1 mile of 530 ft.

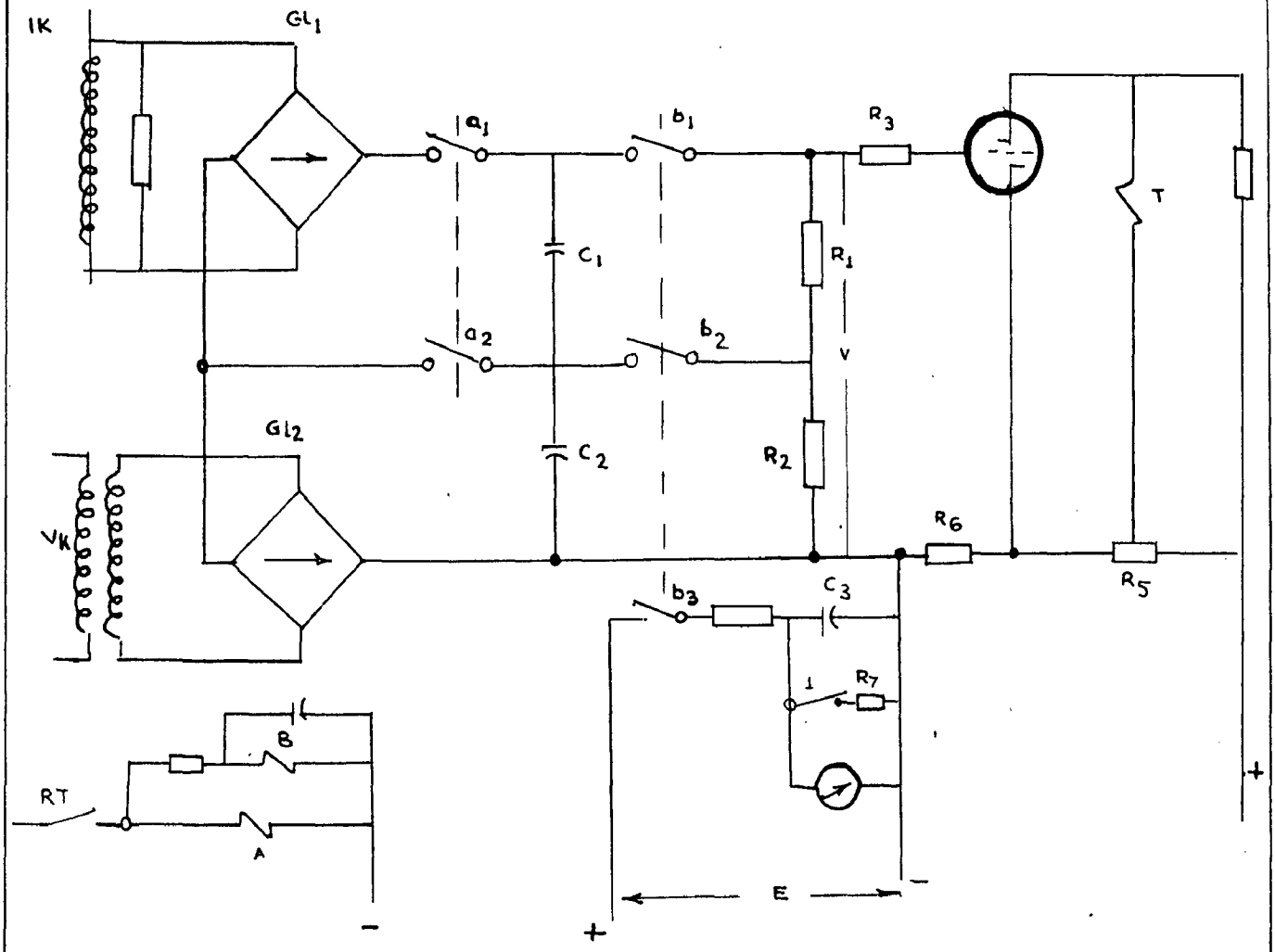
4.9 FAULT LOCATORS BASED ON MEASUREMENT OF IMPEDANCE

4.9.1 Fault Locators based on the measurement of impedance have been developed by Siemens Ltd., in 1965-1966 and the same has been published in the firm's review[65,66]. These fault

FIG. 4·4 - FAULT LOCATOR BASED ON MEASUREMENT OF IMPEDANCE.



(a)- Arrangement for fault locater



(b) Circuit diagram for fault locater.

locators are connected permanently in the system and the fault point is measured on the principle of distance measurement. The device is therefore fed with the fault current and the voltage drop along the faulted conductor. The device determines the quotient of the voltage and current and hence the distance of the fault in the form of an adjustable resistance. If the value of this resistance is made equal to the impedance of the conductor on the line section to be supervised, the length of line section corresponds to 100 percent of the fault scale deflection. The firm manufactures two types one for supervising one single line on any end and the other with an additional relay to supervise as many as four lines. (Refer Fig 4.4)

4.9.2. The CIGRE Committee[68] has made the following observations on these type of fault locators.

(a) the opening time of high speed circuit breakers is sufficient to allow the locator to measure the distance to the fault, the requirement of which is approximately 40 m.secs.

(b) arc resistance influences the measurement, but it can be compensated by using one locator at each line terminal.

(c) double circuit lines require the same compensation as is required in the case of earth faults in distance protection.

(d) the d.c.component of the fault current has a negligible effect.

(e) the error from user countries has been quoted as anywhere between 3 percent to 20 percent and over and these generally refer to laboratory tests.

(f) Artificial fault tests carried out at site to explore operation of the locators have indicated errors greater than 5 percent especially for faults near the fault locator station.

4.10 FAULT LOCATORS BASED ON MEASUREMENT OF INDUCTANCE (Refer Fig 4.5)

4.10.1 A locator based on the measurement of inductance has been developed by M/S G.E.C. Measurements of England[67]. The manufacturers claim that it is ideally suited for short circuit and flashing faults on overhead lines. The device upon the occurrence of a fault measures the line inductance between the fault and the relaying point before the circuit breaker opens and stores this information. This information is retrieved from a plug-in portable unit for interpretation of the fault location after which the stored information is erased. Two types namely XTF 31 and XTF 32 are available, one of which namely XTF 31 is suitable for general use and installation at relaying points while the other type is for use on systems with autoreclosing facilities. In this type the information stored is erased automatically upon the occurrence of subsequent faults and then any subsequent information can be stored. The device requires two separate units to cover all types of faults - one to measure phase to phase faults and the other to measure phase to earth faults. The unit connected for measuring phase to earth faults requires an externally mounted residual current compensating transformer.

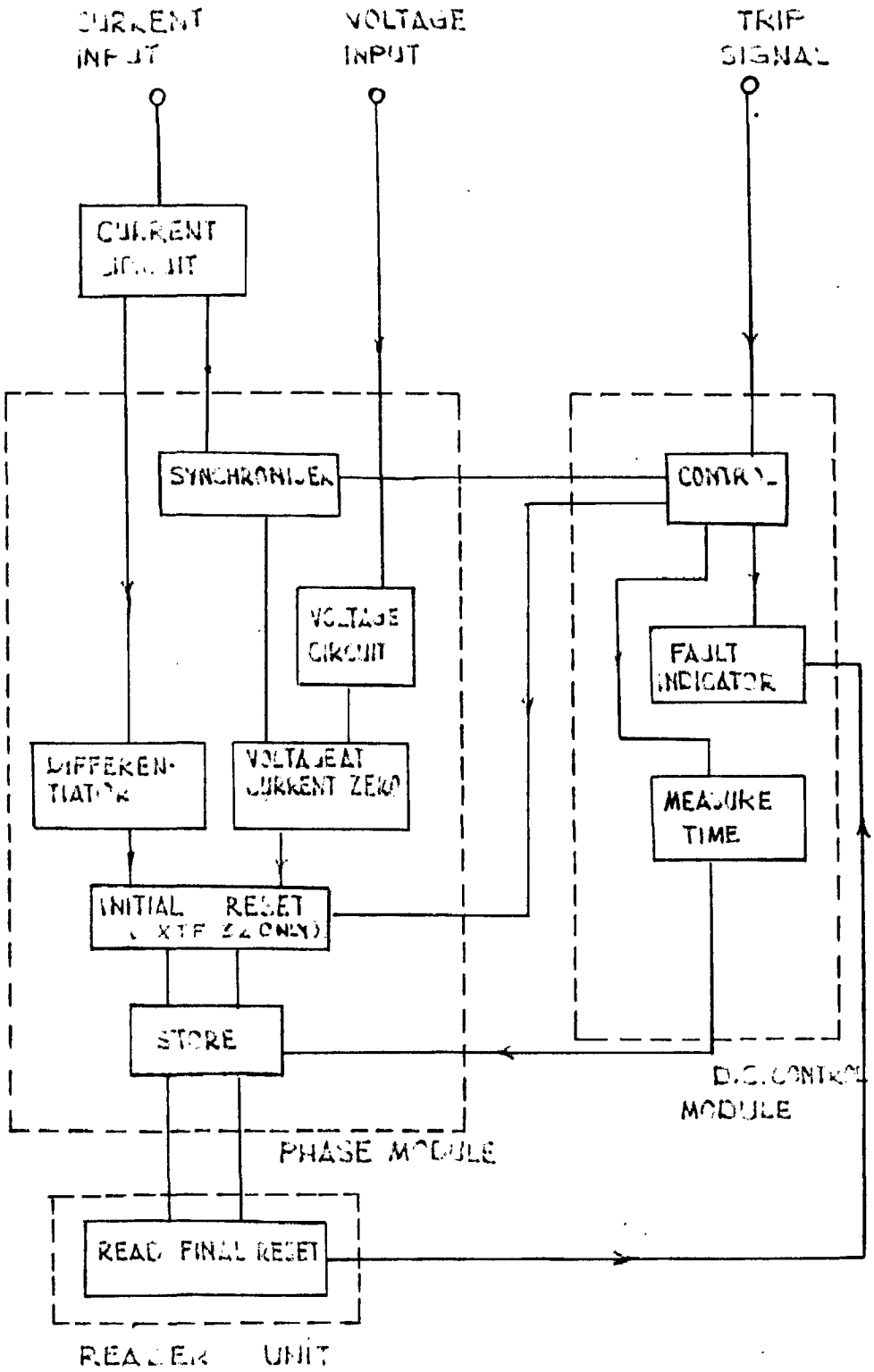


FIG. 4·5- FAULT LOCATOR BASED ON INDUCTANCE MEASUREMENT.

4.10.2 The principle of measurement is based on the instantaneous equation

$$e = L \frac{di}{dt} + iR$$

Where e, L, i, t and R have the usual meaning.

The measurements are taken at time t = 0 and hence the above equation simplifies to

$$e = L \frac{di}{dt}$$

The inductance of the line is measured by comparing the instantaneous voltage 'e' with the rate of rise of current di/dt at current zero and these two quantities are stored in capacitors until the measuring unit is used to measure the ratio $L = \frac{e}{(di/dt)}$.

4.10.3 The principle of measurement of the inductance eliminates the effects of the arc resistance, d.c. component, tower footing resistance, and fault current value. However compensation is required in the case of double circuit lines. The measurement errors according to laboratory and field tests do not exceed 3 percent according to CIGRE report(68).

4.11 PULSE REFLECTION FAULT LOCATORS (Radar Fault Locators)

4.11.1 The pulse reflection locator classified under Radar Locators as described in the CIGRE paper(68) states that r.f. energy or d.c. is used to trigger the time base of a cathode ray oscillograph. The reflected pulses are shown on the oscillograph just on as in the Echoranging type of fault locator such that the distance along the X-axis is proportional

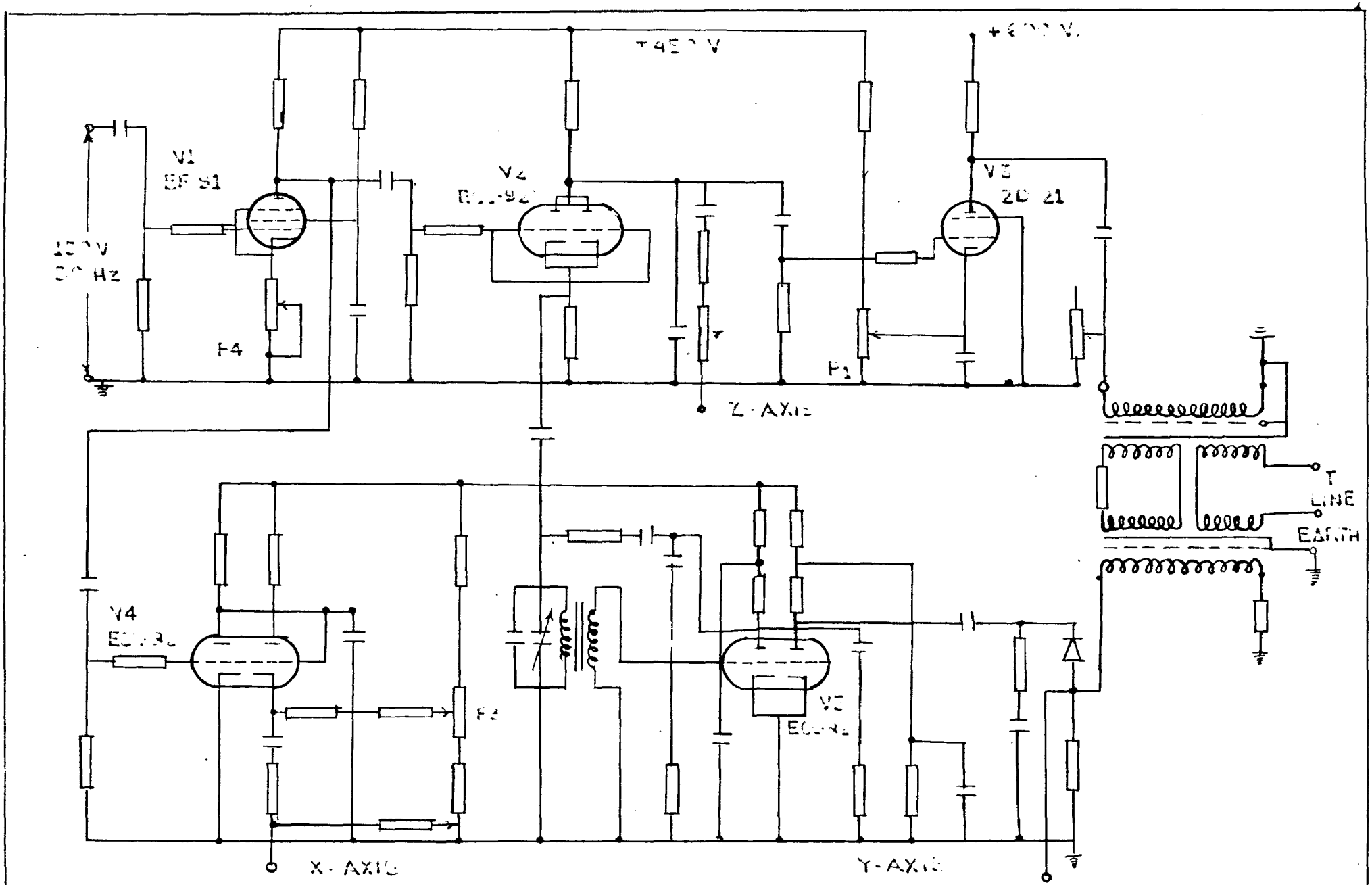


FIG. 4A - PULSE REFLECTION FAULT LOCATOR

to the distance to the reflecting point on the line at the point of fault. The trace can be expanded and shifted along the X-axis to permit more detailed examination of interesting sections. These traces are also compared with photographs showing natural reflections from healthy line sections in order to detect any additional reflections. The accuracy of these fault locators is reported to be good and a fault can be located within ± 300 m to 600 m or within ± 1 percent to 2 percent of the length of the line whichever is the greater. It is mentioned that all countries use the pulse reflection locator on dead lines and only for permanent faults. The coupling to the faulted line is generally done by means of an insulating rod or a shunt capacitor. (Refer Fig 4.6) The line traps have no significance as they are bypassed. The locators may be used for single or double circuit lines and are of course not influenced by arc resistance. The locators are generally provided with arresters to safeguard operating personnel.

4.11.2 The following causes of maloperation have been reported.

(i) faulty components especially with the equipment manufactured earlier and still in use.

(ii) power line carrier signals.

(iii) ice on conductors

(iv) attenuation of the signal due to the coupling by cables to the H.V.lines

(v) inductive disturbance from live busbars

(vi) difficulties in exploring Z-lines and very high resistance faults

(vii) misuse of the devices by operating personnel

4.11.3 It is quite a well known fact that transmission lines across the country are probably the most noisy setting as far as a signal of any type is considered and another characteristic of the line is the attenuation. Associated with noise and attenuation is the limited band width available for any signal applied. Power lines carry not only the power frequency voltage and current but also higher frequencies which are generally used for telemetry, relaying, communication etc. The presence of these higher frequencies limits the available frequency ranges for additional systems. Thus a fault locator placed on the line to operate with the line in the energised condition will have severe bandwidth restrictions.

4.11.4 The pulse system described earlier is essentially a closed loop radar system because the pulse is transmitted along the line instead of into the atmosphere and a reflected pulse is received when a fault exists on the line. The several advantages of a pulse system are

(i) the speed with which the fault is located

(ii) the ability to make the system mobile

(iii) relative simplicity of the system

(iv) very few persons are required to operate the system

The chief disadvantages of the pulse system are

(i) limited band width of the transmission systems causing the transmitting pulse to be distorted

(ii) likelihood of maloperation due to causes such as the presence of carrier signals, attenuation etc.

(iii) relatively high cost.

4.11.5 The Foranti live line monitor[68] explores the live line upon the occurrence of a fault with the monitor switched to the faulted line by it's distance protection. The monitor locates faults by using the principle of radar distance measurements which in effect consists of a transmitting a series of short r.f. pulses of 1 M c/s along the line being monitored and any discontinuity causes the pulse to be reflected back to the monitor receiver. The received signal is displayed as a trace on a cathode ray tube display. Line damage and open or short circuit conditions cause large scale pulse reflections that are easily recognised. The location of the fault is then simply determined by the examination of the trace, the whole length of the X-axis representing the whole length of the line. A polaroid camera is sometimes incorporated to provide automatic recording facilities. Field tests carried out have given encouraging results and an artificial fault was located with a maximum error of one tower for a distance of upto 70 miles. The equipment is rather expensive and problems arisein it's coupling to live Hv lines as also specialised shift personnel are required at stations where they are installed. Hence it's use has become limited to special cases.

4.11.6 The development of new types of radar fault locators[68] use the transient quantities that arise during the occurrence of a fault. Three such new devices have been recently developed. The first of these utilises the high frequency fault transient for detection and location of the fault. The transient waveform generated by a fault has

(i) a d.c. component

(ii) a group of high frequency components

and it has been demonstrated that the high frequency is inversely proportional to the distance of the fault, and the frequency also depends upon the type of fault. Records from automatic oscillographs in the U.S.A. indicate a high harmonic content for ground fault currents of less than 40 percent of current transformer rating and the magnitude, frequency of the harmonics depends upon the ratio of the nonlinear resistance in the circuit to the impedence and increase considerably during a fault with certain frequencies predominating[19]. Thus the new device measures the frequency of the fault transient, it's amplitude and line current and operates under substation computer control which in turn determines the type and location of the fault. Laboratory tests with this device have indicated encouraging results, and the conclusion is that these type of fault locators merit further investigation on account of their feasibility.

The second of these devices uses the pulses from the fault itself. The first travelling wave that reaches the end station will start a time counter in the equipment, the wave then reflects back from the station towards the fault and meets

the arc. If this has a sufficiently low impedance, the wave reflects again and reaches the end station for a second time. The time counter stops and the measured time will correspond to twice the distance to the fault. Field tests on laboratory prototypes have indicated successful locations to about 40 percent only and limits it's proper functioning to lines without any extra reflection points.

The third device is similar to the second device but uses the time difference between the receipt of the travelling waves at both ends of the line. It has been stated that about 65 percent of all faults were located within 2 percent of the length of the line with this type.

4.12 FAULT LOCATOR USING NEGATIVE SEQUENCE QUANTITIES

The CIGRE Committee[68] also reports of the development of a locator which works from negative sequence quantities. It covers all types of faults except a three phase fault. The negative sequence quantities I_{2A}, V_{2A}, I_{2B}, V_{2B} at the ends of a faulted line AB have to be measured. If 'Z_2' is the impedance per KM and 'L' the length of line AB in KM, the distance 'x' between 'A' and the fault is given by

$$x = \frac{(V_{2B} - V_{2A}) + L\, I_{2B}\, Z_2}{(I_{2A} + I_{2B})\, Z_2} \quad \text{KM}$$

It's accuracy is no better than 90 percent.

4.13 USE OF TRANSISTORS IN FAULT LOCATORS

The time available for estimating the distance to fault and leaving a record is the total clearing time of the

fault which, nowadays, is only a few cycles and clearly insufficient for electromagnetic movement. But with transistor circutory very fast measurement and recording is possible and some distance relays already include a transistorised fault locator[49].

4.14 SURVEY OF MAIN TYPES OF FAULT LOCATORS

In their survey of the main types of locators in use, CIGRE Committee[68] has reported that the pulse reflection locator is widely used owing to it's accuracy, it's low cost and as one of the first to be produced by the industry. Many countries use locators which measure directly the distance to the fault by interpreting fault currents and voltages as supplied to distance relays. The poor accuracy of these locators has been pointed out as due to the effects of arc resistance and effects of mutual interference due to double circuit lines.

A few countries locate earth faults only by low inertia ammeters which are clamped automatically at a fixed time after the occurrence of a fault. The reading of the instrument is followed by calculations done by the technical staff, and the accuracy has been acceptable only for single phase faults.

4.15 IMPORTANCE OF A FAULT LOCATOR IN SERVICE

The importance of having a fault locator in service are

(i) to give an idea to the despatcher when having to decide whether to reenergise a tripped line or not.

(ii) to indicate the patrol team to find the point of repair as quickly as possible.

(iii) with the installation of fault locators, it is sufficient to patrol only that section of the line as indicated by the fault locator.

(iv) line patrolling from the ground is relatively slow and expensive in bad weather or rough country and do not always locate the point of occurrence of a transient fault. Sectionalised switches by isolating a sustained fault in a line section simplifies the problem, but does not altogether solve the problem of locating the fault with the minimum possible time. This is overcome by having a fault locator in service.

(v) A fault locator in service reduces permanent outages as timely maintenance of transient faults can be done and this therefore enhances the reliability of the system.

4.16 REASONS FOR RESTRICTED USE OF FAULT LOCATORS

The restricted use of the fault locators appears to be

(i) the locators in use are rather inaccurate

(ii) the cost of new locators is rather high.

There is however a general tendency to increase the use of locators for permanent and transient faults of any kind, in order to limit outages of overhead lines and prevent permanent faults by checking the sections of the line where transient faults have occurred in order to find and repair weak spots

4.17 REQUIREMENTS OF A FAULT LOCATOR[61]

The requirements of an ideal fault locator are

(i) It should complete it's measurement before the fault arc is extinguished. In this way it will locate faults which are not reestablished when the line is reenergised but which may, nevertheless have caused damage.

(ii) It should be able to locate a fault to the nearest tower or span.

(iii) It should be designed for installation in an accessible spot.

(iv) It should not involve slow and cumbersome work such as developing photographic films before answers are available.

(v) The results should be in a form as can be interpreted readily by any station operator or line foreman without having to resort to elaborate, time consuming calculations.

(vi) The equipment should operate with safety to personnel and service.

(vii) The equipment should be simple, rugged and relatively inexpensive.

4.18 CAPABILITY OF A FAULT LOCATOR[71]

A fault locator should be capable of detecting and locating the different types of fault encountered and these are

(i) Momentary or transient faults (an example is a lightning flashover of an insulator which leaves no permanent damage). However these faults should be located to facilitate inspection and also for data collection

purposes for the future.

(ii) Sustained or permanent faults - These include grounded conductors and as well as open and short circuits at all levels of test voltage. This type of fault must be repaired as soon as possible to put the system back into operation.

(iii) High breakdown faults - These appear as faults to only high voltages. An example is a fallen line that is close to but not touching the ground. This creates arcing grounds and prevents circuit breaker reclosure. These faults can also be considered as permanent as they must be cleared before system operation is restored.

(iv) Latent faults - These are localised impairments which do not/prevent successful operation under normal conditions. However the design insulation margin for surges and dynamic overvoltages is degraded. This is a condition that deteriorates with time and should be located with preventive maintenance in mind.

4.19 CONCLUSIONS

In conclusion it may be stated that the existing types of fault locators are reliable and have to a large extent been successful with permanent faults. There is a general tendency towards the greater use of fault locators for locating both permanent and transient faults. New methods and systems of fault locators seem to offer good prospects for locating both permanent and transient faults precisely, satisfying the requirement and capabilities of fault locators.

CHAPTER-5

DESIGN AND DEVELOPMENT OF THE DISTANCE RELAY ALONG WITH THE FAULT LOCATOR USING ANALOG/DIGITAL CIRCUITS

5.1. INTRODUCTION

A relay or relaying devices which in the present case is the fault locator essentially have the following four elements(72) These are detecting, actuating, delaying and controlling elements.

The detecting element responds to external variables and abruptly changes the state of the actuating element when the external variables reach certain values or exceed certain threshol conditions.

The time delay element introduces a time lag in the relay operation.

The actuating element if it effects changes in the pick up settings of the detecting elements of other devices such as a tripping device, is then called the controlling element.

5.2. MEASURING UNITS

The detecting and actuating elements are in a broad sense referred to as the Measuring Unit and the delaying element is inherently present in all such measuring units. Measuring units may be electromagnetic or static, and a comparison of these has been treated in the earlier Chapters. Although the relay and the fault locator proposed for design in this chapter does fall within the domain of static devices, yet it has been treated separately and styled as such as digital circuits deploy an altogether different mode of operation, using a set of well established codes and circuitry which respond to logic governed

by Boolean Algebra. As such a resume of the codes, the logic circuits and functionsperformed by them is listed out in the paragraphs to follow.

5.3. BINARY, DECIMAL AND OCTAL NUMBERS(73,74)

5.3.1. A number system is nothing more than a code representing quantity, and for each distinct quantity there is assigned a symbol. Thus in the decimal number system we have 10 basic symbols or digits from 0 through 9. However in a binary number system we have only two basic symbols namely 0 and 1. In the decimal system, after we reach the number 9 we form combinations of decimal digits to get numbers 10,11 ..... etc. and these are obtained by combining the second digit with the first and so on. Similarly in the binary number system we combine the second digit with the first and others to obtain binary numbers 10,11, 101 ..... etc.

The base or radix of a number system refers to the number of basic symbols used. Hence the decimal system has a base of 10, the binary a base of 2 and the octal a base of 8.

5.3.2. Binary to Decimal Conversion (73)

Each binary digit position has a value or weight which increases from right to left in the ascending powers of 2 commencing from 2^0. Diagramatically the digit positions of a binary number have the following decimal weights ;

etc.←.....	2^4	2^3	2^2	2^1	2^0
etc.←.....	16	8	4	2	1

Hence in a binary system if there is a 1 in a particular digit position, we include the weight of that position and if there is a 0, we disregard the weight of that position. The decimal equivalent is obtained then by adding the remaining weights. This is achieved by directly writing below the binary number the decimal weights, striking out those with 0 digit positions and then adding the remaining weights. As an example the decimal equivalent of 10101 = 16 ß 4 Z 1 = 16+4+1 = 21

However in the case of binary fractions, the weights of each digit position to the right of thebinary point are given by

$$\underset{\uparrow}{\cdot}\ 2^{-1} \quad 2^{-2} \quad 2^{-3} \quad 2^{-4} \ \ldots\ldots\rightarrow \text{etc.}$$

Binary point

Thus the decimal equivalent of 1011. 11 would be

$$(8 + 0 + 2 + 1) \cdot \left(\tfrac{1}{2} + \tfrac{1}{4}\right) = 11.75$$

5.3.3. Decimal to Binary Conversion[73]

Although there are several methods available, the most popular one is the Dibble-Dabble method. In this method, the decimal number is progressively divided by 2, with the remainder being written separately. The remainders taken in the reverse order form the binary number.

As an example

2	25		
2	12	remainder	1
2	6	remainder	0
2	3	remainder	0
2	1	remainder	1
	0	remainder	1

Thus the binary equivalent of 25 is therefore 11001. However in the case of fractions we multiply by 2 and record a carry into the integer position. The carries taken in the forward order is the binary fraction

As an example
$0.625 \times 2 = 1.25$ with a carry of 1
$0.25 \times 2 = 0.5$ with a carry of 0
$0.5 \times 2 = 1.0$ with a carry of 1

Therefore the binary equivalent of 0.625 = 0.101.

5.3.4. Rules of binary addition and subtraction(73)

Addition	Subtraction
0+0 = 0	0-0 = 0
0+1 = 1	1-0 = 1
1+0 = 1	1-1 = 0
1+1 = 10	10-1 = 1

Addition of binary numbers is done easily by following the ordinary rules of addition. However subtraction is done easily by other methods which require the definition of 1's complement and 2's complement of a binary number. The 1's complement of a binary number is the number we get when we change each 0 to 1, and each 1 to a 0. Thus the 1's complement of 1010 is 0101.

The 2's complement of a binary number is what we obtain when we add a 1 to the 1's complement.

Thus 2's complement = 1's complement + 1.

The 2's complement and 1's complement are very useful in subtraction. In subtraction, instead of subtracting a number we add the 2's complement to it, and disregard the last carry.

As an Example to subtract 1010 from 1101

1's complement of 1010 is 0101

2's complement of 1010 = 0101 + 1 = 0110

$\therefore$ 1101 - 1010 = 1101 + 0110 = $\not$ 0011

Disregarding the last carry 1, the solution is 0011.

The other approach using the 1's complement is similarly done by adding the 1's complement of the number. The last carry is then added to the number to get the final answer.

As an example to subtract 1010 from 1101

1's complement of 1010 is 0101

$\therefore$ 1101 - 1010 =

```
  1101
 +0101
 -----
 10010
    |
    +1
 -----
  0011
 -----
```

The carry 1 which was in the last position obtained after adding the 1's complement is removed and added it onto the remainder as shown above. This is called the " End-Around Carry ". The end around carry also indicates if the final answer is positive or negative. If there is no end around carry, the final answer is negative and it is in the 1's complement form. Otherwise with a carry, the answer is +ve and remains as such..

Example to subtract 1101 from 1010

1's complement of 1101 = 0010

$\therefore$ 1010 - 1101 =

```
  1010
 +0010
 -----
  1100
 -----
```

There is no end-around carry, and 1100 obtained is in the 1's complement form. Hence the final solution is the 1's complement of 1100 which is 0011 and the answer is negative. Thus the final answer is -0011 by prefixing the -ve sign.

5.3.5. Binary multiplication and Division(73)

The rules for binary multiplication are

(i) 0 x 0 = 0

(ii) 0 x 1 = 0

(iii) 1 x 0 = 0

(iv) 1 x 1 = 1

Multiplication is done as in ordinary algebra when large numbers are multiplied.

Division follows the same pattern as multiplication.

5.3.6. Octal Numbers(73)

As already mentioned in para 5.3.1. Octal numbers have a base of 8, and the digits of the octal system are 0,1,2 through 7. Those digits from 0 to 7 have exactly the same meaning as in a decimal system. The octal numbers beyond 7 are counted in the same manner as in the binary system, that is by combining the first digit with the second digit and so on. Thus the octal numbers beyond 7 will be

10, 11, ... 17, 20, 21, ... 27, 30, ... 37 etc.

The octal numbers can also be obtained by writing down the decimal numbers and cancelling out those numbers that contain 8 or 9. The remaining numbers will then be the octal numbers.

5.3.7. Octal to Decimal Conversion[73]

In the octal system each digit corresponds to a power of 8. The weights of each digit position in an octal number are reckoned from right to left in the ascending power of 8 commencing from an idex of 0. However in the case of fractions, the weight of each digit position is reckoned beyond the octal point from left to right in the descending power of 8 commencing with an index of (-1). Thus the weights of the digit position is as follows :

$$\text{etc. .... } 8^2,\quad 8^1,\quad 8^0 \;.\; 8^{-1},\quad 8^{-2},\quad 8^{-3} \text{ ..... etc.}$$

Octal point

Thus to convert octal number into its decimal equivalent we need to only multiply each octal digit by its weight and add the resulting products.

Thus $257_8 = 2(8^2) + 5(8^1) + 7(8^0) = 175_{10}$

5.3.8. Decimal to Octal Conversion[73]

A dibble-dabble method as described under decimal to binary conversion is very useful except that the number is progressively divided by 8 and the remainders taken in the reverse order give the octal number.

Example : To convert 175_{10} to an octal number

8	175		
8	21	remainder	7
	2	remainder	5
	0	remainder	2

$\therefore \quad 175_{10} = 257_8$

With decimal fraction we progressively multiply by 8, writing down the carry into the integer position. The carries taken in the forward direction give the octal fraction.

Example: To convert 0.23_{10} to octal fraction

$0.23 \times 8 = 1.84$ with carry 1
$0.84 \times 8 = 6.72$ with carry 6
$0.72 \times 8 = 5.66$ with carry 5

$\therefore \quad 0.23_{10} = 0.165_8$ and so on

5.3.9. Octal to binary Conversion(73)

This is the most important use of octal numbers. The relation between octal digits and binary digits is obtained by writing to 7 in each system.

Binary	000	001	010	011	100	101	110	111
Octal	0	1	2	3	4	5	6	7

From the above tabulation, any octal number upto 7, can be converted into it's binary equivalent. The base 8 of octal numbers is the third power of 2, the base of binary numbers. Hence for numbers greater than 7. We merely convert one octal digit at a time.

Example: $23_8 = (010 \quad 011)_2$

The space left between each group of three digits makes it easier to read the binary number. Mixed octal numbers consisting of integers and fractions are also converted similarly.

Example: $34.562_8 = 011\ 100\ .\ 101\ 110\ 010$

5.3.10. Binary to Octal Conversion[73]

This conversion is a reverse of the process described in para 5.3.9. The binary number is regrouped in bits of three's commencing from right to the left and left to the right of the binary point. If the last bits to the extreme right and left do not make a bit of 3's, then zeros are added to make it into a bit of three.

Example: $1011.\ 01101_2 = 001\ 011\ .\ 011\ 010_2$

$= 13.\ 32_8$

5.3.11. Advantages of octal to binary and vice-versa Conversions[7

(i) Obtaining information in and out of a digital system is easier.

(ii) requires less circuitry because it is easier to program, read, and to print out octal numbers than binary numbers.

(iii) Large decimal numbers are easily converted into binary if we first convert to octal and then to binary. The reason for this is that a direct decimal to binary conversion requires many more divisions than a decimal to octal conversion.

Example : To obtain the binary equivalent of say 363_{10} we first convert it to octal to obtain 553_8. This octal number on conversion to binary yields $101\ 101\ 011_2$, the required binary equivalent.

5.4. BINARY CODES[73,74]

5.4.1. Binary codes are a compromise between the binary and decimal number systems. These are known as binary-coded decimals(BCD) and combine some of the features of both the decimal and binary numbers. There are an enormous number of codes of which the well known are the 8421, Excess 3 bit code and the Gray code.

These codes are used to display directly the result of arithmetic operations and hence most numerical displays interface directly with decimal code representation.

5.4.2. The 8421 Code[73,74]

The 8421 code expresses each decimal digit by it's 4-bit binary equivalent. The process of changing each decimal digit into its 4-bit binary equivalent is termed as 'encoding.

For example a decimal number like 439 encodes itself into 1000 0101 1001 in the 8421 code. The largest 4-bit binary group used in the 8421 is 1001 which indicates that only 10 out of a possible 16, 4-bit groups are used and the rest are not employed. As such the 8421 code is identical to natural binary through decimal number 9. It is because of this, it is called the 8421 code, the weight in each group are 8,4,2,1 in the ascending powers of 2 from 2^0, reading from right to left - the same as for natural binary numbers. Above 9 the 8421 code differs sharply from the binary code. The advantage of this code is the ease of converting to and from decimal numbers as we encode only one digit at a time. A disadvantage is that the rules for binary addition do not apply to the entire 8421 number but only to the individual 4 bit groups. Decoding a 8421 number is merely a reversal of the process of encoding.

5.4.3. The excess 3-bit code [73,74]

To encode a decimal number into its excess 3-form, we add 3 to each decimal digit before converting to binary. It is to be noted here that when we add the number 3, any carry obtained is not carried into the next column, but is retained in the column itself.

Example : To convert 29 to an excess 3-number we proceed as follows

$$\begin{array}{r} 2 \\ +3 \\ \hline 5 \end{array} \qquad \begin{array}{r} 9 \\ +3 \\ \hline 12 \end{array}$$

whose binary equivalent is 0101 1100 and is the required excess 3- number in the excess 3-bit code.

a) As in the case of the 8421 code the excess 3 bit code uses only 10 out of the possible 16, four bit groups.

b) It is a self compensating code which means that 1's complement of any 3-number represents the 9's complement of the decimal number. (The 9's complement is obtained by subtracting each decimal digit from 9. For example 9's complement of 25 is 99-25 = 74).

c) The excess 3-code is an unweighted code.

d) In the excess 3 code whenever we add two decimal digits whose sum is 9 or less, an excess 6 number results and hence to return to excess 3-code we must subtract 3.

e) Whenever we add decimal digits whose sum exceed 9, there will be a carry from one group into the next. When this happens the group that produced the carry will revert to 8421 form. To restore the answer to excess 3-code we must add 3 to the group that produced the carry.

f) The chief advantage of an excess 3-bit code is that all operations in addition use ordinary binary additions.

g) It has also the advantages that 1's and 2's complements as used in binary subtraction can also be used in subtraction of excess 3- numbers.

5.4.4. The Gray Code[73,74]

This code also called as the " Reflected Binary System " is an unweighted code which is particularly not suited for arithmetic operations but is quite useful in analog to digital convertors. It's main characteristics are that each number differs from the preceding gray number by a single bit only.

5.4.4.(i) Conversion from binary to gray[73]

i) The first gray digit is the same as the first binary digit

ii) Each pair of adjacent bits are added to get the next gray digit disregarding any carries that occur.

5.4.4.(ii) Conversion from gray to binary [73]

i) The first gray and binary digit which are the same as retained .

ii) The first binary digits and the next gray digits are added to obtain the second binary disregarding the carries. This process of diagonally adding is continued to get the remaining gray code digits.

5.5. BOOLEAN ALGEBRA AND GATES [73]

5.5.1. Boolean Algebra

Boolean algebra is an algebra invented by George Boole (1815-1864) to describe logic and thought. This algebra symbolises the logic of truth and false statements, and is widely used in digital systems and switching circuits.

5.5.2. Gates and Logic Systems[73,74]

A gate in digital electronics means a circuit with one output and two or more input channels. An output signal occurs for certain combinations of input signals. A table of combina-

nations for several input-output possibilities for a logic circuit is called a truth table. These circuits are also known as logic circuits or Digital circuits as they employ the binary digits 0 and 1. The values assigned for 0 and 1 depend upon the type of logic system. In a positive logic system, the 1 represents the more positive of the two voltage levels whilst in the negative logic system, the 1 stands for the more negative of the two voltages. There is little to choose between these two logic systems and as such for all further reference the positive logic system is employed.

5.5.3. Types of Gates[74]

There are six basic electronic gates. These are (a) OR (b) AND (c) NOT (d) NOR (NOT OR) (e) NAND (NOT AND) and (f) XOR (EXCLUSIVE OR)

The symbolic representation of these gates based on the Military services standard symbology- MIL-STD-806B are given in the table vide Fig.5.1.

5.5.3.(i) OR GATE[73,74]

In the OR gate an output occurs when there is a signal in any one of the input channels. It is therefore known as "any or all gate". A truth table for a two input OR gate is as shown in Fig.5.2.

If the number of inputs are increased to three, then the truth table will have 8 horizontal rows i.e. 2^3. Similarly if the number of inputs are increased to 4, the number of horizontal rows will be 16 or 2^4 in the truth table. In general if there are 'n' inputs, the number of horizontal rows will be 2^n.

5.5.3.(2) AND GATE (73,74)

The AND gate has an output only when all the inputs are present. It is therefore known as " all or nothing gate". A truth table for a two input AND gate is as shown in Fig.5.3.

The 7408 TTL/SSI(78) is an example of QUAD 2-input AND gate.

5.5.3.(3) NOT Gate or Circuit(73,74)

This circuit has only one input and one output. All that the gate does is to invert the signal, if the input is high, the output is low and vice-versa. As such it is also called as a "complementary circuit " or " an Inverter " A truth-table for the NOT circuit is as shown in Fig.5.4.

The 7404 TTL/SSI(78) is an example of a Hexagonal Inverter.

5.5.3.(4) Boolean Algebra differs from ordinary algebra in many ways. In ordinary algebra whenever we solve an equation for its roots we get the solution as a real number which may be +ve, -ve or fractional. In other words the set of numbers that can be obtained is infinite. However in Boolean Algebra when we solve an equation we get either a 0 or a 1. No other answers are possible as the set of numbers include only the binary digits.

5.5.3.(5) The OR Addition(73)

In Boolean Algebra the + sign symbolises the action of the OR gate. In other words the OR gate is an adding device that combines A and B to give a result x (Ref. Fig.5.5).

Thus in Boolean algebra if A + B = x it means that A and B are combined in the same way that an OR gate combines A + B.

Fig. 5.2

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

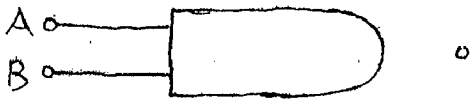


Fig.5.3.

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

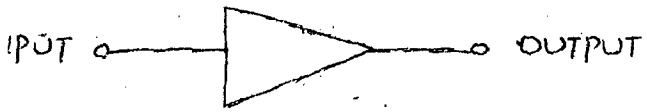


Fig. 5.4.

Input	Output
0	1
1	0

Thus when we write x = A + B it means that x = A or B the logic of the OR gate. The + sign does not stand for algebraic addition but symbolises the action of the OR gate according to its truth table. This is termed as OR gate addition.

Hence 1 + 1 = 2 in ordinary decimal algebra

1 + 1 = 10 in binary addition

1 + 1 = 1 in Boolean Algebra according to OR gate addition.

5.5.3.(6) AND Multiplication(73)

The multiplication sign x or . has a new meaning in Boolean algebra. The AND gate is a device that combines with A and B to give an output x. (Refer Fig.5.6). Thus in Boolean algebra if we write x = A x B or A.B or simply AB it means that A and B are combined in such a manner as an AND gate combines to give an output 'x'. From the truth table of an AND gate it follows that the multiplication sign has the same meaning in both ordinary algebra and in Boolean algebra.

5.5.3.(7) NOT Operation(73)

In Boolean algebra the expression x = $\bar{A}$ means that we are changing A in the same manner as a NOT circuit does(Ref. Fig.5.7). The bar over A implies that we change or complement the quantity to the alternate digit.

5.5.3.(8) NOR Gate

The NOR gate is realised by a NOT gate following on OR gate. Ref Fig 5.8.1

5.5.3.(9) NAND gate[73]

The NAND gate is realised by a NOT gate following an AND gate. Refer Fig 5.8.2

The 7400 TTL/SSI[78] is an example of a QUAD 2 input NAND gate.

5.5.3.(10) De Morgan's Theorems[73]

These theorems are widely used for the inter-changeability of the several gates.

(a) The first theorem states that the complement of a sum equals the product of the complements.

Thus $\overline{A + B} = \overline{A} . \overline{B}$

(b) The second theorem states that the complement of a product equals the sum of the complements.

Thus $\overline{A.B} = \overline{A} + \overline{B}$

The inter-changeability of the several gates which can be realised by the application of the above theorems enables us to realise simplified logic systems using less hardware thereby facilitating cheaper and easy construction. This simplification is possible if one is also aware of the laws of Boolean Algebra.

5.5.3.(11) Laws of Boolean Algebra[73]

I Group : These are similar to laws in ordinary algebra.

(a) Cumulative law wherein the order of adding or multiplying is unimportant as we obtain the same result in any case. Thus $A + B = B + A$; $A.B = B.A$.

(b) Associative law wherein grouping of any two terms of a sum or of a product is possible.

Thus $A + (B + C) = (A + B) + C$, $A(BC) = (AB)C$

(c) Distributive law wherein expressions may be expanded multiplying term by term and also implies that factorisation of expressions is possible.

Thus $A(B + C) = AB + AC$

II Group - These deal with the operations of 0 and are generally thought in terms of OR and AND gates where A and 0 are the inputs.

Thus $A + 0 = A$ in terms of an OR gate

and $A.0 = 0$ in terms of an AND gate

The remaining identities in the group deal with the operations of 1, and are also thought in terms of the OR and AND gates.

Thus $A + 1 = 1$, $A.1 = A$, $A + A = A$,

$A.A = A$

$A + \overline{A} = 1$

$A . \overline{A} = 0$

5.5.3.(12) The Exclusive OR gate (XOR gate) (Ref. Fig.5.9)

The XOR may be realised in several ways by the combination of AND, OR and NAND gates. A truth table for a two input XOR gate is as follows, and an output occurs only when either A or B is equal to 1 but not when they are both equal to 1. This gate is also called the ' Modulo -2 Addition ', the rules of which are similar to the values shown in the truth table shown here below.

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

These rules are the same as for binary addition except that in the last row, the carry is disregarded.

5.6. ARITHMETIC CIRCUITS(73)

5.6.1. The Half Adder

The half adder adds two binary digits at a time, to produce a sum and a carry. The sum is obtained as the output of an XOR gate to which both the inputs are fed. The carry is obtained as the output of an AND gate to which both the inputs are fed. A simple circuit of a half adder is as shown in Fig.5.10

The following is the truth table of a HALF ADDER.

A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

The truth table indicates that the HALF ADDER is capable of doing binary addition, for two binary digits only.

5.6.2. The Full Adder(73)

This is a circuit that can handle three binary digits at a time in binary addition. The Full Adder is obtained by connecting two half addersand an OR gate as shown in Fig.5.11.

A truth table of a full adder is as shown below :

A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

5.6.3. A Parallel Binary Adder(73)

A parallel binary adder adds two binary numbers. The circuit is obtained by connecting full adders and and half adders. A circuit arrangement to add 4 bit binary numbers is shown in Fig.5.12.

5.6.4. A Parallel binary subtractor (73)

A parallel binary subtractor subtracts one binary from another binary number. The circuit is obtained by connecting Full Adders and NAND gates. The NAND gates are used to obtain the 1's complement and the method of subtraction is by adding the 1's complements and the end around carry. Such a scheme is shown in Fig.5.13 for subtracting a 4 bit binary from a similar binary number.

5.6.5. Similarly by combining Half and Full Addors along with logic gates it is possible to develop An 8421 Addor., An Excess 3 bit Adder., Half and Full subtractors. The addor and subtractors give us the basic circuits for a binary system for performing arithmetic operations. Multiplication and division can be performed by repeated Addition and subtraction respectively.

5.7. INTEGRATED CIRCUITS(75)

5.7.1. Typically an integrated circuit or I.C. consists of transistors, resistors, and diodes etched into a semiconductor material. The material is usually silicon and is finally used in the form of a " chip ". Since all of the components are fabricated on the same chip, construction of an IC is called "monolithic ". All of the devices are interconnected to perform a definite function or operation, and is a complete circuit. To make the IC package operable, it must be connected to a power source, an input and an output.

5.7.2. There are three basic IC packages namely the transistor package, the flat-pack (FP) and the dual-in-line package (DIP).

5.7.3. In the transistor package, the chip is mounted inside a transistor case such as a can, and instead of the usual three leads found in a transistor can, there will be 10,12,14 and more leads to accommodate the various power source, input/output connections required in a complete circuit.

5.7.4. In the flat pack, the chip is encapsulated in a rectangular case with terminal leads extending through the sides and ends.

5.7.5. In the dual-in-line package, the chip is encapsulated in a rectangular case similar to the flat pack but, longer than the flat pack. In general the DIP has replaced the FP for most applications.

5.7.6. Difference between discrete and integrated circuits

Although the basic circuits used in IC's are similar to those of discrete transistors, there are certain differences. For example, inductances (coils) are never found as part of an I.C., as it is impossible to form a useful inductance on a material that contains transistors and resistors. Likewise large value capacitors (about 100 pF) are not formed as part of an I.C. Whenever a large value capacitor or an inductance is required, these components are made as part of an external circuit. Transistors are often used in place of resistors in IC packages. Usually such a transistor is a Field Effect Transistor (FET) since the FET acts somewhat like a resistor.

5.7.7. Basic Integrated Circuit Types

There are two types of integrated circuits namely digital and linear.

5.7.8. Digital I.C.'s

Digital I.C.'s are the integrated circuit equivalents of basic logic circuits or transistor circuits combining the functions of logic to form circuits, such as multivibrators, counters, decoders etc. A digital IC is a complete functioning logic network, usually requiring nothing more than an input, output and a power source. Digital circuits are generally associated with only two levels of voltage. Digital circuits are commercially built in three sizes depending upon the complexity

of the circuits and are known as Large Scale I.C.'s (L.S.I.), medium scale I.C.'s (MSI) and small scale I.C.'s (SSI). Most of the basic logic circuits such as AND, NAND, OR etc. gates are available in the SSI range.

5.7.9. Linear Integrated Circuits

Linear I.C.'s are the integrated circuit equivalents of basic transistor circuits such as amplifiers, oscillators, mixers, etc. Although linear I.C.'s are complete functioning circuits, they often require additional external components in addition to a power supply for satisfactory operation. A typical example of such an external component is a resistor to convert a linear amplifier into an operational amplifier. Linear I.C.'s are of two basic types. They can be versatile general purpose devices that may be adapted to provide many different types of circuit functions. Alternatively they may be of the special purpose type for specific circuit functions. A further treatment of a basic linear IC is given in para 5.11.

5.8. CLASSIFICATION OF LOGIC SYSTEMS(74)

5.8.1. Logic systems may be built using a variety of components like diodes, and resistors, or diodes and transistors, or resistors and transistors. It is because of these that logic systems are often classified by the parts used. There are eight families of logic.

(i) Resistor-Transistor logic (RTL)

(ii) Diode-Transistor Logic (DTL)

(iii) Transistor-Transistor Logic (TTL)

(iv) Complementary Transistor Logic (CTL)

(v) Emitter Coupled Logic (ECL)

(vi) Metal Oxide Semi-conductor (MOS)

(vii) Complementary metal-Oxide Semi-conductor (CMOS) , and

(viii) Integrated Injection logic (I²L)

They all have different characteristics. Amongst the eight types, TTL, ECL, MOS, and CMOS are popularly used, in S.S.I. and M.S.I.

5.8.2. Characteristics and comparison of the major IC logic families[74]

It is always appropriate to look at the general characteristics of the IC logic gates before describing the different types, so that the differences between the several types can be better appreciated. These general characteristics are as follows:

1) Threshold voltage

The voltage level at the input of a circuit at which the circuit changes from one state to another is called the threshold voltage. One approximation of this is the voltage at the mid-point of the transition between the two states.

ii) Operating speed

The time delay between the application of a level change at the input and the change of state at the output of a circuit is called the propagation delay of the circuit. Generally the propagation of an IC gate is in the range of 2 to 50 ns (a ns-nanosecond = 10^{-9} of a sec.). The total propagation delay time of a logic system will be the delay per gate multiplied by the number of gates in series.

iii) Power dissipation

The power dissipation of a logic circuit is usually defined as the supply power required for the gate to operate with a 50 percent duty cycle at a specific frequency (i.e. equal times in the 0 and 1 states). The power dissipation of a typical logic IC ranges from a few microwatts to about 50 milliwatts per gate depending upon the type of circuit.

iv) Noise Margin

The difference between the operating input-logic voltage level and the threshold voltage is called the Noise Margin of the circuit. It is therefore the maximum amount of deviation from the nominal values of V(0) and V(1) that the circuit can tolerate without changing state. The circuit for stable operation should have equal logical 0 and logical 1 noise margins.

v) Logic voltage levels

The values for the voltage levels corresponding to logic 1 and logic 0 affect several other specifications for a system such as power dissipation, speed and noise immunity. The problem of voltage levels must be such that interfacing with other systems is possible and this is made simpler by choosing a family of gates that have the same logic voltage levels as the system to which they must interface.

vi) Fan-in and Fan-out

The fan-in of a logic system is the number of inputs it is designed to have. It is a measurement of how much that input will load a driving source. The fan-out of a logic gate is the number of IC gates that can be reliably driven by the gate.

vii) Operating Temperature

All IC gates are semi-conductor devices that are temperature sensitive. They must be designed to give a satisfactory performance over a wide range of temperature.

The general characteristics of the eight IC logic families are tabulated as shown. Values quoted are representative on a comparison basis.

Logic family	Propagation time per gate(Ns)	Power dissipation per gate(mW)	Typical noise margin (V)	Typical fan-in	Typical fan-out	Relative cost per gate
RTL	50	10	0.2	3	4	Medium
DTL	25	15	0.7	8	8	Medium
TTL	10	20	0.4	8	12	Low
CTL	5	50	0.4	5	25	High
ECL	2	50	0.4	5	25	High
MOS	250	1	2.5	10	5	Very low
CMOS	30	0.05 Micro W	Depends on V_{DD} Typical 45% of V_{DD}	10	100	Low
IIL	40	1	0.35	1	8	Very low

5.8.3. The Direct Coupled Transistor Logic(DCTL) was the earliest to be developed[73]. These consisted of circuits in which the input signals were directly coupled into bases and outputs signals taken from the emitters or collectors of transistors. These however suffered from current hogging. Further there was no guarantee that the i-v characteristics of the bases of the transistors would be identical, thereby there

was a possibility of some of the bases turning on before the others. This serious impediment prevented it's further exploitation and as such has not been classified in the above logic family. The RTL logic is an improvement over the DCTL wherein current hogging is prevented by including resistors in the bases of the transistors. The resistors however degrade the switching time and to improve the switching time capacitors are connected across the resistors. These capacitors are called as speed up capacitors and these circuits are sometimes called as Resistance capacitance Transistor logic (RCTL) which are only a mild variation of RTL. The RTL logic has no doubt offered high performance, but suffers from insufficient noise margins, and low fan-in and fan-out capabilities. DTL logic on the other hand is slower, but easier to use and has comparatively large fan-in and fan-out capabilities. They have been gradually superseded by TTL which offers higher speed, better noise immunity and driving capability. Hence, by for the largest number of SSI gates are manufactured with the TTL logic. CTL logic offers high speed at moderate cost and power dissipation. ECL logic however, offers the highest spee and is the ultimate in choice for very fast systems. MOS logic offers greatly increased complexity and low poer consumption but significantly less speed. CMOS offers extremely low power consumption when operated at low speed and it's speed is between TTL and MOS. Finally, IIL logic which is a very recent development and has a packing density greater than MOS and simpler processing than all other technologies.

5.8.4.As mentioned above, because of it's high speed, low power dissipation, sufficient noise margins, high fan-in and fan-out and

low cost, TTL logic offers by for the largest number of standard SSL gates. The most commonly used[74] TTL/SSI integrated circuit series is the SN 54/SN 74 series where SN stands for semi conductor network. The 54 series are guaranteed in the temperature range over -55 to 125°C and were generally made for the military market where size, power consumption and reliability requirements were of paramount importance. The 74 series are guaranteed for a temperatu range over 0°C tp 70°C and are primarily meant for commercial use. Thus the SN 54/74 series provide a complete range of ready made gates namely NAND, NOT, AND, NOR, OR, XOR, in addition to binary adders and other arithmetic circuits.

5.9 MULTIBRATORS AND FLIP FLOPS:[73]

5.9.1. A multivibrator is a regenerative circuit with two active devices designed so that one device conducts while the other cuts off. Multivibrators can store binary numbers, count electrical pulses, control digital circuits, synchronise arithmetic operations, produce rectangular pulses and do many other things that are vital to modern digital systems.

5.9.2 There are basically three types of multivibrations:

i) Bistable - which has two stable states, and a circuit can stay in either state indefinitely

ii) Astable - without any stable state and it means that a circuit oscillates back and forth between the two unstable states.

iii) Monostable - with only one stable state and the output of a circuit can remain indefinitely in it's only stable state.

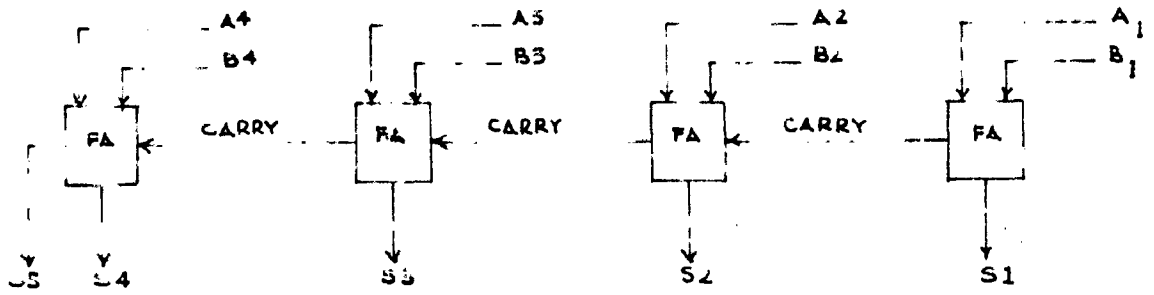


FIG.-5·12- PARALLEL BINARY ADDER.

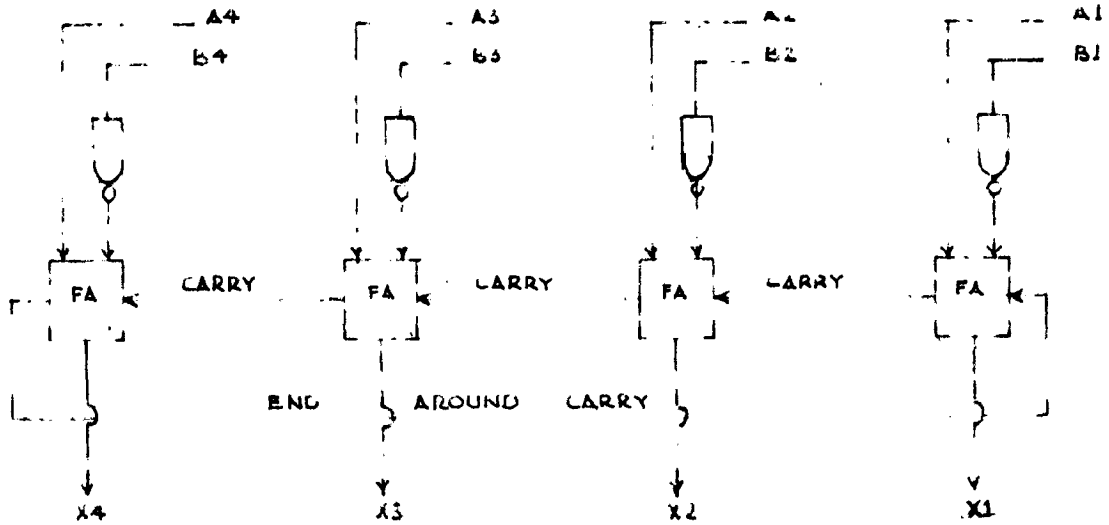


FIG.-5·13- PARALLEL BINARY SUBTRACTOR

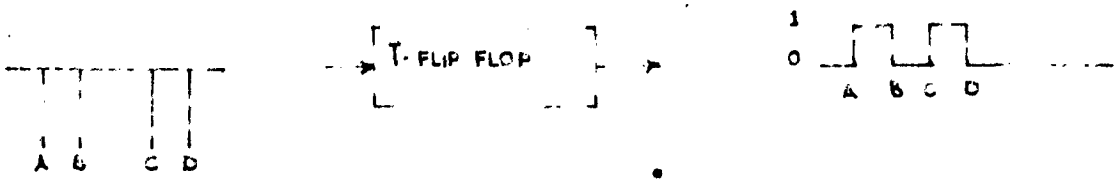


FIG.-5·14 (a) - T-FLIP FLOP

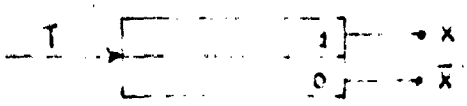


FIG.-5·14(b)- BLOCK DIAGRAM OF T-FLIP FLOP

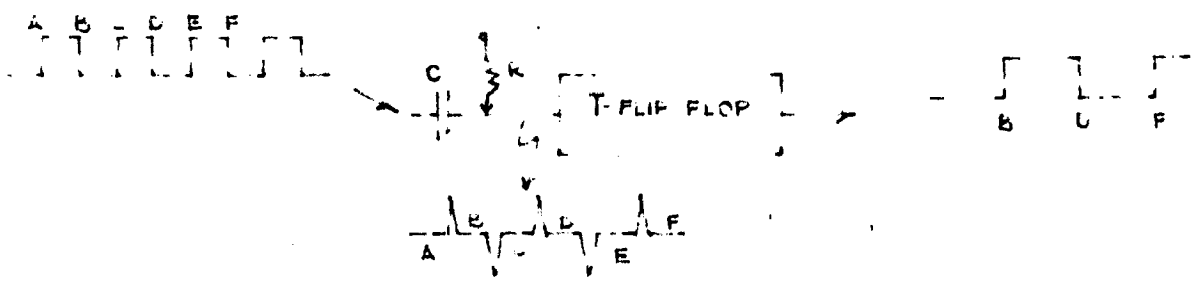


FIG.-5·14 (c)- DIFFERENTIATING CIRCUIT.

5.9.3. Flip - Flops

A flip-flop is a bistable multivibrator whose output can be either a high or a low voltage that is either a 1 or a 0,state. The output stays low or high until the circuit is driven by an input.

The driving input to a flip-flop is called a trigger. The trigger is a ∠ sharp pulse of short duration which when driving the flip-flop causes it to change it'sstate. When a trigger pulse arrives, the circuit flips to one state and upon the arrival of a second pulse it flops back to it's original state. Very often in digital circuits, a flip-flop has to be driven by a square wave input. These square waves are changed into triggers by using a resistance-capacitance combination of a differentiating circuit. Flip-flops are also sometimes called as latches:

5.9.4.Types of Flip-Flops(73)

The types in common use are the T flip flop, the RS and RST flip-flops, the JK flipflip, etc. The JK, RS and RST flip-flops are mostly manufactured in TTL/MSI Integrated circuits(75).

5.9.4.(1) The T Flip-flip :

In the diagram of Fig. 5.14(a) when negative triggers arrive at points A,B,C,D the T flip-flop changes to the opposite state. Thus at point A in time the output changes from a 0 to 1 and remains so until the next trigger arrives at B when it changes state from 1 to 0, and so on. The T flip-flop has one input and two outputs. It is symbolically represented by the block diagram shown in Fig. 5.14(b). The 'x' output is sometimes called the '1' output and '$\bar{x}$' the 'o' output. Since a T flipflop responds only to the negative trigger it divides the frequency by 2 if a

into sharp triggers by the use of a differentiating circuit as shown in Fig.5.14(c). Thus a scaler to divide successively the input frequencies by 2 can be developed by cascading several flip flops in series.

5.9.4.(ii) The RS and RST Flip-flops(73)

The RS is a reset-set flip-flop and has two inputs and two outputs. This flipflip is obtained by modifying a T flip-flop in regard to it's triggering. The set and reset inputs are made to respond to ensure that if the 'x' output is 1 due to a positive trigger on the set input, then a positive trigger on the reset input ensures that the 'x' out put will be a zero. ... The RS flip-flop is symbolically represented by the following block diagram of Fig. 5.15. The RS flip-flop is also known as a S-R latch.

A RST flip-flop combines an RS flip-flop and a T flip-flop The RST flip-flop can set, reset and can trigger. The trigger input responds to negative-going voltages whilst the set and reset inputs respond to positive going voltages. When negative pulses are applied to the trigger inputs, the flip-flop toggles back and forth between it's two stable states. When a positive pulse arrives at the set input, the 'x' output becomes a 1 if it is not already a 1; when a positive pulse hits the reset input, the 'x' output becomes a 0 if it is not already a 0. The RST flip-flop can be built in many ways. All three inputs can be made to respon to positive triggers or perhaps to negative triggers or to a combination of positive and negative triggers. The RST flip-flop is symbolically represented by the following block diagram of Fig. 5.15(b).

5.9.4.(iii) The JK Flip-flop[73]

The JK flip flop has three inputs and two outputs. The middle input is called the trigger or clock input and the other inputs are the J and K inputs. The flip flop a symbolically represented by the following block diagram of Fig.5.16. The flip-flop response is determined by the values of J and K at the instant that the trigger or clock pulse arrives. There are four cases to described.

(a) When J = 1, K = 1, the flip flop toggles each time a trigger on clock pulse arrives and thus acts like a T flip-flop.

(b) When J = 1, K = 0, the flip-flop will set on the next clock pulse. On succeeding triggers the flip-flop stays set and thus acts like setting a RS flipflop.

(c) When J = 0, K = 1, the flip-flop will reset on the next trigger and they stay reset on succeeding clock pulses and thus acts like resetting a RS flip-flop.

(d) When J = 0, K = 0, the flipflop remains in whatever state it is in

The above actions of the J-K flip-flop are summarised below in a truth table. Here 'b' is the value of the output just before the trigger or clock pulse arrives.

J	K	Output after trigger
0	0	b (same)
0	1	0 (reset)
1	0	1 (set)
1	1	T (toggle)

5.9.4.(iv) Master-Slave flip flops[74]

The circuit of the master slave flipflop is basically two latches connected serially. The first latch is called the Master and the second is termed the Slave.

5.9.4.(v) Edge Triggered flip flops[74]

The d.c. or edge triggered clock is one that causes flip flip operation at a particular voltage when either a positive (positive edge trigger) or a negative (negative edge trigger) transition occurs. Either one or the other is recognised, but not both, for any chosen device. This type of clock enables the data inputs and transfers the data to the output simultaneously, resulting in a high speed clocking technique that is relatively independent of the clock rise and fall times.

5.9.5. The SchmittTrigger[73]

The Schmit trigger is a bistable multivibrator. The circuit is an amplitude sensitve circuit. The output voltage which jumps from a low value to a high value is called the upper trip point (UTP) and the corresponding voltage which jumps from a high value to a low value is called the lower trip point (LTP). Once the input voltage exceeds the UTP, the output voltage goes from a low value to a high value i.e. from a 0 to a 1. When the input voltage drops below the LTP, the output voltage drops from a 1 to a 0. It is because of this that a Schmitt circuit can be used to detect when the input voltage crosses certain voltage levels. It is also to be noted that when a Schmitt trigger circuit is driven by a periodic signal whose peak value exceeds the UTP, the output will be a rectangular waveform. As such the Schmitt trigger is sometimes known as a "Squaring Circuit" and the output frequency is equal to the input frequency.

5.9.6. The Astable Multivibrator (73)

The Astable vibrator has two states, but is stable in neither. It oscillates back and forth between these two states, producing a square wave output. Hence the astable multivibrator is a square-wave oscillator.

Often in digital systems a single astable multivibrator keeps all the different circuit operations in step with one another. This multivibrator is then like a master clock that synchronises all parts of the digital system. This property has enabled an astable multivibrator to be known as a "clock".

5.9.7. The Monostable Multivibrator (73)

This multi-vibrator is stable in only one state but is unstable in the other. When it is triggered it goes from the stable state into the unstable state. It remains in the unstable state temporarily and then returns to the stable state.

The diagrams of Fig.5.16 show the general idea of monostable multivibrator. At point A in time a trigger hits the input. This causes the output voltage to go from a low to a high value. The high state is an unstable state, so that after a while the output voltage returns to the low state. The output remains in the low state until the next trigger arrives at point B in time. Again the output jumps to the high state and after a while return to the low state, where it stays until the trigger comes in at point C in time. Thus for each input trigger there is one rectangular output pulse. It is because of this property that a monostable multivibrator is often called as a "one-shot" multivibrator. A square wave can drive a one-shot multi-vibrator provided we differentiate the square wave input. The one-shot multivibrator is useful for reshaping ragged pulses, for introducing

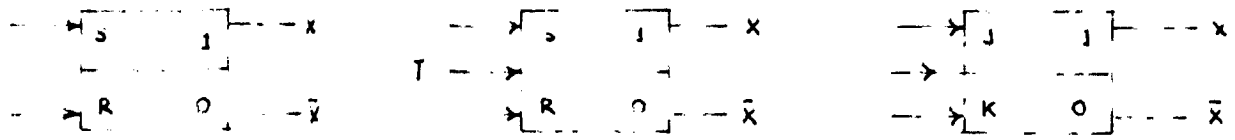


FIG.-5·15(a)- RS. FLIP FLOP. FIG.-5·15(b)- RST-FLIP FLOP FIG-5·15(c)- JK-FLIP-FLOP

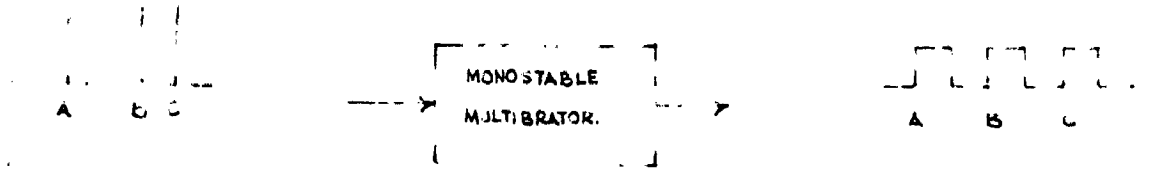


FIG. 5·16- MONOSTABLE MULTIVIBRATOR

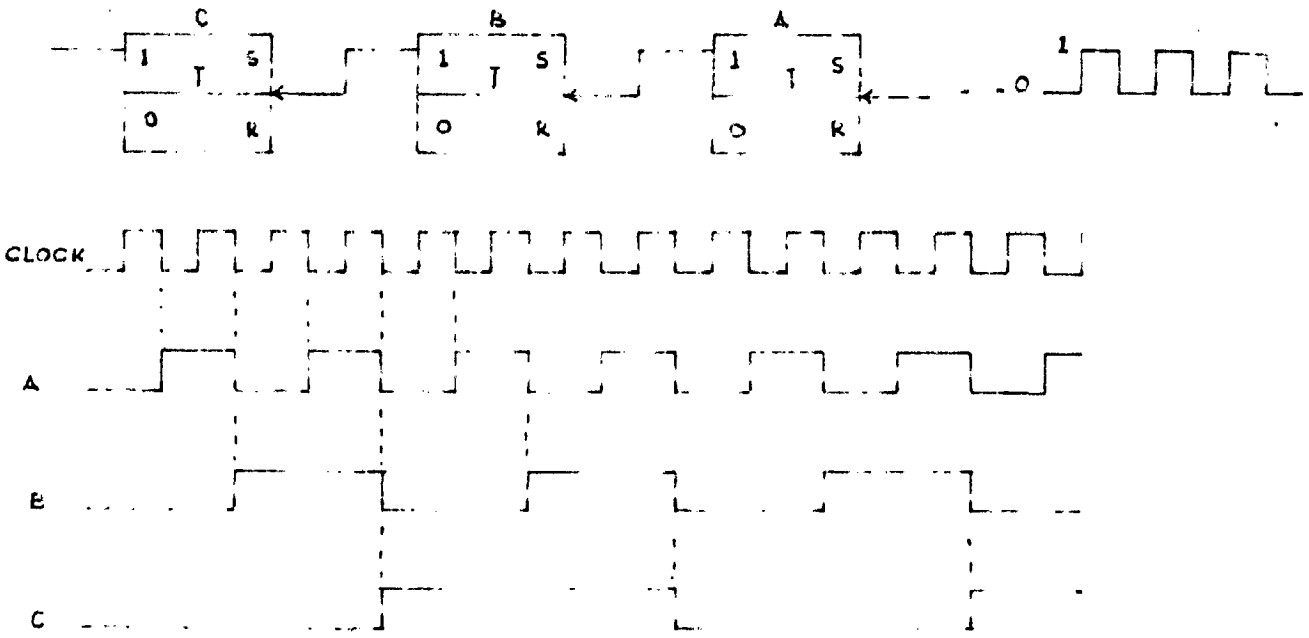


FIG.-5·17- USING FLOPS TO COUNT

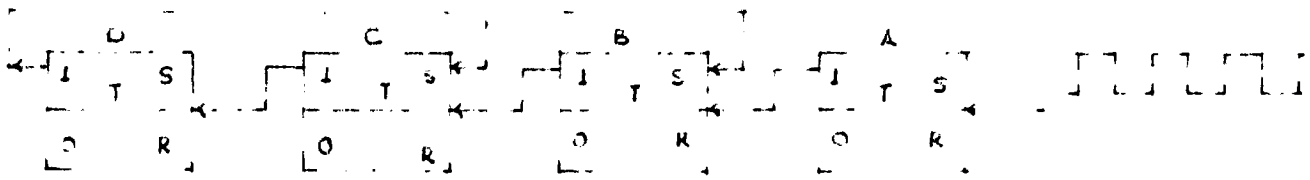


FIG.- 5·18- DECADE COUNTER

5.10. BASIC ELECTRONIC COUNTERS

5.10.1. Using Flip-Flops to Count[73]

Flip-flops connected in cascade serve as an electronic counter. (Refer Fig. 5.17). A, B and C are three flip-flops connected in cascade as shown. A square wave also called the "clock" signal drives the A flip-flop. The output of the A flip-flop drives the B flip-flop and it in turn drives the C flip-flop. Let all flip-flops be initially in the 0 state. When a clock pulse comes in, the A flip-flop changes on the negative going part of the pulse and it therefore changes it's state each time the clock changes from a 1 to 0. The B flip-flop toggles on negative going changes. It therefore changes its state each time that A goes from a 1 to a 0 as shown in Fig. 5.17 Similarly the C flip-flop toggles each time B goes from a 1 to 0. Thus a succeeding flip-flop toggles only if the flip-flop to the right has changed from a 1 to 0.

Thus initially if CBA = 000

Then at the end of the 1st pulse CBA = 001, (A changes from 0 to 1)

at the end of 2nd pulse CBA = 010, (A changes from 1 to 0, B changes from 0 to 1)

at the end of 3rd pulse , A changes from 0 to 1

$\therefore$ CBA = 011 and so on

The above operations can be summarized in a truth table which incidentally gives the count.

C	B	A	CBA Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	8

The value of CBA shown as count in the truth table indicates the system of a binary counter, from 0 to 7 and on receipt of the eighth pulse CBA returns to 000 because all flip-flops reset to 0.

5.10.2. Binary Counters[73,74]

It is shown in para 5.10.1 that by connecting flip-flops in cascade we obtain a binary counter. The capacity of a binary counter canbe increased, by including more flip-flops. Thus if four flip-flops are used, we have a binary counter that can count from 0000 through 1111 before it resets, that is there are 16 distinct states. In general if we cascade 'n' flip-flops together we get 2^n states.

5.10.3. Ripple Counter[73,74]

It was described in para 5.10.1 that the output of one flip-flop drives the output of the next flip-flop. Such a counter is called a " ripple counter ", wherein the flip-flop to the

right of the one in question must change its state before the flip-flop that is considered can change its state. The triggers move though the flip-flops or the counter like a ripple in water. Hence the name ' ripple counter '. A ripple counter can be constructed with RST or JK flipflops.

5.10.4. A DeCade Counter (73)

The familiarity of decimal numbers has resulted in the development of a decade counter. A decade counter has 10 distinct states corresponding to the 10 numbers of a decimal count. If 4 flip-flops are used, then 16 distinct states are obtained. In order to obtain the 10 distinct states required for a decade counter some of the states have to be skipped through. This is achieved by providing a feed back from the D flip-flop to the B and C flip flops as shown in Fig.5.18. Starting with DCBA=0000, the counter advances to the next binary number when each clock pulse comes in. The feed back does nothing for the first seven counts, that is DCBA changes during the first seven clock pulses as follows upto the natural binary count seven.

0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111. Upon receipt of the eighth pulse, DCBA changes from 0111 to 1000. This 1000 state is only temporary because the D output has changed from a 0 to 1, a positive change. This positive change goes back to the set inputs of B and C flip flops, thereby forcing these flipflops to change state from a 0 to 1. Thus the value of DCBA now becomes 1110. The counter has now skipped through some of it's natural states. Thus the count 1110 stands for eight. Upon receipt of the next clock pulse, DCBA becomes 1111 which stands for count 9 and on the next or tenth clock pulse DCBA resets to 0000.

5.10.5. 8421 BCD Decade Counter[73,74]

The 8421 BCD code has a natural binary progression upto nine and then the count resets. This sequence can be obtained as shown in Fig.5.19. The system acts as a straight binary sequence upto the decimal number 9. At this point DCBA = 1001. When the tenth clock pulse comes in, DCBA becomes 1010. But this condition is only temporary as the positive change of B flipflop is fed to the reset input of D flipflop causing D to change from a 1 to 0, that is DCBA is now is 0010. The $\bar{D}$ output which has changed from a 0 to 1 goes back to the B flip flop causing B to change from a 1 to 0. Therefore DCBA now becomes 0000.

The 7490 TTL/SSI[78] is an example of decade counter consisting of four dual rank master slave flipflops which are connected internally.

5.10.6. Decoding a Counter[73,74]

A very simple method of decoding a counter is by connecting lamps to the output of each flip-flop. If the output of a flip-flop is 1, the lamp will glow and if it's output is 0 it will not glow. But this has the disadvantage that the decimal number has to be decoded mentally which is not desirable.

It is however possible to convert the BCD number stored in the counter into its decimal equivalent using logic circuits so that on display we read decimal numbers. A simple method of decoding a counter isby the use of ten AND gates and each AND gate is made use of to drive a numbered lamp. Each AND gate has for inputs connected from the flip flops. For instance

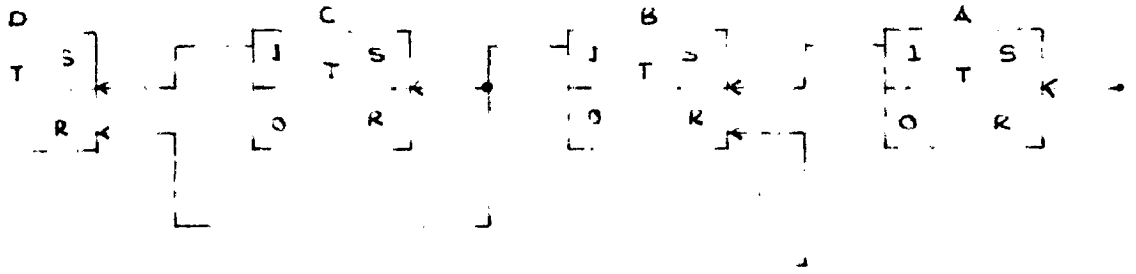
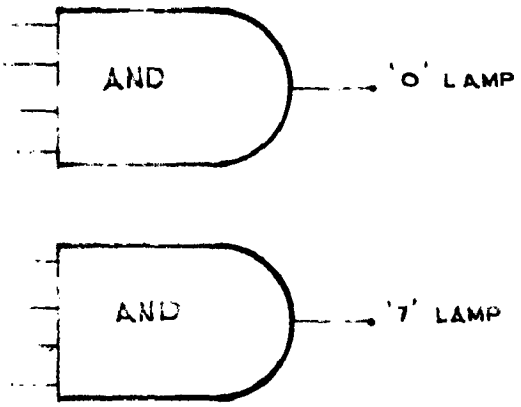
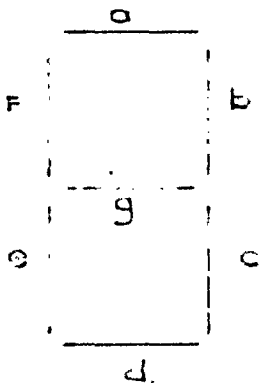


FIG.-5·19- A-8421- BCD-DECADE COUNTER





·20-(a) · DECADING COUNTERS

FIG·5·20-b- LED DISPLAY FIG. OF. 8.

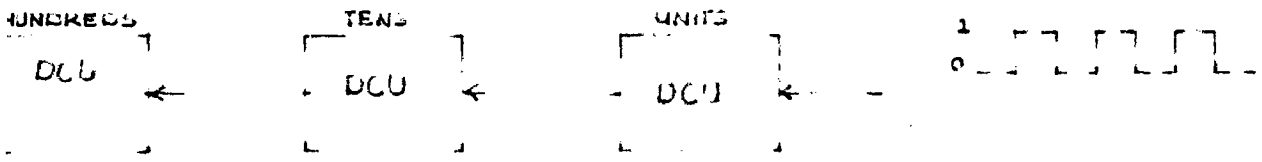


FIG.-5·21- CASCADING DECADE COUNTER UNITS

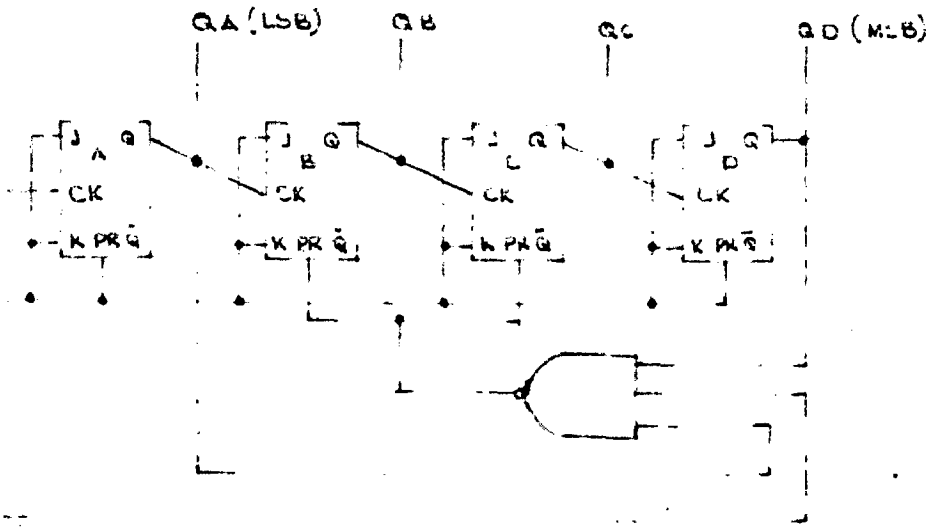


FIG. 5·22- DECADE RIPPLE COUNTER

(Fig.5.20 a), the AND gate for lamp 0, has its four inputs connected to $\overline{A},\overline{B},\overline{C},\overline{D}$, so that when the output DCBA is 0000, the lamp glows because all inputs to the AND gate are $\overline{DCBA}$ = 1111 which enables it to drive the lamp. Similarly for lamp 7, the output of the flipflops is 0111, so that the input to it's AND gate will be $\overline{D}CBA$ = 1111 to enable AND & thus drive the lamp.

Earlier instead of using 10 separate lamps, a single lamp known as a ' nixie tube ' was used. It contains the numbers 0 through 9, stacked on top of each other. There are 10 input leads to the nixie tube, and when a voltage is applied to one of these inputs, the decimal number associated with that number is lit.

Nixie tubes have gradually been replaced by LED's (Light emitting diodes). The LED's are arranged to form a figure of eight as shown in Fig.5.20b. It has seven inputs corresponding to the seven LED's a,b,c,d,e,f,g which are commonly referred to as the seven segments. Thus for instance if the binary count stored is 0, the segments a,b,c,d,e, and f are enabled to be lit by a combination of logic circuits to obtain the figure of 0. Similarly for a count of 7, segments a,b and c are lit to give the figure of 7.

The 7448 TTL/MSI[76] is a BCD to 7 segment decoder. It consists of NAND gates and seven AND-OR-INVERT gates connected internally.

5.10.1. Cascading Decade Counter Units

Decade counters are cascaded to increase the capacity of a counter. For instance, if we want to count from 0 through 999 we need only cascade three decade counter units (DCU's) as shown in Fig.5.21.

If at the beginning of the count, all DCU's are reset to 0, then when nine clock pulses have arrived, the DCU's will read 009. On the arrival of the tenth clock pulse, the D flipflop in the 'Units' DCU will change from a 1 to 0. This negative change goes into the ' tens' DCU, causing it to advance by one count. Thus after 10 clock pulses the DCU's read 010. As additional clock pulses arrive, the units DCU advances one count for each clock pulse. Every time the units DCU resets to 0, it produces a negative change that advances the tens DCU. After 99 clock pulses have arrived, the DCU's read 099. Upon receipt of the 100th clock pulse, the tens DCU resets to 0. This produces a negative change that triggers the hundredth DCU advancing it by one count, Hence after 100 clock pulses have arrived the DCU's read 100. In this way the system can handle upto 999 clock pulses.

5.10.8. Divide by 'N' Counters[74]

It has been described in paras 5.10.2 and 5.10.3, that the total number of counts or discrete states through which the counter can progress is given by 2^n where 'n' is the total number of flip-flops used. Thus a binary ripple counter with 4 flip-flops is capable of counting through 16 discrete states. Such a counter is often referred to as ' Modulus - 16 ' counter or just Mod-16 counter. The modulusof a counter defines the total number of states through which thecountor can progress.

It is often desirable to have counters which have modulii other than 2,4,8,16 ..... A smaller modulus counter can always be constructed from a larger modulus counter by skipping states. This has resulted in the Divide-by- N counters.

A general procedure for designing a divide-by-N ripple counter using JK flip-flops with preset is as follows.

i) Determine the number 'n' of flipflops by the equation $n = \lceil \log_2 N \rceil$ where the symbol $\lceil \log_2 N \rceil$ denotes the smallest integer that is equal to or greater than $\lceil \log_2 N \rceil$

ii) Connect the 'n' flip-flops as a ripple counter.

iii) Determine the binary representation of(N-1)

iv) Connect all flip-flop outputs that are 1, at the counter N-1 as inputs to a NAND gate. The clock pulse is also to be fed to the NAND gate.

v) Connect the NAND gate output to the preset inputs of all the flip-flops for which Q = 0 at the count N-1.

The counter resets in the following manner. At the positive going edge of the N^{th} clock pulse all flip-flops are present to the 1 states. On the trailing edge of the same clock pulse all flip-flops count to the 0 state.

An example of a Decade (Divide by 10 or Modulo-10) ripple counter is as follows.

For $N = 10$, $n = \lceil \log_2 10 \rceil = \lceil 3.332 \rceil = 4$.

Thus we use four J-K negative edge triggered flip flops and connect them as a ripple counter. Since $N = 9_{10} = 1001_2$, outputs Q_B and Q_C are connected to the NAND gate whose output is fed to the preset's of the flip-flops. This decade counter is shown in Fig.5.22.

5.10.9. Parallel or Synchronous Counters[73,74]

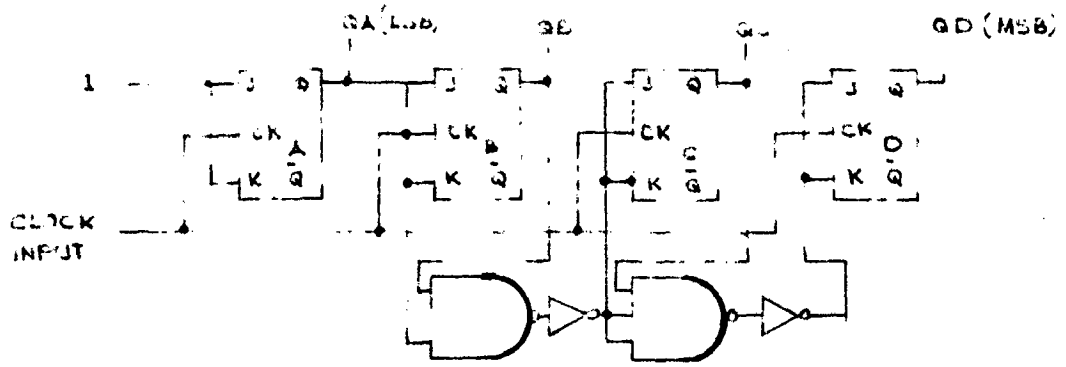
The ripple counter though simple to build, has certain limitations on it's highest operating frequency. Each flip-flop has a certain delay time. In a ripple counter these delay times are additive and the total setting time for the counter is approximately the delay time the total number of flip-flops. This speed limitation can be overcome by a synchronous or parallel counter. Every flip-flop in such a counter istriggered by the clock and thus they all make their transitions simultaneously.

There are basically two methods of flip-flop control in synchronous counters one with ripple carry and the other with parallel carry or carry look-ahead. The latter is the faster of the two methods. But as the number of stages in a synchronous counter with parallel carry increases, the flip-flops must drive an ever increasing number of NAND gates and the number of inputs per control gate also increase.

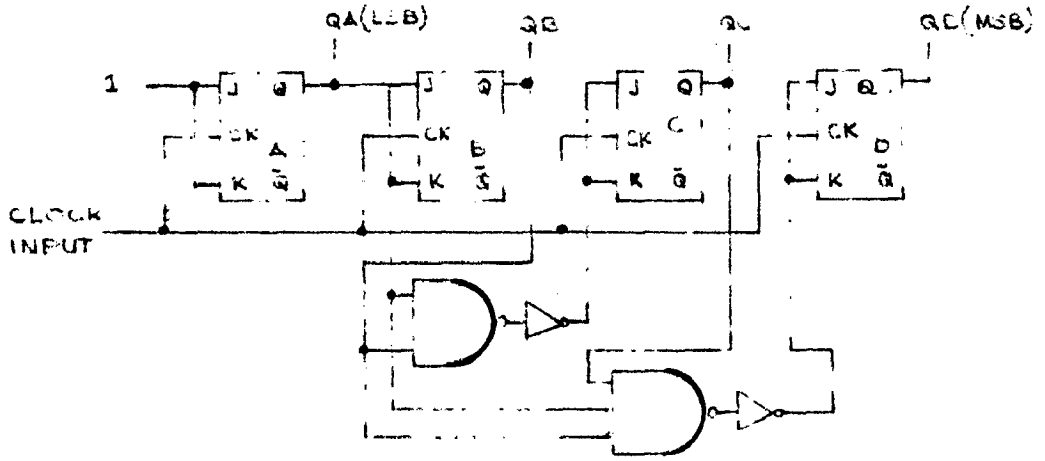
Two 4-bit synchronous counters using J-K positive edge triggered flip-flops are shown in Fig.5.23(a) and (b) for these counters with ripple carry and for parallel carry.

The output of the flip-flops A and B when it is high causes the output of the NAND gates to go low. This output is inverted and fed to the inputs of the succeeding flip-flop C, and in cascade with another NAND and NOT gate to flip-flop D in the ripple counter while in the parallel counter the input to D is in parallel with the output of A, B and C flipflops.

Synchronous counters can also be modified as described in para 5.10.8 to form counters of different modulii.

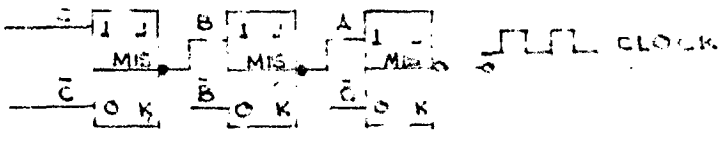


(a) - 4-bit synchronous counters with ripple carry

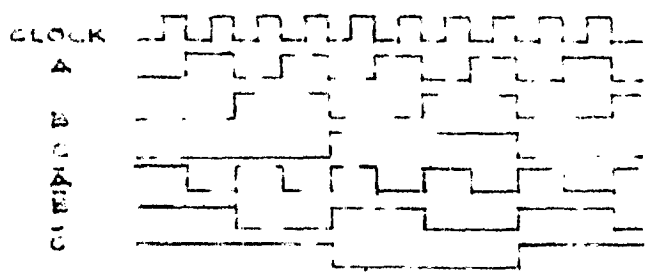


(b) - 4-bit synchronous counters with parallel carry

FIG. 5·23 - 4-BIT SYNCHRONOUS COUNTERS



(a) - Logic diagram



(b) - Waveforms

COUNT	C	B	A	C	B	A	COUNT
7	1	1	1	0	0	0	0
6	1	1	0	0	0	1	1
5	1	0	1	0	1	0	2
4	1	0	0	0	1	1	3
3	0	1	1	1	0	0	4
2	0	1	0	1	0	1	5
1	0	0	1	1	1	0	6
0	0	0	0	1	1	1	7

(c) - Truth Table

FIG. 5·24 - A THREE FLIP FLOP RIPPLE COUNTER

5.10.10. Up/Down Counters

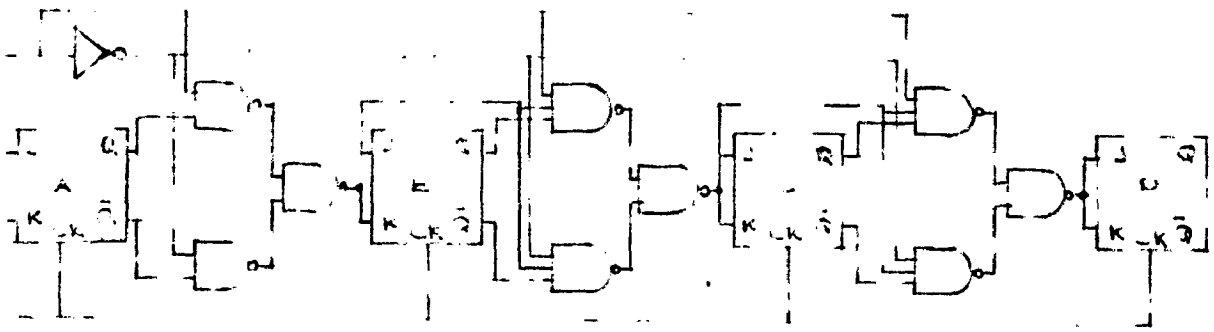
The counters discussed so far are unidirectional counting up. Some applications require counters which can count in a downward sequence. Any of the binary counters discussed so far can be used to implement a down counter.

A three-flip-flop ripple counter along with the waveforms and a truth table is shown in Fig.5.24. The wave forms also show the outputs of the '0' sides of the flip-flop. Likewise in the truth-table the normal count sequence from 0 through 7 is shown under ' COUNT ' corresponding to the state of the output 1 side of the flip flops A, B and C. The '0' sides of the flip-flops are simply the negative of the 1 sides and these are shown under $\overline{A}$, $\overline{B}$ and $\overline{C}$ and their binary states are shown under ' $\overline{\text{Count}}$.'

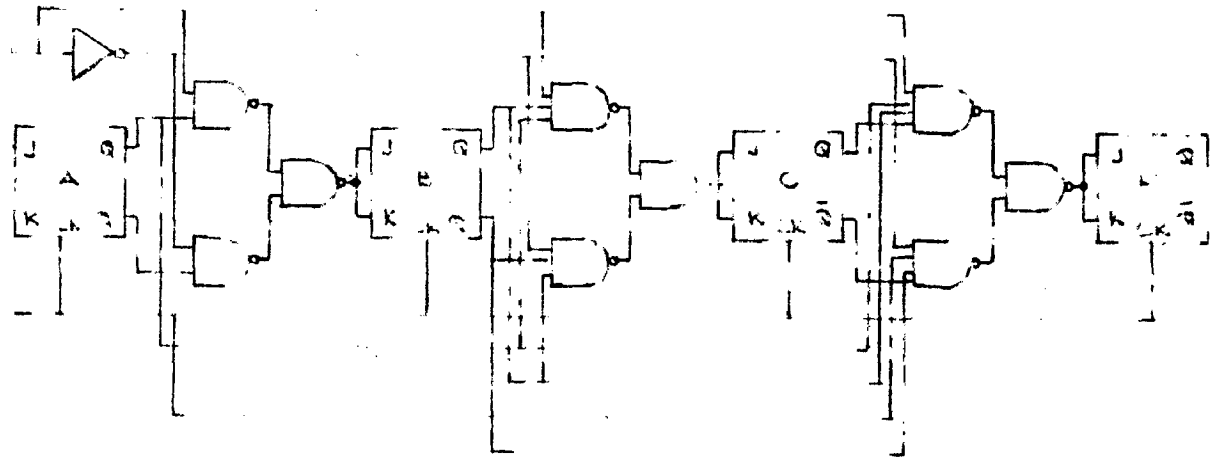
It is seen from the truth table that the count sequence under $\overline{\text{count}}$ progress in a downward fashion (7-6-5-4-3-2-1-0). Thus this counter could be decoded to provide a count-down sequence of waveforms. A parallel or synchronous Up/Down counter may also be formed as described in para 5.10. Fig.5.25(a) and (b) shows the J-K flip-flop realisations of four-stage up/down decade counter 8421 one with parallel carry and the other with ripple carry.

5.11. OPERATIONAL AMPLIFIERS (op-Amps)

The most common form of linear IC is the operational amplifier. These amplifiers are high gain, direct coupled circuits where the gain and frequency response are controlled by external feed back networks. The most common type of linear IC op-amp uses a balanced differential circuit. IC op-amps generally use several different stages in cascade to provide common mode rejection and



(a)



(b)

Fig. 5.25 - TWO MSI/TTL UP/DOWN COUNTERS.

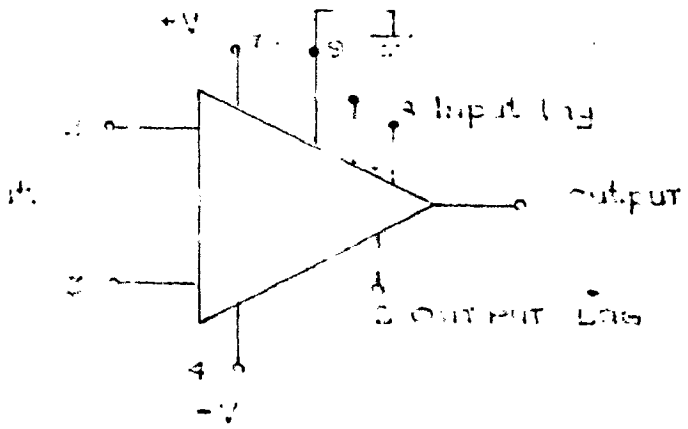


Fig. 5.26 - OPERATIONAL AMPLIFIER BLOCK DIAGRAM.

high gain. Thus they generally require both positive and negative power supplies. The power supplies are usually equal or symmetrical such as +9 V and - 9V or +15 V and -15 V. The figure of 5.26 represents the block diagram of a typical op-amp.(75)

5.12 DESIGN OF THE PROPOSED RELAY AND FAULT LOCATOR

5.12.1 The design problem consists of the following two sub-problems.

(i) the fault detection problem

and (ii) the fault location problem.

The first sub-problem is the determination of whether or not any of a prescribed list of faults which may include all possible single faults and multiple faults has occurred. This is achieved by the development of a distance relay using analog and digital circuits. The distance relay proposed is a mho relay as several relay manufacturers employ the mho relay as the fault detecting unit or the third zone starting relay.

The second subproblem is the determination of the location of the distance to the fault so that the distance to the fault is read directly from a digital display. The fault locator is also proposed for being developed using analog and digital circuits.

5.12.2 Principle of Operation of the Relay

5.12.2(i) The principle of operation is easily explained with reference to the schematic block diagram of fig. 5.27. This block diagram encloses within dotted lines two blocks

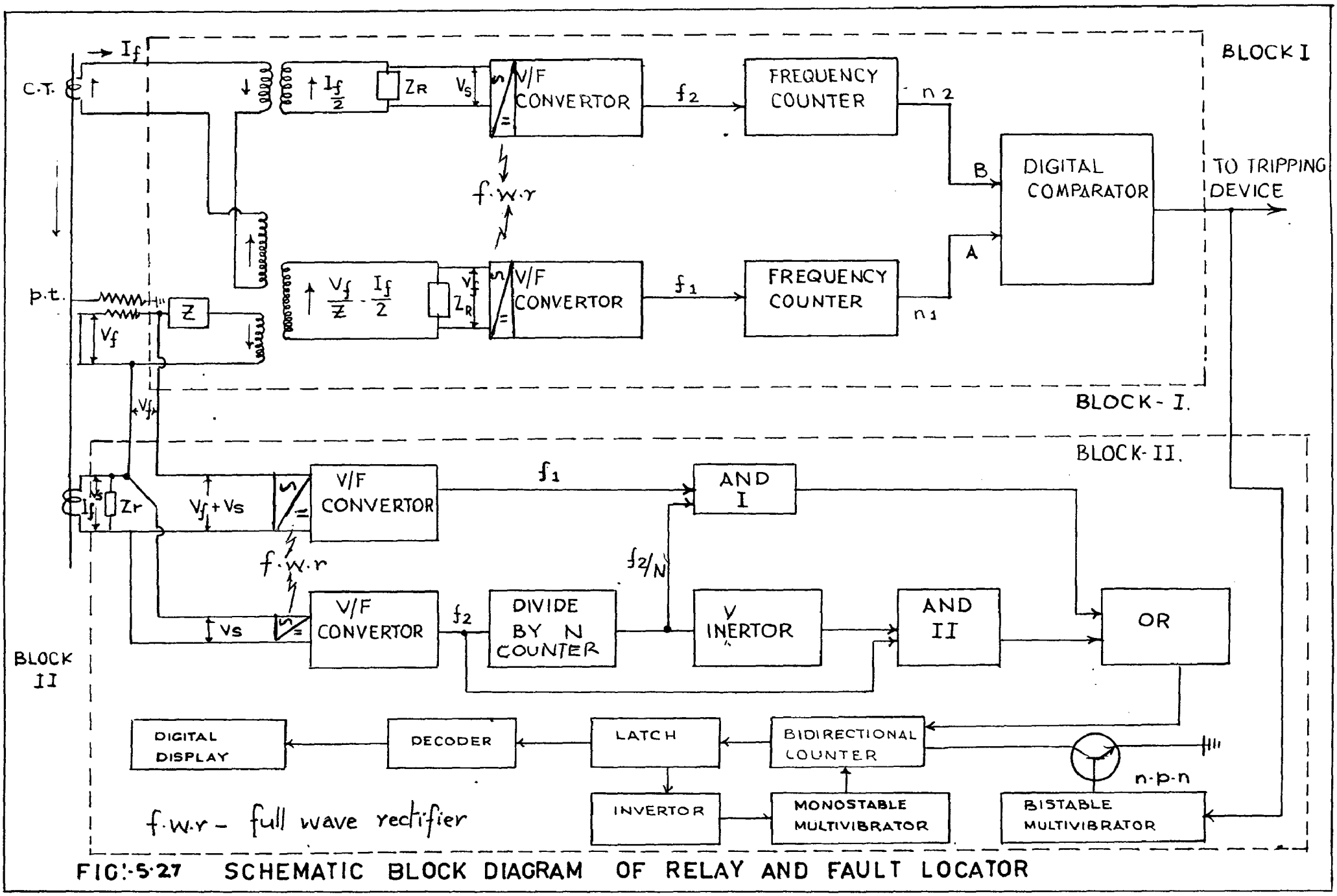


FIG:-5·27 SCHEMATIC BLOCK DIAGRAM OF RELAY AND FAULT LOCATOR

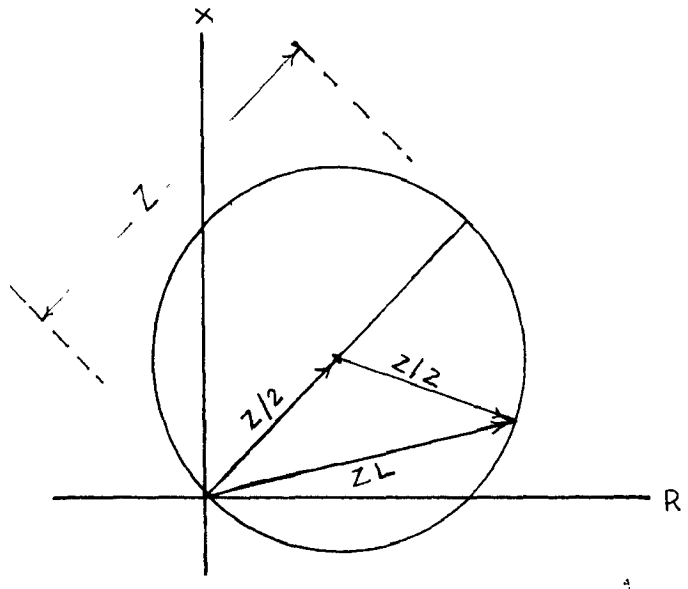


FIG:- 5·28

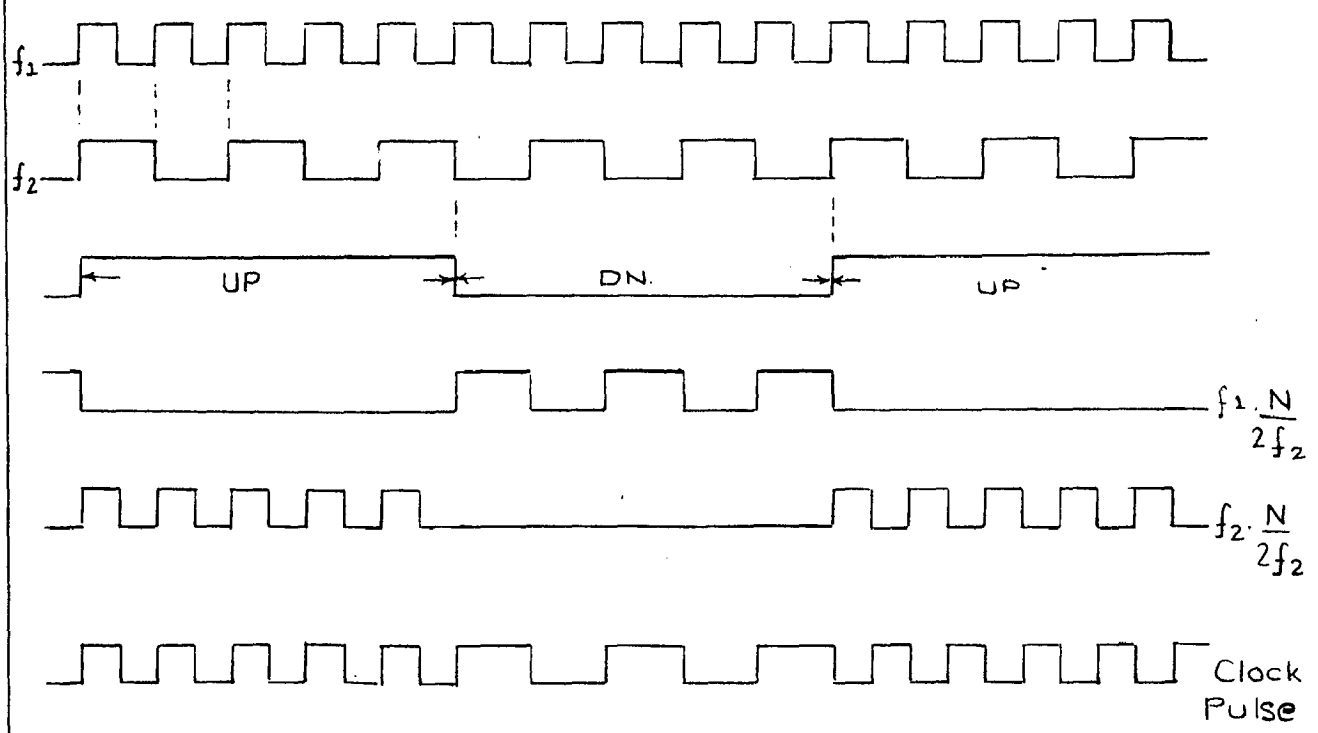


FIG:-5·29. TIMING WAVE DIAGRAM.

namely Block - I which is the Relay and Block - II which is the Distance to Fault Locator.

5.12.2(2) Inputs to the Relay

Now referring to Block I we have the following inputs to the the relay namely

$$\left| \frac{V_f}{n} - \frac{I_f}{2} \right| \quad \text{and} \left| \frac{I_f}{2} \right|$$

where V_f and I_f are the voltage and current of the faulted circuit.

The consideration for using these inputs is as follows. The characteristic of the the relay is a circle passing through the origin on the R-X diagram. In the Fig. 5.23, z is the diameter of the characteristic circle and represents the reach of the relay in the direction of the maximum torque angle, α_L is the impedance of the line. The characteristic equation for the threshold condition can therefore be written as

$$\left| \alpha_L - \frac{\pi}{2} \right| = \left| \frac{\pi}{2} \right|$$

Multiplying the above equation by I_f we have

$$\left| I_f \alpha_L - \frac{I_f \pi}{2} \right| = \left| \frac{\pi}{2} \right|$$

or $$\left| V_f - I_f \cdot \frac{\pi}{2} \right| = \left| I_f \cdot \frac{\pi}{2} \right|$$

$$\text{or} \quad \left| \frac{V_2}{n} - \frac{I_2}{2} \right| = \left| \frac{I_2}{2} \right| \qquad \text{eqn. (1)}$$

Hence the inputs to the rectifiers are $\left| \frac{V_2}{n} - \frac{I_2}{2} \right|$ and $\left| \frac{I_2}{2} \right|$. These are realised by the circuit diagram as shown in the schematic block diagram of Fig. 5.27.

These input currents are dropped across a resistive impedance Z_R to give voltage drops V_D and V_S respectively such that

$$V_D = \left| \frac{V_2}{n} - \frac{I_2}{2} \right| Z_R \qquad \text{eqn. (2)}$$

$$\text{and} \quad V_S = \left| \frac{I_2}{2} \right| Z_R \qquad \text{eqn. (3)}$$

5.12.2(3) Voltage to Frequency Converters

These voltage drops V_D and V_S are rectified and fed to two linear voltage to frequency converters such that

$$V_D \propto f_1 \quad \text{or} \quad V_D = K_1 f_1 \qquad \text{eqn. (4)}$$

$$\text{and} \quad V_S \propto f_2 \quad \text{or} \quad V_S = K_2 f_2 \qquad \text{eqn. (5)}$$

5.12.2(4) Frequency Counters

The frequencies f_1 and f_2 thus obtained are accurately counted over a period of time in a Frequency Counter. The period of time depends upon the gating frequency. The gate frequency is produced by an Astable

Multivibrator or a One Shot Monostable Multivibrator which supplies the gating pulse to both the Frequency Counters. During the period of the gating time, the counter counts the number of pulses. At the end of the gating time the counter stops counting, and the number stored in it is the number of pulses counted in the interval of the gating time. Since the gating time is the same for both the counters, the number of pulses stored in the counters corresponds to the same interval of time.

If the gating frequency is 1KHz, then the gating time is $1/1000 = 1 \times 10^{-3}$ secs.

or gating time = $1/F$ where F is the gating frequency.

Let n_1 and n_2 be the number of pulses stored in the frequency counters.

Then $n_1 = \frac{1}{F} \times f_1$ or $f_1 = F.n_1$ eqn. (6)

and $n_2 = \frac{1}{F} \times f_2$ or $f_2 = F.n_2$ eqn. (7)

5.12.2(5) Digital Comparator

The digital comparator proposed to be used is a two 4 bit word comparator having inputs A and B. This comparator gives three outputs namely, $A > B$, $A = B$ and $A < B$. The stored pulses n_1 and n_2 are fed to the inputs A and B of the comparator.

The output $A < B$ is fed to the tripping device to cause the operation of the relay.

The threshold condition for the rho relay is given by equation (1) i.e.

$$\left| \frac{V_r}{n} - \frac{I_r}{2} \right| = \left| \frac{I_r}{2} \right|$$

The relay therefore operates when

$$\left| \frac{V_r}{n} - \frac{I_r}{2} \right| < \left| \frac{I_r}{2} \right|$$

or $$n_1 \left| \frac{V_r}{n} - \frac{I_r}{2} \right| < n_2 \left| \frac{I_r}{2} \right|$$

$V_D < V_S$ from eqns. (2) and (3)

$K_1 S_1 < K_2 S_2$ from eqns. (4) and (5)

If $K_1 = K_2$. then $S_1 < S_2$

or $P n_1 < P n_2$ from eqn. (6) and (7)

or $n_1 < n_2$

But n_1 = Input A and n_2 Input B of the Digital Comparator. Therefore the relay operates when $B > A$. or $A < B$

5.12.3. Principle of Operation of the Distance to Fault Locator

The distance to fault is determined by measuring the impedance upto the fault. This therefore requires the measurement of the current and voltage of the faulted circuit. Now referring to block II of schematic diagram 5.27 we have the following

5.12.3(1) Current Measurement

The current to be measured is converted to a proportional voltage using a replica impedance z_r as shown, so as to give a voltage drop $V_s = I_f z_r$ where I_f is the current in the faulted circuit. This voltage V_s is rectified and fed to a linear voltage to frequency convertor to obtain a frequency 'f_2'. Thus

$$V_s \propto f_2$$

or $$I_f z_r \propto f_2$$

or $$I_f \propto f_2$$

5.12.3(2) Voltage Measurement

The secondary voltage V_f of the faulted circuit and the voltage V_s are together rectified and fed to a linear voltage to frequency convertor to obtain a frequency 'f_1' such that $(V_f + V_s) \propto f_1$.

5.12.3(3) Distance to Fault Measurement

The frequency signal 'f_2' which is proportional to the current is divided by an integer N so as to obtain a timing wave 'f_2/N' as shown in the timing wave diagram of Figure 5.29.

The signal 'f_2' is also gated through the AND gate II along with the inverted timing wave.

The signal 'f_1' is gated through the AND gate I along with the timing wave 'f_2/N'.

The outputs of the AND gates I and II are ORed. The output of AND gate I is an envelope containing pulses of frequency 'f_1' in the second half or negative half of the timing wave as shown in Fig. 5.29. The output of AND gate II is an envelope containing pulses of frequency f_2 in the positive or first half of the timing wave.

Since the outputs of the AND gate I and II are ORed, the output of the OR gate will consist of frequencies f_1 and f_2 as shown in the timing diagram. The output of the OR gate is fed to a bidirectional decade counter. The bi-directional counter counts up or down depending upon the control signal fed to the UP/DN terminal of the counter. The UP/DN signal is obtained from the timing wave f_2/N. Then counter counts UP in the positive half cycle with a frequency 'f_1' and DOWN in the negative half cycle with a frequency f_2. At the end of each cycle of the timing wave, the counter stores the difference of the pulses (n) obtained in both halves of a cycle.

The period of the timing wave is given by

$$T = \frac{1}{f_2/N} = \frac{N}{f_2}$$

The difference of pulses (n) is given by

$$n = n_1 - n_2$$

Where n_1=number of pulses counted UP

n_2 = number of pulses counted DN

$$n = n_1 - n_2$$

$$= f_1 \cdot \frac{N}{2 f_2} - f_2 \cdot \frac{N}{2 f_2}$$

$$= \frac{N}{2}\left(\frac{f_1}{f_2} - 1\right)$$

But $(V_f + V_S)\,\alpha^1\, f_1$

and $V_S\,\alpha^1\, f_2$

$$\therefore \quad \frac{f_1}{f_2} = \frac{V_f + V_S}{V_S}$$

$$= \left(\frac{V_f}{V_S} + 1\right)$$

$$\therefore \quad n = \frac{N}{2}\left(\frac{V_f}{V_S} + 1 - 1\right)$$

$$= \frac{N}{2}\left(\frac{V_f}{V_S}\right)$$

$$\frac{V_f}{V_S} = \frac{2}{N} \cdot n$$

$$\frac{V_f}{I_f \cdot Z_r} = \frac{2}{N} \cdot n$$

or $$\frac{V_f}{I_f} = \left(\frac{2}{N} \cdot Z_r\right) n$$

$$\therefore \quad Z_f = \left(\frac{2}{N} \cdot Z_r\right) n$$

Where Z_f is the impedance to the fault.

Now since N and Z_r are constant we have

$$Z_f \;\alpha^1\; n$$

From the above it is clear that the impedance to the fault is proportional to the number of pulses stored.

The fault locator if it is to give the distance to the fault directly, then the impedance to the fault Z_f will have to be divided by the impedance of the line per KM length of the line. Let Z_l be the impedance per KM length of the line. Then L_f the distance to the fault in KMS is given by

$$L_f = \frac{Z_f}{Z_l}$$

But $$Z_f = \left(\frac{2}{N} \cdot Z_r \right) n$$

$$\therefore \quad L_f = \left(\frac{2}{N} \cdot \frac{Z_r}{Z_l} \right) n$$

Now if the number of pulses stored and subsequently displayed is to indicate directly the distance to the fault then the quantity $\left(\frac{2}{N} \cdot \frac{Z_r}{Z_l} \right)$ should be made equal to unity.

Thus if $\left(\frac{2}{N} \cdot \frac{Z_r}{Z_l} \right) = 1$, then $L_f = n$ that is the distance to the fault in KMS is directly indicated by the digital display of 'n' the number of pulses stored.

In the quantity $\left(\frac{2}{N} \cdot \frac{Z_r}{Z_l} \right)$, Z_l the impedance/KM length of the line is a constant.

Hence $$Z_r = \frac{N \cdot Z_l}{2}$$

and therefore by adjusting N/2 with the value of Z_l, the above equation of Z_r may be made true and hence the value of Z_r may be fixed, in relation to N and Z_l.

For example a typical value of Z_L for a 220 KV line of route length 109 KM using 'DRAKE' ACSR Conductor is (0.77°j 42.22) ohms[79].

$\therefore$ If KM Z_L/KM length of the line = $\left(\frac{0.77}{109} \circ j \frac{42.22}{109}\right)$

$= (0.03 \circ j\ 0.4)\Omega$

If D is fixed at 10, then $Z_p = 10/2\ (0.03 \circ j\ 0.04)$

$= (0.4 \circ j\ 2.03)\Omega$

5.19 DESCRIPTION OF THE CIRCUITRY

5.19.1 Voltage to Frequency Converter

A complete IC Chip may be used for a voltage to frequency converter or it may be formed using Op Amps. A scheme using Coo - Moo operational amplifiers[80] is shown in Fig. 5.30(a). Alternately a scheme using transistors developed in the R&D-Fairchild development laboratories[81] which is a simple configuration of the familiar no-stable multivibrator may also be used. This scheme is shown in Fig. 5.30(b). Even a voltage to frequency converter using a Burr-Brown VFC 32 Op Amp. adapted to function over the voltage range with resistors can also be used[82]. This scheme is shown in Fig. 5.30(c). The voltage to frequency converter used should however have both linearity and stability over the entire range of voltage.

5.19.2 Frequency Counters

A frequency counter may be built using the schematic diagram shown in Fig. 5.31. The unknown frequency is applied

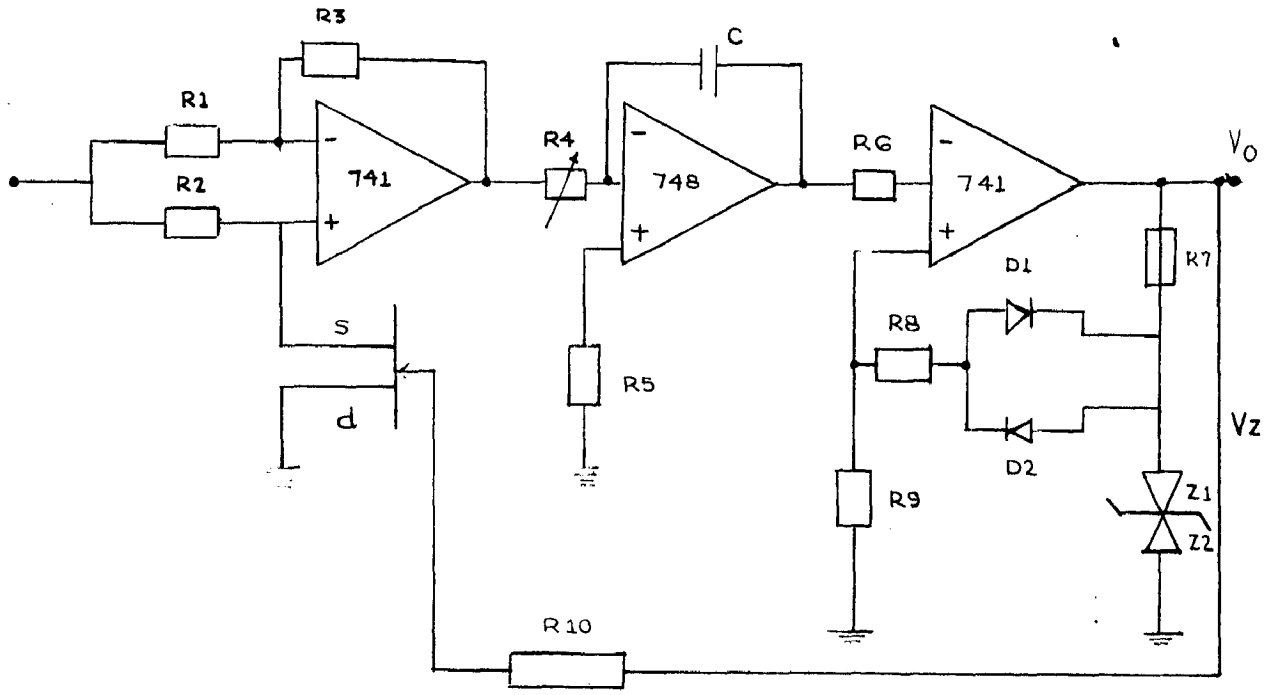


FIG:5·30(a)- VOLTAGE TO FREQUENCY CONVERTOR .

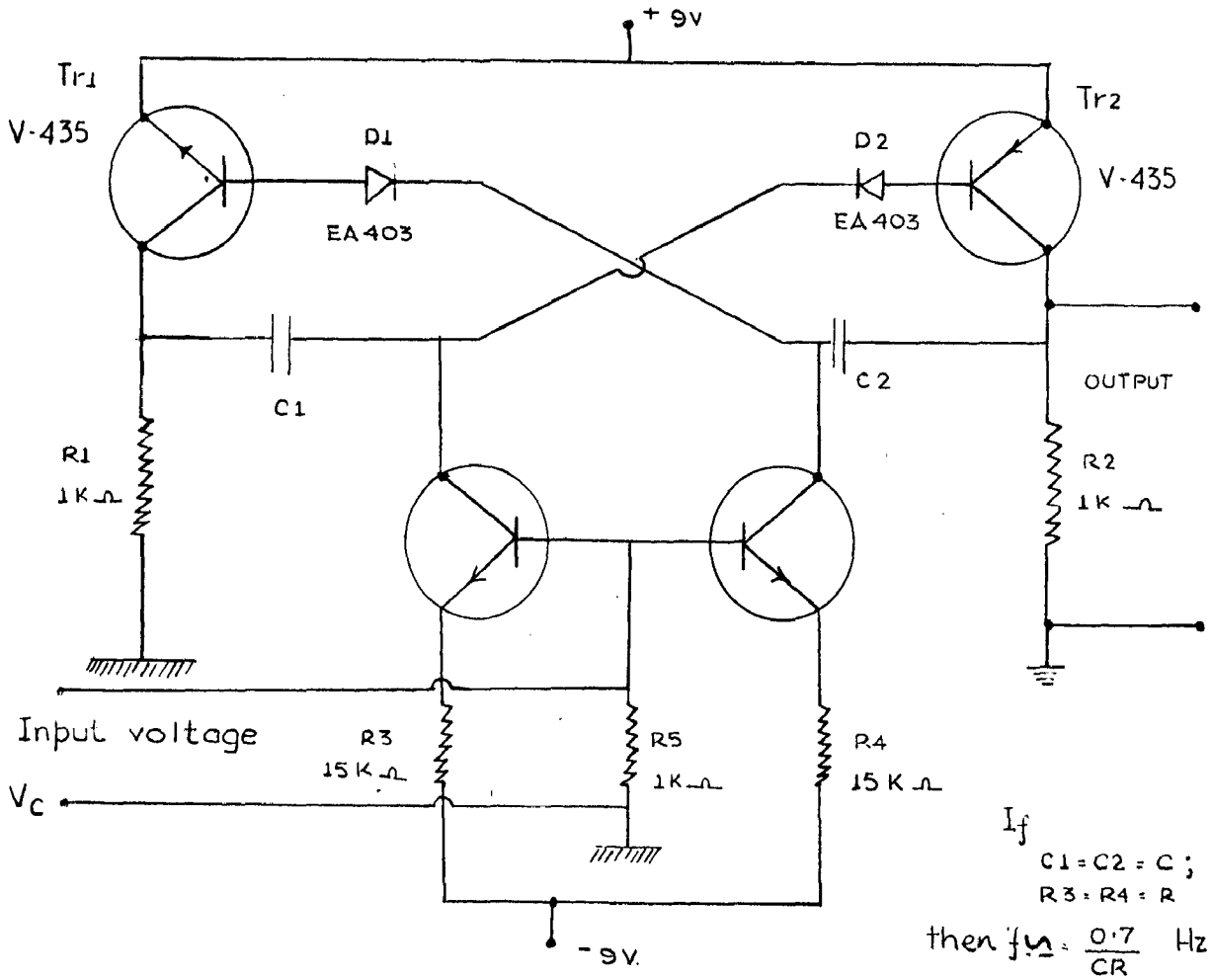


FIG:· 5·30(b)- VOLTAGE TO FREQUENCY CONVERTOR .

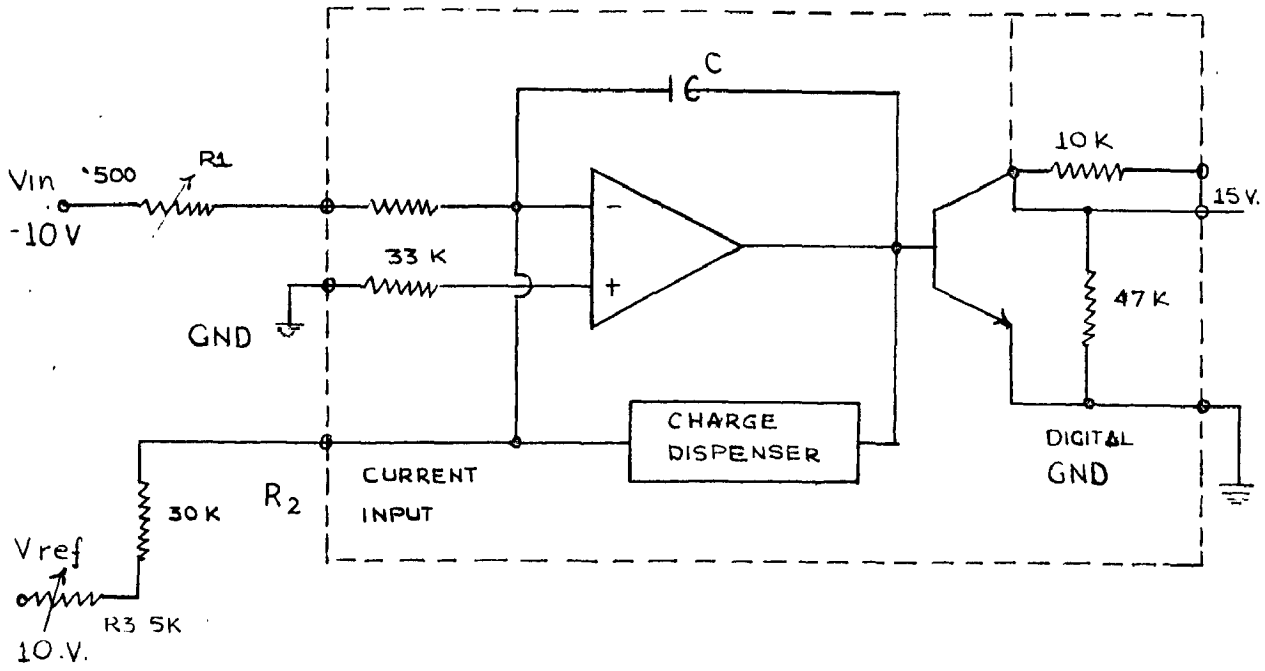


FIG:-5·30·(C)- V/F CONVERTOR USING BURR-BROWN VFC150P AMP.

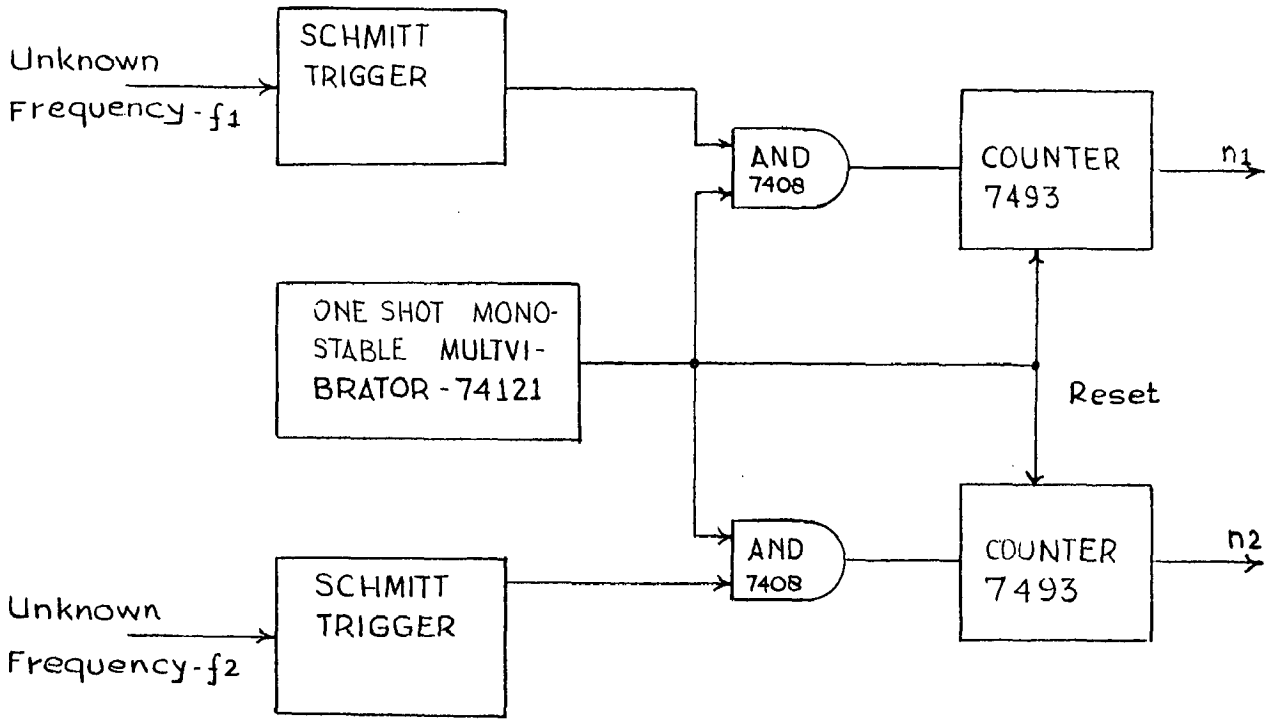


FIG:- 5·31 - FREQUENCY COUNTER

through a Schmitt trigger to obtain a square wave which forms the first input to the AND gate. The second input to the AND gate is the gating pulse. If the gating pulse frequency is 1 KHz, then the counter counts the pulses in a period of 10^{-3} secs. The gating pulse may be obtained from an astable multivibrator of Fig. 5.50(b) or from a monostable multivibrator.

The Schmitt Trigger circuit, the monostable multivibrator, the AND gates and the counter are all available in Fairchild TTL Digital Circuits. These are indicated in the Schematic diagram of Fig. 5.51.(76)

The capacity of the counter may be increased by using three or four 7493 binary counters in cascade with parallel clocking and cabling.

5.19.3. Digital Comparator

A 4 bit word magnitude comparator IC 7485 or 9325(70) is available in Chip form. It compares straight binary and straight BCD Codes. Three fully coded decisions about two 4 bit words A, B are made and are externally available at three outputs. Words of greater length may be compared by connecting comparators in Cascade.

If three 4 bit binary counters 7493 are used then three IC 7485 comparators have to be connected in Cascade and their cascaded output gives the final comparison $A \lessgtr B$.

The final output causes the operation of the relay as also causes the operation of the bidirectional counter in the fault locator circuit as described in para 5.19.3.

5.19.4. Divide By N Counter

The divide by N counter proposed is a Module-10 counter which requires that four flipflops be connected as a ripple counter using a NAND gate as described in para 5.10.0. This may be formed either by using TTL/MSI IC 7493 4-Bit Binary Counters or TTL/MSI IC 7490 Decade Counter[70]. Both of these counters have four dual rank, master slave flip-flops which are internally connected and can be connected externally through the NAND gate incorporated within the ip itself to form a divide-by-ten counter to divide the frequency f_2 by 10.

5.19.5 Bi-Directional Counter

A synchronous UP/DN Counter TTL/MSI IC 74190[70] is proposed to be used as a bidirectional counter. Synchronous operation is provided by having all flip-flops clocked simultaneously. During up-counting the counter counts the clock-pulses f_1 and during the down-counting it counts the clock pulses f_2. Three such counters are to be used in cascade with parallel clocking and parallel cabling so as to increase the capacity of the counter units . The bidirectional counter will start counting only when a positive indication that a fault has occurred is obtained. This is achieved by grounding the ground terminal no. 8 of the first unit counters through an emitter grounded n-p-n-transistor. The base of this transistor is fed from the output of a bistable multivibrator or a Schmitt trigger circuit which changes its state only when a pulse is obtained from the relay unit of Block I as shown.

5.13.6 Latch Units

Latches are used for temporary storage of binary information between the counting units and the decoding units. A monostable multivibrator latches the counter output so that it stores the binary values at the end of each cycle of the timing wave. Each counter unit is provided with a latch. The latch proposed to be used is a TTL/MSI SN 7475(78) unit and TTL/MSI 74121(78) one shot multivibrator is to be used as a monostable multivibrator.

5.13.7. Decoding Units

The decoding units proposed to be used are the TTL/MSI SN 7448(78) BCD to 7 segment decoder. These are decoders consisting of NAND gates, some AND-OR-INVERT gates. The output of the decoding units is fed directly to the LED's for digital display.

CHAPTER - 6
CONCLUSIONS

The review work indicates that the quadrilateral characteristic is the ideal characteristic. However the standard characteristics of circle and straight lines as obtained by conventional electromagnetic and static relays are quite satisfactory for all practical purposes unless special considerations dictate the use of other characteristics such as cone, quadrilateral etc. Those special considerations may be blocking on large power swings, to avoid maloperation due to fault arcs etc. The review work also suggests that static relays have definite economic and operational advantages over electromagnetic relays and the general tendency is to use static relays in the main protective scheme with electromagnetic relays in the back up mode. However with the development of digital computers, particularly in regard to the reliability of hardware circuitry microprocessors and minicomputers are finding wide application. The cost of microprocessors and minicomputers is prohibitive unless they are used for other functions such as data logging etc. There is therefore a general trend to have protective relays and schemes operating on a digital mode. It is for this reason that a mho distance relay has been proposed for development in Chapter V using analog and digital circuitry. The cost of such a scheme would be comparatively less when compared to other protective relays and schemes. The relay will have to be developed, tested for its characteristics on an artificial transmission line and subsequently subject to field tests.

The review work on fault locators indicated the need for the proper use of fault locators, their requirements and capabilities. The several fault locating methods are discussed, and there is scope for development of fault locators with cheaper circuitry and to have the same permanently connected on the line. As such a novel method of fault location is proposed for development using analog and digital circuits. The fault locator thus developed will have to be tested on an artificial transmission line and then subject to subsequent field tests. This testing will enable to overcome the deficiencies in the locator. These deficiencies may be incorrect indication of the distance due to fault arcs, tower foot resistances and effects of mutual inductances for which necessary compensation will have to be provided, to overcome them. The circuitry cost of such a fault locator would be quite cheap and comparable with the other fault locators in use. It may also be possible to develop other types of fault locators based on measurement of resistance and inductance by modifying the inputs to the fault locator.

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