AGGA-4 – Core device for GNSS space-receivers of the next decade

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INTRODUCTION

The development of the first AGGA (Advanced GPS/GLONASS ASIC) device was initiated within ESA's Earth Observation Preparatory Programme (EOPP) in order to support the Earth observation applications of navigation signals. After prototyping iterations, the flight component known as AGGA-2 was manufactured under Atmel product code T7905E [0]. The AGGA-2 is a space-qualified digital integrated circuit providing all the high-speed digital signal processing functionality for EO applications such as atmospheric sounding with radio occultation (RO) [2] and precise orbit determination (POD) of Low Earth orbiters for gravity field determination, altimetry, SAR interferometry, etc. The AGGA-2 design includes novel techniques for which international patents were assigned to the Agency.

Applications, techniques and technologies have evolved substantially since the specifications of the first AGGA device were established regarding for example:

- the understanding of the processing functionality that is optimal for atmospheric sounding, in particular through the development of the GRAS instrument in METOP
- new requirements regarding geodetic-quality receivers (e.g. for GMES Sentinel).
- enhanced GNSS signals from a larger number of GNSS systems (GPS / Galileo / Compass / Glonass) calling for extra functionality in the signal processing.
- advances in space ASIC technology that allow on-chip integration of much more functionality

The AGGA-3 [3] development was built upon the requirements, specifications and design of its predecessor (AGGA-2), as well as on industry feedback and signal specifications from Galileo available at that time. AGGA-3 represents a substantial upgrade of AGGA-2, mainly regarding:

- adding functionality to process new Galileo public signals (E1b, E1c, L5a, L5b) [4] and new Optimized GPS (L1 C/A, L2C, L5) signals [6], [7], [8]
- integration of more functionality on-chip (e.g. among others, digital down-conversion from Intermediate Frequency, the LEON2-FT microprocessor IP core [9] called "LEON" herebelow, high-speed SpaceWire interfaces [10], more baseband channels, tracking aids, etc); This non-exhaustive list is complemented in more detail later within this paper

Due to recent changes in the specifications of Galileo and modernized GPS signals, the existing VHDL design of AGGA-3 needed to be further consolidated through an on-going ESA contract with Astrium GmbH and Austrian Aerospace, finally leading to the production of the AGGA-4 ASIC. The AGGA-4 will include several improvements:

- enhancement of flexibility to process both memory-based codes, mainly for E1b, E1c, while keeping long LFSR generated codes for GPS L2C
- the optimisation of the GNSS channel to process more efficiently the new Pilot / Data components of the new GNSS signals
- improvement of the design methodology, optimising the device scalability and reducing the gate count, so that a larger number of GNSS channel can be fitted in the chip.

SCOPE OF THIS PAPER

This paper presents the architecture of the AGGA-4, with particular emphasis, among others on:

- the GNSS module, capable of processing all public (current and future) GPS signals as well as all open access Galileo signals. The GNSS module includes:

- front-end with four scaleable input modules that can be connected to multiple antennas and supports digital down-conversion, beam-forming, and enhanced power level detection
- not less than 30 highly configurable single-frequency / double code GNSS channels.
- code and carrier loop aiding support, and optimized raw sampling for open-loop signal tracking.

- the FFT module to support fast acquisition
- the on-chip LEON microprocessor [9], with its IEEE-754 compliant Floating Point Unit
- external interfaces like for example the high speed SpaceWire interfaces [10] among others

This paper also gives an overview of all the GNSS signals that AGGA-4 can process, namely:

- public modernized GPS signals: L1, L2C and L5 [5], [6], [7]
- public Galileo signals: E1b, E1c, E5a and E5b [4]
- and potentially the Chinese Compass-Beidou and new Glonass CDMA signals, thanks to the high level of flexibility in the architecture of AGGA-4.

In addition, this paper provides examples of configuration of AGGA-4 to process the relevant GNSS signals, as well as a short description of the AGGA-4 ASIC and final conclusions.

AGGA-4 DESCRIPTION

General

The AGGA-4 consists mainly of the GNSS module, the FFT module for fast acquisition, the On-chip LEON processor with its Floating Point Unit, and a series of extra logic and interface modules, as presented for AGGA-3 in [3]. Data is shared between the relevant modules through the AMBA High-performance Bus (AHB) and the AMBA Peripheral Bus (APB).

In terms of functionality, only the GNSS module has undergone major changes during the upgrade of AGGA-3 to AGGA-4. A high-level overview of the AGGA-4 device is given in the following figure.

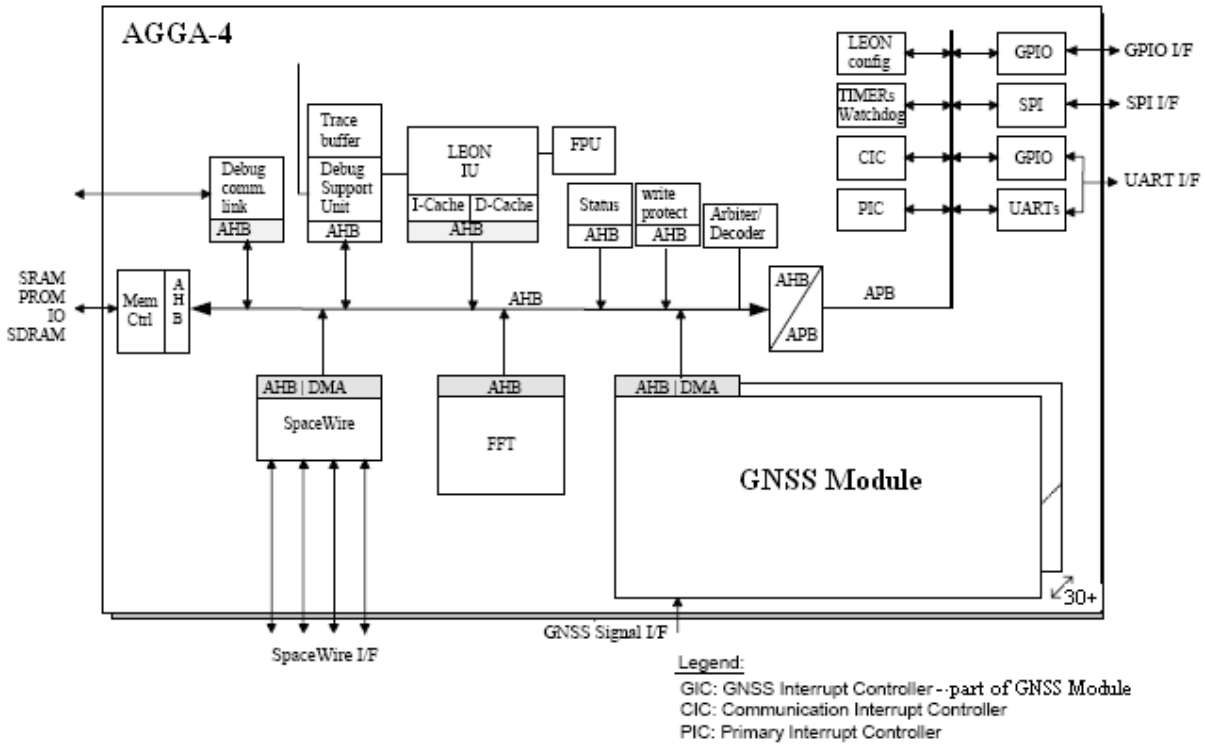

Figure 1 Overview of the AGGA-4 device

GNSS Module

The GNSS baseband processor is capable of processing the current and future GPS signals L1 C/A, L2C, L5 as well as the open access Galileo signals (E1B, E1C, E5a and E5b) that have shift register based codes and BOC(m,n) subcarrier. The GNSS Module shown in Figure **2** and Figure 3 includes the following sub-modules below:

- Front-end interface with scaleable input modules that can be connected to multiple antennas and supports digital down-conversion, two digital beam-forming (DBF), and enhanced power level detection,
- A Channel Matrix with not less than 30 (target 36) highly configurable single-frequency / double code GNSS channels. Each channel includes double code generators (for Pilot and Data components), complex code correlators and integration stages.
- code and carrier loop aiding support in each channel, and optimized raw sampling for open-loop signal tracking
- the Channel Matrix also has an Antenna Switch Controller (ASC) and a Time Base Generator.

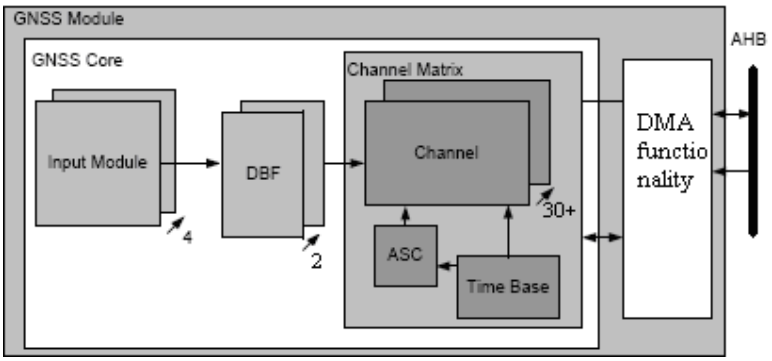

Figure 2 **GNSS module**

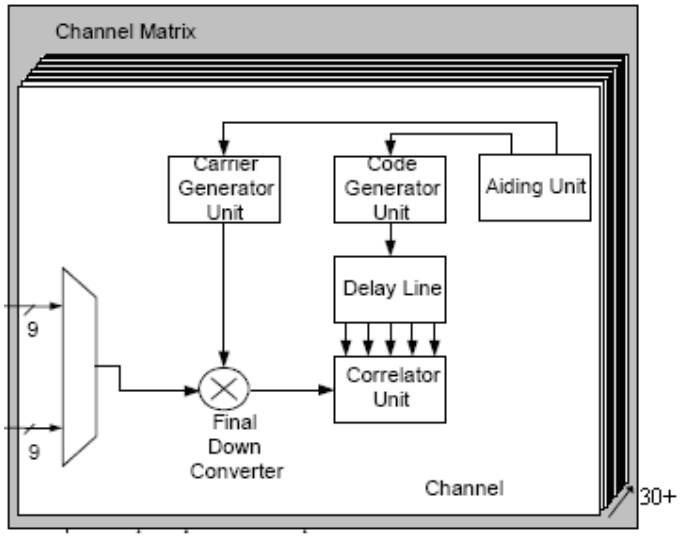

Figure 3 Functionality in the channel matrix (one of the not less than 30 channels)

Front-End Interface and Beam-Forming Module

AGGA-4 provides the same type of interfaces as AGGA-3. AGGA-3/AGGA-4 include functionality not present in AGGA-2, namely an interface for wide bandwidth navigation comparable to the interface of the digital down-conversion ASIC used in METOP GRAS.

AGGA-4 provides four input modules that support multiple input format in baseband (complex format) and in intermediate frequency (real format). Implementation losses are reduced through pre-pre-processing (I/Q mixer, FIR decimation, and re-quantisation) which also converts all input formats into a common 3-bit I and 3-bit Q output format. The front-end also provides Power Level Control functionality, including Digital to Analogue (DAC) conversion to support Automatic Gain Control.

Each of the two digital beam-forming (DBF) modules shown in Figure **2** performs digital phase shifting and combination of two antenna signals prior to the channel correlations. In total, the two DBF modules can process the inputs from four antennas. See example of application in Figure 4.

Channel Matrix with Configurable Single-Frequency / Double Code GNSS Channels

AGGA-4 aims at having not less than 30 (target is 36) highly configurable single-frequency double-code (for pilot and data components) GNSS channels are available. Each channel includes:

- Very flexible primary code generator units with:
    - a Linear Feedback Shift Registers (LFSR) allowing the generation of very long spreading codes for signals like GPS L2CL (767,250 chips)
    - memory-based capabilities allowing the generation of spreading codes required in signals like E1b and E1c.
- Support of Binary Offset Carrier (BOC) and secondary code sequences and secondary code stripping, in order to process the modernized GPS and new Galileo signals. By supporting BOC(m,n), AGGA-4 is also capable of generating 'sin' and 'cos', as opposed to AGGA-3 that could only do BOC(n,n) or 'sin'.
- 5 complex code correlators, to allow the Early-Early, Early, Puctual, Late, Late-Late correlations required for the processing of BOC signals. Code search during acquisition also benefits from this.
- Two configurable delay lines, which allow the tracking of double-code (pilot/data) signals in one channel

Thanks to the dual-code capabilities per channel, AGGA-4 will allow the processing of Data and Pilot components in just one channel (rather than two slaving channels as in AGGA-2/3).

In order to reduce the gate count per channel, hence maximising the number of channels, AGGA-4, as opposed to AGGA-2, will not contain any more the second integration stage necessary to perform codeless tracking of P-codes. This restriction is largely compensated by the number of new GNSS signals available and supported by AGGA-4.

Note also that code generation of Multiplex BOC (MBOC) signals in the form of Time MBOC (TMBOC) or Composite BOC (CBOC) is not supported in AGGA-4. However, MBOC signals can still be processed with the BOC codes generated by AGGA-4 at the expense of roughly 1dB loss in code phase tracking sensitivity. This drawback is considered negligible as compared to the savings in gate count, little need for multipath mitigation in space receivers and still great improvements when using BOC codes as compared to the codeless processing in AGGA-2.

As shown in Figure 1, the data from the GNSS baseband processor is transferred to memory by direct memory access (DMA) to the AMBA High-performance Bus (AHB).

Code and Carrier Loop Aiding Unit and Optimized Raw Sampling for Open-Loop Signal Tracking

Acquisition and tracking of GNSS signals requires regular intervention of a processor, in order to close the loops in software and to maintain tracking. These integration epochs typically lead to interrupts to the microprocessor with a rate between 1 to 20ms per GNSS channel, depending on the type of application and the signal properties. With a high number of channels to be serviced by a single processor, the interrupt rate can be prohibitive, unless functional blocks traditionally located in software (as for AGGA-2 based receivers) are moved from software to hardware. .

As compared to AGGA-2, two steps are supported by hardware in AGGA-4 in order to reduce significantly the interrupt frequency:

- by a DMA mechanism that allows the transfer the Integration results (either Raw Samples in open loop tracking or in closed loop tracking with navigation data information) without processor intervention into the external memory for a less time-constraint post-processing (e.g. packetisation or navigation data decoding).
- by providing a hardware Aiding Unit (see Figure 3), allowing autonomous code and carrier phase aiding in order to compensate for the Doppler rate caused by high orbit dynamics. The Aiding Unitsupports a second order correction function for both code and carrier.

Typically the aiding frequencies are computed immediately after a new navigation solution has become available, either at each Measurement Epoch (ME) or at each Pulse Per Second (PPS) event.

Other Functions in the Channel Matrix

For completeness regarding Figure 3, two more modules need to be mentioned.

The Antenna Switch Controller (ASC), as for AGGA-2, provides functionality to support the controlling of up to four antennas for attitude determination.

The Time Based Generator (TBG) produces the Measurement Epoch (ME) strobe, the Pulse-per-Second (PPS) strobe for synchronising external equipment, and the Epoch Clock (EPC). It also provides the Instrument Measurement time (IMT) counter. It is possible to select between an internally generated ME signal and an external input. The ME can be configured to sampling rates between 1Hz and 100 Hz.

FFT Module

A typical frequency search interval at the signal acquisition is 1 kHz. For carrier loop pull-in frequency however, errors smaller than 100Hz are required. Therefore, it is either necessary to have narrow frequency spacing during frequency search (resulting in long search times), or to provide other means for frequency estimation.

In AGGA-4, frequency estimation during acquisition is supported by a 128 point hardware FFT module (see Figure 1). The FFT could have been implemented in software as for AGGA-2, but the FFT results under high dynamic conditions may be outdated before they can be applied in the acquisition or tracking loop and this may also overload the LEON CPU.

On-Chip LEON Processor Modules

The LEON2-FT [9] processor implements the SPARC V8 standard as defined in the SPARC V8 architectural manual. The LEON processor and periphery consist of a cache sub-system, a memory controller, interrupt controller, two UARTS, two 32-bit timers, one 32-bit watchdog, bus status register, a write protection unit, a watch point registers and a 16-bit I/O-port.

AHB/APB buses (AMBA High-performance Bus and AMBA Peripheral Bus) are used to connect the processor to the peripheral devices and the other modules.

Unlike the DSP 21020 used in METOP-GRAS, the LEON architecture is not optimised for scientific floating point calculations, and therefore requires the support of a Floating Point Unit (FPU), which is also implemented on-chip in AGGA-4. The selected FPU is the IEEE-754 compliant GRFPU from Gaisler Research. The memory interface can use 8-, 32-, and 39-bit memories. Target frequency for LEON in AGGA-4 is 80 MHz.

Main AGGA-4 External Interfaces

This section gives further description of the main AGGA-4 external interfaces already shown in Figure 1.

UARTS:

Two UARTs are implemented in the AGGA-4, including two 16 byte FIFOs per UART, one in receive and one in transmit direction.

SpaceWire interfaces:

AGGA-4 has four bidirectional SpaceWire [10] interfaces are implemented with single-ended IO's (no LVDS) for general communication purposes (e.g. connection to EGSE, booting, extracting RAW samples, etc), the maximum data rate per SpaceWire link is around 30 Mbit/s per link.

Serial Peripheral Interface (SPI)

The SPI module provides select lines than can control more than one RF-ASIC.

Additional General Input and Output Ports

In addition to the 16 bit I/O port provided by the LEON on-chip peripherals, 16 additional general purpose bidirectional input/output ports are implemented.

GNSS SIGNALS SUMMARY

Compared to the AGGA-3 design [3], AGGA-4 will contain the following major changes:

- Processing both components (data and pilot) of most of the signals is possible in just one channel (slaving of 2 channels were needed in AGGA-3)
- P-code (codelesss) processing will not be possible any more.
- Memory-code capabilities are introduced in order to allow the processing of E1b-E1c signals, while a single LFSR is kept in order to allow the processing of the very long L2CL (767,250 chips) codes.

The following Table shows the signals that can be processed with AGGA-4.

Table 1 GPS signals and number or channels needed in AGGA-4 to process them.

GPS signals:	Nb. Channels needed	Remarks
- GPS/SBAS L1 C/A	1	
- GPS L1 P-code	N/A	P-code NOT possible in AGGA-4
- GPS L2 P-code		
- GPS L2CM (Data) (alone)	1	
- GPS L2CL (Pilot) (alone)	1	
- GPS L2CM and L2CL (jointly)	1	
- GPS L5 I (Data) (alone)	1	
- GPS L5 Q (Pilot) (alone)	1	
- GPS L5-I and L5-Q (jointly)	1	

Table 2 Galileo public signals and number or channels needed in AGGA-4 to process them.

Galileo signals:	Nb. Channels	Remarks
- Galileo E1-B (Data) (alone)	1	All public signals in Galileo
- Galileo E1-C (Pilot) (alone)	1	
- Galileo E1-B and E1-C (jointly)	1	
- Galileo E5a-I (Data) (alone)	1	
- Galileo E5a-Q (Pilot) (alone)	1	
- Galileo E5a-I and E5a-Q (jointly)	1	
- Galileo E5b-I (Data) (alone)	1	
- Galileo E5b-Q (Pilot) (alone)	1	
- Galileo E5b-I and E5b-Q (jointly)	1	
- ALTBOC (E5a and E5b) - (jointly)	**N/A**	Not supported. Priority given to optimize number gate count and number of channels
- Galileo PRS signals (E6 and E1-a)	N/A	PRS, SoL, CS specifications not analyzed for use in AGGA-4
- Galileo SoL signals		
- Galileo CS signals		

Should the Compass-Beidou and the new L1/L5 CDMA-Glonass public signal parameters remain as known by ESTEC in 2008, AGGA-4 will also be able to process those signals.

In short, AGGA-4 will be compatible with the processing of all GPS and Galileo Open Service (OS) signals. The following signals will not be compatible with AGGA-4:

- GPS P-codeless processin
- E5 AltBoc
- Galileo PRS (Public Regulated Service), Galileo CS (Commercial Service) and Galileo SoL (Safety of Life Service)

APPLICATION OF THE AGGA-4

In a typical environment (see Figure 4), the AGGA-4 receives the incoming down-converted navigation signal from an Analogue/Digital converter (ADC). 32 input pins are provided by the AGGA-4 ADC interface for the incoming signals. A synchronization (Synch) signal with the ADC can be generated by the AGGA-4. Additionally, the results of the power level measurements inside the AGGA-4 can be used to establish an Automatic Gain Control (AGC) loop to minimise saturation. Despreading of the navigation signal is performed in the signal processing part of the chip. Tracking loops closed by software executed on the on-chip LEON processor allow for code and carrier phase measurements and navigation data demodulation. The results are transmitted via SpaceWire to the Onboard Computer (OBC), Electrical Ground Support Equipment (EGSE) or Telemetry system.

A major difference between AGGA-4 (with at least 30 channels and a microprocessor on-chip) and AGGA-2 (with 12 channels) is the much larger number of satellite signals that can be processed in just one chip. In principle, with AGGA-4 it will not be necessary to chain two AGGA devices to process for example the 24 channels that were processed in the Metop GRAS instrument.

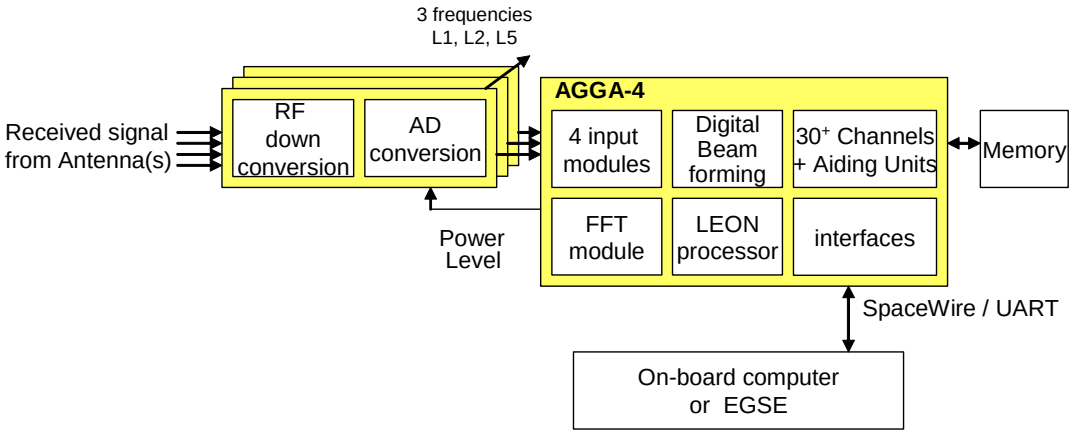

Figure 4: AGGA-4 typical application

Note that AGGA-4 is compatible with for example the Nemerix chipset (NJ1008 for RF down conversion and the NJ1017 or NJ1018 for the AD conversion).

AGGA-4 ASIC DESCRIPTION

The AGGA-4 chip will be manufactured by Atmel in the ATC18RHA 0.18 μm technology. The assumed package for the AGGA-4 device is an Atmel MQFP package with 352 pins. ASIC components are expected to become available for the whole European space industry in 3Q-2010.

The GNSS part of the AGGA-4 chip runs at max. 40 MHz and the LEON part runs at max. 80 MHz.

CONCLUSION

The AGGA-4 is under development at Astrium GmbH and Austrian Aerospace under ESA guidance. AGGA-4 components should be commercially available by 3Q-2010 for all European space industry. Like for AGGA-2 and AGGA-3, the resulting Intellectual Property Rights (IPR) of AGGA-4 will continue to belong to ESA.

AGGA-4 takes advantage of the major improvements already included in the AGGA-3 design such as the integration on-chip of the LEON2-FT fault-tolerant microprocessor with a powerful Floating Point Unit, the aiding unit in each GNSS channel within the GNSS module to release the CPU load of the LEON, an FFT module for fast cold acquisition, and many external interfaces to for example the on-board computer or the telemetry system.

During the upgrade of AGGA-3 to AGGA-4, only the GNSS channels within the GNSS module are undergoing major changes in terms of design and functionality in order to ensure full compatibility with the modernized GPS public signals (L1, L2C, L5) and the public Galileo signals (E1b+E1c, E5a, E5b). The AGGA-4 ASIC will include not less than 30 (target is 36) GNSS channels. AGGA-4 will be able to process in just one GNSS channel both Pilot and Data components for the open signals mentioned above. AGGA-4 would also allow the processing of the currently known Chinese Compass/Beidou signals and the new CDMA signals in Glonass thanks to the high level of flexibility present in the architecture of AGGA-4.

ACKNOWLEDGEMENTS

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