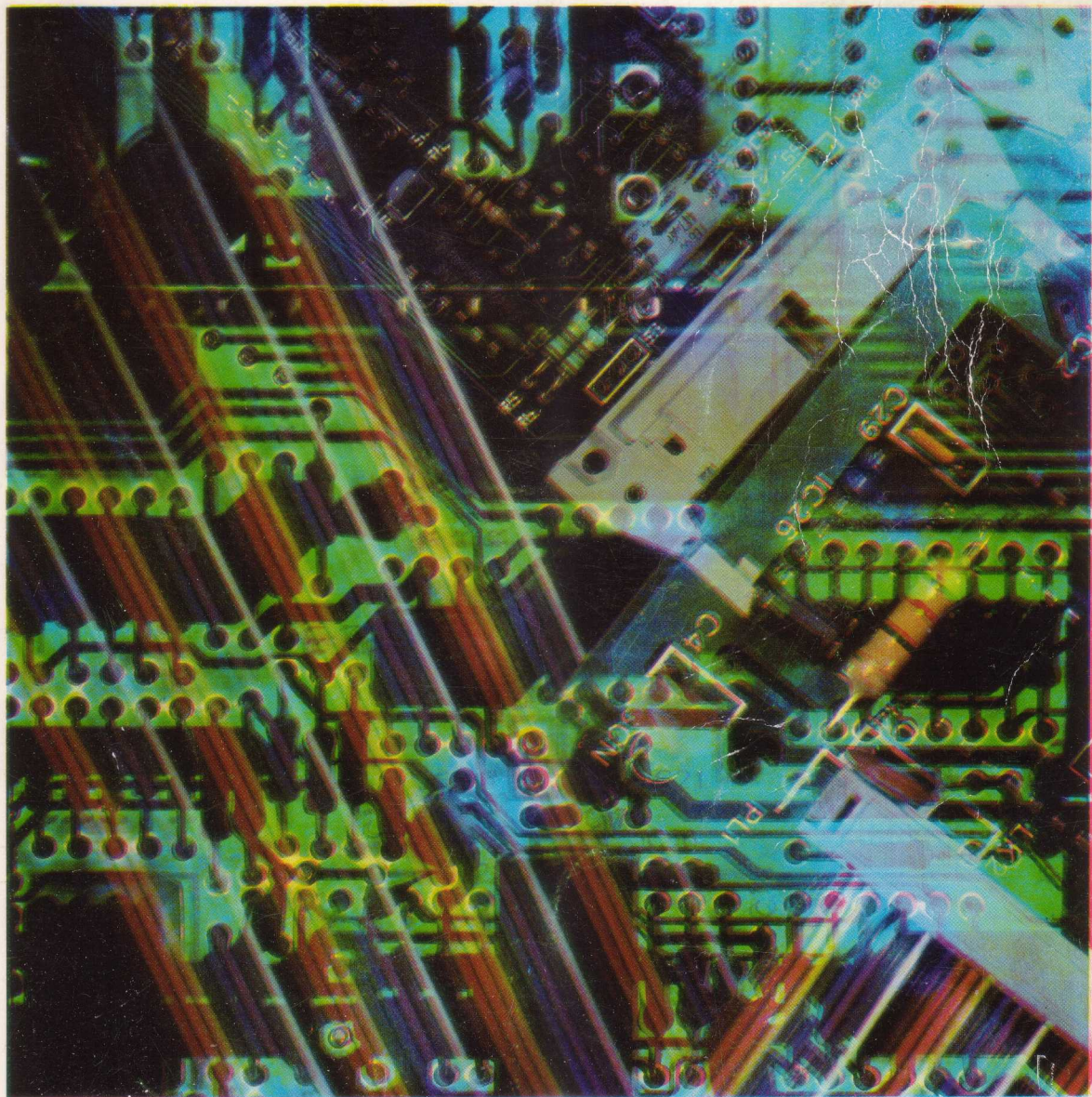


 **ACORN COMPUTER**

BBC Microcomputer Service Manual



BBC Microcomputer service manual

SECTION 1 BBC Microcomputer Models A and B (ANA01 - ANB04)

SECTION 2 BBC Microcomputer Model B+ (ANB51 - ANB54)

SECTION 3 Additional Upgrades

1770 Disc interface daughter board upgrade
64K Sideways RAM upgrade

Part No. 0433,001
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BBC Microcomputer Service Manual

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WARNING: THE COMPUTER MUST BE EARTHED

IMPORTANT: The wires in the mains lead for the computer are coloured in accordance with the following code:

GREEN & YELLOW - EARTH
BLUE - NEUTRAL
BROWN - LIVE

As the colours of the wires may not correspond with the coloured markings identifying the terminals in your plug, proceed as follows:

The wire which is coloured green and yellow must be connected to the terminal in the plug which is marked by the letter E, or by the safety earth symbol =|= , or coloured either green or green and yellow.

The wire which is coloured blue must be connected to the terminal which is marked by the letter N, or coloured black.

The wire which is coloured brown must be connected to the terminal which is marked by the letter L, or coloured red.

If the socket outlet available is not suitable for the plug supplied, the plug should be cut off and the appropriate plug fitted and wired as previously noted. The moulded plug which was cut off must be disposed of as it would be a potential shock hazard if it were to be plugged in with the cut off end of mains cord exposed.

The moulded plug must be used with the fuse and the fuse carrier firmly in place. The fuse carrier is of the same basic colour* as the coloured insert in the base of the plug. Different manufacturers' plugs and fuse carriers are not interchangeable. In the event of loss of the fuse carrier the moulded plug MUST NOT be used. Either replace the moulded plug with another conventional plug wired as previously described, or obtain a replacement fuse carrier from an authorised BBC Microcomputer dealer. In the event of the fuse blowing, it should be replaced, after clearing any faults, with a 3 amp fuse that is ASTA approved to BS 1362.

This computer was designed and manufactured to comply with BS 415. In order to ensure the continued safety of Acorn products, power supplies should be returned to Acorn for repair.

Do not use the Microcomputer in conditions of extreme heat, cold, humidity or dust or in places subject to vibration. Do not block ventilation under or behind the computer. Ensure that ,no foreign objects are inserted through any openings in the Microcomputer.

*Not necessarily the same shade of that colour.

1 Introduction

1.1 Nature and Purpose of the Manual

The purpose of this manual is to provide technical and diagnostic information about the BBC Microcomputer.

After giving general information about the technical specification and the mechanical assembly of the BBC Microcomputer, it gives a detailed description of the operation of the whole of the circuit. Information is also given about how to upgrade the various models of microcomputer and the purpose of the various links on the circuit board. Some details are also given of the ways in which the circuit has changed in its evolution from issue 1 up to issue 7. There is some guidance about servicing and fault-finding, further information about interfacing and a few suggestions about possible applications. Finally there is a section of hardware hints and tips which is a compilation of ideas from various sources.

1.2 Technical Specification

The BBC Microcomputer is supplied with two levels of hardware provision, designated, model A and model B, the former being fully upgradable to the latter.

1.2.1 Model A Specification

A fast, powerful self-contained computer system generating high resolution colour graphics and capable of synthesising 3 part music + 1 channel of noise. The computer is contained in a rigid injection moulded thermoplastic case. The following are contained within the computer thus ensuring the minimum of connecting wires.

* 73 key full travel QWERTY keyboard including 10 user definable function keys. The keyboard has two key rollover and auto repeat.

* Internal power supply is fully encased and manufactured to BS 415 Class 1.

* The internal loudspeaker is driven from a 4-channel sound synthesis circuit with full ADSR envelope control.

* A colour television signal, for connection to a normal domestic television aerial socket, is available through a phono connector. This signal is 625 line, 50Hz, interlaced, fully encoded PAL and is modulated on UHF channel 36.

* A BNC connector supplies a composite video output to drive a black and white or PAL colour monitor.

* A standard audio cassette recorder can be used to record computer programs and data at 300 or 1200 baud using the Computer Users Tape Standard tones. The cassette recorder is under full automatic motor control and is connected to the computer via a 7 pin DIN connector.

- * An interrupt driven elapsed time clock enables real-time control and timing of user responses.
- * The unit uses a 2 MHz 6502A and includes 16K of Random Access Memory.
- * A 16K Read Only Memory (ROM) integrated circuit contains a Machine Operating System designed to interface easily to high level languages.
- * A further 16K Language ROM contains a fast BASIC interpreter. The interpreter includes a 6502 assembler which enables BASIC statements to be freely mixed with 6502 assembly language.
- * Up to four 16K "sideways" ROMs may be plugged into the machine at any time. These four ROMs are "paged" and may include Pascal, word processing, computer aided design software, disc and Econet filing systems or Teletext acquisition software.
- * The full-colour Teletext display of 40 characters by 25 lines, known as mode 7, has character rounding, with double height, flashing, coloured background and text plus pixel graphics - all to the Teletext standard.
- * The non-Teletext display modes (modes 0 to 6) provide user definable characters in addition to the standard upper and lower case alphanumeric font. In these modes, graphics may be freely mixed with text. Text characters can be positioned not only on, for example, a 40 x 32 grid, but at any intermediate position.
- * Separate or overlapping text and graphic windows can be easily user-defined over any area of the display. Each of these windows may be filled separately and the text window scrolls independently of the rest of the screen.
- * The Model A is able to support the following modes:-
 - Mode 4: 320 x 256, 2 colour graphics and 40 x 32 text (10K)
 - Mode 5: 160 x 256, 4 colour graphics and 20 x 32 text (10K)
 - Mode 6: 40 x 25, 2 colour text only (8K)
 - Mode 7: 40 x 25, Teletext display (1K)
- * All graphics access is "transparent" (see section 2.2), resulting in a fast, snow-free display.
- * Extensive support is provided in the Machine Operating System for the graphics facilities, and this is reflected in the BASIC interpreter. These facilities include the ability to draw lines very rapidly and to fill large areas of colour. In addition, very rapid changes of areas of colour can be effected by the use of a colour "palette".
- * The Model A BBC Microcomputer can be expanded at any time to the Model B. In addition, or as an alternative, other facilities such as the Econet may be fitted within the computer system.

1.2.2 Model B Specification

The Model B BBC Microcomputer is an enhanced version of the Model A Microcomputer with the following differences:-

* 32K Random Access Memory (RAM). This enables the following extra graphics modes to be used:-

Mode 0: 640 x 256, 2 colour graphics and 80 x 32 text (20K)

Mode 1: 320 x 256, 4 colour graphics and 40 x 32 text (20K)

Mode 2: 160 x 256, 16 colour graphics and 20 x 32 text (20K)

Mode 3: 80 x 25, 2 colour text only (16K)

* The installed RAM is divided between the high resolution graphics display, the user's program and Machine Operating System variables. If higher resolutions are required with large programs, then the second processor option may be fitted.

* 6 pin DIN connector provides separate RGB and sync outputs at TTL levels. RGB are all high true, and sync is link selectable as high or low true, pulse duration 4.7 microseconds.

* Serial interface to RS423 standard. The new standard has been designed to be inter-operable with RS232C equipment but offers a considerably enhanced specification - for example in maximum length of cable and maximum data transfer rates. Baud rates are software selectable between 75 baud and 9600 baud. The interface provides not only two-way data transfer, but also two-way hand-shaking using RTS and CTS lines. The software for implementing this interface is only provided with operating systems 1.2 onwards.

* An 8 bit input/output port with 2 control bits is also provided.

* Four analogue input channels are provided. Each channel has an input voltage range of 0 - 1.8V. The conversion time for each channel is 10 milliseconds. These analogue inputs can be used not only as inputs for games-paddles or joysticks but also in laboratory control situations. The resolution of the ADC chip is 12 bits, but its conversion is such that only 9 or 10 bits are significant. However with suitable averaging, this can be extended to the full 12 bits accuracy.

* A 1 MHz buffered extension bus is provided for connection to a variety of external hardware such as a Teletext acquisition unit, IEEE 488 interface, Winchester disc drive etc.

1.2.3 Expansion

The following expansion options are available, some of which may be fitted internally at purchase, but all of which could be fitted by Dealers at a later date:-

- * Floppy disc interface (fitted as an option at purchase)
- * Econet network interface (fitted as an option at purchase)
- * Voice synthesis circuit with cartridge ROM pack interface
- * Various alternative high-level languages in ROM

External options which plug directly into the machine include:-

- * Games paddles
- * Cassette Recorder
- * Black and White and colour monitors and televisions
- * 5 1/4" disc drives, ranging from single-sided single density (100K) to dual double sided double track density (800K).
- * Dot-matrix or daisy wheel printers, serial or parallel interface
- * Teletext acquisition unit enabling Tele-software to be downloaded into the BBC Computer as well as providing access to the normal Teletext services. Pages may be "grabbed" and stored for later use.
- * 3 MHz 6502 second processor with 64K of RAM.
- * Z80 second processor with 64K of RAM and a fully CP/M-compatible operating system.
- * IEEE interface
- * Winchester 10 megabyte disc drive
- * Prestel adaptor unit

1.2.4 Software

Considerable attention has been paid to the overall design of both systems and applications software. A modular approach has been adopted specifically to ease the interfacing of various high-level languages (such as BASIC and Pascal) to the operating system.

1.2.5 Machine Operating System

A 16K ROM is used for the MOS. This software controls all input/output devices using a well defined interface. The MOS supports the following interrupts (the full implementation only being available from MOS 1.2 onwards):-

- * Event Timer (10ms) (used as an elapsed time clock)
- * 4 channel analogue to digital converter
- * Vertical sync
- * Keyboard and keyboard buffer
- * Music tone generation and buffer
- * Serial interface, input and output buffers
- * Parallel input/output port

and 'hooks' are provided to support other devices such as:-

- * Teletext acquisition
- * Prestel acquisition
- * Econet file system
- * Disk file system
- * Byte transfer to second processor

The majority of the operating system calls are vectored to enable the user to change them if required.

1.2.6 BASIC

The **BASIC** interpreter is an extremely fast implementation, with **numerous powerful** extensions:-

- * **Long variable** names
- * **Integer**, floating point and string variables
- * Multi-dimension integer, floating point and string arrays
- * **Extensive** support for string handling
- * **IF ... THEN ... ELSE**
- * **REPEAT ... UNTIL**
- * Multi-line integer, floating point and string functions
- * Procedures
- * **Local** variables
- * Full recursion on all functions and procedures
- * Effective error trapping and handling
- * Cassette loading and saving of programs and data
- * Full support for the extensive colour graphics facilities
- * Easy control of the built-in music generation circuits
- * Built-in 6502 mnemonic assembler enabling BASIC and assembler to be mixed, or pure assembly language programs to be produced.

1.3 Packaging

The BBC Microcomputer is supplied in a two part moulded polystyrene packing which is further packaged within a cardboard sleeve. With the Microcomputer, a User's Manual, a Welcome Cassette package and a UHF TV lead are also supplied. The packaging should be kept intact in case it becomes necessary to transport the unit at a later date.

1.4 Mechanical assembly of case etc

The lid of the Microcomputer case may be removed after undoing four fixing screws, two on the rear panel and two underneath. When reassembling, press the lid down at the rear whilst tightening the two rear fixing screws. Take care not to lose the two spire clips pushed onto the case lid, into which the rear fixing screws locate. NB Do not remove the lid with the mains power connected.

Inside the Microcomputer are three main sub-assemblies:
power supply unit, keyboard and the main printed circuit board.

To remove the keyboard, undo the two or, in some cases, three screws and nuts holding it to the case bottom, take care to note the positions of the associated washers. Unplug the 17 way keyboard connector and the 2-way loudspeaker connector from the main printed circuit board, and the 10 way serial-ROM connector, if fitted.

The power supply unit is connected to the main circuit board by seven push-on connectors which may be unplugged. Three screws on the underside of the case are undone allowing the unit to be removed. On reassembly, ensure that the same type of screw is used.

The main printed circuit board can be removed after the two wires to SK2 (composite video BNC socket) have been disconnected. Undo the four fixing screws (five or seven screws on later issue boards) and remove the circuit board from the case by sliding it forwards and then lifting it from the rear.

2 General Description of Hardware

2.1 Introduction

This next section gives a general description of the hardware of the computer, and reference is made to the functional block diagram (section 9.1) which is laid out approximately as the components are situated on the printed circuit board. General areas and component orientations are referred to by using compass points, as shown on the block diagram. When any reference needs to be made to the specific position of a component, then X-Y co-ordinates will be used, giving the distances in millimetres from the SW corner. This is also shown on the block diagram. A list is given in section 8 of this manual of all the integrated circuits, transistors, diodes, capacitors, resistors and selection links by number, including their X-Y co-ordinates on the PCB and on the main circuit diagram.

As each section of the hardware is described, reference is made to sections of the following chapter in which more detailed descriptions are given. The heart of the hardware is the 6502 microprocessor, and in this general description we shall move around the 6502 in an anti-clockwise direction starting from the SE corner of the PCB.

2.2 Hardware description

The 6502 accesses an area of just less than 32 Kbytes of ROM. (3/4K of this memory allocation is actually used for memory-mapped input/output.) The ROM is arranged in such a way that one group of 16K bytes forms a fixed part of the memory map (15 1/4K ROM for the operating system + 3/4K of I/O), whilst the other 16K has been organised to give as much flexibility as possible. There is a ROM select facility for accessing up to 16 different memory devices, although only four sideways ROM sockets are available on the PCB. It is expected that the normal way in which these four sockets will be used is to provide 2 MHz access to each of 4 chips which could be either 16K or 8K, ROMs or EPROMs. [See section 3.2]

The RAM is also divided into two sections of 16 Kbytes, each of which contains eight 16K by 1 bit DRAM chips. In the model A microcomputer, only one bank of 16K is present whilst both are present in the model B. This RAM has to be accessed by both the processor itself and also the CRT controller. This is done by using a form of "transparent access" in which both the processor and the CRT controller can access the RAM at the full clock speed by interleaving the accesses on alternate phases of the system clock. [See section 3.3]

The display is extremely versatile, and uses two entirely different methods depending on screen mode. Mode 7 uses Teletext hardware which produces RGB signals by having its own character generator and accepting data from the RAM as ASCII characters. This means that it uses very little RAM (only 1 Kbyte), and apart from providing the addressing for the RAM, the only thing which the CRT controller has to do is to add the cursor information and sync signals.

In the other screen modes, the information is stored in RAM as actual bit patterns for every character that is written to the screen. This is expensive in terms of memory usage, (between 8K and 20K in the different modes) but it makes it extremely versatile, especially when mixing graphics with text. The addressing of the RAM for the different modes is performed by the 6845 CRT controller, whilst the data is taken from the RAM and serialised by a custom designed circuit, known as the video processor. This data is not used directly to produce RGB information, but can be thought of as a set of logical colour numbers which are passed to an area of high speed RAM within the video processor referred to as the colour palette. This determines, for each logical colour number, which combination of red, green and blue is produced, and whether or not the colour is flashing. The video processor is also responsible for selecting either the RGB signals coming from the Teletext chip or the signals coming from the palette and sending them out to the RGB buffers and the PAL encoder.

This RGB information is presented, after buffering, on the RGB connector. To provide a UHF output, the RGB signals are combined with the sync signals and fed into a UHF modulator. A video output is also provided which consists of a summing of the RGB signals in such a way as to give an appropriate grey scale. On issue 4 boards onwards, the option is given of adding colour to the video signal in order to provide a PAL encoded video output. [See section 3.4]

Moving on round in an anti-clockwise direction we come to the two serial interfaces, the cassette interface and the RS423. These facilities are both provided by a standard ACIA (Asynchronous Communications Interface Adaptor) - the 6850, and a custom designed circuit referred to as, the serial processor. This processor contains the programmable baud rate generators for transmit and receive which provide the clocks for the ACIA. The ACIA itself is responsible for serialising the data, providing the control lines for the RS423 and generating interrupts, whilst the serial processor switches these data and control lines between the cassette and RS423 interfaces. The serial processor also provides data separator and sinewave synthesis circuits for the cassette recorder as well as a means of detecting the presence of the incoming tone from the recorder. [See section 3.5]

The next section is the analogue input port which is a four channel 12 bit converter which is discussed in more detail in section 3.9 and the interfacing survey (see chapter 7).

In the NW corner is the Econet section which centres around a 68B54 Advanced Data-Link Controller (ADLC). This is a sophisticated serial communications device allowing the sending and receiving of data at a variety of speeds between as many as 254 computers. The data transfer is synchronised by a clock signal fed to all the computers as a differential signal on one pair of cables, whilst the data itself uses another pair of cables. Data is both transmitted and received on the same pair of cables, but obviously only one computer at a time is able to "broadcast" onto the data highway. [See section 3.12]

There are two 6522 versatile interface adaptors (VIA) on the PCB (one on the model A), the first being used mainly for internal control and the second for external interfacing. VIA-A is used both for control of internal hardware and also for generating interrupts from various devices such as the ADC and the keyboard. Of its two internal timers, the first is used for generating regular interrupts at one centisecond intervals and the second is used occasionally by the operating system. [See section 3.6]

Of the two ports on this VIA, PA is used to provide a slow (1 MHz) data bus for the sound and speech chips and also for the keyboard, whilst PB is used to provide control lines for various functions throughout the circuit board. The sound is produced by a four-channel sound generator chip (SN76489) whilst the speech is produced by a TMS 5220 which can get its data either from RAM through VIA-A or from a serial ROM, the TMS 6100. This facility for accessing serial ROMs is also used to provide an external serial ROM facility on the keyboard. [See sections 3.7 and 3.8]

Moving down to the SW corner we have the disc controller interface based on an 8271 floppy-disc controller. This is responsible for sending out the command signals for a floppy disk drive, and for reading and writing the data from and to the disk drive. [See section 3.10]

The next device is VIA-B, referred to as the external VIA, which is used to provide interfaces for a printer and user applications. It also has two timers which are available to the user for his own applications programs. [See section 3.11]

The last two sections of the circuit board are the 1 MHz extension bus and the TUBE. These provide two different ways of accessing various external devices. The 1 MHz bus is available for more general use but works at the slower speed of 1 MHz, whilst the TUBE works at the full 2 MHz but is only intended for use with second processors. [See section 3.13]

3. Detailed Circuit Description

3.1 Processor + clock circuitry + reset circuitry

The microprocessor is a 6502A and runs at either 1 or 2 MHz. Most processing is done at 2 MHz, including accesses to the RAM and ROM, but the processor slows down to 1 MHz when addressing slow devices, viz. the 1 MHz extension bus, the ADC, the two VIA's, the 6845 CRT controller, the ACIA, and the serial processor. Clock signals for the microprocessor are produced by a 16 MHz crystal oscillator (IC43) in conjunction with divider circuitry in part of the video processor (IC6) which produces 8, 4, 2 and 1 MHz signals. The 1 MHz signal coming directly from the video processor is only used for the Teletext generator chip, whilst a D-type flip-flop (half of IC34) divides the 2 MHz clock signal in order to produce the system 1 MHz clock (1 MHzE). A 2 MHz signal of suitable phase is produced at the output of another D-type (half of IC31) which remembers when a 1 MHz cycle has been requested. At the appropriate time, as governed by the 2 MHz clock, one of the 2 MHz clock cycles is masked off by the D-type (half of IC34) and when this happens the D-type that remembered that a request had been made, is cleared. Depending on the phase relationship between the 1 and 2 MHz clocks at the time of the request, the delay on the 2 MHzE clock is different as illustrated by the diagrams below. The following simple program will produce these conditions alternately, so that they may be viewed with an oscilloscope.

```
10 P%=&3000
20 [ SEI
30 .start
40 STA &FC00
50 STA &FC00
60 JMP start
70 ]
80 CALL &3000
```

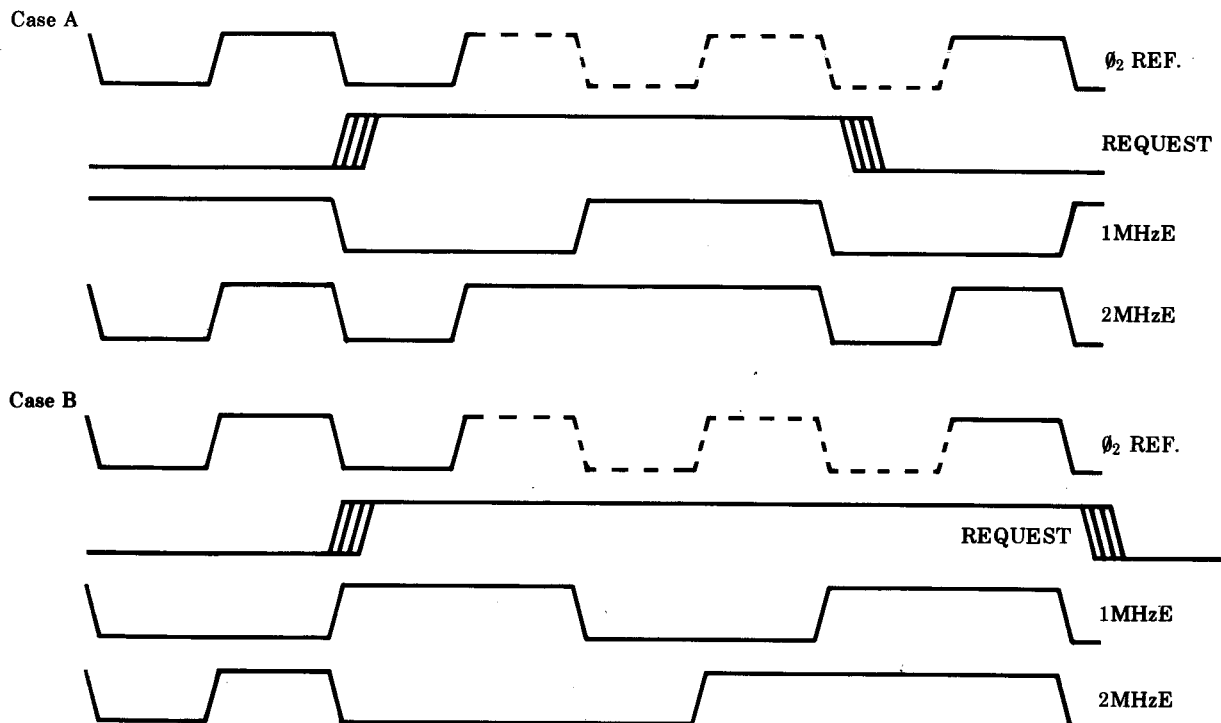


Figure 1 2-1 MHz stretching

A 555 timer circuit (IC16) provides a reset signal both at power up and also when the BREAK key is pressed. There is also a separate reset circuit using a CR combination from the +5 volt power supply (C10 and R20 and D1), to provide a signal called Reset A which is fed to IC3, the internal VIA. The idea is that although the 555 timer produces a general reset at power up or when the BREAK key is pressed, Reset A goes low only on power up. By interrogating the interrupt register on IC3 on the occurrence of a general reset, the microprocessor can discover whether it was a "cold start", ie power up, or a "warm start", ie the BREAK key has been pressed when the system has already been in use for some time.

3.2 Memory and address decoding

31 1/4 Kbytes of ROM are catered for in the address map. 15 1/4 Kbytes of this are contained in the operating system (IC51). This is in fact a 16K device but 3/4K of it is left unused and it is in this area that the I-0 device memory map is situated. Four other ROMs (ICs 52, 88, 100 and 101) are on the main circuit board. They may all be 16 Kbyte devices, in which case any one of them may be switched into the 16 Kbyte space in the memory map by writing to the ROM select latch (IC76). Alternatively, four 4 Kbyte ROMs may be in these four sockets in order to fill the 16 Kbyte space assigned. In this case, a two line to four line decoder (half of IC20) is used to select which of the four devices is being addressed by the address lines A12 and A13. Mixtures of these two cases are allowed for, for instance two pairs of 8 Kbyte ROMs, one pair or the other being selected by the ROM select latch and then the ROM to be used in each pair being selected by the 2-4 line address decoder. Address decoding for the ROMs is by IC21 which decodes memory addresses &8000 to &C000 and &C000 to &FFFF. Locations from 0 - &7FFF are assigned to the dynamic RAM, and this is decoded by feeding A15 into pin 4 of IC21. All the rest of the hardware is mapped within locations &FC00 to &FEFF. This is decoded by IC22, whilst ICs 20 and 25 are used to mask off the ROM over this range of addresses. ICs 24 and 26 decode the individual devices within this range, some of which are read or write only. IC23 detects when a slow 1 MHz device is being addressed and it calls for the 6502 to execute a slow clock cycle.

Note that in early versions of the BBC Microcomputer, the operating system was contained within 4 EPROMs in IC positions 52, 88, 100 and 101 while the BASIC interpreter was located in IC51. This arrangement is abnormal and has been phased out. Refer to the link selection survey (5.1) for more detailed information on this.

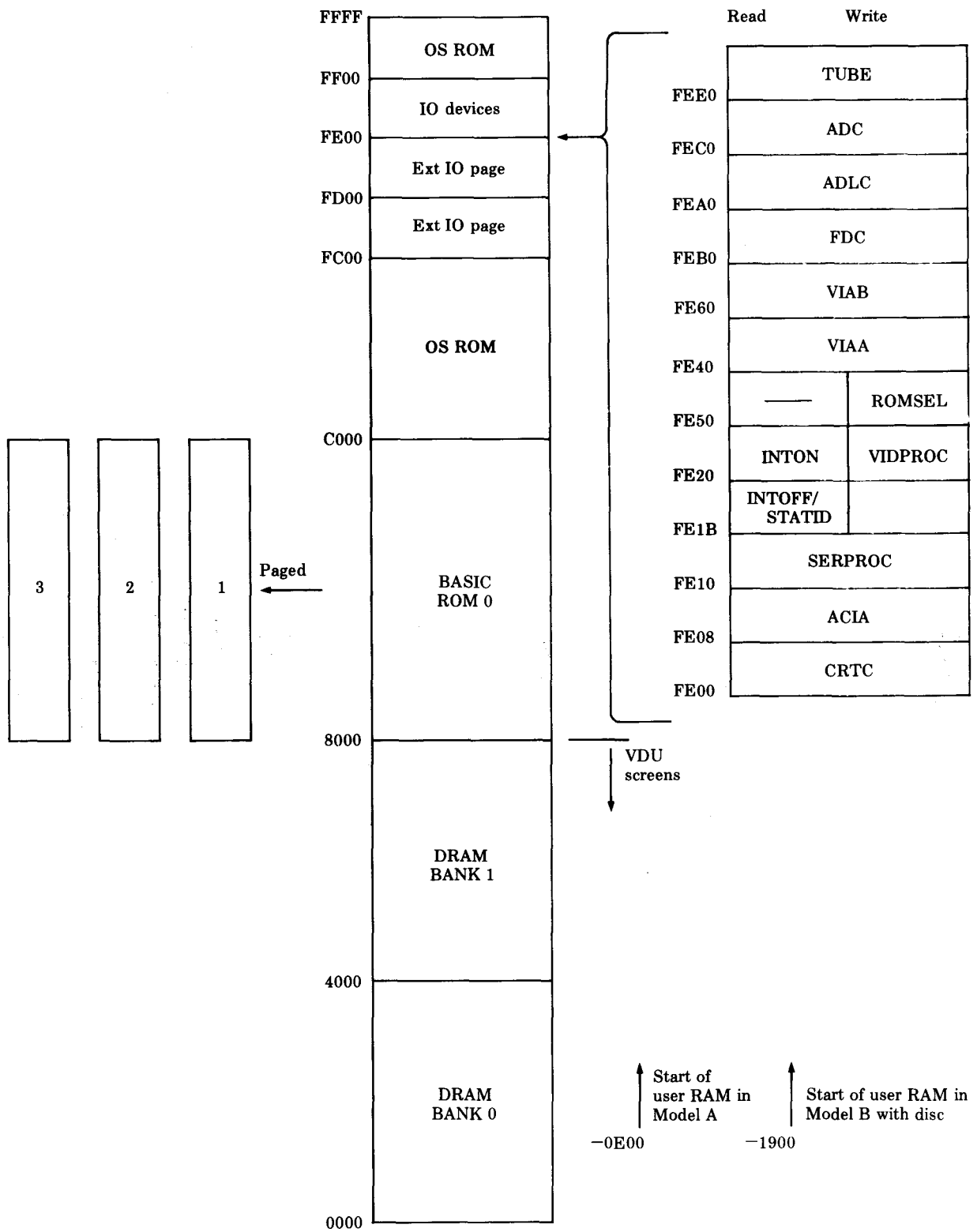


Figure 2 Memory map, including internal hardware

3.3 CRT controller + video processor + Teletext hardware

Random Access Memory on the Microcomputer is provided by either 8 or 16 dynamic memory devices (ICs 53-68). These devices store 16K bits each and therefore in the Model B, the data inputs and outputs of one pair of devices are paralleled for each of the 8 data bits, D0 to D7. To address 16K bits requires 14 address lines, and this is achieved on the 4816 by having 7 inputs and latching in the addresses in two halves by using a row address strobe (RAS) and a column address strobe (CAS). Two octal buffers (81LS95) have to be used to multiplex the appropriate processor address lines onto the RAM address lines. (ICs 12 and 13). However, the 6845 CRT controller (IC2) also needs to access the RAM, and what is more, it accesses it differently depending on whether it is working in the Teletext mode or in one of the other graphics modes. Therefore two more pairs of octal buffers are used, ICs 10 and 11 for the Teletext mode, and ICs 8 and 9 for the other modes, the main difference being that in these modes the three least significant address bits are produced by the character row address lines from the CRT controller in order to give the bit-mapping of the characters in the RAM memory rather than having the ROM character generator as in the Teletext mode.

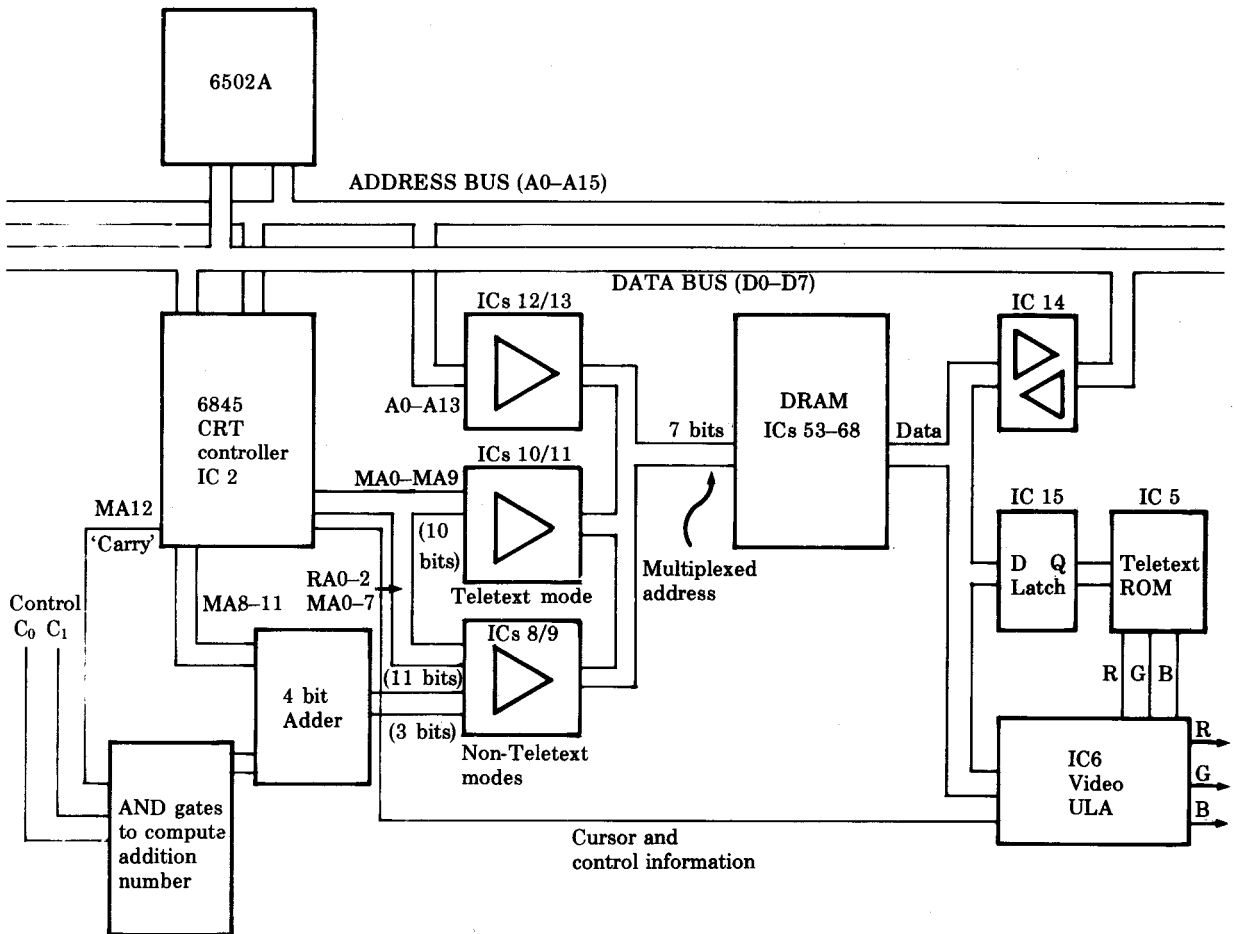


Figure 3 Block diagram of CPU, RAM and CRT controller

The 6502 microprocessor runs from a constant clock and so its requirements for memory access are predictable. Every 250 nanoseconds, control of the RAM address lines is switched between the microprocessor and the CRTC. Thus, in each one microsecond period, the microprocessor has two RAM accesses and the CRTC has two RAM accesses. Because the CRTC generates a sequence of addresses in order to refresh the VDU display, all the row address lines of the RAMs are constantly cycled. The addressing methods have been designed so that in each screen mode the dynamic RAMs are automatically refreshed by virtue of the sequential CRTC accesses.

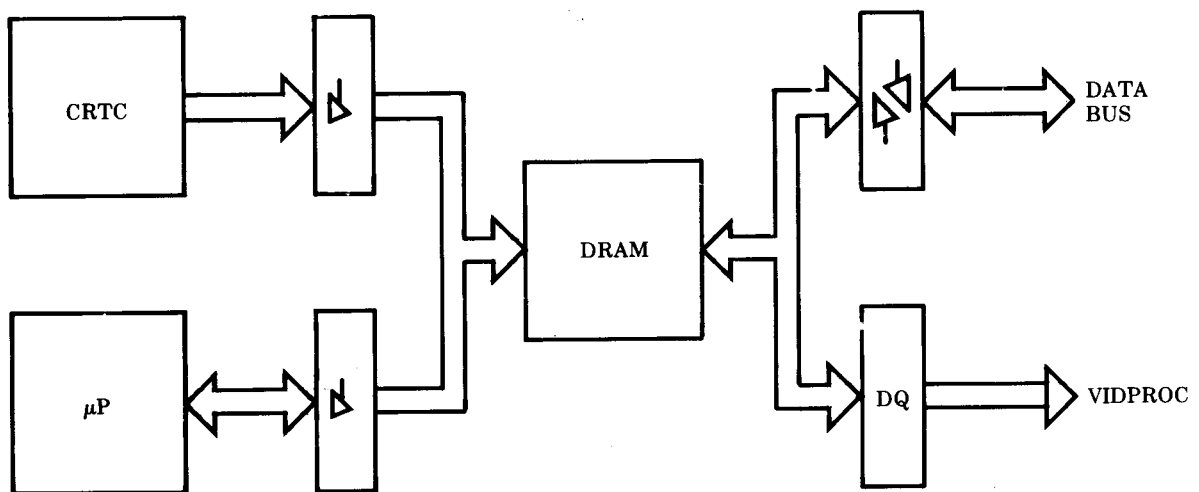
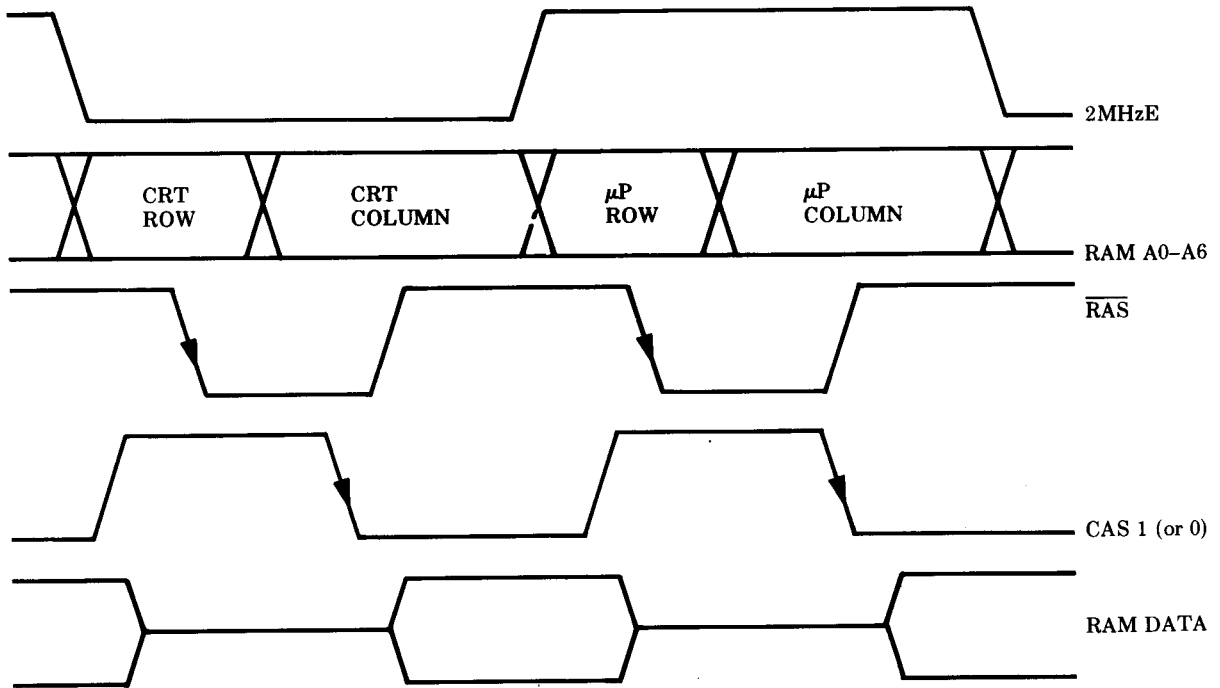


Figure 4 DRAM operation

The row address strobe signal is produced by a D-type flip-flop connected to the 8 and 4 MHz clock signals (half of IC44). This RAS signal then drives all of the dynamic RAMs via R106. The two banks of RAM are enabled by virtue of having their column address strobes individually available. In model A computers, with only one bank of RAM, CAS 1 is used. In the model B, CAS 0 controls the lower 16K and CAS 1 the upper 16K. The second bank of RAMs is selected by a 74LS51 circuit (half of IC28) which controls the ,74S139 (half of IC45) producing the CAS signals. When A14 is high the B input is low thus selecting CAS 1. The other half of IC45 is used to select between the processor and CRT address lines.

Using this technique, two bytes of information are available per microsecond for refreshing the raster scanned video display. With each horizontal line having a period of 64 microseconds, a 40 microseconds active display area is usual. Thus, 640 bits (2 bytes x 8 bits x 40 microseconds) of information per horizontal line are produced from the memory-mapped display. At the end of each 250 nanosecond CRTC access period, the video processor (IC6) latches the byte from the RAM and, according to the display mode in operation, serialises the byte into a single bit stream of 8 bits, or two bit streams of 4 bits or four bit streams of 2 bits. In this way, display modes varying from 640 pixels in 2 logical colours to 160 pixels in 16 logical colours can be produced.

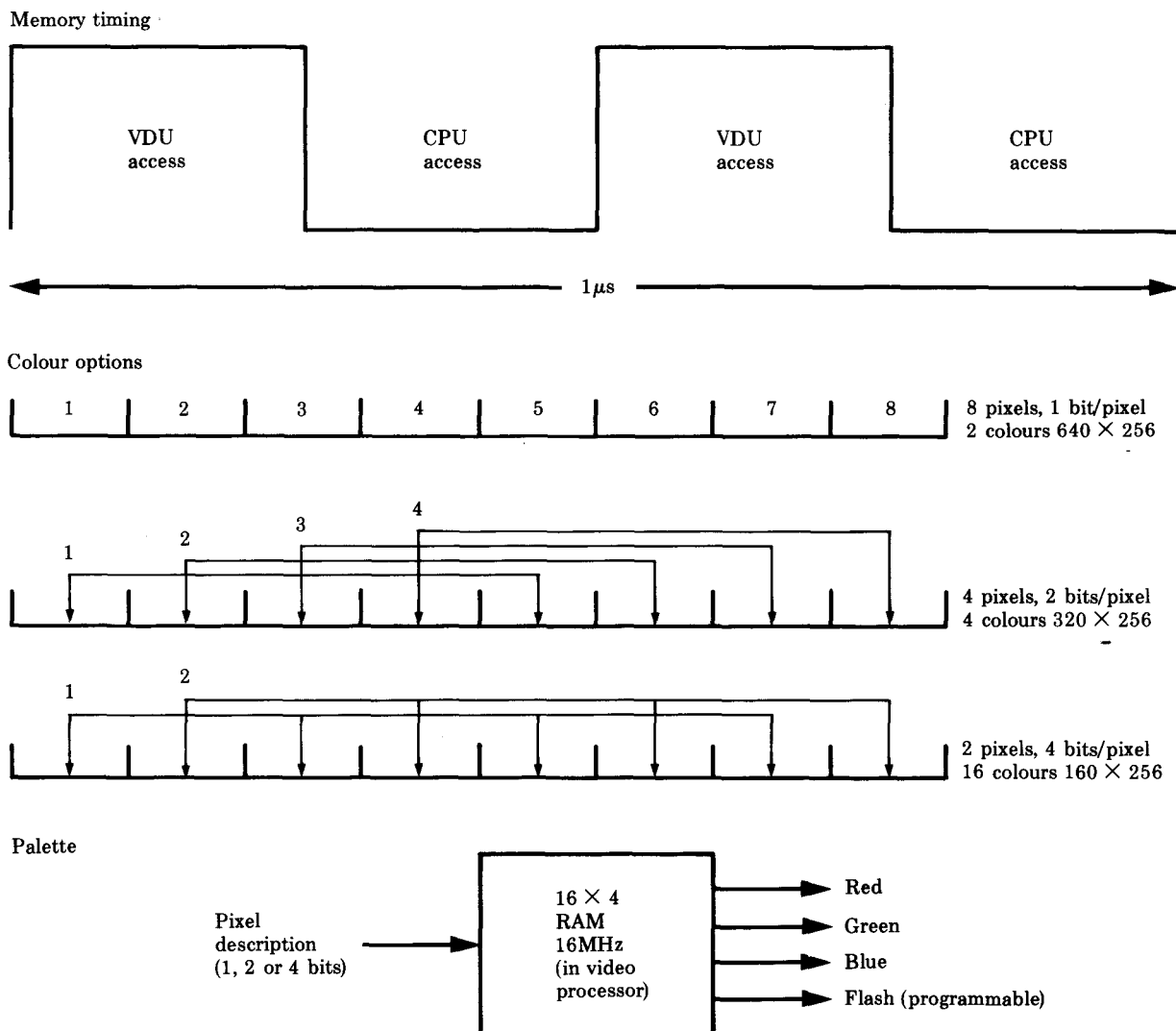


Figure 5 Colour palette operation

The video processor contains a piece of high speed (16MHz) static RAM called a palette. This memory can be programmed to define the relationship between the logical colour number produced by the RAM and the physical colour which will appear on the display. Note that the information in the main RAM is unchanged by changing the palette; it is its interpretation into physical colours which changes. Modes 0 to 6 in the Microcomputer use software generated characters, that is to say, the character font to be produced on the screen is held in the memory-mapped display area of the RAM so that graphics and/or characters may be held. The definition of these characters is stored in the operating system ROM from 0000 to C2FF.

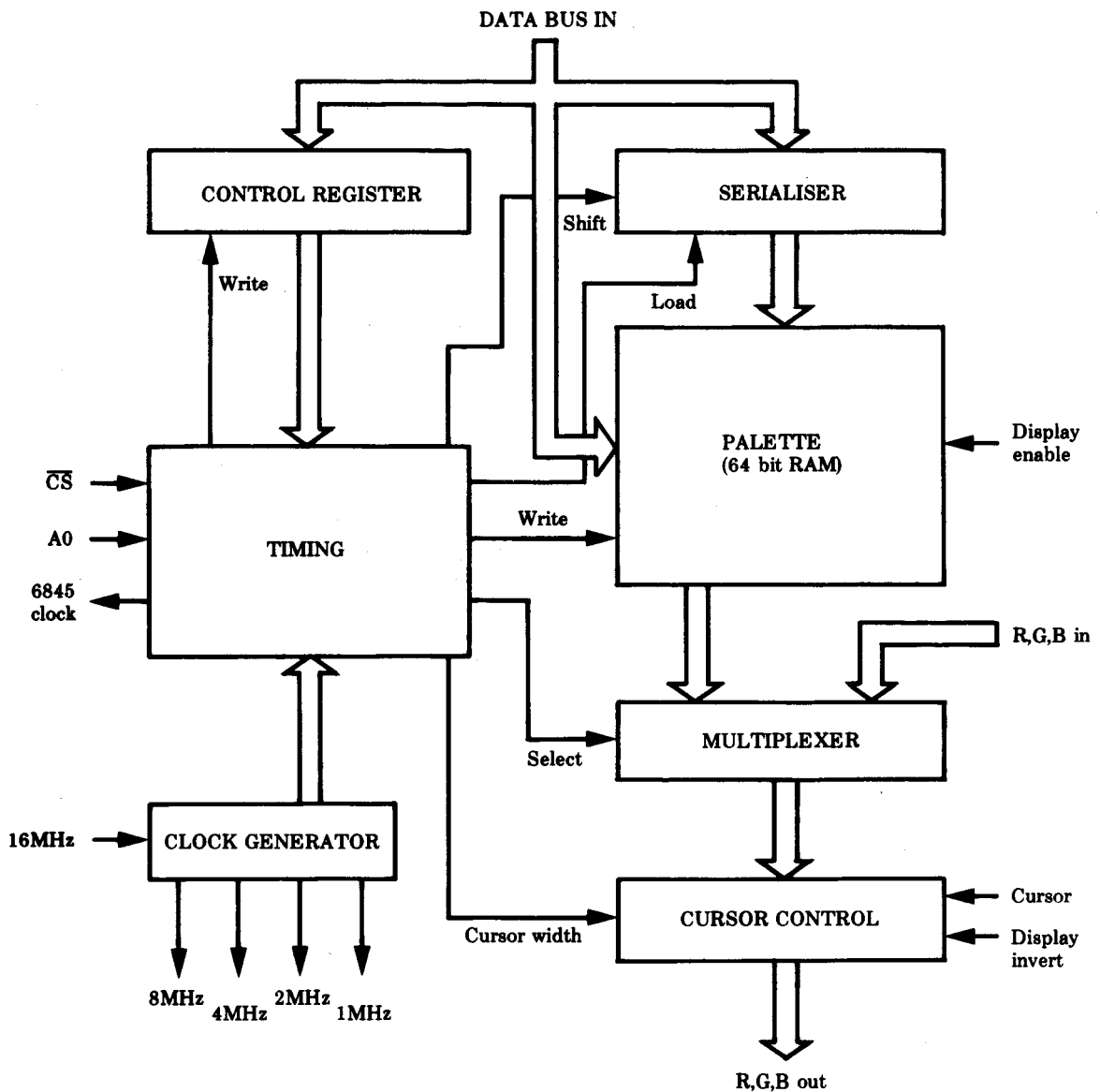


Figure 6 Video ULA block diagram

The speed of printing on the screen is much increased by the use of hardware scrolling. There is a register in the CRTC which is used to define the start of screen address in the screen memory. Thus in order to scroll the screen, it is only necessary to increment this register by the number of characters per line and then write to the memory address where the last screen data was. The number of address lines from the CRTC, used to address the screen memory, has to be sufficient to cater for the biggest screen (20 Kbytes). Thus 14 address lines have to be used which means that when using the hardware scrolling technique, the picture scrolls around in 32 Kbytes. Consider a scroll of 8 Kbytes in a 20 Kbyte screen. The original start of screen for the 20 Kbyte mode was &3000. After an 8 Kbyte scroll, the current start of screen address is &5000 with the end of the screen as seen by the CRTC at &5000 plus 20 Kbytes, which comes to &9FFF, as illustrated below.

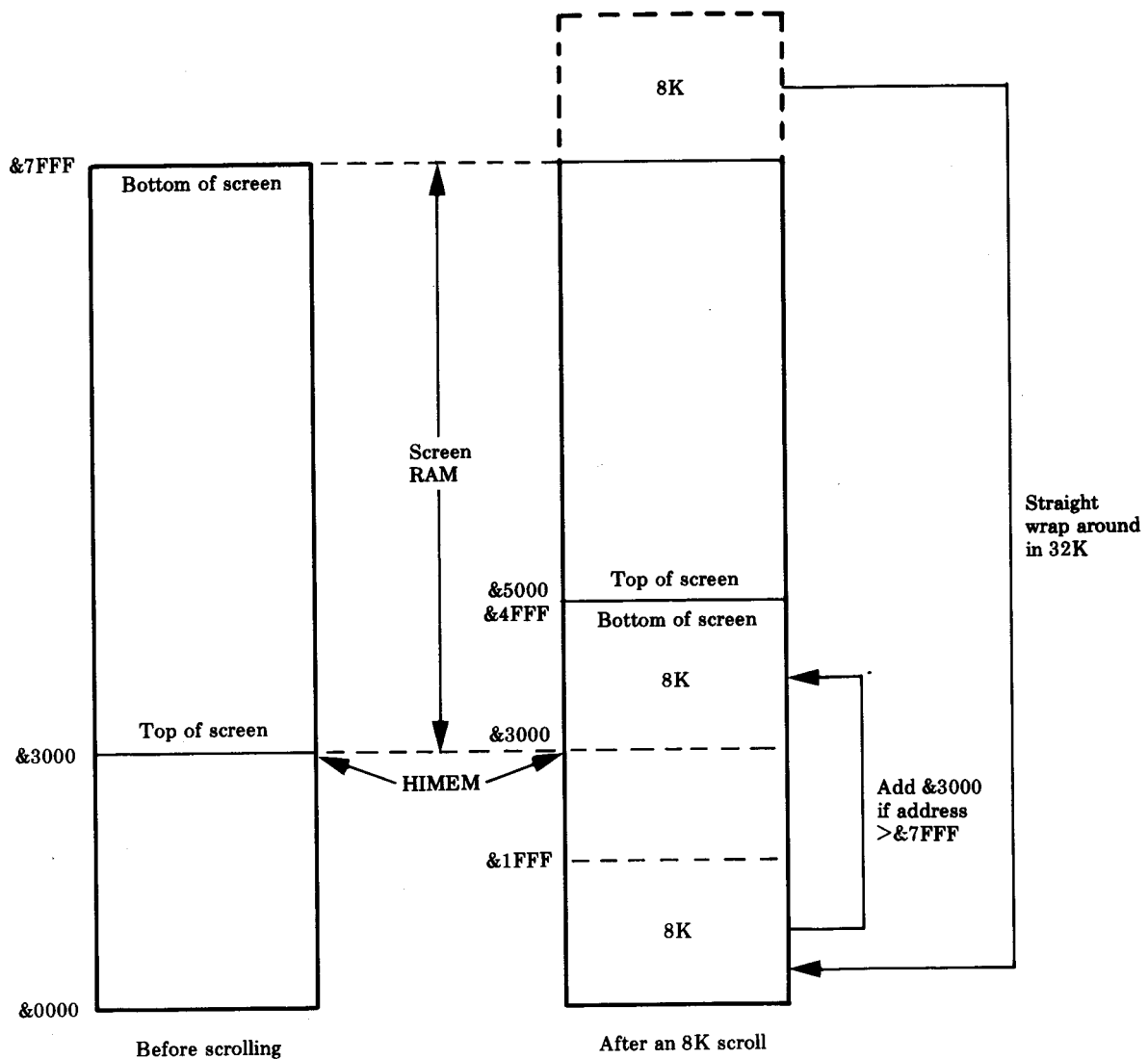


Figure 7 Memory map to show addition of CRTC addresses

Since there is only 32 Kbytes of RAM this would mean that instead of accessing addresses &8000 to &9FFF you would be accessing locations &0000 to &1FFF. Therefore when the address produced by the CRTC is greater than &7FFF (ie MA12 = 1) you have to add to the address from the CRTC, a number which will bring the actual address back up to the area of RAM which is currently being used for the screen ie above HIMEM. Thus for numbers greater than &7FFF you simply add the number &3000 which brings the addresses back to the range &3000 to &4FFF, as illustrated in the diagram above. In the 20K modes you add &3000 (=12K), in the 16K mode you add &4000 (=16K), in the 10K mode you add &5800 (=22K) and in the 8K mode you add &6000 (=24K). This number to be added is defined by the control lines CO and C1 from the 74LS259 (IC32), and computed by some AND gates with the result being added to the higher CRTC refresh address lines by a 74LS283 adder (IC39). The CRTC address line MA12 is used as a "carry" to determine whether zero or the number computed by the AND gates is added to the address lines. (Confusion may arise when looking at IC 9 on the circuit diagram since it looks as if AA0 to AA2 are being buffered to AO to A2. But if you look at the pin numbers and compare them with the other 81LS95's you will see that they are in fact buffered to the top three bits, A4 to A6. MA4 to MA7 are buffered to AO to A3.)

Display mode 7 is a Teletext mode and to implement this an SAA 5050 (IC5) Teletext character generator Read Only Memory is used. IC15 latches the information coming from the RAM prior to the SAA 5050. When using this mode, only 1K of RAM is devoted to the display memory and the characters are held within it as ASCII bytes. The SAA 5050 then translates these bytes into a standard Teletext/Prestel format display.

A 6 MHz clock signal is required for the Teletext character generator (IC5). This signal is produced by knocking a reset flip-flop (two quarters of IC40) backwards and forwards from the 8 MHz and 4 MHz clock signals. The output of this flip-flop is then itself inverted according to the state of the 2 MHz clock signal by an exclusive OR gate (1/4 of IC38). Glitches on this output are removed by R119 and C48 to produce the 6 MHz clock signal at Pin 8 of IC37.

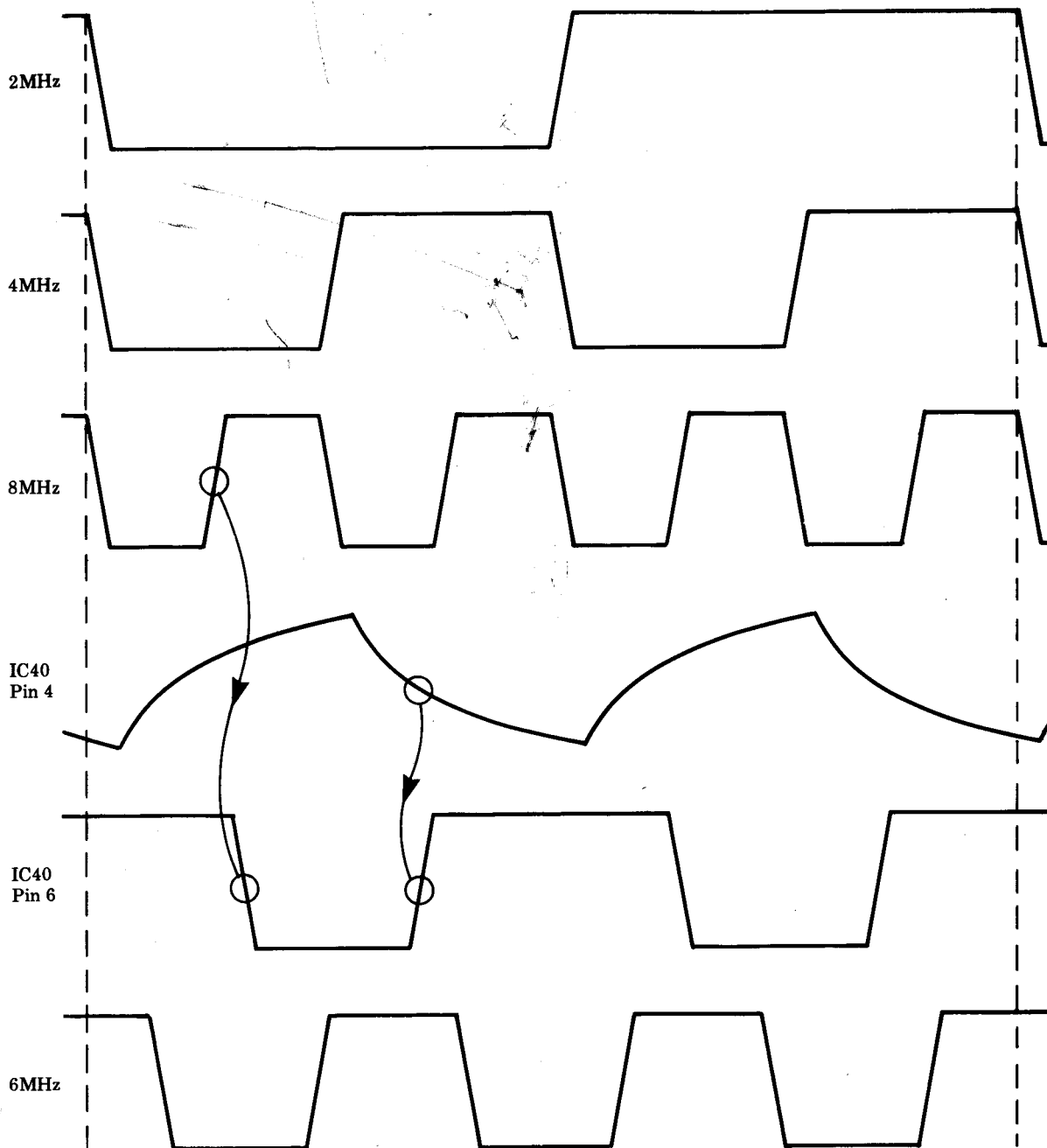


Figure 8 6MHz clock generation

The CRTC is still used to generate the RAM addresses even in the Teletext mode, but using only 1K means that only 10 address lines are needed hence the top four address lines on the 81LS95 (IC11) are tied to logic 1. The Teletext mode is selected by setting the value of video address start (registers 12 and 13 in the CRTC) so high that an extra "carry" is generated on MA13. This is used to enable ICs 10 and 11, disable ICs 8 and 9 and also enable the data latch (IC15).

3.4 RGB + PAL encoder + UHF output _

The red, green and blue logic signals -produced by the -_video processor are buffered by transistors Q4, Q5 and Q6 and fed out together with a composite sync signal to the RGB connector (SK 3). The red, green and blue lines are summed together by binary weighted resistors to feed Q7 which produces a 1V composite video signal suitable for feeding to monochrome monitors, on which the different-colours will appear as different shades of grey. Also available, from the main printed circuit board, is a UHF TV signal on channel 36, suitable for feeding to the aerial input of a domestic television. This output is modulated using a UM1233 for PAL. Colour is provided for domestic televisions by a PAL (phase alternating line) encoder circuit which modulates the colour information on to the colour subcarrier -frequency. Q10 is a 17.73 MHz oscillator circuit which is divided by a ring counter (IC46) giving 2 outputs at the colour subcarrier frequency of 4.433618 MHz. One of these two outputs is switched by the horizontal line frequency in order to produce the alternate phase on each TV line. Thus on IC46 pin 9, we have the 'U' signal and on IC48 pin 11, the '+/-V' signal. A row of exclusive OR gates is used to select different phases of the 'U' and 'V' signals according to whether a red, green, blue, cyan, magenta or yellow colour is to be produced. These signals then drive resistors via a row of NAND gates in order to produce the colour subcarrier signal which is added to the luminance output from Q8 by the buffer Q9. In order for the receiving television to interpret the colour information, a reference colour burst has to be provided at the beginning of each line. A burst gate pulse of approximately 5uS immediately after the horizontal sync pulse for each line is produced at pin 4 of IC41, and it is timed by C45 and R109. This burst gate allows through a standard colour subcarrier signal which the television uses as its reference for the rest of- that line. The PAL signal may be added to the 1V video connector, with the addition of a 470 pF capacitor between the emitter of Q9 and the base of Q7. This is provided as a link selectable option on later issues of the PCB (issue 4 on). In modulated PAL, diodes D20, 21 and 22 increase the luminance of the darker colours, eg blue, in order to make coloured text displays more readable.

3.5 Cassette + RS423 + serial processor

For both the cassette and RS423 interfaces, a 6850 asynchronous communications interface adaptor (ACIA) (IC4) is used to buffer and serialise or deserialise the data. The serial processor (IC7), specifically designed for the BBC Microcomputer, contains two programmable baud rate generators, a cassette data/clock separator, switching to select either RS423 or cassette operations and also a circuit to synthesise a sinewave to be fed out to the cassette recorder. IC42 divides the 16 MHz clock signal by 13 (1.23 MHz) and this signal is divided further (by 1024) within the serial processor to produce the 1200 Hz cassette signal. Automatic motor control of an audio cassette recorder is achieved by using a small relay driven by a transistor (Q3) from the serial processor. The signal coming from the cassette recorder is buffered, filtered and shaped by a three stage amplifier (IC35). The RS423 data in and data out signals and the request to send output (RTS) and clear to send input (CTS) signals are interfaced by ICs 74 and 75 which translate between TTL and standard RS423/232 signal levels (+5V and -5V). The control register, which is memory-mapped at &FE10, specifies the frequencies for the transmit clock (bits 0-2) and the receive clock (bits 3-5) used by the 6850 (IC4). The switching between the cassette and RS423 inputs and outputs

is also determined by the control register (bit 6), and so is the motor control (bit7). R75 and C28 provide the necessary timing elements for delay between receiving the high tone run-in signal and asserting the data carrier detect signal to the ACIA. The value of resistor needed is affected by the output impedance of that pin on the serial processor which has been subject to a certain amount of variation. Thus the value of R75 has changed through the evolution of the circuit.

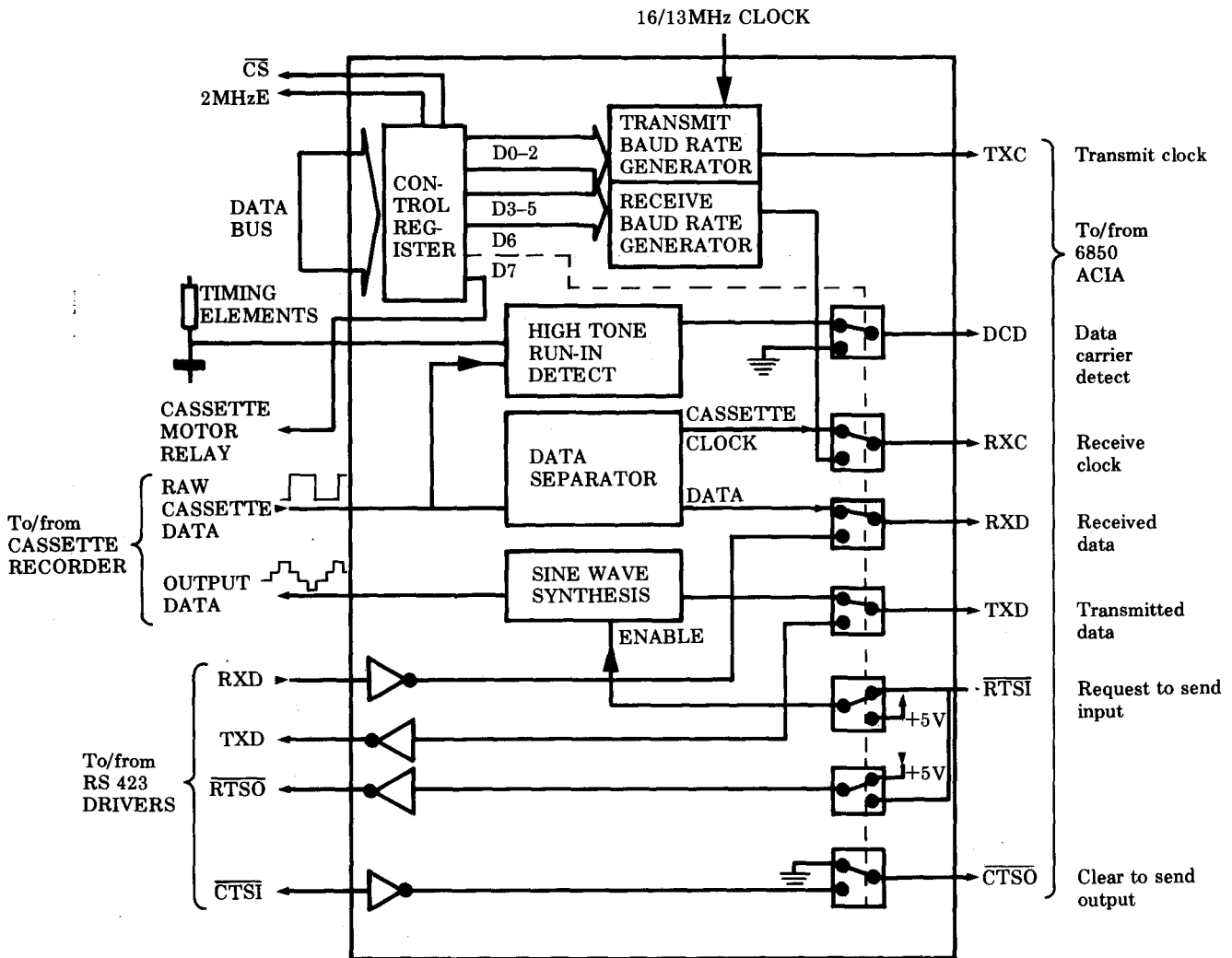


Figure 9 Serial ULA block diagram

3.6 Internal VIA

One 6522 VIA device (IC9) is devoted to internal system operation. Port B drives an addressable latch (IC32) which is used to provide read and write strobe signals for the speech interface, the keyboard and the sound generator chip. Also coming from this latch are control lines CO and C1 which provide the memory address addition for the CRT controller depending on the amount of RAM devoted to the display memory. Pins 6 and 7 of the addressable latch drive the capitals lock and shift lock LEDs on the keyboard. The rest of Port B on the internal system VIA is used to input the two "fire button" signals from the analogue to digital convertor interface and two response lines from the speech interface. Each time the system VIA is written to, any changes on Port B which should affect the addressable latch are strobed into it by a flip-flop (IC31) which is triggered from the 1 MHz clock signal. Port A of this VIA is a slow data bus which connects to the keyboard, the speech system chip and the sound generator.

3.7 Keyboard'

The keyboard circuit (Section 9.5) connects via PL 13. A 1 MHz clock signal is fed to a 74LS163 binary counter, the outputs of which are decoded by a 7445 decoder driver circuit. These outputs drive the rows of the keyboard matrix, each row being driven in turn. If any key is depressed, the 74LS30 gate will produce an output when that row is strobed and this will interrupt the computer through line CA 2 of IC3. On this interrupt, the computer will enter the key reading software. In order to discover which key was pressed, the microprocessor loads directly into the 74LS163 the address of each key matrix row allowing it to interrogate each row in turn. Also, the microprocessor loads into a 74LS251 data selector, the address of each specific key on that row. ie column addresses. In this way, the microprocessor can interrogate each individual key in turn until it discovers which one was depressed and causing the interrupt. Once read, the keyboard assumes its free running mode.

3.8 Sound + speech + serial ROM interfaces

The speech system device used is a TMS 5220 (IC99) which, on instructions from the Microprocessor, will either produce at its audio output speech from its associated memory (IC98) or from speech data fed to it directly from the Microcomputer's memory. On later issue boards a variable resistor is provided (VR 2) to adjust the clock frequency to give the best effect of the speech. IC18 is a four channel sound generator chip which may be programmed to give varying frequency and varying attenuation on each channel. The audio output of the speech system device is filtered by an operational amplifier circuit with a cut-off frequency of 7 kHz. This signal is then added to an amplified and level shifted signal from the sound generator by a virtual earth amplifier to which is also added an extra analogue input from the 1 MHz extension bus. This summated audio signal is then finally filtered by an 8 kHz low pass filter. All of these operations are done by a quad operational amplifier (IC17). IC19 provides audio power amplification to drive a speaker from PL15. A low level audio output is provided from PL16 for feeding the auxiliary input of an external power amplifier.

3.9 A to D convertors

A four channel analogue to digital convertor facility is provided by IC73. This device connects straight to the Microcomputer's data bus and is a dual slope -convertor with its voltage reference being provided by the three diodes, D6, D7 and D8. Each time a conversion is completed, the microprocessor is interrupted through CB1 of the internal VIA which responds by reading the value and storing it in a memory location.

3.10 Disc interface

IC78 is a floppy disc controller circuit which is used to interface to one or two, single or double sided 5 1/4 inch floppy disc drives. Logic signals from the controller to the disc drive are buffered by two open collector driver packages IC79 and 80. The incoming signal from the disc drive is first conditioned by monostable IC87 producing a pulse train with each pulse of fixed width. These pulses are then fed to the data separation circuits ICs 81 and 82. These form a digital monostable. IC86 divides the 8 MHz clock signal down to 31.25 kHz. ICs 83, 84 and 85 are then used to detect index pulses coming in from the drive which show that the drive is ready for a read or write operation.

3.11 Printer + user port interfaces

1069 is a versatile interface adaptor. Port A is used to provide a centronics standard parallel printer interface, with an octal buffer, IC70, to improve on the current driving capabilities of the data lines. Control line CA2 is used as the strobe line having been buffered by part of IC27 and Q11. It is asserted low for approximately 5uS to signal that the data is ready. This circuit has been changed on the various issues of the PCB as explained in section 4.4.

Port B is left uncommitted and is free for user applications as either input or output. For full details of what can be done with the user port you should refer to the 6522 data sheet, but basically, apart from being used as a straightforward input/output port, PB7 can be used as a programmable pulse output using one of the timers, PB6 can be used as an input to the other timer for pulse counting, and CB1 and CB2 can be used for automatic hand-shaking and in conjunction with the VIA's own shift register.

3.12 Econet

ICs 89 to 96 are concerned with the Econet interface. IC89 is an Advanced Data Link Controller Circuit, type 6854 which handles the Econet protocol. Data to be transmitted on to the network is fed from the ADLC to the line drive circuit (IC93) via an inverting Schmitt trigger circuit (part of IC91). Transmit data then goes through the line driver circuit which produces a differential signal drive to the Econet cables. Received data is detected and converted to a logic signal by one half of IC94 which is a dual comparator circuit, type LM319. The received data is then fed back to the data link controller circuit.

An Econet installation has a single master clock station which provides the clock for the whole of the network. This clock signal is transmitted around the network as a second differential line signal and it is used to clock the data in and out of the data link controller circuits. The network clock is detected using the other half of IC94, and the detected clock signal is then fed to both receive clock and transmit clock inputs on the 6854. In the presence of a network clock, the monostable circuit (IC87) is permanently triggered and thus providing a data carrier detect signal for the data link controller chip. Once the network clock is removed, the monostable immediately drops out and the data carrier is no longer detected.

The Econet is a broadcast system on which a number of stations may attempt to transmit their data over the network at any given time. In this case, a situation called a collision can occur and then the transmitting stations should detect the collision and back off before trying again to transmit over the network. Collision arbitration software is included in the Econet system and is based on the station ID number. Collisions on the network data lines result in the differential signal on the two data wires being reduced and this condition is detected by IC95 which is another dual comparator circuit. When there is a good differential data signal on the network one output of IC95 or the other will be low, in which case the output of IC91 pin 6 will be high, indicating no collision. When there are no collisions on the network, and the network clock is detected by the clock monostable, the data link controller is clear to send data over the network. When there is a collision on the network both outputs of IC95 will go high and the clear to send condition will cease. Note that when the computer is not connected to the network a collision-like situation results, in which case again the data link controller will not get a clear to send condition.

Up to 254 stations may be connected to each Econet with each station being identified by a unique station identification number. This station ID is programmed on the links S11 and the ID can then be read by the octal buffer IC96. The data link controller circuit produces interrupts which are fed to the processor's NMI line. These interrupts can be enabled and disabled under software control by using the address-decoded signals, INTOFF which is achieved by reading the station ID at &FE18, and INTON which is generated by reading &FE20. (Writing &FE20 loads the Video processor register.)

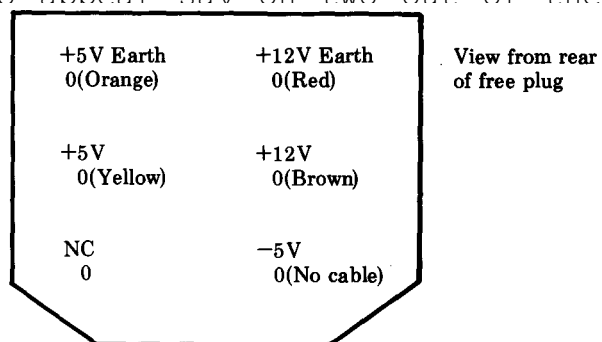
3.13 1 MHz bus

The address and data lines, A0 - A7 and D0 - D7, together with two page select lines are available as the 1 MHz extension bus to which various peripheral devices may be connected, eg Teletext interface. All accesses to this bus will be at a 1 MHz processor speed, although links are, provided to increase this to 2 MHz if desired (see the selection link survey). The octal buffer (IC71) and the octal transceiver (IC72) are used to interface these signals to the internal data and address buses, IC72 being enabled only when either "FRED" or "JIM" is accessed (pages &FC00 and &FD00).

3.14 Power supply

The power supply unit produces 5 volts at 3.75 amps and -5 volts at 100 milliamps for use on the main circuit board. Some auxiliary power for accessories is also available on an external connector and this includes +12 volts at 1.25 amps, but the amount of power available depends on what hardware is connected internally - Econet, disc interface, sideways ROMs etc.

The power supply connects to the main circuit board by seven push-on connectors with the +5 volts being fed to three different points across the main circuit board. These points are all connected together electrically. However, by distributing the power in this way the need for very large copper tracks to distribute power around the board is avoided. Most computers in production will have a switched-mode power supply, the circuit diagram for which is given. However it is not recommended that attempts should be made to repair this power supply, instead it should be treated as a module to be exchanged. This is because of the stringent safety regulations relating to such units. A small number of early computers have a linear power supply unit with a conventional mains transformer and regulator circuit. These also should be treated as modules to be exchanged rather than serviced, though it should be noted that the three outputs are from separate regulators, thus it is possible for power to appear say on two out of the three



Supplies: +5V @ 1.25A
+12V @ 1.25A
-5V @ 75mA

Mating connector is AMP housing 1-350234-9
+ male pins 350-664-1

Figure 10 BBC auxiliary PSU outputs

4 Upgrading the PCB

In these instructions about how to add extra hardware to the PCB for disc, Econet, speech etc, some differences may occur depending on which hardware is already fitted. This is made clear within each set of instructions. In order to locate the positions of various of the selection links, reference should be made to section 5.2 which gives the X-Y coordinates of each link. Dealers and service centres performing these upgrades must also conform to upgrade procedures and requirements as notified by their supplier, and should refer to any available information updates for latest details.

4.1 Modification A

Convert from EPROM MOS to ROM MOS

- i) Remove the four MOS EPROMs from their sockets IC52, IC88, IC100 and IC101.
- ii) Remove the BASIC ROM from the IC51 socket and replace it in the IC52 socket.
- iii) Insert the MOS ROM into the IC51 socket.
- iv) Set the following link positions using MOLEX jumpers (if fitted or, tinned copper wire):-

S18 - North
S19 - East
S20 - North
S21 - 2 x East/West
S22 - North
S32 - West
S33 - West

- v) Test using a FIT and, if available, a PET (see section 6.2).

4.2 Modification B

Convert Model A to Model B

- i) The following parts are required:-
 - 8 off 4816AP-3 IC61 to 68
 - 1 off 6522 IC69
 - 2 off 74LS244 IC70, 71
 - 1 off 74LS245 IC72
 - 1 off uPD7002 IC73
 - 1 off 88LS120 IC74
 - 1 off DS3691 IC75
 - 1 off 74LS163 IC76
 - 1 off 74LS00 IC77
 - 1 off 6-pin DIN socket MAB6H SK3
 - 1 off 5-pin DIN socket MAB5WH SK4
 - 1 off 15-way D-type socket 164801-1 SK6
 - 2 off 34-way header 3431-1302 PL8, PL11
 - 1 off 26-way header 3429-1302 PL9
 - 1 off 20-way header 3428-1302 PL10
 - 1 off 40-way header 3432-1302 PL12

ii) Insert the above ICs into the sockets provided on the main circuit board. Solder the connectors on to the printed circuit board.

iii) Cut the wire links at link positions S12 and S13. Move the MOLEX link at position S25 from South to North.

iv) On issue 1, 2 or 3 circuit boards only, add a 2k2 ohm resistor between PL9 pin 1 and +5v on the solder side of the circuit board using a resistor with sleeved leads. +5v is available at IC85, pin 16 (33 mm due North of pin 1).

v) On issue 1, 2 or 3 circuit boards only, cut the track connected to PL9 pin 23 (this may have previously been cut), then link IC69 pin 40 to PL9 pin 19. This modification may have been made, and, if so, a check should be made to ensure that it has been correctly performed.

vi) On issue 1 and 2 circuit boards only, PL9 pin 26 should be cut out of the header. Care should be taken to ensure that the pin is cut right back so that no connection can be made to it.

vii) On issue 1 and 2 circuit boards only, a BC239 transistor should be added in place of link S1 as follows:- Cut the track between the centre and South pins of S1 on the solder side of the circuit board. Cut the two tracks connected to the North pin of S1 on the solder side of the circuit board, then reconnect the ends of these tracks leaving the North pin isolated. Insert a BC239 transistor into the S1 position with the base in the South pin, the emitter in the North pin, and the collector in the centre pin. Finally, link the North pin of S1 to IC27 pin 7 with a short length of insulated wire.

viii) On issue 1 or 2 circuit boards only, add a 4k7 ohm resistor (R162) between the existing two holes located approximately 5 mm East of IC70 pins 11 and 13, as shown below.

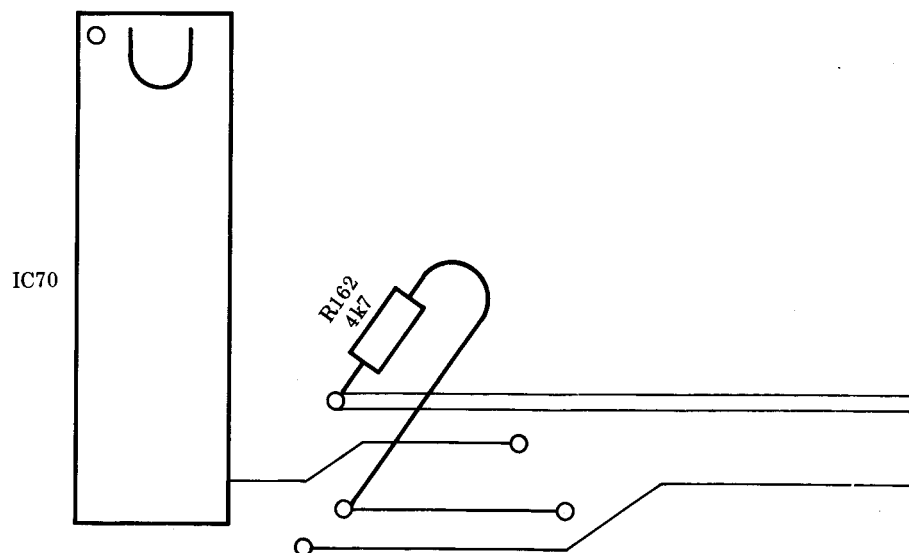


Figure 11 Adding R162 on issues 1 and 2 of PCB

ix) On issue 1 circuit boards only, disconnect the LPSTB signal between IC69 pin 18 and PL10 pin 2 by cutting the track on the solder side of the circuit board which is connected to IC69 pin 18.

x) Test using a FIT and, if available, a PET.

4.3 Modification C

Add Speech Option

i) The following components are required:-

1 off Integrated Circuit TMS6100	IC98
1 off Integrated Circuit TMS5220	IC99

ii) On issues 2 and 3, the following modifications are needed.

On the component side of the main PCB:

- Cut the track between IC3 pin 16 and the through-hole 8mm to the west.
- Cut the track between IC3 pin 17 and the through-hole 10mm to the west.

On the solder side of the PCB:

- Link the through-hole 10mm to the west of IC3 pin 17 to IC3 pin 16
- Link the through-hole 8mm to the west of IC3 pin 16 to IC3 pin 17.

(These operations switch the signal lines to IC3 pins 16 and 17.)

Then, also on the solder side of the PCB:

- Cut the track between IC98 pins 13 and 14.
- Link IC98 pin 13 to PL14 pin 3 (0 volts).

iii) Issue 1 keyboard PCBs also need modifying as follows:-

On the solder side of the PCB, cut the track between pins 14 and 15 of the edgcard connector. The pins are those furthest from the speaker. (ie further east).

On the solder side of the PCB, link pin 14 of the edgcard connector to 0 volts. This can be found on either of the capacitor legs nearer the centre of the PCB.

iv) When the modifications are complete, procede as follows:-

Reconnect the keyboard to the main PCB. Add the new connector for PL14, then, with the computer turned off, test for continuity between the following points:

Edge connector pin number |6|7|8|9|10|11|12|13|14|15|

IC98 pin number |1|3|4|5| 6| 7|10|11|13|14|

Note: On the edge connector, pin 1 is nearest the speaker, thus the polarising key is pin 3 and pins 4 and 5 are "empty".

Also check that there are no short-circuits between any of the edge connector pins. Repeat the tests for the other edge connector.

v) Insert ICs 98 and 99, turn the machine on and type:

```
REPEAT SOUND-1,GET,0,0:UNTIL0 <RETURN>
```

Now press any alphanumeric key and you should hear the voice synthesis operating. If the pitch is wrong, follow the instructions in vi) below.

If there is no speech, double check the modifications and try again.

vi) The pitch of the speech must be set. From Issue 4 PCBs onwards this is a simple matter of adjusting VR2 which is situated just west of IC98. On Issue 1, 2 and 3 PCBs, the resistor R32 (between ICs 98 and 99) may need to be changed to achieve the best result. The method for setting the pitch is to connect a frequency meter to pin 3 of IC99 and to adjust VR2 until the meter reads 160 kHz (+ or - 100 Hz), or as close as is obtainable by changing R32.

vii) Reassemble the machine. Before fitting the ROM socket cover into the

the case lid, remove the rforated section of the black label above the ROM sockets. It may be necessary to trim the label to match the case cutout. For early version cases (without a rib on the underside behind the keyboard cutout), remove the two small lugs on the ROM socket cover before fitting.

viii) Test using a FIT and, if available, a PET.

4.4 Modification D

Add 5 1/4 inch Disc Interface to Basic Model B

i) The following parts are required:-

1 off 8271 IC78
2 off 7438 ICs 79,80
1 off 74LS10 IC82
2 off 74LS393 ICs 81,86
2 off CD4013B ICs 83,84
1 off CD4020B IC85
1 off 74LS123 IC87 (Not required if Econet already fitted)
1 off 2764 EPROM (DFS) IC88 (or IC100 if Econet fitted; but not required if DNFS already fitted)

ii) Insert the ICs listed above into the sockets provided on the main circuit board.

iii) On issue 1 or 2 circuit boards only, connect the two pads of link position S8 with a wire link.

- iv) If the MOS ROM version 0.1 is fitted in position IC51 then it must be replaced by a 1.2 MOS, see modification A.
- v) If the existing power supply does not incorporate an auxiliary power output socket it must be exchanged for a suitable unit (eg ASTEC type).
- vi) On issue 1, 2 or 3 circuit boards only, cut the leg of IC27 pin 9 as close to the PCB as possible and the track connected to it on the component side of the circuit board between IC27 and IC89, then reconnect the cut IC leg to the East pad of link S9 with a short Length of insulated wire.
- vii) On issue 4 boards onwards, cut the TCW link at position S9.
- viii) Set the following link positions using MOLEX jumpers:-
 - S18-North
 - S19-East
 - S20-North
 - S21-2 x East/West
 - S22-North
 - S32-West
 - S33-West
- ix) Test using a FIT and, if available, a PET.

4.5 Modification E

Add Econet Interface to Model A

- i) The following parts are required:-

- 5 off 14-pin DIL IC sockets
- 1 off 20-pin DIL IC sockets
- 1 off 28-pin DIL IC sockets
- 1 off 74LS163 IC76 (already fitted on model B)
- 1 off 74LS123 IC87 (Not required if disc already fitted)
- 1 off 68B54 IC89
- 1 off 74LS132 IC91
- 1 off 75159 IC93
- 2 off LM319 ICs 94,95
- 1 off 74LS244 IC96
- 1 off 74LS74 IC97

- 1 off 10uF Tantalum Capacitor C18
- 1 off 10uF Ceramic Capacitor C23

- 1 off 5-pin 180 degree DIN socket SK7
- 1 off 8X22K SIL resistor pack RP2
- 1 off 2764 EPROM with NFS IC88 (not required if DNFS already fitted)
- 2 off Rows of 8 MOLEX pins S11

- 20 off 2% tolerance 1/4W resistors as follows:-

- R34-10k R40-100k R48-1k R62-56k
- R35-10k R41-100k R51-10k R63-56k
- R64-1M5 R44-1M5 R52-1k0
- R36-1M5 R45-10k R59-56k
- R38-100k R46-1k0 R60-56k

R39-100k R47-1k5 R61-1k0

- ii) Solder all of the above passive components onto the main PCB.
- iii) Insert all of the above integrated circuits into their sockets.
- iv) Cut the wire links at link positions S2, S12 and S13. (S12 and S13 should already have been cut on Model B's)

v) Set the following link positions using MOLEX jumpers:-

S18-North
S19-East
S20-North
S21-2 x East/West
S22-North
S32-West
S33-West

vi) On issue 1, 2 or 3 boards only, the following modifications are required:

Remove the capacitor C17 and replace it with a 2.2nF capacitor. Cut the PCB track from IC26 pin 6 to IC96 pins 1 and 19 leaving the track from IC26 pin 6 to IC97 pin 2 intact. Cut the track from IC89 pin 26 to IC97 pin 4 and link IC26 pin 9 to IC96 pins 1 and 19 and also to IC97 pin 4.

vii) Test using a FIT and, if available, a PET.

4.6 Modification F

Add 8 inch disc interface to Model B

(As Modification D - Add 5 1/4 inch disc interface, but add....)

x) Set the following link positions by cutting the indicated PCB track and inserting a wire link.

LINK CUT TRACK	WIRE LINK.
S4 East (Solder side)	West
S10 West (Component side)	East
S27 West (Solder side)	East

4.7 Partial upgrading

If you want to upgrade a Model A to enable it to run software intended for use with a model B, but do not want all the various interfacing facilities, then it is only really necessary to add the RAM and the 6522 VIA and change link 525. The VIA is needed as some professional software uses its hardware timers.

If you want to use sideways ROMs then you will need to add the 74LS163 (IC76) and be sure that links S12 and S13 are cut.

5 Selection links and circuit changes

5.1 Selection Link Survey

Here is a survey of the options which may be selected on the Microcomputer by selection links S1 to S39. These links may take the form of tracks on the circuit board which can be cut, soldered wire links, or shorting jumpers, plugging on to the rows of pins. This is followed by a tabular survey of the options selected in production on a standard model B Microcomputer.

Option Select Links are as follows:-

1. Used only on issue 4 and succeeding boards to select printer strobe or direct output from CA2.

2. OPEN enables ECONET NMI
CLOSED disables ECONET NMI

- Do not fit this link with IC91 in place.

3. Clock base frequency selection for ECONET
Not used after issue 3.

4. EAST selects 5 1/4" disc
WEST selects 8" disc.

- This changes the pin connection of the "side select" line on the disc interface.

5. NORTH enables ECONET clock
SOUTH disables ECONET clock.

- Not used after issue 3.

6. NORTH divides ECONET clock by 2
SOUTH divides ECONET clock, by 4.

- Not used after issue 3.

7. WEST applies 4-5v to pin 30 of disc controller (IC78).
EAST applies 0v to pin 30 of disc controller.

- Readable by software, bit 0 of the result register of the 8271. Not used.

8. CLOSED links disc head load signal to PL8.
OPEN isolates disc head load signal from PL8.

9. CLOSED disables DISC NMI.
OPEN enables DISC NMI.

Do not fit IC78 with this link closed. Due to PCB faults, various different modifications are necessary with different issue boards in order to use the disc interface. (See section 4, modification D.)

10. WEST selects 5 1/4" disc.
EAST selects 8" disc.

- Changes the pin connection of the "index" line on the disc interface.

11. Selects Econet station ID. (NORTH is LSB)

- See Econet upgrade instructions - section 4, modification E.

12. CLOSED ties ROM select line A to 0V.
OPEN ROM select line A driven by IC76.

- On model A's, IC76 is not fitted because sideways ROM'S are not used. ROM 0 (IC52) is permanently selected. Do not fit IC76 with this link closed.

13. CLOSED ties ROM select line B to 0V at IC20.
OPEN ROM select line B driven by IC76.

- Do not fit IC76 with this link closed. See comments on link 12.

14. CLOSED disables ROM output from page FD, enables JIM.
OPEN enables ROM output from page FD, disables JIM.

- If link 14 is open then link 15 must be closed and R72 must be fitted. The purpose of this link was to provide access to an extra page of the OS ROM for development purposes. It is unlikely to be used in production machines as it disables the 1MHz bus.

15. CLOSED disables fast access to page FD via IC23.
OPEN enables fast access to page FD via IC23.

- Link 15 must be closed if link 14 is open and R72 must be fitted. See comments on link 14.

16. CLOSED disables fast access to page FC via IC23.
OPEN enables fast access to page FC via IC23.

- Link 16 must be closed if link 17 is open and R73 must be fitted. See comments on link 14.

17. CLOSED disables ROM output from page FC, enables FRED.
OPEN enables ROM output from page FC, disables FRED.

- If link 17 is open then link 16 must be closed and R73 must be fitted. See comments on link 14.

18. SOUTH forces slow access to IC100 ROM.
NORTH allows fast access to IC100 ROM.

- To allow the use of 1MHz EPROMs.

19. WEST forces slow access to ROMs IC52, IC88 and IC101.
EAST allows fast access to ROMs IC52, IC88 and IC101.
- Diodes D10, D11 and D12 may be selectively added to slow down ROMs IC101, IC88 and IC52 respectively when link 19 is in WEST position, but for any ICs to have slow access, R55 must be added.
D10, 11 & 12 and R55 are not fitted from issue 7 onwards.
20. SOUTH connects high ROM select bit to IC20 decoder from A 13.
NORTH connects high ROM select bit to IC20 decoder from ROMSEL 1.
21. 2 x NORTH/SOUTH selects blocks 8 to B in IC51 and blocks C to F in ICs 52, 88, 100, and 101. (4 EPROMs for OS)
2 x EAST/WEST selects blocks C to F in IC51 and blocks 8 to B in ICs 52, 88, 100 and 101. (OS in IC51)
22. SOUTH connects low ROM select bit to IC20 decoder from A 12 .
NORTH connects low ROM select bit to IC20 decoder from ROMSEL 0.
23. OPEN RS 423 receiver not terminated (DATA).
CLOSED RS 423 receiver terminated (DATA).
24. OPEN RS 423 receiver not terminated (CTS).
CLOSED RS 423 receiver terminated (CTS).
25. SOUTH selects CAS 1 only, for 16K RAM configuration.
NORTH selects CAS 0 and 1 for 32K RAM configuration.
- If removed altogether, this selects CAS 0 only, but this should only be used for testing purposes on a Model B.
26. WEST selects normal video output.
EAST selects inverted video output.
27. WEST selects 8 MHz clock for 5 1/4" disc.
EAST selects 16 MHz clock for 8" disc.
28. WEST selects base baud rate. (1200 baud)
EAST selects 1300 baud cassette rate.
- If link 28 EAST position RS 423 baud rate is also changed by the same factor:- 13/12.
29. EAST selects base baud rate. (1200 baud)
WEST selects 1300 baud cassette rate.
- If link 28 is in the WEST position, RS 423 baud rates are also affected.
- 30o increase the flexibility used for the addition of extra sideways ROM sockets. This would be in connecton with other links (S20,21,22) to enable a total of 16 sideways ROMS to be selected.
31. WEST selects +ve CSYNC to RGB video output.
EAST selects -ve CSYNC to RGB video output.

32. WEST selects A 13 input to pin 26 of ROMs IC52 and IC88.
EAST selects +5v input to pin 26 of ROMs IC52 and IC88.

- This enables 24 pin ROMs to be used in the 28 pin socket.

33. WEST selects A 13 input to pin 26 of ROMs IC100 and IC101.
EAST selects +5v input to pin 26 of ROMs IC100 and IC101.

- This enables 24 pin ROMs to be used in the 28 pin socket.

34-38. These are used to provide contact with the ROM decoder (IC20) and the chip select lines of ROMs 52, 88, 100 and 101, in order to allow the use of extra ROM sockets on an external PCB. (Implemented from issue 4.)

39. CLOSED adds colour burst signal to the black and white video signal to produce PAL encoded video on the BNC socket.

OPEN Black and white video on BNC socket. (Implemented from issue 4.)

5.2 Table of link options.

The following table gives a list of selection links showing their positions on the circuit board (mm E,N from SW corner) and on the circuit diagram (grid reference, see main PCB circuit diagram). The links made in production on a standard model B without disc or Econet interfaces are also given.

P = pluggable link, T = track, W = wire link, C = closed, 0 = open.
N S E and W refer to orientation of tracks or plugs.

Some links have been omitted on later issue boards, whilst others have been added.

LINK	PCB position	Circuit diagram	Options (Model B)
1.	2,1082,5	T N	(Not used on issues 2 and 3)
2.	2,16112,7	W C	
3.	2,17314,14-	- -	(Not fitted after issue 4)
4.	12, 12	1,9	T E
5.	26,195	14,9	- - (Not fitted after issue 4)
6.	26,205	15,9	- - (Not fitted after issue 4)
7.	30, 65	4,9	T E
8.	32, 15	2,9	T C
9.	35,128	3,10	W C
10.	45, 15	1,8	T W
11.	75,210	13,10	P - (When Econet fitted)
12.	97, 70	9,8	W 0 (Wire link in Model A)
13.	100, 67	9,8	W 0 (Wire link in Model A)
14.	101, 53	7,10	T C
15.	107, 97	7,9	T C
16.	108, 90	7,9	T C
17.	108, 52	7,10	T C
18.	110, 52	7,8	P N
19.	102,102	7,8	P E
20.	123, 55	9,8	P N
21.	122, 65	9,8	P 2 x EW
22.	127, 70	9,8	P N
23.	177,215	13,3	W 0
24.	181,195	13,3	W 0
25.	215,185	7,5	P N
26.	221, 68	10,1	P W
27.	226, 95	1,7	T W
28.	237,144	12,6	T W
29.	237,146	12,6	T E
30.	284, 20	8,8	- - (For external connections)
31.	270,170	14,3	P W
32.	295, 65	9,9	P W
33.	295, 67	10,9	P W
34.	200, 65	9,8	T C (From issue 4 onwards)
35.	245, 20	9,8	T C (From issue 4 onwards)
36.	260, 20	9,8	T C (From issue 4 onwards)
37.	280, 20	9,8	T C (From issue 4 onwards)
38.	300, 15	9,8	T C (From issue 4 onwards)
39.	255,215	9,8	T 0 (From issue 4 onwards)

5.3 Circuit Modifications from issue 1 to issue 7.

In this next section are listed the more important changes which have taken place in the circuit design as it has evolved from issue 1 to issue 7. Since there are so few issue 1 boards in circulation at the moment, we will ignore the changes from 1 to 2 and suggest that if you come across an issue 1 board and cannot solve any fault which occurs on it, that you should consult the Technical Services Department of Acorn Computers Ltd.

5.3.1 Changes from issue 2 to 3.

1. The ACK line on PL9, the printer port, was moved from pin 23 to pin 19.
2. A 4k7 resistor (R162) was added to the ACK line to pull it up to +5v.
3. Link S1 was removed in order to put in a transistor inverter, Q11.
4. Pin 26 of PL9 was left unconnected to avoid the problem that this pin is used on some printers as the reset line.
(Changes 1-4 were made retrospectively on most of the issue 1 and 2 circuit boards).
5. Various modifications were made in the region of S9 and IC27 at various stages, and so for the correct implementation, see section 4 on the modification for adding the disc interface.
6. A 2k2 pull up resistor (R170) was added to the strobe line of the printer port (pin 1 of PL9).
7. R109 became select on test (SOT) with a value between 1k8 and 2k7 in order to set the correct colour burst length.
8. C51 also became SOT at a value between 15pF and 22pF in order to set the colour burst frequency to the correct value of 4.4336 MHz + or - 100 Hz.
9. In order to improve the waveform of the 16MHz signal, C42 was at one stage a fixed capacitor with a trimming capacitor in parallel. Therefore various issues of boards will have various different values for C42. Also the gate used (IC40) was changed from a 74LS00 to a 74S00.

5.3.2 Changes from issue 3 to issue 4.

1. The Econet circuitry was modified in various ways. The clock generator and terminator components were removed, certain component values were changed in order to improve circuit performance and the layout was altered in order to improve the shielding and to reduce cross-talk.
2. A 22k resistor (R174) was introduced from pin 20 of IC7, the serial processor, to 0 volts to ensure that if IC74 was absent that the CTSI line was held low.
3. Having added the 2k2 pull up resistor (R170) to printer port strobe line and put Q11 in its own position, S1 was reinstated.
4. The circuitry associated with S14 to S17, which change the 1MHz bus to 2MHz, on the issue 3 PCB was incorrect. This should be checked against the current circuit diagram if it is to be used.
5. The position of D13 was changed to put it in parallel with the relay coil rather than across the collector and emitter of the transistor (Q3).
6. The connections from the speech circuit (IC99) to the VIA were changed. VSPRDY and VSPINT were changed over to connect to PB7 and PB6 respectively.

7. A resistor (R171) was connected in series with the EOC line of the ADC (1C73) in order to prevent momentary output contention which may occur during power-up.
8. A 4k7 resistor (R173) was connected between pin 7 of IC89 and +5v, as the output is open collector.
9. Resistors R104, R125, R142, R149, and R153 which were in series with the ROM chip select lines were replaced by copper links formed on the component side of the PCB. (S34 to 38)
10. A 10k resistor (R172) was introduced between the analogue input on the 1MHz bus and 0 volts in order to reduce the input impedance and hence improve the signal to noise ratio. (See section 6.4)
11. Link S39 was added in order to connect the 470pF capacitor, C58 from the base of Q7 to the emitter of Q9.
12. A 220nF capacitor (C59) was added in series with R90 in order to AC couple the log amplifier on the cassette interface.
13. A number of changes were made to the Econet control lines in order to speed up software control. For details of how to bring earlier issue boards up to the current issue, see the section on upgrading the Econet system (section 4, modification E).
14. Provision was made for mounting a right-angled phono socket as an alternative to the free-wired BNC socket normally used for video output.
15. A 200k potentiometer (VR2) was added in parallel with R32 in order to adjust the operating frequency of IC99 for the appropriate pitch of the speech output.
16. At some stage between issues 3 and 4, C34, the cassette output coupling capacitor was increased from 47nF to 220nF.

5.3.3 Changes from issue 4 to issue 7.

(Issues 5 and 6 never went into production).

1. R114 changed to its present value of 18 ohms 1W, and C42 changed to 33pF.
2. R75 went to its final value of 82k. (The reason for the change in value of R75 was to control the data carrier detect delay time to avoid loosing the first bit of the first byte of the first block when recording data.)
3. The diodes and resistors on the ROM select circuitry which can be used to produce 1MHz operation were omitted.
4. Links S18 and S19 are made with tinned copper wire.
5. When the video processor ULA was replaced by the first set of custom-designed ICs, a modification was necessary. S26 was left unconnected and a wire link was made from the TTX-VDU line (pin 17 of IC2) to the invert input of the videoprocessor (pin 27 of IC6). Later versions of the custom IC made this modification unnecessary.

All other changes from issue 4 to issue 7 were cosmetic changes including some thickening up of the tracks to improve the power supply distribution.

6 Servicing and Fault-finding

6.1 Introduction

Before starting, it should be realised that attempt at repair by any person other than a registered dealer or service agent will void the warranty.

6.2 Test Equipment

The very minimum test equipment required in order to trace even the simplest fault is a digital multi-meter and an oscilloscope (or possibly a logic probe). It is difficult in a book such as this to do more than give a few general guide-lines as to the sort of problems to look for, and a few techniques which might be used.

Acorn Computers Ltd supply two pieces of test equipment which are specifically designed for the BBC Microcomputer which are known as the PET (Progressive Establishment Tester) and the FIT (Final Inspection Tester). Whilst the service agent or dealer might be expected to have these pieces of equipment, the average user is unlikely to feel that it is worth purchasing them for the limited amount of fault-finding he or she would be likely to do. The purpose of the PET, which is the more expensive of the two items, is to take an apparently lifeless computer and attempt to find out where the fault lies. The FIT on the other hand is somewhat simpler and its aim is not to isolate a known fault but to check whether an apparently working computer is in fact working in all respects. Both the PET and the FIT are the subject of entirely separate documents produced by Acorn Computers PLC.

Two other very useful pieces of "test equipment" are a can of freezer spray and a hair-dryer! It is fairly common for faults in some of the ICs to be associated with temperature conditions. Therefore if you have reason to suspect a particular component, it is sometimes helpful to "exercise" the device by the use of these two items. This can sometimes show up a fault quite clearly. However, this can be slightly misleading in cases where the fault is caused by a timing problem on some device. This is because changing the temperature conditions of one device which may not itself be at fault, may, by changing the relative timing, bring the timing back into a working condition. Therefore having discovered a device which apparently has a temperature fault, before de-soldering it, it is well worth temperature cycling the associated components.

6.3 Fault Isolation

Having checked that the apparent fault is not a problem with the program, the first thing, to do is to isolate the problem to a particular area of the computer. For example, if the problem is in loading and saving programs with a cassette recorder then attention should be focussed on the cassette interface itself. However, this is not as easy as it sounds in some cases because of the links between various sections of the circuit. It would probably be worthwhile reading through most of the circuit description given in this book, in order to try to gain an understanding of the operation of the computer as a whole before trying to deal with one apparently isolated section of the computer's hardware.

The simplest fault to check for is malfunctioning of the power supply. Voltages can be measured at the terminals on the PCB where the power leads are attached, but it is worth checking, particularly with the older linear type power supplies, that the +5 volts is available on each of the three pairs of connectors. It is also worth checking that the -5 volts is present because although the processor, memory and VDU will all function normally if the -5 volts is not present, it is essential for cassette, sound, speech and RS423 interfaces.

If the power supply is NOT working then you should NOT attempt to repair it. The reason is that in order to maintain the safety specification to which the computer was designed, any repair to the power supply, including replacement of power supply cable, must be checked for earth continuity at a current of not less than 10 A, and must undergo a Dielectric Withstand Test between both live and neutral to ground of 1500 V AC. This requires specialist equipment and training and should not even be attempted by dealers, unless they have the necessary equipment and expertise.

The worst kind of fault with a microprocessor system is that the processor is unable to fetch instructions from the ROM, process them and then produce some sort of result which the operator can see or hear. In the case of such faults, the whole system appears completely dead and it is very difficult to locate the specific fault. This kind of problem is made worse on this particular computer because of the technique used to refresh the dynamic RAM. Not only must the processor fetch instructions from ROM and process them, but also it must successfully program the CRT controller which, in turn, must begin to produce refresh addresses for the dynamic RAM before the system memory can operate.

Assuming then that the machine appears totally dead even though the power supply unit is apparently working, and that you do not have access to a PET, then here are a number of things you could check:-

i) Check that the reset line on the 6502A (pin 40) is high, and only goes low when BREAK is pressed.

ii) Check that the IRQ line is not permanently in either a low or high state. (Pin 4 of the 6502A)

iii) Check for the presence of the various clock signals, for example, the clock input and output on the 6502A (pins 37 and 3), and the 1, 2, 4 and 8 MHz signals on pins 4, 5, 6 and 7 of the video processor (IC6).

iv) A very useful pin to check is pin 7 on the 6502A. This is the sync pin and, although it is not actually used in the circuit, it gives an indication of whether or not the 6502A is fetching any instructions. If this is permanently high or low then the 6502A is totally stalled.

v) Check that the read-write line (pin 34) of the 6502A is working normally and also check that the same signal, having been inverted and re-inverted, is available at pin 10 of IC33.

vi) Check for the horizontal and vertical sync signals coming from the CRTIC (pins 39 and 40 of IC2) which will reveal whether or not the CRTIC has been successfully programmed at system reset.

If you do detect something abnormal in one of these tests then the next stage would be to remove from the board any devices in IC sockets which are unnecessary to the basic operation of the computer. For example, the 6850 ACIA (IC4), the serial processor (IC7), the ADC Converter (IC73) and the external 6522 (IC69). Having removed these devices, if the fault disappears, then it may simply be a case of replacing them one by one until the fault reappears. If the fault remains, then if you have any spare ICs, or another machine with which you could exchange ICs, it would be worth replacing the internal VIA (IC3), the 6502A (IC1), the 6845 (IC2) and the video processor (IC5).

At this stage the next thing to try is to examine each of the individual address and data lines to see if one or more of these lines is permanently high or low. If so, look for short circuits, solder bridges etc on that line. It is worth checking these lines both on the 6502A itself and also IC51, the operating system ROM.

When looking around the board at various points with an oscilloscope, try to find any waveforms which either have "slack" edges, ie sloping rather than square, or which have voltage levels which are not within the normal TTL range. (Logic 1 must be greater than 2.8V and logic 0 less than 0.8V, though normally one would not expect to see voltages of less than about 3.4V or more than 0.4V.)

Another very useful test with a model B, is to move link S25 to the south position to see if the computer will operate in the 16K mode, in which case, it suggests a problem with the CAS 0 area of RAM. Then if you remove S25 altogether, it puts the machine again into the 16K mode but this time with the CAS 0 area enabled and the CAS 1 area inoperative.

6.4 Most Common Faults

In the following section, we shall try to give some ideas which have been collected from various people who have been doing a good deal of servicing and repair work on BBC Microcomputers. There will be no particular order to the comments but reading through all of them should give some useful ideas about faults which are likely to occur.

* A common reason for getting sound-on-vision effects is that the power leads have become intermittent. To check whether they are giving a problem, a quick flick with one finger is what the experts recommend. If this causes the display to flicker then switch off the unit, remove the power leads, pull back the insulating sleeves, solder along the area where the wire is crimped by the terminal, and replace them, being careful not to exchange the 0 and +5 volt connectors.

* It is possible for the ROM sockets to develop bad contacts. This is sometimes caused by heavy-handed use of the "butterfly" carrier boards which were used at various stages to put two 8K eproms into one single 16K socket. The only solution for this is to replace the ROM socket entirely, and you would be well advised to use the best quality socket available. This is not an easy task unless you are experienced in the use of desoldering equipment.

* The most common reason for the cassette system becoming inoperative is a damaged LM324. Another problem is with the clock input to the serial processor and it is worth checking that this is the correct frequency (ie 1.23 MHz = 812 ns periodic time). Another problem which sometimes occurs is that the value of R75 needs to be changed. The optimum value is different for different issues of the serial processor ULA because of the variation in impedance of pin 15 to earth. This affects the timing between receiving a high tone lead-in and asserting the data-carrier detect on the ACIA. For ICs numbered 2C199E and 2C199E-3, R75 should be 100k or 56k as required for consistent loading of data. For 2C199E-7, R75 should be 82k.

* One simple problem, but unfortunately fairly common, is that the pins of ICs tend to get bent as they are pushed into the sockets. If you have isolated the fault to a particular area, then this is something to look out for. It is also not unknown for the IC socket itself to have a pin bent underneath. This may not have been noticed by quality control if the IC socket was empty at the time of production eg speech IC socket.

* If you wish to get two BBC Microcomputers to send programs to each other on the cassette system, then it is possible to do so by a direct connection, provided a 1.5k resistor is connected between the signal line and ground. With the later issue boards, that have the 220nF output capacitor on the cassette system, a smaller value may be necessary. The resistor is necessary to adjust the relative phase of the two tones of the cassette signal.

* On a number of occasions, the tracks on the right hand side of the keyboard PCB have become broken in transit. This occurred more frequently on earlier versions and less so since the newly modified case has been used, but if any of the keys on the right hand side are inoperative then this is a likely cause. Excessively hard use of the keyboard may also cause solder pads to lift. A group of non-functional keys would indicate that this has happened. This could be checked quite simply by the use of a meter to test continuity.

* A number of people complain of interference on the sound signal. This is caused by the pick up of digital noise as the track goes from the 1MHz extension bus input to the audio stages. The solution is to connect a 10k resistor across from this line to ground. This should only be necessary on issues 1 to 3 of the PCB. It can be done by connecting the resistor between pin 8 of IC20, which is ground, to the plated-through hole just to the south of that pin. It is necessary to scratch away the solder resist very carefully from around this hole, before you can successfully solder into it.

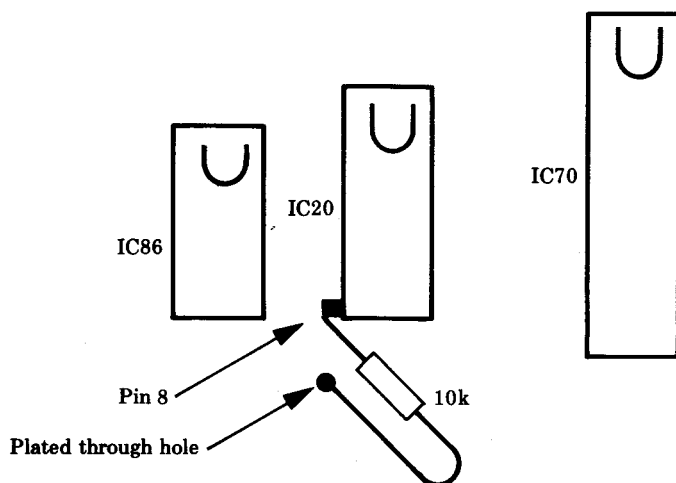


Figure 12 Reducing noise on 1MHz audio input

* One simple problem that sometimes occurs is that of getting twinkling characters in some of the higher modes of graphics, or smearing of the cursor. If this was not originally a problem but has developed after some months of use, then it may well be that the heat sink on the video processor has become dislodged. This can be put right by applying firm pressure to the heat sink and also possibly by applying more heatsink compound between it and the top of the integrated circuit.

* Certain other faults on the VDU display associated' with the UHF output can be cured by adding extra decoupling to the supply to the modulator to improve its stability. A 10 ohm series resistor with a 4.7 uF capacitor to earth is usually sufficient.

* It has been noticed that problems can occur with some of the 74LS74 ICs, especially from certain manufacturers. If there is any problem therefore with the cleanliness of the clock pulses applied to the 6502A, or problems with the PAL encoder circuit, or more likely with the RAS signal, it would be worth checking the output of these ICs to see if they are driving to the full TTL levels.

* Unfortunately, a number of problems also arise when people have tried to do their own upgrades and have made mistakes or used bad soldering techniques. In particular, a number of people seem to get the printer upgrade on the issue 2 board wrong and therefore this should be checked very carefully (see section 4). Also it is worth checking the soldering very carefully, particularly around the area of the IDC connectors. This is because it is easy to get solder bridges over the tracks which are fed in between the pins on this connector. The worst place seems to be in the area of the tube connector.

* If there are problems associated with the PAL or cassette circuitry, it is worth checking very carefully whether the correct resistor values have been used. Since there are so many resistors so closely packed together, it is very easy to get resistors in the wrong places. To check this, it is best to remove the circuit board from the case entirely and use a strong light source in order to view the resistor's colour codes carefully. This is well worth doing, as it can save a lot of time looking for faults which are basically simple but which would be difficult to diagnose.

* Our service centres tell us that there is a series of rather obscure faults which they have detected which is associated with timing problems with the RAM. One symptom is twinkling characters in mode 7 but not in the other modes of graphics, and another is that when playing Acornsoft's "Defender" (not the later version of "Planetoids") some very strange effects occur as the game continues. Also there is a program of 3D Noughts and Crosses from Beebug which produces a strange fault, stopping inexplicably at one particular line and giving a No Room error. These faults, being related to relative timing, can sometimes be cured by changing the 6502 processor, or the 74LS245 (IC14) and are more often noticed where the RAM in CAS 1 is a different type from the RAM in CAS 0, when an A to B upgrade has been done. In particular it seems to be that the Fujitsu RAMs do not mix well with the Mostek or Hitachi RAMs.

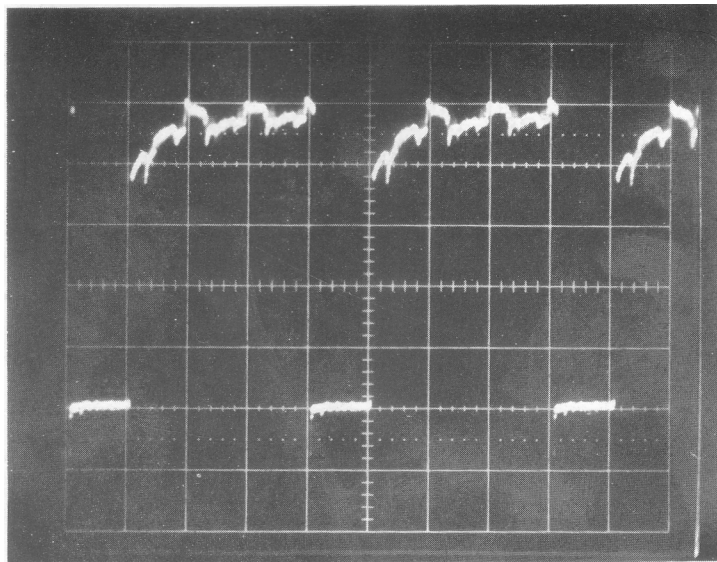
6.5 Test programs and sample waveforms

6.5.1 Test program

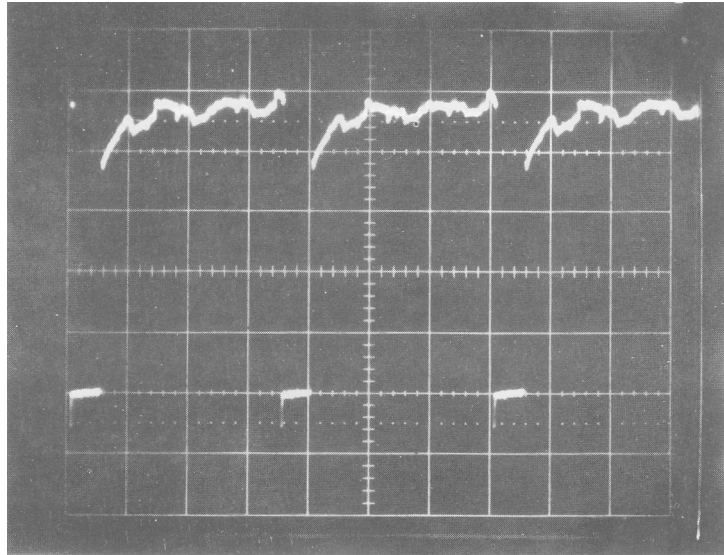
The following program allows you to test the chip select lines of any of the devices on the computer. It sets up a machine code loop which accesses the address which you specify as hexadecimal number. Since it is a closed loop, the only way to escape is to use the break key which is programmed to re-enter the BASIC program. To escape, enter a zero address. If you are accessing a slow device, its chip select line should go low for a full microsecond, but with a fast device, it will only be low for 500 nanoseconds. In either case, the waveform should be high for 3 microseconds.

```
10 *KEY10 OLD|M RUN|M
20 CLS
30 DIM CODE 20
40 P%=CODE
50 INPUT "ADDRESS",M$
60 M%=EVAL("&" + M$)
70 IF M%=0 THEN END
80 [SEI
90 SEC
100 .again
110 LDA M%
120 BCS again
130 ]
140 CALL CODE
```

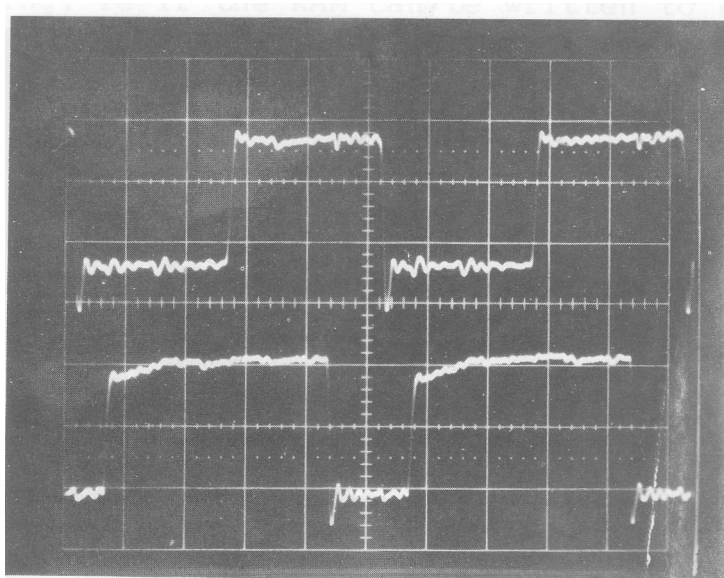
The following is a reproduction of a photograph showing the waveform on pin 23 of the ADC chip, IC73, when the above test program is running with address &FECO selected. Scope parameters are 1V/cm, 1 μ s/cm.



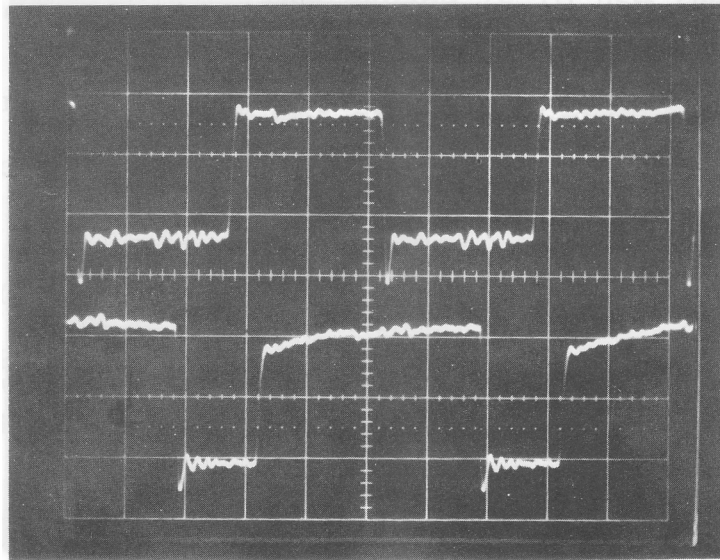
The following shows pin 24 of the disc controller chip, 1C78, selected by using address &FE80. Scope parameters are 1V/cm, 1us/cm.



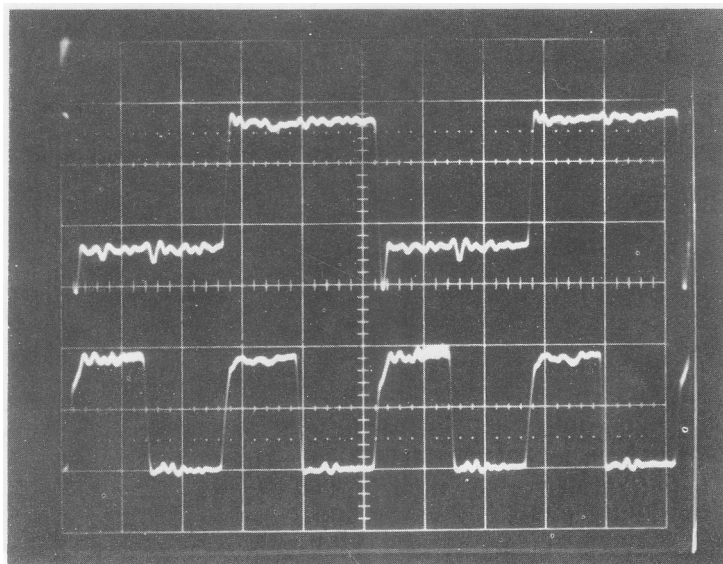
The following shows two traces while the test program is running: top trace is 2MHz clock pin 37 IC1, and bottom trace is CAS0 pin 7 1C45. Scope parameters are 2V/cm, 100ns/cm.



The following shows two more traces while the test program is running: top trace is 2MHz pin 37 IC1, and bottom trace is CAS1 pin 5 IC45. Scope parameters are 2V/cm, 100ns/cm.



The following shows two more traces while the test program is running: top trace is 2MHz pin 37 IC1, and bottom trace is RAS pin 12 IC43. Scope parameters are 2V/cm, 100ns/cm.



6.5.2 Test ROM

The listing shown below is the object code for a ROM which could prove extremely useful for fault-finding an apparently dead machine, especially if you do not have a PET. There are three routines given, but you could extend the idea for up to 8 different routines if you wanted to do so. The idea is that a 2764 ROM is put in place of the operating system ROM and the routine which the system starts on power-up or break is determined by taking the address lines that would normally be connected to A10, A11 and A12 (pins 21, 23 and 2 of the 2764 respectively) and have some means of attaching them to +5 volts or 0 volts.

This can be done crudely by bending up the three pins so that they don't engage in the IC socket, and soldering on to them three leads terminating in crocodile clips. These can then be used to select the address by clipping on to the +5V and 0V rails, being careful not to let them short out. For a system that is to be used regularly for fault-finding, it is wise to use either a DIL switch or better still a thumbwheel switch, properly mounted.

The three routines given are:-

Routine "0": Provides a chip select pulse for each memory-mapped device around the board in turn. The pin numbers at which each pulse should appear are given in the program.

Routine "1": This sets up the teletext mode of graphics by programming the 6845 and the video processor appropriately. Then codes 0 to 255 are stored in the first four pages of video RAM. If there is a RAM fault then the display will not be the succession of ASCII character which you would expect, and by careful thought about which characters are in error, you should be able to diagnose where the problem lies. The pattern is periodically re-written so that intermittent faults will show up and you can try temperature exercising any suspect chips.

Routine "2": This is similar to the previous routine but by incrementing a location on the screen it checks the combination of reading and writing; ie if the RAM can be written to but not read then the character at location &7C01 will not cycle through 0 to 255 since the read instruction will be in error. All these routines are working in machine code at high speed and therefore it is easy to use an oscilloscope to probe around the circuit to see what has gone wrong.

```
10 FOR N% = 0 TO 2 : REM ie 3 tests available
20   PROCtest(N%)
30   NEXT
40 *SAVE ROMIMAG 3000 + 2000
50 END
60
70 DEFPROCtest(N%)
80 offset% = &400*N%
90 0% = &3000 + offset%
100 P% = &F800
110 table% = P% + &200
120 !(&33FC + offset%) = &F800 : REM RESET vector
130 opt% = 5
140 IF N% = 0 PROC strobe select lines
150 IF N% = 1 PROC DRAM test
160 IF N% = 2 PROC RNW exercise
```

```

170 !(&3200 + offset%) = &4433283F
180 !(&3204 + offset%) = &1B19021E
190 !(&3208 + offset%) = &13721293
200 !(&320C + offset%) = &002C002C
210 ENDPROC
220
230 DEFPROC strobe select lines
240 [OPT opt%
250
260 .loop
270 LDA &FE00 \ IC2 pin 25 (CRTC)
280 LDA &FE08 \ IC4 pin 9 (ACIA)
290 LDA &FE10 \ IC7 pin 9 (SER PROC)
300 LDA &FE18 \ IC96 pin 1 (STATID) or IC97 pin 4 (INTOFF)
310 LDA &FE20 \ IC97 pin 2 (INTON)
320 STA &FE20 \ IC6 pin 3 (VID PROC)
330 STA &FE30 \ IC76 pin 9 -(ROMSEL)
340 LDA &FE40 \ IC3 pin 23 (VIA A)
350 LDA &FE60 \ IC69 pin 23 (VIA B)
360 LDA &FE80 \ IC78 pin 24 (FDC)
370 LDA &FEA0 \ IC89 pin 9 (ADLC)
380 LDA &FECA \ IC73 pin 23 (ADC)
390 LDA &FEE0 \ PL 12 pin 8 (TUBE)
400 LDA &FC00 \ PL 11 pin 10 (FRED)
410 LDA &FD00 \ PL 11 pin 12 (JIM)
420 JMP loop
430 ]
440 ENDPROC
450
460 DEFPROC DRAM test
470 [OPTopt%
480 LDX £&OF
490 STX &FE20 \ Write to Vidproc
500
510 .setup_6845
520 LDA table%,X \ table of 6845 data
530 STX &FE00 \ Register number
540 STA &FE01 \ Contents of register
550 DEX
560 BPL setup_6845
570 LDA £3
580 STA &FEFE \ send down TUBE
590
600 .restart
610 LDY £0
620
630 .loop2
640 NOP
650 TYA
660 STA &7C00,Y
670 STA &7D00,Y
680 STA &7E00,Y
690 STA &7F00,Y
700 INY
710 BNE loop2
720
730 LDA £&42
740 STA &FE20 \ Write to Vidproc
750 JMP restart
760 ]

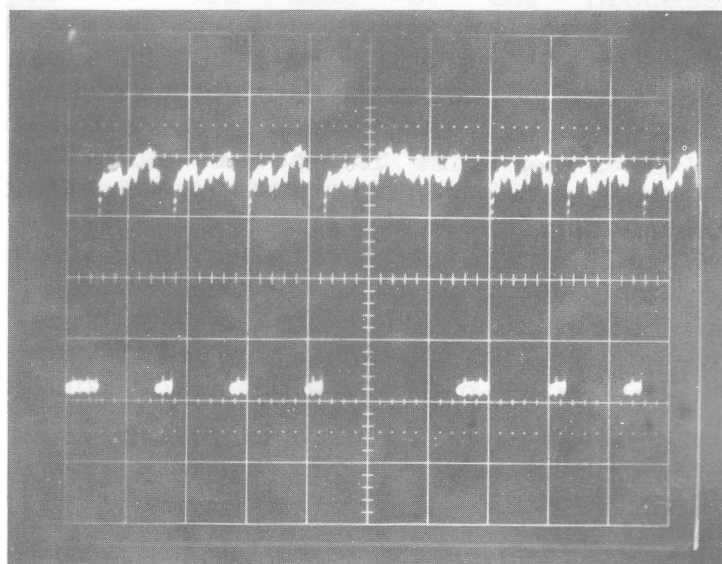
```

```

770 ENDPROC
780
790 DEFPROC_RNW_exercise
800
810 [OPT opt%
820 LDX £&0F
830 STX &FE20 \ Write to Vidproc
840
850 .setup 6845
860 LDA table%,X \ table of 6845 data
870 STX &FE00 \ Register number
880 STA &FE01 \ Contents of register
890 DEX
900 BPL setup_6845
910
920 LDA £3
930 STA &FEFE \ send down TUBE
940
950 LDA £&41 \ Character "A"
960 LDY £0
970
980 .write
990 INC &7C01 \ Change character on screen
1000 STA &7D00,Y
1010 STA &7E00,Y
1020 STA &7F00,Y
1030 INY
1040 BNE write
1050
1060 LDA £&42 \ Character "B"
1070 STA &FE20 \ Write to Vidproc
1080 JMP write
1090 ]
1100 ENDPROC

```

The following is a reproduction of a photograph showing the waveform on pin 34 of the 6502 (R/W of IC1). Scope parameters are 1V/cm, 2us/cm.



7 Interfacing Survey

7.1 Purpose of each interface

Since there are so many different interface connections on the BBC microcomputer, it may be a help to look at each in turn and talk about possible applications for each. Working from left to right on the back of the computer, we start with the UHF output, which provides a PAL colour TV signal for use with a normal colour television. Next is a video output on a BNC connector which is intended to be used with a black and white video monitor. However it is possible to introduce the colour burst information onto this signal in order to produce a PAL composite video signal. On circuit boards issue 4 onwards, it is possible to introduce this signal by adding a simple link, S39. On previous issue boards it is necessary to introduce a 470pF capacitor from the emitter of Q9 to the base of Q7. This capacitor would have to be soldered directly on to the circuit board.

The third connector which is provided for video output is a 6-way, 240 degree DIN plug. This provides the red, green, blue and sync signals needed for an RGB monitor. The sync signal is a 5 volts, negative going pulse of 4.7uS duration, but it can be changed to positive going by changing link S31. Also provided on this connector are a 0 volt and a +5 volt supply, but these should not be used for providing more than a few milliamps to external circuits.

The next connector is a serial port of the RS423 standard. This is a standard which has superior drive capabilities to the RS232 interface and is run in this case between +5 volt and -5 volt levels. The speed is software selectable at 75, 150, 300, 1200, 2400, 4800 or 9600 baud. There is a higher speed of 19200 baud, but this **is** not guaranteed to be error-free. It is also possible to get the interface to work at 110 baud, but this requires a modification which would also change the speed of the cassette interface. (See section 7.3 on hardware hints and tips for more information.) The control signals provided are the normal CTS and RTS lines, the RTS output also working on +5 volt and -5 volt. NB When making up a connector for the RS423, note that connections as shown on the circuit diagram refer to the socket. For the plug connections, refer to page 504 of the User Guide which gives the connections as seen from outside the case.

Apart from using the RS423 interface to run a serial printer it is also possible to use it to communicate with other computers. For example, it is possible to communicate with a mainframe computer either directly within a building on a wired link or, by using the telephone network, to a computer in another building or even another country. This would of course require the use of an acoustic coupler.

There are various levels at which this link could be used. Firstly the computer could be used as a "dumb terminal" which would simply be capable of sending characters typed on the keyboard to the mainframe computer and receiving characters from the mainframe and printing them on the screen. The following program will allow you to do so.

```

10 REM Dumb Terminal Program
20 REM Only works on OS 1.0 & following
30 REM Works even if Tube fitted.'
40 REM
50 OSASCI = &FFE3
60 OSBYTE = &FFF4
70 OSWRCH = &FFEE
80 CLS
110 DIM CODE 50
120 FOR J=0 TO 2 STEP2
130   P%=CODE
140   [OPT J
150   .RS423
160   LDA £&91
170   LDX £1
180   JSR OSBYTE\character in RS423 buffer?
190   BCS keyboard
200   TYA
220   JSR OSWRCH\or OSASCI for CRLF
230   .keyboard
240   LDA £&91
250   LDX £0
260   JSR OSBYTE\character in keyboard buffer?
270   BCS RS423
280   TYA
290   JSR OSWRCH\or OSASCI for CRLF
300   LDA £&8A
310   LDX £2
320   JSR OSBYTE\Put character in RS423 output buffer
330   JMP RS423
340   ]
350   NEXT
360 *FX 7,7
370 *FX 8,7
380 *FX 2,2
390 CLS
400 CALL CODE

```

The next level would be its use as a semi-intelligent terminal which would enable you to use some of the processing of the BBC Microcomputer to deal with file handling, so. that the text could be prepared off line, stored on disc and then spooled down to the mainframe when the link is made. The third level then would be to use the graphics facilities of the BBC Microcomputer in addition to its ability to print text. This produces the possibility of using the computer as a colour-graphics terminal to a mainframe computer at a fraction of the cost. All that is needed is for someone to write the appropriate terminal emulation software and put it in sideways ROM. There are now a number of such packages commercially available.

The other way in which the RS423 can be used is to link two BBC computers together. One reason for doing this would be to enable software to be downloaded from a disc system to another computer which does not have a disc interface. A 15K program can be downloaded using an RS423 link in approximately 20 seconds which is clearly faster than using a cassette to cassette link. The only software involved in doing this is to type in, on the receiving computer:

```
NEW <RETURN>
*FX2,1 <RETURN>
(This sets the RS423 as input instead of the keyboard.)
```

and then on the sending computer you would type in:

```
*FX3,7 <RETURN>
LIST <RETURN>
*FX3,0 <RETURN>
(This enables the RS423 as the output and sends a listing of the program so that, to the receiving computer,, it is as if it were being typed in from the keyboard.)
```

If you have a number of transfers to do, then these commands could be programmed onto a single key on each machine. When the program has been sent down, you simply have to press BREAK on the receiving computer, type OLD <RETURN> and then the program is ready for use. If you are doing a BBC to BBC link over a short distance and want to use the full speed of the interface then you will have to connect the hand-shake lines as well as the data lines. The "data out" from one computer should be connected to the "data in" of the other computer and vice-versa, and in a similar way for the control lines, the RTS on one should be connected to the CTS on the other and vice-versa. If you are working over a longer distance and want to use only three cables, data in, data out, and ground and are prepared to work at a slower speed without any handshaking, then you have to loop back the RTS to the CTS on each of the computers so that each is permanently enabled for sending. If you do not do so, the RS423 output buffer fills up and printing stops after a number of characters have been sent to the screen.

If you want to use the RS423 interface over a long distance at high speed using the hand shake lines, it might be necessary to terminate the receivers by making links S23 and S24. This terminates the line with its characteristic impedance of 180 ohms.

The cassette interface is a standard CUTS cassette interface. It has two speeds, 300 and 1200 baud, controllable by software. There is also motor control provided on pins 6 and 7 of the 7-way DIN plug. The rating of the relay contacts is 24V at 1A DC, and they should not, under any circumstances, be used to switch mains voltages, no matter how small the current. If you wish to get two BBC Microcomputers to send programs to each other on the cassette system, then it is possible to do so by a direct connection, provided a 1.5k resistor is connected between the signal line and ground.

The analogue input is on a 15-way D-type connector and provides four A to D converter channels and two digital input lines which work on the internal 6522 VIA. The pin connections are arranged so that the signals are divided into two sets intended for use with two games paddles, each of which will have two A to D inputs and a voltage reference source as well as the ground and one of the digital input lines.

The conversion time for each channel is 10 milliseconds, but you can choose to have as few or as many of the channels working as you wish by using the *FX16 command. Therefore if all four converters are required, you need to allow 40 milliseconds to be sure of a successful conversion on any one channel. However ADVAL(0) in BASIC, or OSBYTE call 128 in machine code, can be used to see which channel has just converted, and OSBYTE call 17 allows you to force a particular ADC channel to convert, out of turn. The resolution is software selectable between 8 and 12 bits resolution using OSBYTE 190. However in the 12 bit resolution mode, the true resolution is somewhat less than 12 bits. It is probably more realistic to think in terms of a 9 or 10 bit accuracy.

Also provided on this connector is an input to the light pen strobe on the 6845 CRT controller. The hardware involved in setting up a light pen system is quite simple. The light pen circuit has to produce a positive-going 5 volt pulse with a duration of greater than 100 ns. However the software involved is quite complicated if you want to do more than identify character blocks. This is because of the way in which the 6845 has been extended beyond its normal memory range in order to provide bit-mapped graphics.

The final connector which is provided on the back of the computer is only available when the unit has been upgraded with an Econet interface. This is a standard 5 pin 180 degree DIN plug to provide the necessary data and clock signals for the Econet interface.

Underneath the computer is a set of standard IDC connectors. First of all there is a 34 way connector for the disc drive(s). This connector carries the standard connections for a 5.25" disc drive. The next two are a 26-way and a 20-way IDC connector which are used to provide connections to the two ports of the external 6522 VIA. The 26-way connector links to port A, and is arranged in a standard format for use with a Centronics-type parallel printer. The 8 port lines are buffered to provide better drive capabilities, but it does mean that they can only be used for output. If you want to use these lines to drive some other device, you should work on the basis of each line being able to sink 10 mA at logic 0 or to source 400 uA at logic 1. Of the two control lines, CA1 is available as an input with a single 4k7 pull up resistor on it, whilst the CA2 line is available as an output, the line being buffered by a single transistor (Q11) to improve the current sinking. On boards from issue 4 onwards, there is a selection link (S1) which will enable this line to provide direct connection to CA2 so that it can be used as either input or output.

The 20-way User Port is much simpler in that all connections go directly to the lines on the VIA (PBO to PB7 and also control lines CB1 and CB2). If you are using these lines for output you should consult the 6522 data sheet to establish the amount of drive current available.

The next connector, another 34-way IDC, provides an extremely versatile interface known as the 1MHz extension bus. This interface is the subject of a separate Application Note and at this stage it is sufficient to say that it provides two "pages" (2 x 256 bytes) of memory locations mapped between &FC00 to &FDFF. By using one of these locations (&FCFF) as a paging register it is possible to extend the memory addressing capability to a full 64K bytes.

The final connector is a 40-way IDC which provides an interface known as the "Tube", intended for use with a second processor. Although the hardware on the BBC microcomputer side is very simple, the hardware on the second processor is extremely complex and it really requires a ULA to incorporate all the hardware necessary to handle the protocol. It is therefore suggested that any interfacing to the Tube should be done only using products from Acorn Computers Ltd.

7.2 Interfacing to various printers.

It is possible to interface to a wide variety of printers using the two interfaces provided. First of all, for serial printers, the RS423 connector can be used and secondly, for parallel printers the Centronics interface can be used. It is also possible to link up to various other non-standard printers such as the IEEE 488 printers used for the Commodore Pet computers. This is more difficult and requires connection not only to the Printer Port, but also the User Port to provide extra control lines and also requires extra software within the machine.

It is possible to write your own printer driver routine which works through the operating system.

In order to link up to teletype printers, which run at 110 baud, you have to change the position of link S28. This is explained in detail in section 7.3.

One important point to note is that on issue 1 printed circuit boards, the pin connections on the printer port are not quite the same as later issues. Pin 19 is the ACK line and pin 26 is not open circuit as it should be for certain printers. If you wish to use this interface, for example with the Seikosha GP80A, you will encounter problems since pin 26 is used as a reset line. Another problem which may occur on the early issue boards is that there is no pull-up resistor on the CA2 line thus leaving the collector of transistor Q11 open circuit.

7.3 Hardware Hints and Tips

Here are a number of miscellaneous hints and tips which have come from various sources.

* RS423 at 110 baud

In order to get the RS423 interface to work at 110 baud, all that has to be done is to use the *FX8,1 command in order to set 75 baud and then change the position of link S28. This link is made by a track on the PCB, between the centre pin and the west pin. This link has to be broken and a solder link made from the centre pin to the east pin. This has the effect of speeding up all of the baud rates, both send and receive by 44%, and also makes the cassette port run fast by the same amount, so a single pole double throw switch could be wired to S28 in order to select the normal speed or the fast speed for the 110 baud. The actual speed produced is 108.333 but this is near enough for most teletype printers.

* Disabling Break

For certain applications, particularly when the computer is being used by very young children, it is most frustrating when the user presses the break key. It is easy enough to disable the escape key within a program, but the break key is more of a problem. You could use *KEY10 OLD|M RUN|M but even this is not very satisfactory. The alternative is to disable the break key electrically, which can be done by removing a link from the keyboard PCB. You could then wire it up to a miniature ON-OFF toggle switch which can be mounted on the back of the case by drilling a suitable hole, or leave it open circuit and use the contacts at the back of the main PCB marked "RST SW", to provide an alternative break key. The disadvantage of doing this though is that if you are using a disc system, you may want to be able to do a SHIFT break in order to boot the disc. The position of the link to be removed is shown below.

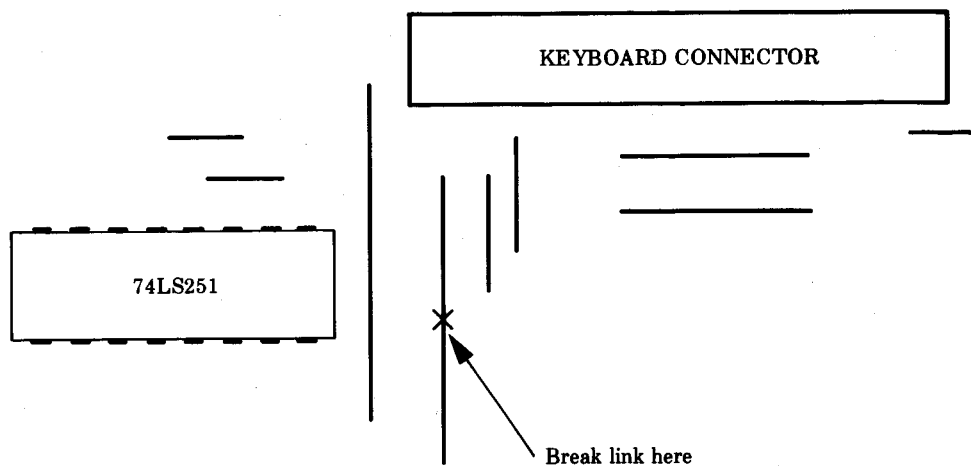


Figure 13 Disabling the BREAK key

8 Component location tables

The following lists of components should enable you to locate any component on the main circuit diagram by its X and Y grid reference (see grid numbers on main PCB circuit diagram). For ICs and selection links, their positions on the PCB itself are also given. These are defined by X and Y coordinates in millimetres, measuring from the SW corner of the PCB.

8.1 Integrated circuits

NB Some ICs which contain more than one circuit will appear at more than one place on the circuit diagram.

IC Type	PCB Position	Circuit Diagram	Comments
1 6502A	160,85	10,6	
2 6845	160,140	5,3	CRT controller
3 6522	90,75	5,9	Internal VIA
4 6850	128,141	11,5	ACIA
5 SAA5050	187,102	10,2	Teletext ROM
6 5C094	214,71	7,6 10,1	Video ULA
7 2C199	128,182	12,4	Serial ULA
8 81LS95	241,62	5,1	
9 81LS95	241,93	5,2	
10 81LS95	252,63	5,3	
11 81LS95	252,93	5,4	
12 81LS95	275,62	5,4	
13 81LS95	264,62	5,5	
14 74LS245	184,71	9,4	
15 74LS273	196,71	9,2	
16 LM555	7,210	6,7	
17 LM324	6,28	4,6	
18 76489	.22,44	5,6	Sound generator
19 LM386	52,23	5,5	
20 74LS139	120,23	7,10 9,8	
21 74LS00	120,55	10,8	
22 74LS30	137,55	6,10	
23 74LS30	120,80	8,9	
24 74LS138	135,78	6,10	
25 74LS20	120,108	7,10 10,6	
26 74LS139	137,105	6,8	
27 7438	3,124	2,4 4,2 4,10 12,7	
28 74LS51	50,143	7,7 9,6	
29 74LS32	65,143	5,6 8,7 8,8	
30 74LS74	78,143	8,6	
31 74LS34	90,143	5,9 8,7	
32 74LS259	105,143	5,10	
33 74LS04	58,164	4,9 10,9 10,3	
34 74LS74	71,164	8,7	
35 LM324	151,205	13,5	
36 74LS10	215,122	4,2 10,3	
37 74LS04	228,122	8,6 10,3 10,6	
38 74LS86	241,122	5,3	
39 74LS283	197,145	5,2	
40 74S00	206,149	4,2 6,5 8,6	(Previously 74LS00)
41 74LS02	228,149	4,4 7,4	
42 74LS163	241,158	12,6	
43 74S04	187,174	7,6 8,4	

44	74LS74	206,174	12,1	
45	74S139	228,172	7,5	
46	74S74	252,183	12,2	
47	74LS86	264,183	13,2	
48	74LS86	275,183	13,1	
49	74LS00	286,183	13,2	
50	74LS00	298,183	12,6	13,1
51	(27128)	214,24	8,9	Operating system ROM
52	(27128)	233,24	9,9	BASIC ROM
53	4816	287,69	8,2	
54	4816	287,93	8,2	
55	4816	275,93	8,3	
56	4816	298,146	8,4	
57	4816	287,146	8,2	
58	4816	275,146	8,2	
59	4816	264,146	8,3	
60	4816	252,146	8,4	
61	4816	298,68	6,2	
62	4816	298,93	6,2	
63	4816	264,93	6,3	
64	4816	298,122	6,4	
65	4816	287,122	7,2	
66	4816	275,122	7,2	
67	4816	264,122	7,3	
68	4816	252,122	7,4	
69	6522	160,29	2,6	External VIA
70	74LS244	137,24	2,6	
71	74LS244	184,29	2,4	
72	74LS245	199,29	2,3	
73	uPD7002	100,173	14,6	ADC convertor
74	88LS120	183,201	13,4	
75	3691	207,199	14,4	
76	74LS163	70,44	10,8	
77	74S00	38,143	4,8	4,9
78	8271	60,75	3,9	Disc controller
79	7438	42,46	2,9	
80	7438	57,46	2,9	
81	74LS393	82,46	2,8	
82	74LS10	97,46	3,8	
83	4013	67,24	4,7	
84	4013	82,24	3,7	
85	4020	97,21	2,7	
86	74LS393	108,23	2,7	
87	74LS123	43,164	2,10	13,8
88	2764	252,24	9,9	
89	68B54	15,125	12,8	ADLC - Econet
90	40178	16,162	13,10	(Not fitted)
91	74LS132	27,166	12,7	14,9
92	74LS74	16,188	14,10	(Not fitted)
93	75159	13,166	14,9	
94	LM319	45,93	13,8	
95	LM319	20,193	13,7	
96	74LS244	82,185	12,10	
97	74LS74	4,171	13,9	
98	TMS6100	15,75	4,8	Speech ROM
99	TMS5220	35,75	5,7	Speech generator
100	(27128)	272,24	10,9	Sideways ROM
101	(27128)	290,24	11,9	Sideways ROM

8,2 Transistors

Q	Type	Circuit Diagram
1	BC239	13,5
2	BC239	13,5
3	BC239	13,5
4	BC239	11,3
5	BC239	12,3
6	BC239	12,3
7	BC309	14,2
8	BC309	13,2
9	BC239	14,1
10	2N3906	11,2
11	BC239	2,4

8.3 Diodes

D	Type	Circuit Diagram
1	1N4148	6,8
2	1N4148	4,6
3	1N4148	14,7
4	1N4148	10,8 Not fitted
5	1N4148	10,8 Not fitted
6	1N4148	14,6
7	1N4148	14,6
8	1N4148	14,6
9	1N4148	12,5 Not fitted
10	1N4148	8,8 Not fitted, issue 7 onwards
11	1N4148	8,8 Not fitted, issue 7 onwards
12	1N4148	8,8 Not fitted, issue 7 onwards
13	1N4148	13,5
14	1N4148	3,3
15	1N4148	3,3
16	1N4002	11,1
17	1N4002	11,1
18	1N4002	11,1
19	1N4148	13,1
20	1N4148	13,3
21	1N4148	13,3
22	1N4148	13,3

8.4 Capacitors

C	Type	Circuit Diagram
1	2n2F Plate ceramic	4,6
2	4u7F 16V Elec	4,5
3	2n2F Plate ceramic	4,6
4	Not used	
5	10uF 16V Elec	4,5
6	100nF Disc ceramic	6,7
7	2n2F Plate ceramic	4,5
8	100nF Disc ceramic	6,7

9	10uF 16V Elec	4,4	
10	10nF Plate ceramic	6,7	
11	2n2F Plate ceramic	4,5	
12	10pF Plate ceramic	5,7	
13	1nF Plate ceramic	2,10	
14	47uF 10V Elec	3,1	
15	100nF Disc ceramic	5,5	
16	47uF 10V Elec	5,5	
17	2n2F Plate ceramic	13,9	
18	10uF 10V Tant	14,8	
19	Not used		
20	47nF Disc ceramic	5,5	
21	100nF Disc ceramic	5,7	
22	Not used		
23	10nF Plate ceramic	13,8	
24	100nF Disc ceramic	6,7	
25	33 ⁿ F Polyester	14,6	
26	47uF 10V Elec	4,1	
27	1uF 35V Tant	14,6	
28	4u7F 10V Tant	12,5	
29	2n2F Plate ceramic	13,5	
30	10uF 10V Tant	12,5	
31	820pF Plate ceramic	15,5	
32	4n7F Plate ceramic	14,5	
33	4n7F Plate ceramic	13,5	
34	200/220nF	14,5	
35	820pF Plate ceramic	15,5	
36	47uF 10V Tant	4,1	
37	33pF Plate ceramic	6,6	
38	2n2F Plate ceramic	13,3	
39	2n2F Plate ceramic	13,3	
40	10nF Plate ceramic	7,6	
41	220pF Plate ceramic	8,5	
42	33pF Plate ceramic	6,5	
43	47pF Plate ceramic	14,4	
44	Not used		
45	10nF Plate ceramic	13,1	
46	47pF Plate ceramic	14,4	
47	10uF 10V Tant	11,1	
48	270pF Plate ceramic	8,5	
49	150pF Plate ceramic	13,2	
50	47pF Plate ceramic	14,2	
51	15/22pF Plate ceramic 11,2		(SOT)
52	390pF Plate ceramic	11,2	
53	100pF Plate ceramic	11,2	
54	47uF 10V Tant	4,1	
55	100pF Plate ceramic	11,1	
56	39pF Plate ceramic	14,1	
57	10uF 10V Tant	3,1	
58	470pF Plate ceramic	14,2	
59	220nF	13,5	
60	4u7F 10V Tant	3,1	

8,5 Resistors

R	Value	Circuit Diagram
1	10k	4,6
2	10k	5,6
3	10k	5,6
4	22k	4,6
5	100k	3,6
6	4k7	1,5
7	100k	3,6
8	10k	4,5
9	39k	4,6
10	3k3	4,2
11	100k	3,6
12	220k	3,6
13	1M	6,7
14	10R	4,5
15	39k	3,5
16	22k	4,5
17	10k	4,5
18	10R	4,4
19	Not used	
20	1M	6,8
21	1M	6,7
22	150R	3,9
23	150R	3,9
24	39k	4,4
25	Not used	
26	Not used	
27	10k	3,5
28	4k7	3,5
29	1k	3,5
30	10k	5,6
31	4k7	5,6
32	150k	5,7
33	1k	2,10
34	10k (2%)	14,8
35	10k (2%)	14,8
36	1M5	13,8
37	k	2,9
38	100K (2%)	14,8
39	100K (2%)	14,8
40	100K (2%)	14,8
41	100K (2%)	14,8
42	Not used	
43	Not used	
44	1M5	13,9
45	10k (2%)	13,8
46	k	13,8
47	k5 (2%)	14,8
48	k (2%)	14,8
49	150R	2,10
50	39k	12,9
51	10k (2%)	14,8
52	k	13,9
53	1k	4,7
54	Not used	
55	3k3	8,8 Not fitted, issue 7 onwards

56 Not used
57 10R 5,5
58 150R 1,7
59 56k (2%) 13,7
60 56k (2%) 13,7
61 1k 13,8
62 56k (2%) 13,7
63 56k (2%) 13,7
64 1M5 13,7
65 3k3 3,10
66 10k 5,10
67 10k 5,10
68 3k3 2,7
69 3k3 10,8
70 3k3 2,6
71 2k7 14,6
72 3k3 8,9 Not fitted, issue 7 onwards
73 3k3 7,9 Not fitted, issue 7 onwards
74 2k2 12,5
75 82k 12,5
76 10k 13,5
77 100k 13,5
78 150k 14,4
79 820k 15,5
80 39k 14,5
81 3k3 10,6
82 150k 14,4
83 4k7 5,4
84 10k 13,5
85 3k3 10,6
86 220k 14,5
87 8k2 14,5
88 8k2 14,5
89 4k7 13,4
90 4k7 13,5
91 820R 7,6
92 820R 7,6
93 3k3 14,4
94 ,100R 8,6
95 2k2 14,4
96 3k3 14,4
97 2k2 14,4
98 1k2 7,5
99 1k2 10,2
100 1k2 11,2
101 1k0 11,2
102 100R 6,5
103 1k0 10,2
104 100R 9,8 Not fitted, issue 4 onwards
105 100R 8,6
106 56R 8,4
107 1k0 7,5
108 3k3 3,3
109 1k8/2k7 13,1 SOT
110 68R 14,2
111 68R 14,3
112 68R 14,3
113 68R 14,3
114 18R 1W 11,1
115 1k0 14,2

116	3k9	14,2
117	2k2	14,2
118	1k0	14,2
119	100R	8,5
120	82R	12,3
121	82R	11,3
122	82R	11,3
123	470R	14,2
124	56R	7,4
125	100R	9,8 Not fitted, issue 4 onwards
126	3k9	14,1
127	1k5	14,2
128	470R	13,2
129	68R	14,2
130	68R	13,2
131	56R	7,4
132	120k	14,1
133	120k	14,1
134	1k0	14,2
135	1k0	14,1
136	2k2	13,3
137	3k9	13,2
138	1k5	13,2
139	1k0	13,2
140	1k0	14,2
141	2k7	14,2
142	100R	9,8 Not fitted, issue 4 onwards
143	12k	11,2
144	15k	11,2
145	1k0	11,2
146	1k5	11,1
147	3k9	11,1
148	820R	14,2
149	100R	9,8 Not fitted, issue 4 onwards
150	680R	14,2
151	470R	14,1
152	2k2	14,2
153	100R	9,8 Not fitted, issue 4 onwards
154	1k2	14,1
155	680R	14,1
156	3k3	14,1
157	680R	14,1
158	470R	14,1
159	270k	13,5
160	3k3	12,4
161	5k6	13,4
162	4k7	1,6
163	Not used	
164	Not used	
165	Not used	
166	Not used	
167	Not used	
168	Not used	
169	Not used	
170	2k2	2,5
171	100R	13,6
172	10k	4,6
173	4k7	12,8
174	22k	12,3

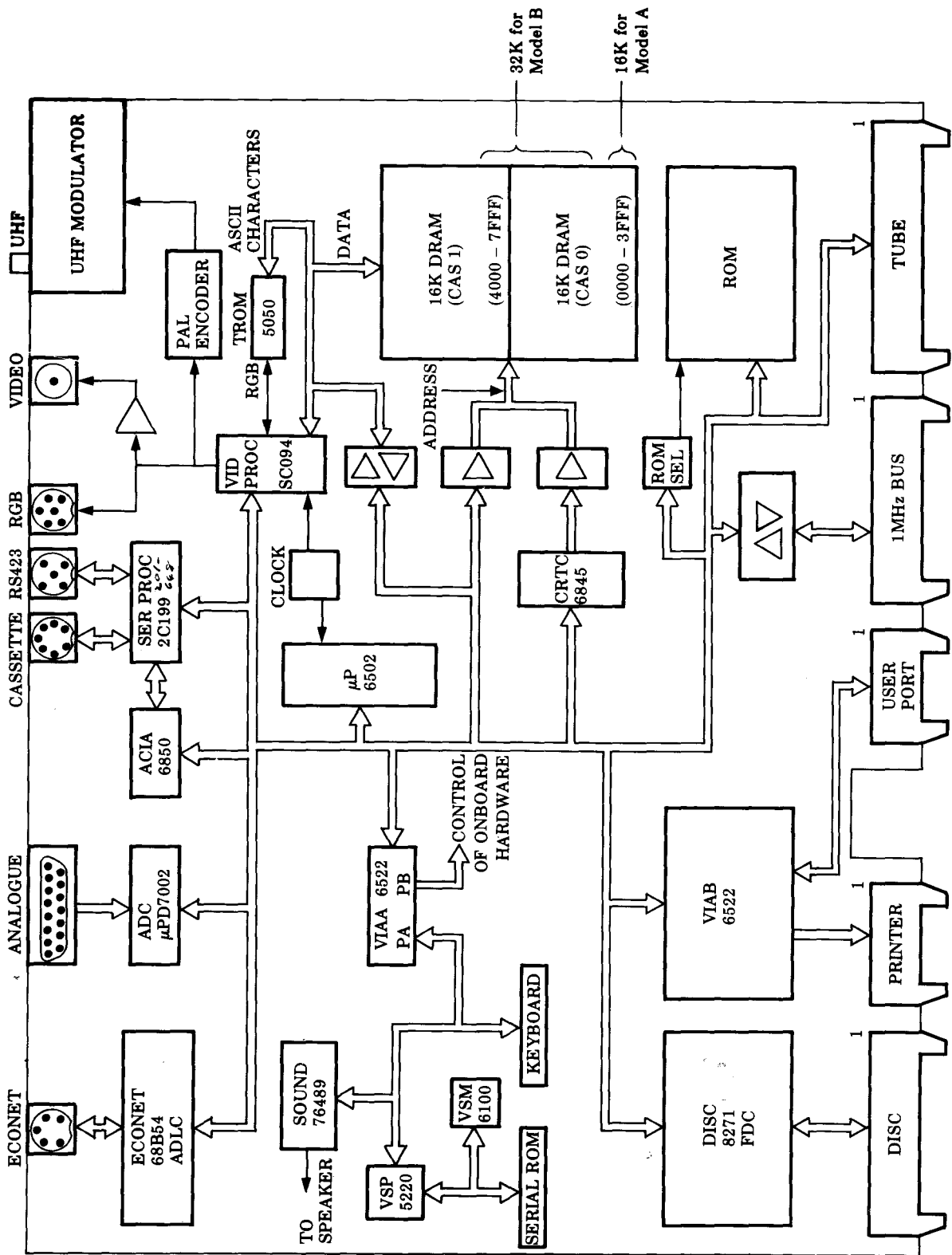
8.6 Links

Some links have been omitted on later issue boards, whilst others have been added.

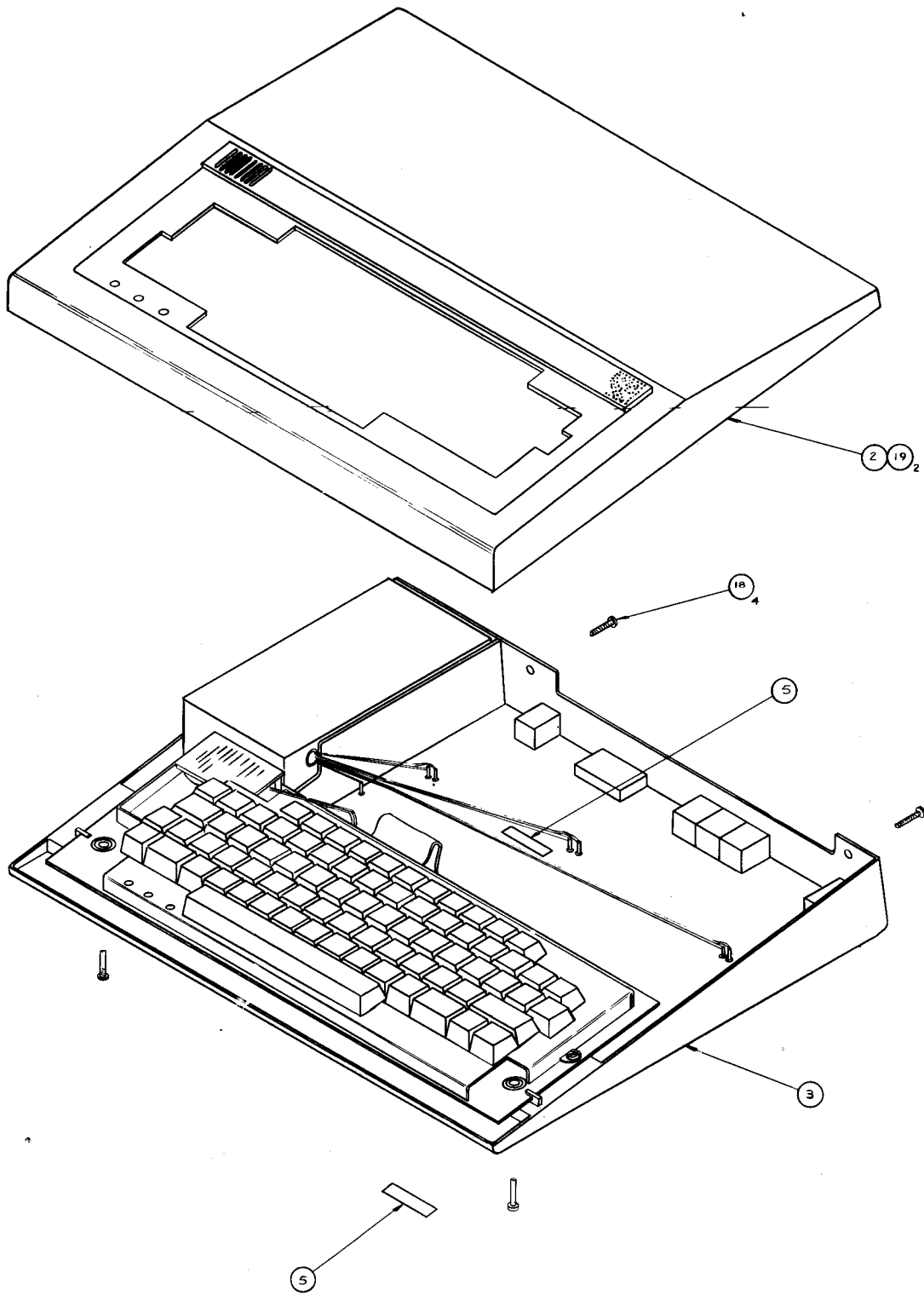
LINK PCB Circuit position diagram

1.	2,108	2,5 (Not used on issues 2 and 3)
2.	2,161	12,7
3.	2,173	14,14 (Only fitted on issues 1,2,3)
4.	12, 12	1,9
5.	26,195	14,9 (Only fitted on issues 1,2,3)
6.	26,205	15,9 (Only fitted on issues 1,2,3)
7.	30, 65	4,9
8.	32, 15	2,9
9.	35,128	3,10
10.	45, 15	1,8
11.	75,210	13,10
12.	97, 70	9,8
13.	100, 67	9,8
14.	101, 53	7,10
15.	107, 97	7,9
16.	108, 90	7,9
17.	108, 52	7,10
18.	110, 52	7,8
19.	102,102	7,8
20.	123, 55	9,8
21.	122, 65	9,8
22.	127, 70	9,8
23.	177,215	13,3
24.	181,195	13,3
25.	215,185	7,5
26.	221, 68	10,1
27.	226, 95	1,7
28.	237,144	12,6
29.	237,146	12,6
30.	284, 20	8,8
31.	270,170	14,3
32.	295, 65	9,9
33.	295, 67	10,9
34.	200, 65	9,8 (From issue 4 onwards)
35.	245, 20	9,8 (From issue 4 onwards)
36.	260, 20	9,8 (From issue 4 onwards)
37.	280, 20	9,8 (From issue 4 onwards)
38.	300, 15	9,8 (From issue 4 onwards)
39.	255,215	9,8 (From issue 4 onwards)

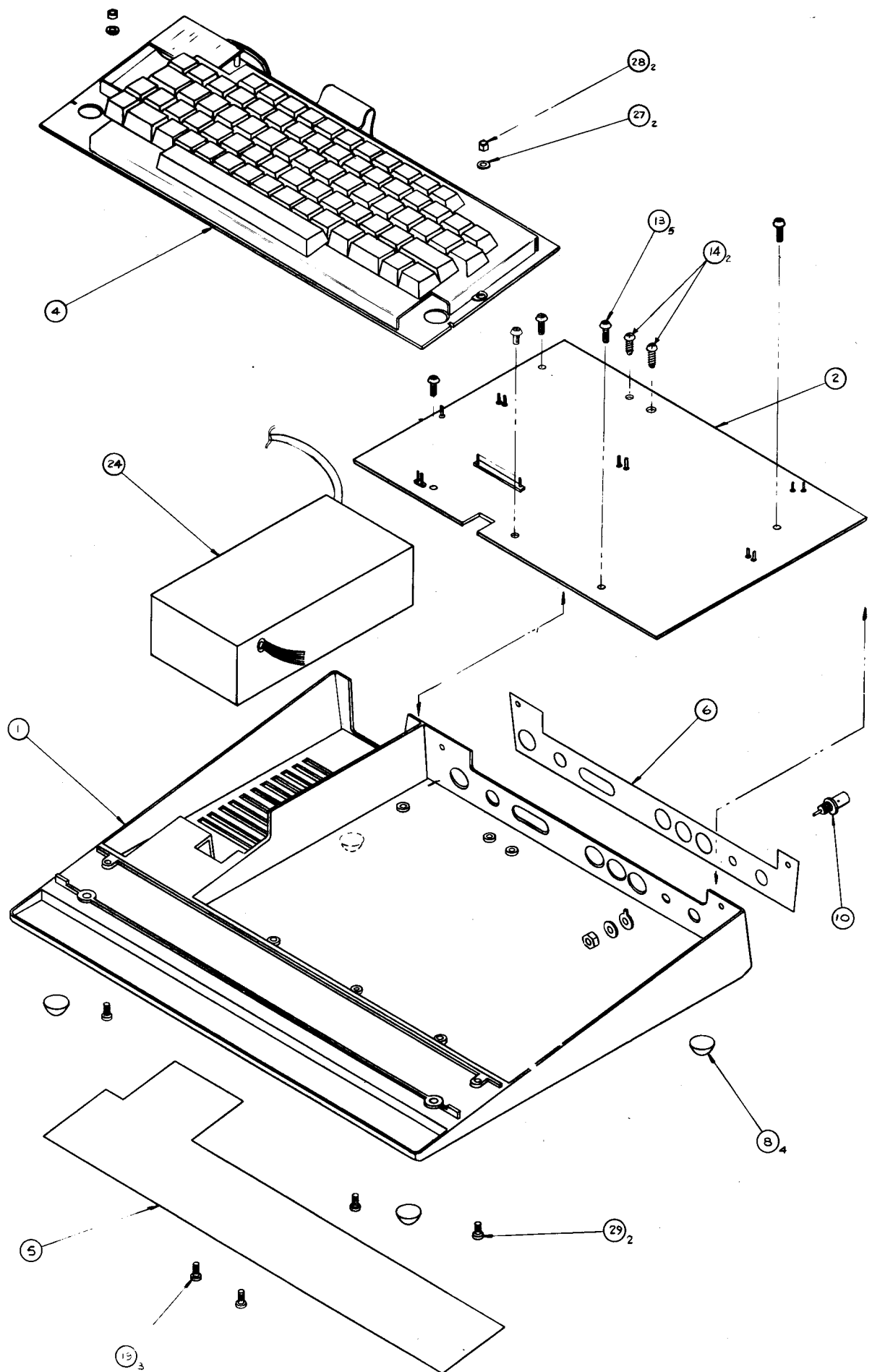
9 Appendices



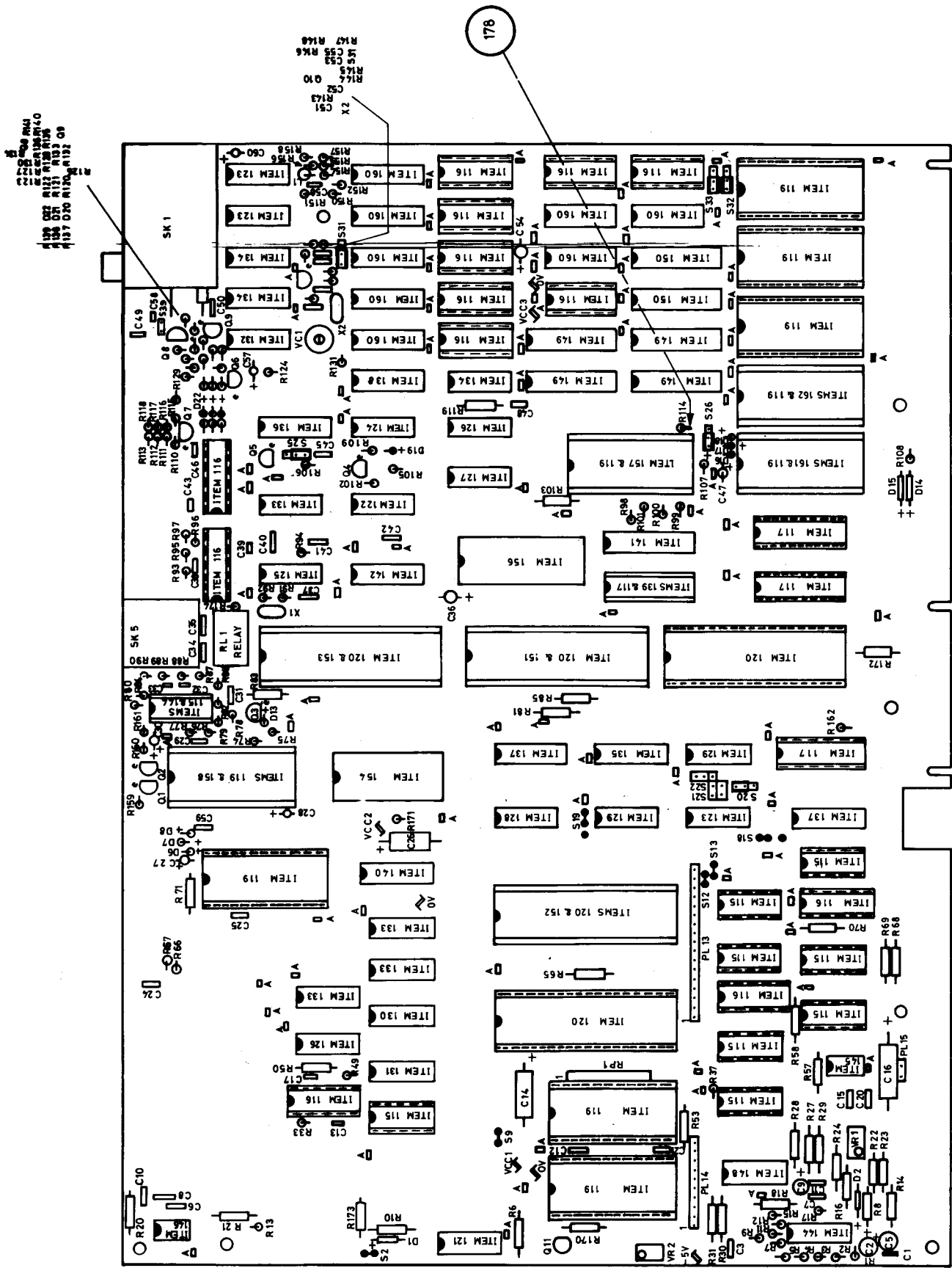
9.1 Circuit block diagram





9.2 Assembly drawing

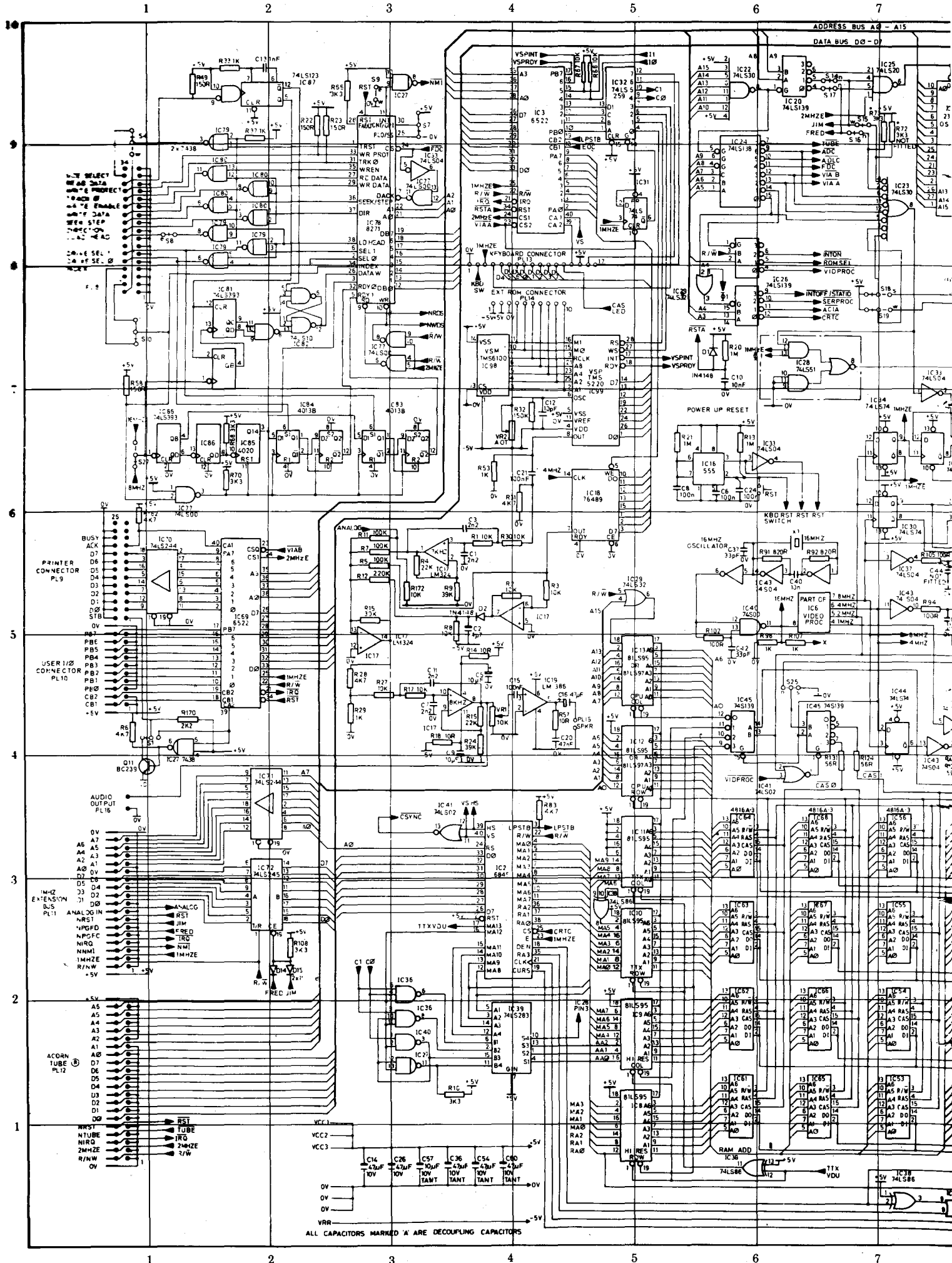


9.3 Case lower assembly drawing



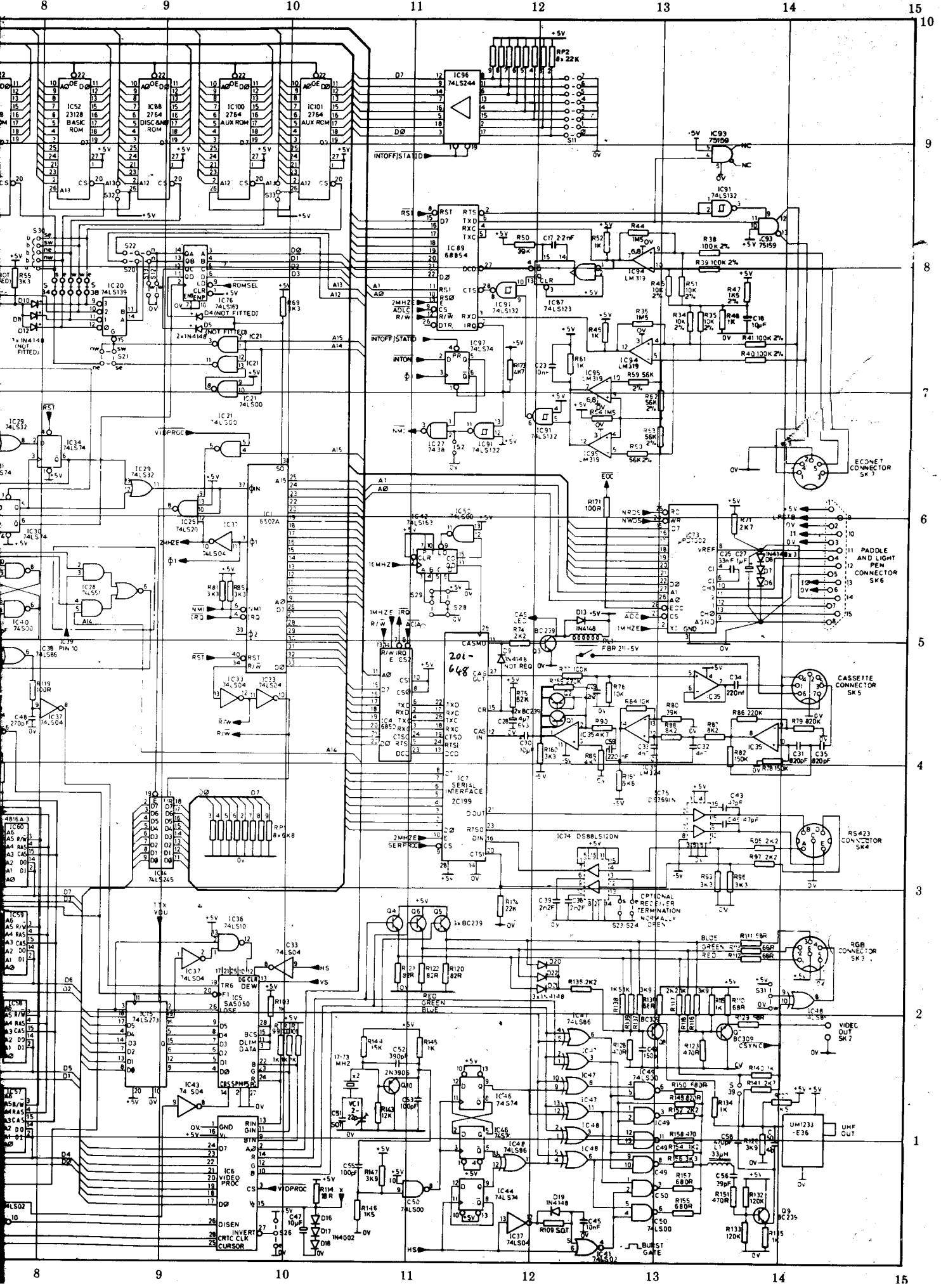
9.4 Main PCB layout

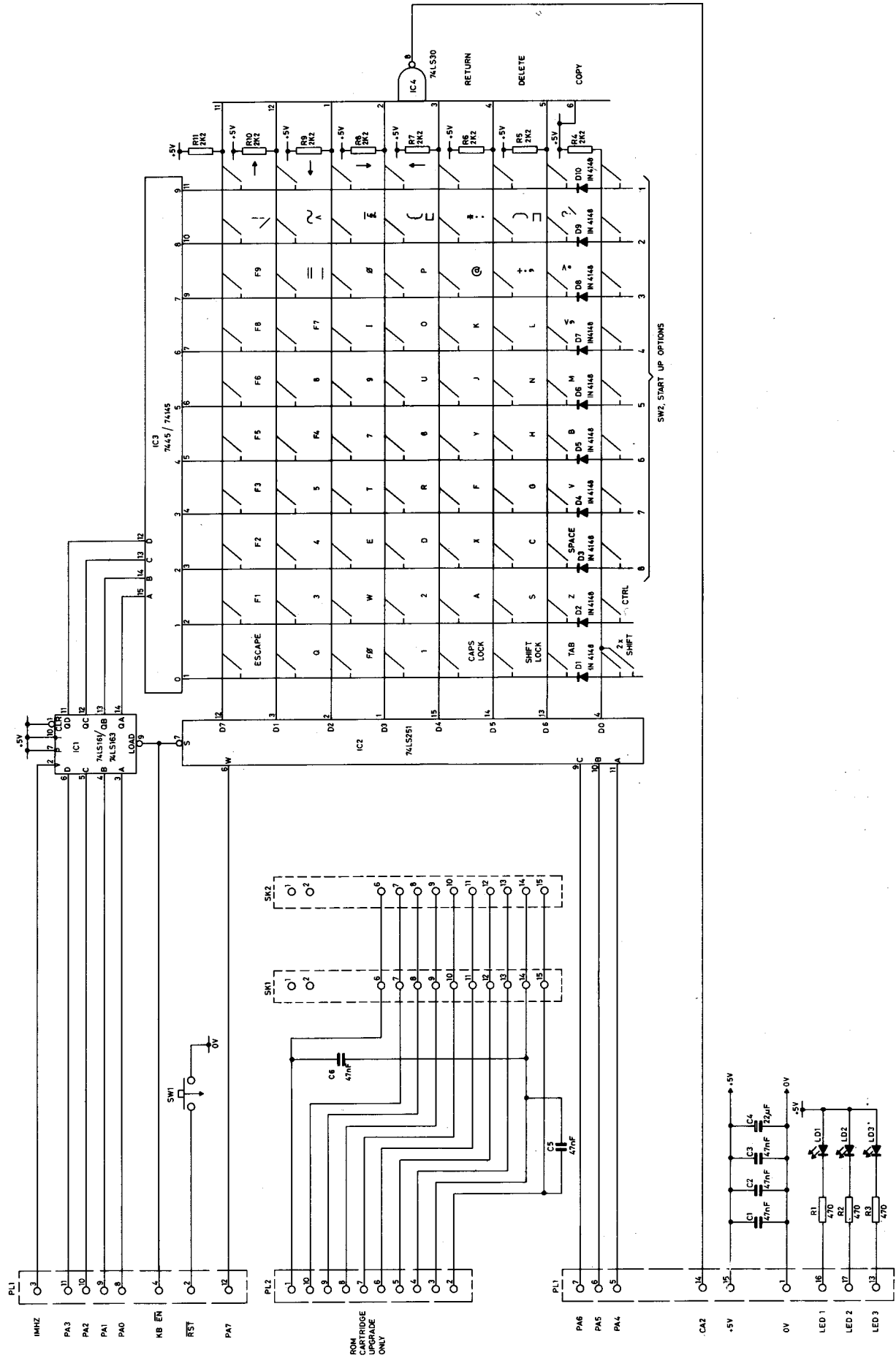
- NOTES:-
1. INSERT WIRE LINKS SHOWN THUS  USING WIRE (ITEM 176)
 2. ENSURE POSITION OF LINK SHUNTS (ITEM 173) IS CORRECT TO DRAWING
 3. INSERT FASTON TAB (ITEM 177) IN POSITIONS SHOWN THUS 
 4. FIT HEATSINK (ITEM 175) TO IC6 (ITEM 157) WHEN RECD



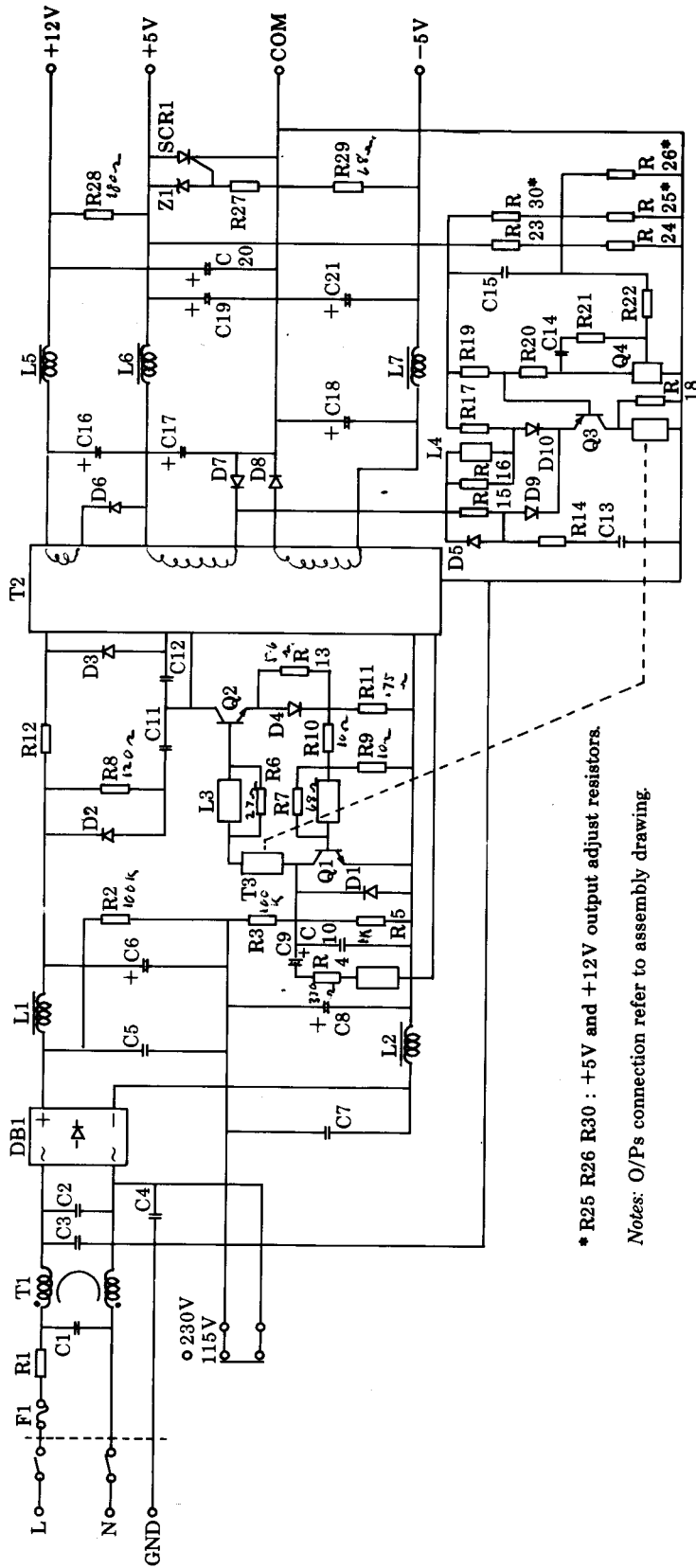
ALL CAPACITORS MARKED 'A' ARE DECOUPLING CAPACITORS

circuit diagram





9.6 Keyboard circuit diagram



* R25 R26 R30 : +5V and +12V output adjust resistors.
 Notes: O/Ps connection refer to assembly drawing.

9.7 Power supply circuit diagram

9.8 Parts list

CASE LOWER ASSEMBLY MODEL B + ECONET + DISC

ITEM	PART No	DESCRIPTION	QTY	REMARKS
1	A2/210,232	CASE LOWER	1	
2	A2/103,500	MAIN PCB ASSEMBLY MODEL B+ECONET+DISC	1	
3	A1/103,004/A	CASE LOWER ASSY		REF 'STANDARD' DRG
4	A1/103,001	KEYBOARD ASSEMBLY (INC SPKR)	1	
5	A2/21,111	CUT RIGID PVC LABEL BOTTOM ACCESS	1	
6	A2/201,098	CUT RIGID PVC LABEL REAR ACCESS	1	
7				
8	890,000	STICK ON FEET	4	
9				
10	800,600	B.N.C. CONNECTOR 75R	1	PANEL MOUNT SK2
11	870,109	WIRE 7/0,2 WHITE PVC	2	2" LENGTH
12				
13	882,644	No 8 x 9.5 FLANGE HEAD POSIDRIV	5	BLACK SELF TAP
14	882,712	No 4 x 7/16" PAN HD SUPERDRIVE	2	PLASTITE
15	882,986	NYLON WASHER I/D 5mm	5	
16				
17				
18				
19	882,022	M3 x 8mm CHEESE HEAD POST DRIVE	3	USE WITH ITEM 24
20				
21				
22				
23				
24	103.003	POWER SUPPLY UNIT	1	ASTEC SMPS
25				
26				
27	882,988	4 BA INTERNAL TOOTH SHAKEPROOF WASHER	2	
28	882,914	4BA NUT FULL	2	
29	882,343	4BA x 5/8" PAN HD POSIDRIV	2	
30				

MAIN CIRCUIT BOARD MODEL B + DISC + ECONET

ITEM	PART No	DESCRIPTION	QTY	REMARKS
1	203000	PRINTED CIRCUIT BOARD	1	
2	103,500/A	ASSEMBLY DRAWING MODEL B +DISC+ECONET	1	PER WORKS ORDER
3				
4	520,180	RESISTOR 18R 1W 10% CARBON FILM	1	R114
5				
6	500,100	RESISTOR 10R 1/4W 10% CARBON FILM	3	R14 18 57
7	500,560	RESISTOR 56R 10% CARBON FILM	3	8106,124,131
8	500,680	RESISTOR 68R 1/4W 10% CARBON FILM	6	R110,113,129,130
9	500,820	RESISTOR 82R 1/4W 10% CARBON FILM	3	R120,121,122
10	500,101	RESISTOR 100R 1/4W 10% CARBON FILM	5	R94,102,105,119, 171
11	500,151	RESISTOR 150R 14W 10% CARBON FILM	4	R22,23,49,
12	500,471	RESISTOR 470R 1/4W 10% CARBON FILM	4	R123,128,155,18,151
13	500,681	RESISTOR 680R 1/4W 10% CARBON FILM	3	R150,155,157
14	500,821	RESISTOR 820R 1/4W 10% CARBON FILM	3	R91,92,148
15				
16	500,102	RESISTOR 1K 1/4W 10% CARBON FILM	20	R29,33,37,46,52, 53,61,101,103, 107,115,118,134, 135,139,140,145, 98,99,100
17				
18				
19	500,122	RESISTOR 1K2 1/4W 10% CARBON FILM	2	R154,127
20	500,152	RESISTOR 1K5 1/4W 10% CARBON FILM	2	R138,146
21	500,222	RESISTOR 2K2 1/4W 10% CARBON FILM	7	R74,95,97,117, 136,152,170
22	500,272	RESISTOR 2K7 1/4W 10% CARBON FILM	1	R71
23	500,332	RESISTOR 3K3 1/4W 10% CARBON FILM	12	R10,65,68,69,70,81,85,93,96, 108,156,160
24				
25	500,182	RESISTOR 1K8 1/4W 10% CARBON FILM	1	R141
26	500,392	RESISTOR 3K9 10% CARBON FILM	4	R116 126,137 147
27	500,472	RESISTOR 4K7 1/4W 10% CARBON FILM	8	R6,28,31,83,89, 90,162,173
28	500,562	RESISTOR 5K6 1/4W 10% CARBON FILM	1	R161
29	500,822	RESISTOR 8K2 1/4W 10% CARBON FILM	2	R87,88
30				
31	500,103	RESISTOR 10K 1/4W 10% CARBON FILM	12	R1-3,8,17,27,30, 66,67,76,84,172
32				
33	500,123	RESISTOR 12K 1/4W 10% CARBON FILM	1	R143
34	500,153	RESISTOR 15K 1/4W 10% CARBON FILM	1	R144
35	500,223	RESISTOR 22K 1/4W 10% CARBON FILM	3	R4,16,174
36	500,393	RESISTOR 39K 1/4W 10% CARBON FILM	5	R9,15,24,50,80
37	500,823	RESISTOR 82K 1/4W 10% CARBON FILM	1	R75
38	500,104	RESISTOR 100K 1/4W 10% CARBON FILM	4	R5,7,11,77
39	500,124	RESISTOR 120K 1/4W 10% CARBON FILM	2	R132,133
40	500,154	RESISTOR 150K 1/4W 10% CARBON FILM	2	78,82
41				
42	500,224	RESISTOR 220K 1/4W 10% CARBON FILM	2	R12,86
43	500,274	RESISTOR 270K 1/4W 10% CARBON FILM	1	R159
44	500,824	RESISTOR 820K 1/4W 10% CARBON FILM	1	R79
45				
46	500,105	RESISTOR 1M 1/4W 10% CARBON	3	R13,20,21
47	500,155	RESISTOR 1M5 1/4W 10% CARBON	3	R36,44,64
48	590,682	RESISTOR PACK S.I.P. 6K8 x 8	1	RP1
49	590,223	RESISTOR PACK S.I.P. 22K x 8	1	RP2
50	580,103	POTENTIOMETER 10K VERT. MIN. PRESET	1	VR1
51	580,204	POTENTIOMETER 200K VERT. MIN. PRESET	1	VR2
52				
53	500,182/272	RESISTOR 1K8/2K7 1/4W 10% CARBON FILM	1	R109,S.O.T. ON BATCH BASIS
54				
55	505,102	RESISTOR 1K 1/4W 2% CARBON	1	R48
56	505,152	RESISTOR 1K5 1/4W 2% CARBON	1	R47
57	505,103	RESISTOR 10K 1/4W 2% CARBON	4	834,35,45,51
58	505,563	RESISTOR 56K 1/4W 2% CARBON	4	859,60,62,63
59	505,104	RESISTOR 100K 1/4W 2% CARBON	4	838,39,40,41
60				
61	631,010	CAPACITOR 10pF PLATE CERAMIC	1	C12
62	631M015/022	CAPACITOR 15722pF PLATE CERAMIC	1	C51,S.O.I. ON BATCH BASIS
63	631,033	CAPACITOR 33pF PLATE CERAMIC	2	C37,42
64	631,039	CAPACITOR 39pF PLATE CERAMIC	1	C56

65	631,047	CAPACITOR 47pF PLATE CERAMIC	1	C50
66	631,100	CAPACITOR 100pF PLATE CERAMIC	2	C53,55
67	631,150	CAPACITOR 150pF PLATE CERAMIC	1	C49
68				
69	631,220	CAPACITOR 220pF PLATE CERAMIC	1	C41
70	631,270	CAPACITOR 270pF PLATE CERAMIC	1	C48
71	630,039	CAPACITOR 390pF PLATE CERAMIC	1	C52
72	630,082	CAPACITOR 820pF PLATE CERAMIC	2	C31,35
73	632,047	CAPACITOR 47pF PLATE CERAMIC	2	C43,46
74	633,047	CAPACITOR 470pF PLATE CERAMIC	1	C58
75	629,001 ^	CAPACITOR 1nF PLATE CERAMIC	1	C13
76	629,002	CAPACITOR 2n2F PLATE CERAMIC	6	C1,3,7,11,17,29
77	634,004	CAPACITOR 4u7F PLATE CERAMIC	2	C32,33
78	629,010	CAPACITOR 10nF PLATE CERAMIC	4	C10,23,40,45
79	650,333	CAPACITOR 33nF POLYESTER	1	C25
80	680,001	CAPACITOR, DECOUPLER 33/47 nF	76	A
81	628,470	CAPACITOR 47nF DISC CERAMIC	1	C20
82	628,101	CAPACITOR 100nF DISC CERAMIC	5	C6,8,15,21,24
83	634,002	CAPACITOR 2n2F PLATE CERAMIC	2	C38,39
84	651,224	CAPACITOR 220nF	1	C59
85	613,100	CAPACITOR 1uF 35V TANTALUM	1	C27
86	610,005	CAPACITOR 4u7F 10V TANTALUM	2	C28,60
87	635,047	CAPACITOR 4u7F 16V RADIAL ELEC	1	C2
88	610,010	CAPACITOR 10uF 10V TANTALUM	4	C18,30,47,57
89	635,100	CAPACITOR 10uF 16V RADIAL ELEC	2	C5,9
90	610,047	CAPACITOR 47uF 10V TANTALUM	2	C36,54
91	621,470	CAPACITOR 47uF 10V AXIAL ELEC	3	C14,16,26
92	651,204/224	CAPACITOR 200/220nF	1	C34
93				
94	699,001	TRIMMING CAPACITOR 2-22pF	1	VC1
95				
96				
97	860,005	CHOKER 33 uH	1	L1
98				
99				
100	820,160	CRYSTAL 16 MHz	1	X1
101	820,177	CRYSTAL 17,7345 MHz	1	X2
102				
103				
104	794,002	DIODE IN 4002	3	D16,17,18
105	794,148	DIODE IN 4148	12	D1,2,6,7,8, 13-15,19-22
106				
107				
108	810,001	RELAY 5V	1	RL1
109				
110				
111	780,239	TRANSISTOR BC 239	8	Q1-6,9,11
112	780,309	TRANSISTOR BC309	2	Q7,8
113	783,906	TRANSISTOR 2N3906	1	Q10
114				
115				
116	800,114	I.C. SOCKET D.I.L. 14 PIN	4	55,94,95,93
117	800,120	I.C. SOCKET D.I.L. 20 PIN	1	IC14
118				
119	800,128	I.C. SOCKET D.I.L. 28 PIN	11	IC6,7,51,52,73, 89,98,99,100,101
120	800,140	I.C. SOCKET D.I.L. 40 PIN	5	ICI-3,69,78
121	740,038	INTEGRATED CIRCUIT 7438	3	IC27,79,80
122	741,000	INTEGRATED CIRCUIT 74S00	1	IC40
123	742,000	INTEGRATED CIRCUIT 74LS00	4	IC21,49,50,77
124	742,002	INTEGRATED CIRCUIT 74LS02	1	IC41
125	741,004	INTEGRATED CIRCUIT 74S04	1	IC43
126	742,004	INTEGRATED CIRCUIT 74LS04	2	IC33,37
127	742,010	INTEGRATED CIRCUIT 74LS10	2	IC36,82
128	742,020	INTEGRATED CIRCUIT 74LS20	1	IC25
129	742,030	INTEGRATED CIRCUIT 74LS30	2	IC22,23
130	742,032	INTEGRATED CIRCUIT 74LS32	1	IC29
131	742,051	INTEGRATED CIRCUIT 74LS51	1	IC28
132	741,074	INTEGRATED CIRCUIT 74S74	1	IC46
133	742,074	INTEGRATED CIRCUIT 74LS74	5	IC30,31,34,44,97
134	742,086	INTEGRATED CIRCUIT 74LS86	3	IC38,47,48
135	742,138	INTEGRATED CIRCUIT 74LS138	1	IC24
136	741,139	INTEGRATED CIRCUIT 74S139	1	IC45
137	742,139	INTEGRATED CIRCUIT 74LS139	2	IC20,26
138	742,163	INTEGRATED CIRCUIT 74LS163	2	IC42,76
139	742,244	INTEGRATED CIRCUIT 74LS244	3	IC70,71,96
140	742,245	INTEGRATED CIRCUIT 74LS245	2	IC14,72
141	742,259	INTEGRATED CIRCUIT 74LS259	1	IC32
142	742,273	INTEGRATED CIRCUIT 74LS273	1	IC15

	143	742,283	INTEGRATED CIRCUIT	74LS283	1	IC39
	144	770,324	INTEGRATED CIRCUIT	LM324	2	IC17,35
	145	770,386	INTEGRATED CIRCUIT	LM386	1	IC19
	146	770,555	INTEGRATED CIRCUIT	LM555	1	IC16
	147	738,095/097				INTEGRATED CIRCUIT 81
LS95/97	2		IC12,13			
	148	706,489	INTEGRATED CIRCUIT	76489	1	IC18
	149	738,095	INTEGRATED CIRCUIT	81LS95	4	IC8-11
	150	739,120	INTEGRATED CIRCUIT	88LS120	1	IC74
	151	706,502	INTEGRATED CIRCUIT	6502A	1	IC1
	152	706,522	INTEGRATED CIRCUIT	6522	2	IC3,69
	153	706,845	INTEGRATED CIRCUIT	6845	1	IC2
	154	706,850	INTEGRATED CIRCUIT	6850	1	IC4
	155	733,691	INTEGRATED CIRCUIT	3691	1	IC75
	156	705,050	INTEGRATED CIRCUIT	SAA5050	1	IC5
	157	201,601/647				INTEGRATED CIRCUIT
VIDEO			PROCESSOR		1	IC6
	158	201,602/648				INTEGRATED CIRCUIT
SERIAL			PROCESSOR		1	IC7
	159	707,002	INTEGRATED CIRCUIT	7002	1	IC73
	160	704,816	INTEGRATED CIRCUIT	4816	16	IC53-68
	161	201,629	INTEGRATED CIRCUIT	23128	1	IC51 (OPERATING SYSTEM)
	162	201,628	INTEGRATED CIRCUIT	23128	1	IC52 (BASIC)
163						
	164	800,004	SOCKET D.I.N. 5 WAY		1	SK7
	165	825,000	SOCKET UM1233-E36		1	SK1 (UHF MODULATOR)
	166	800,002	SOCKET D.I.N. 6 WAY		1	SK3
	167	800,001	SOCKET D.I.N. 5 WAY DOMINO		1	SK4
	168	800,003	SOCKET D.I.N. 7 WAY		1	SK5
	169	800,304	SOCKET 'D' TYPE 15 WAY		1	SK6
170						
	171	800,059	PLUG 17 WAY		1	PL13 (KEYBOARD)
	172	800,055	PLUG 10 WAY		1	PL14 (SERIAL ROM)
	173	800,050	PLUG 2 WAY		4	PL15 S21(2),39
	174	800,051	PLUG 3 WAY		7	S20,22,25,26,31-33
	175	800,070	SHUNT		16	S20,21(2),22,25,26,31-33,S11(7)
	176	800,054	PLUG 8 WAY		2	S11
	177	880,040	SLEEVING BLACK NEOPRENE		A/R	FIT TO R114
	178	201,029	HEATSINK		1	FIT TO IC6 IF 201,601
	179	870,420	WIRE TCW		A/R	18(N),19(E)
	180	800,200	FASHION TAB		7	
	181	800,006	CONNECTOR IDC 34 WAY		2	PL8,11
	182	800,008	CONNECTOR IDC 26 WAY		1	PL9
	183	800,009	CONNECTOR IDC 20 WAY		1	PL10
	184	800,007	CONNECTOR IDC 40 WAY		1	PL12
185						
	186	742,123	INTEGRATED CIRCUIT	74LS123	1	IC87
	187	742,132	INTEGRATED CIRCUIT	74LS132	1	IC91
	188	742,393	INTEGRATED CIRCUIT	74LS393	2	IC81,86
	189	735,159	INTEGRATED CIRCUIT	75159	1	IC93
	190	706,854	INTEGRATED CIRCUIT	68B54	1	IC89
	191	754,013	INTEGRATED CIRCUIT	4013	2	IC83,84
	192	754,020	INTEGRATED CIRCUIT	4020	1	IC85
	193	708,271	INTEGRATED CIRCUIT	8271	1	IC78
	194	770,319	INTEGRATED CIRCUIT	LM319	2	IC94,95
	195	201,666	INTEGRATED CIRCUIT	27128*	1	IC88 (DNFS ROM)

9.9 Glossary of abbreviations

ACK	ACKnowledge line on the printer port
ACIA	Asynchronous Communications Interface Adaptor - serial to parallel and parallel to serial converter (6850)
ADC	Analogue to Digital Converter
ADLC	Advanced Data Link Controller - Econet control IC (68B54)
ADSR	Attack, Decay, Sustain, Release - defining the envelope of a sound
ASCII	American Standard Code for Information Interchange - binary code for representing alphanumeric characters.
BASIC	Beginners All-purpose Symbolic Instruction Code
BBC	British Broadcasting Corporation
BNC	Bayonet-Neill-Concelman - the type of bayonet connector used for the video output
CA1/2	Control lines associated with the PA port on a VIA
CAS	Column Address Strobe - control line :for the dynamic RAM
CAS0	Refers to the area of RAM selected by the CAS0 line
CAS1	Refers to the area of RAM selected by the CAS1 line
CB1/2	Control lines associated with the PB port on a VIA
CP/M	Control Program for Microcomputers - Z80 based operating system
CPU	Central Processor Unit (6502)
CR	Capacitor Resistor network
CRT	Cathode Ray Tube
CRTC	Cathode Ray Tube Controller IC (6845)
CSYNC	Composite SYNChronisation pulse from the CRTC
CTS	Clear To Send - control input on the RS423 port
CUTS	An American standard for frequency shift keying - ie using two different tones to represent logic levels
DIN	Connectors such as the cassette socket, RGB socket etc
DRAM	Dynamic RAM
EPROM	Erasable Programmable -Read Only Memory
FIT	Final Inspection Tester
FDC	Floppy Disc Controller (8271)
IC	Integrated Circuit
ID	IDentity - refers to the unique number of a given Econet station
IDC	Insulation Displacement Connectors - parallel cable connectors underneath the computer
IEEE488	A parallel interface usually associated with automatically controlled test instruments
I/O	Input Output
IRQ	Interrupt ReQuest - control line on the 6502 processor
LK	PCB link
MAO-13	Memory Access - control lines out of the CRTC
MOS	Machine Operating System
MPU	Microprocessor Unit
NMI	Non-Maskable Interrupt - control line on the 6502 processor
PA	Port A - One of the two ports of a VIA
PAL	Phase Alternation Line - coding method used for combining separate colour information into a single signal
PB	Port B - The other port of a VIA
PCB	Printed Circuit Board
PET	Progressive Establishment Tester
PL	Header plug
PSU	Power Supply Unit Q1 etc Transistor numbers

QWERTY These are the **upper** left keys on the keyboard ie refers to the standard keyboard layout
 RA0-2 Row Address lines from the **CRTC** to access the RAM
 RAM Random Access read/write Memory
 RAS Row Address Strobe - **Control** line for the **DRAM**
 RC Resistor Capacitor network
 RGB Red Green Blue - individual colour signals for the **VDU**
 ROM Read Only Memory ROMSEL ROM SElect latch
 RS423C An internationally defined convention for serial transmission of data

 RTS Ready To Send - control output **on** RS423 port
 SK Socket
 SOT Select On Test
 SW South West
 Taw Tinned Copper Wire
 TTL Tranistor Transistor Logic a standard type of digital IC (74- series)

 UHF Ultra High Frequency- signal for input to a TV aerial socket
 ULA Uncommitted Logic Array - semi-custom IC
 VDU Visual Display Unit
 VIA Versatile Interface Adaptor (6522)
 VR Variable .Resistor
 Z80 a' **commonly** used 8 bit microprocessor
 1MHz 1 MegaHertz - usually refers to the interface bus running at that speed
 1MHzE Strobe to which the **processor is** synchronised when accessing "slow devices such as 6522 VIA and 1MHz bus
 2MHzF Strobe' to which the **processor is** synchronised when accessing "fast" devices such as ROM and DRAMs.